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(54) **Title:** CONTROL SYSTEM WITH ERROR DETECTION

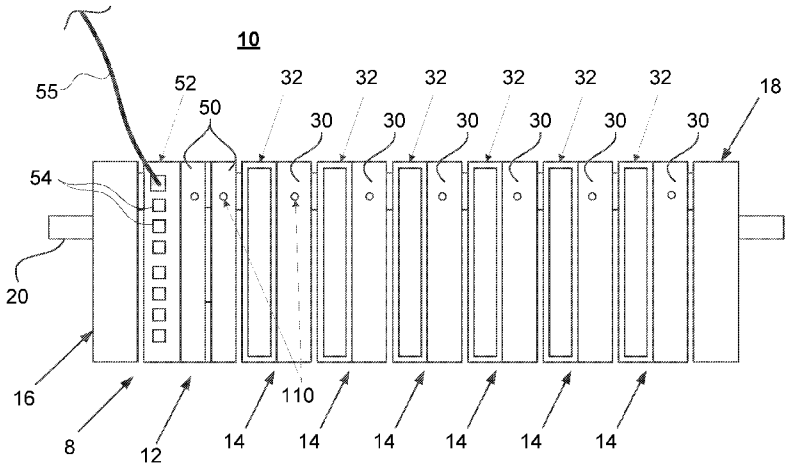

Fig. 1

(57) **Abstract:** A control system for controlling a process. The control system includes primary and secondary module buses over which information may be transmitted between a controller and a plurality of I/O modules. Each of the controller and I/O modules has a power sense circuit for detecting current on the high side of a driver and a ground sense circuit for detecting current on the low side of the driver. The driver is determined to have failed if either the current on the high side of the driver measured by the power sense circuit is outside a predetermined high range or the current on the low side of the driver measured by the ground sense circuit is outside a predetermined low range.

WO 2016/205490 A1

CONTROL SYSTEM WITH ERROR DETECTION

BACKGROUND

[0001] The present disclosure relates to industrial control systems and more particularly to industrial control systems having a controller and input/output modules that communicate over a module bus.

[0002] Industrial control systems, such as distributed control systems, often include one or more controllers that utilize input signals from field devices, such as flow meters, to provide control output signals to final control elements, such as valves, in order to control a process or one or more sub-processes. Such control systems are typically module-based and include one or more controller modules and a plurality of input/output (I/O) modules through which the controller module receives and sends input and output signals from and to the field, respectively. The I/O modules communicate with the controller module(s) over one or more module buses. In conventional control systems, when there is a communication failure on the module bus, it is typically not known whether the communication failure was caused by a failure of the module bus or one of the modules. Detecting the source of the communication failure requires extensive testing.

[0003] The present disclosure is directed to a control system having error detection.

SUMMARY

[0004] In one aspect of the present disclosure, a process control system includes a module bus and a controller module connected to communicate over the module bus. The controller module is programmed to perform operations for controlling the process using data transmitted over the module bus. The control system further includes a plurality of I/O modules connected to communicate with the controller module over the module bus. Each I/O module includes a microprocessor with memory and a driver for sending information to the module bus. The driver has a high side connected to a voltage source and a low side connected to ground. A sense circuit detects current on the high side of the driver. The microprocessor is operable to execute computer-executable instructions stored in the memory to perform an I/O module error detection method that determines whether the current on the high side of the driver measured by

the sense circuit is outside a predetermined high range and, if so, determines that the driver has failed.

[0005] In another aspect of the disclosure, a process control system includes a controller module connected to communicate over first and second module buses. The controller module is programmed to perform operations for controlling the process using data transmitted over the module bus. The control system further includes a plurality of I/O modules connected to communicate with the controller module over the first and second module buses. The controller module and each of the I/O modules include a microprocessor with memory and a driver for sending information to the first module bus. The driver has a high side connected to a voltage source and a low side connected to ground. A power sense circuit detects current on the high side of the driver and a ground sense circuit for detecting current on the low side of the driver. The microprocessor is operable to execute computer-executable instructions stored in the memory to perform a module error detection method that includes determining whether a communication error has occurred on the first module bus. If a communication error has occurred on the first module bus, a determination is made whether the current on the high side of the driver measured by the power sense circuit is outside a predetermined high range and whether the current on the low side of the driver measured by the ground sense circuit is outside a predetermined low range. If either the current on the high side of the driver is determined to be outside the predetermined high range or the current on the low side of the driver is determined to be outside the predetermined low range, a determination is made that the driver has failed.

[0006] In still another aspect of the disclosure, there is a method of detecting errors in a process control system having a plurality of modules connected to communicate over first and second module buses. Each module has a driver for sending information to the first module bus. The driver has a high side connected to a voltage source and a low side connected to ground. In accordance with the method, a determination is made in each of the modules whether a communication error has occurred on the first module bus. The current is measured on the high side of the driver in each of the modules where a communication error has been determined to have occurred. The current is

also measured on the low side of the driver in each of the modules where a communication error has been determined to have occurred. The measured current on the high side of the driver in each of the modules where a high side measurement has been made is compared to a predetermined high range, and the measured current on the low side of the driver in each of the modules where a low side measurement has been made is compared to a predetermined low range. The driver in one of the modules is determined to have failed if either the current on the high side of the driver is outside the predetermined high range or the current on the low side of the driver is outside the predetermined low range.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The features, aspects, and advantages of the present disclosure will become better understood with regard to the following description, appended claims, and accompanying drawings where:

[0008] Fig. 1 shows a front view of a module row of a control system;

[0009] Fig. 2 shows a schematic of the communication connections of the control system;

[0010] Fig. 3 shows a communication circuit within the modules;

[001 1] Fig. 4 shows a flow chart of a module error detection program of the modules; and

[001 2] Fig. 5 shows a flow chart of a system error detection program of the control system.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0013] It should be noted that in the detailed description that follows, identical components have the same reference numerals, regardless of whether they are shown in different embodiments of the present disclosure. It should also be noted that in order to be more clear and concise, the drawings may not necessarily be to scale and certain features of an embodiment may be shown in somewhat schematic form.

[0014] Referring now to FIG. 1, there is shown a schematic view of a module row 8

of a node of an industrial control system 10. The module row 8 comprises a controller assembly 12, a plurality of I/O assemblies 14 and end modules 16, 18 connected to each other and mounted to a top hat DIN rail 20, which may extend horizontally or vertically. The node may include one or more additional module rows, each comprising more I/O assemblies 14 and first and second end modules 16, 18. Each additional module row may be mounted to a separate DIN rail 20. The node may be used to control all or a portion of an industrial process, such as a power generation process. Further, the node may be connected to other nodes of the industrial control system 10, as described more fully below. The module row 8 and other module rows of the control system 10 may be mounted in an enclosure such as a cabinet.

[0015] The controller assembly 12 communicates with the I/O assemblies 14 over one or more module buses 22. Typically, a pair of redundant module buses 22a,b are utilized to increase the integrity of the control system 10. Communication among the modules takes place over both of the module buses 22a,b. However, the modules only use data from the primary bus 22a if it is operating properly. If the primary module bus 22a fails, the modules then use the data from the secondary module bus 22b. Each module bus 22 includes a clock line 24 and a data line 26. The data line 26 carries data between the controller assembly 12 and the I/O assemblies 14, while the clock line 24 provides synchronization between the controller assembly 12 and the I/O assemblies 14. The message structure and communication protocol utilized by the controller assembly 12 and the I/O assemblies 14 to communicate over the module buses 22a,b include one or more features for ensuring data integrity, such as a cyclical redundancy check (CRC) feature and/or a checksum feature. For example each message sent over the module buses 22a,b may contain a CRC code, which is based on the remainder of a polynomial division of the message's data block. When the message is received, the receiving device either compares the CRC code of the message with one freshly calculated from the data block, or equivalent^, performs a CRC on the whole message and compares the resulting check value with an expected residue constant. If the check values do not match, then the message is determined to contain an error.

[0016] Each I/O assembly 14 handles a plurality of inputs and/or a plurality of

outputs. A typical control system has a plurality of I/O assemblies 14 handling inputs and/or outputs. The inputs may be analog inputs, digital inputs, thermocouple inputs or RTD inputs. The outputs may be analog outputs or digital outputs. The inputs and outputs (I/O) are typically powered by the sensors and control elements in the field. However, digital outputs may be powered by the I/O assembly 14, such as when the digital outputs are used to energize relay coils.

[0017] Each I/O assembly 14 comprises an I/O module 30 releasably mounted to an I/O base 32. Each I/O module 30 includes an outer housing enclosing one or more circuit boards. The circuit board(s) of each I/O module 30 includes a microprocessor 34 with memory and a plurality of communication circuits 36 for communicating over the module buses 22a,b. Conditioning circuitry on the circuit board(s) processes field inputs received from sensors in the field or control outputs received from the controller assembly 12, depending on whether the I/O module 30 handles inputs and/or outputs. More specifically, the conditioning circuitry converts between field signals (e.g., analog 4-20 mA, digital 24VDC etc.) and digital bus signals, such as by using analog-to-digital and/or digital-to-analog converters. The conditioning circuitry also conditions the signals received from or going to the field, such as by using switches, filters and multiplexers, and isolates the field signals from the controller assembly 12.

[0018] The controller assembly 12 includes a pair of redundant controller modules 50 releasably mounted to a controller base 52. Each of the controller modules 50 has a construction similar to each I/O module 30 and includes one or more circuit boards mounted inside an outer housing. The circuit board(s) in each controller module 50 includes a microprocessor 33 with memory and a plurality of the communication circuits 36 for communicating over the module buses 22a,b. The memory stores control programs that may be executed by the microprocessor 33 of each controller module 50. The control programs in each controller module 50 include one or more control loops, such as PID loops, which work on one or more field inputs to generate control outputs. The field inputs and control outputs are routed to and from the controller assembly 12 through the I/O assemblies 14 via the module buses 22a,b. Each controller module 50 is programmed with and can execute the same control programs; however, only one of

the controller modules 50 (the primary) executes the control programs to control the industrial process at any one time. If the primary controller module 50 fails, the other controller module 50 (the secondary) automatically takes over and executes the control programs to control the industrial process.

[0019] The controller base 52 has a plurality of Ethernet jacks 54 that are adapted to receive plugs of Ethernet cables 55, respectively. The Ethernet jacks 54 are connected to Ethernet foreign device interfaces 56 in the controller modules 50. In this manner, the controller modules 50 can communicate with other devices over Ethernet cables 55 plugged into the Ethernet jacks. More specifically, the controller modules 50 can communicate with other controller modules 50 (in other nodes) similarly connected to the Ethernet cables 55, and/or with an operator workstation 58 connected to the Ethernet cables 55. The controllers 50 may use a protocol, such as Modbus TCP, to communicate with other devices connected to the Ethernet cables. The operator workstation 58 may have a graphical user interface (GUI) that displays information from the controller modules 50.

[0020] As described above, each I/O module 30 and each controller module 50 includes a plurality of communication circuits 36 for communicating over the module buses 22a,b. More specifically, each I/O module 30 and each controller module 50 has four communication circuits 36, two for each module bus 22, with one being used for the clock line 24 and the other being used for the data line 26 of the module bus 22. Each communication circuit 36 is substantially the same. Thus, for purposes of brevity, only one communication circuit 36 will be shown and described, it being understood that the schematic representation and description apply to the other communication circuits 36 as well.

[0021] Referring now to Fig. 3, there is shown a communication circuit 36, which generally includes a transceiver 42, a power sense circuit 44 and a ground sense circuit 46. The transceiver 42 is connected between the microprocessor 33 or 34 and the module bus 22 and generally includes a driver 60 and a receiver 62. The driver 60 transmits signals from microprocessor 33 or 34 to the module bus 22, while the receiver 62 transmits signals from the module bus 22 to the microprocessor 33 or 34. The

power sense circuit 44 is connected to the high side (VCC) of the driver 60, while the ground sense circuit 46 is connected to the low side (GND) of the driver 60.

[0022] The power sense circuit 44 is operable to sense the current of the high side of the driver 60, which is connected to a power source 64, such a 3 Volt DC power supply. The power sense circuit 44 may simply comprise a single resistor. Alternately, the power sense circuit 44 may comprise a differential amplifier connected across a main resistor 68. The differential amplifier includes an operational amplifier 70 and resistors 70, 72, 74, 76. An output of the differential amplifier is connected to a gain resistor 78. The differential amplifier 66 and the gain resistor 78 operate to increase the voltage differential across the main resistor 68 to provide a larger range of acceptable operating values. In this manner, an error value (outside the range) is more distinguishable, thereby reducing the number of false error indications. The output from the power sense circuit 44 is an analog signal representative of the current of the high side of the driver 60. This analog signal is fed to an analog-to-digital converter (ADC) 80 that converts the analog signal to a digital signal, which is then fed to the microprocessor 33 or 34.

[0023] The ground sense circuit 46 is operable to sense the current of the low side of the driver 60. The ground sense circuit 46 may simply comprise a single resistor. Alternately, the ground sense circuit 46 may comprise a single-ended amplifier connected between gain resistors 84, 86. The single-ended amplifier comprises an operational amplifier 82 with a negative feedback circuit having resistors 90, 92. The single-ended amplifier 82 and gain resistors 84, 86 operate to increase the voltage differential between the low side of the driver 60 and ground to provide a larger range of acceptable operating values. In this manner, an error value (outside the range) is more distinguishable, thereby reducing the number of false error indications. The output from the ground sense circuit 46 is an analog signal representative of the current of the low side of the driver 60. This analog signal is fed to the analog-to-digital converter (ADC) 80 that converts the analog signal to a digital signal, which is then fed to the microprocessor 33 or 34.

[0024] The microprocessor 33 in each controller module 50 receives from each of the communications circuits 36 in the controller module 50 the high side current signal

generated by the power sense circuit 44 and the low side current signal generated by the ground sense circuit 46. Similarly, the microprocessor 34 in each I/O module 30 receives from each of the communications circuits 36 in the I/O module 30 the high side current signal generated by the power sense circuit 44 and the low side current signal generated by the ground sense circuit 46. Thus, each microprocessor 33, 34 receives more than eight current signals.

[0025] The eight current signals are used by a module error detection program 100 in each I/O module 30 to determine whether one of the drivers 60 of the I/O module 30 has failed (e.g., shorted). In each I/O module 30, the error detection program 100 is stored in memory and executed by the microprocessor 34. With reference now to Fig. 4, the module error detection program 100 initially determines in steps 102, 104, 106, 108 whether a communication error has occurred on the clock lines 24 and/or the data lines 26 of the module buses 22a,b. This determination may be made using a CRC function or other data integrity function. If a communication error has occurred, the program 100 proceeds to step 110, 112, 114 and/or 116, as the case may be, where the program 100 waits until the driver(s) 60 for the faulted line(s) send a message to the faulted line(s). As soon as an affected driver 60 sends a message, the program 100 moves to step 120, 122, 124 and/or 126, as the case may be, where the program 100 determines whether the affected driver 60 has a high side current outside of a high range (such as from about 8 mA to about 14 mA) or a low side current outside of a low range (such as from about 2 imA to about 4 imA). In this regard, it should be noted that the determination of the high side and low side currents should be made contemporaneously with the transmission of a message by the driver 60.

[0026] If the affected driver 60 has a high side current outside the high range (such as 7mA or 15mA) or a low side current outside the low range (such as 1ma or 5mA), it is determined that the affected driver 60 has failed . In step 130, the program 100 determines whether any of the drivers 60 has a high side current or a low side current that is out of range. If one or more of the drivers 60 has a current out of range, the program 100 energizes a red LED 110 on the I/O module 30 in step 132 to provide a visual indication of the error. In addition, the program 100 in step 134 transmits an error

message to the primary controller module 50a over the module bus 22a,b that does not have the communication error. The error message includes the address of the I/O module 30 and informs the primary controller module 50a that a communication error was detected and that one of the drivers 60 has been determined to have failed. The error message may also identify the line (clock or data), whose driver 60 has failed. If in step 130, the program 100 determines that none of the drivers 60 has a high side current or a low side current that is out of range, the error detection program 100 in step 136 transmits a status message to the primary controller module 50a over the module bus 22a,b that does not have the communication error. The status message includes the address of the I/O module 30 and informs the primary controller module 50a that a communication error was detected, but none of the drivers 60 in the I/O module 30 have been determined to have failed.

[0027] Each controller module 50 also has a module error detection program stored in memory. However, only the primary controller module 50a executes the program (with its microprocessor 33) to determine whether one of its drivers 60 has failed. The module error detection program in each controller module 50 is the same as the error detection program 100 utilized in the I/O modules 30, except it does not include steps 134 and 136.

[0028] In addition to its module error detection program, each controller module 50 also has a system error detection program 150 stored in memory. However, only the primary controller module 50a executes the system error detection program 150 (with its microprocessor 33). Referring now to Fig. 5, the system error detection program 150 initially determines in step 152 whether a communication error has occurred on the clock lines 24 and/or the data lines 26 of the module buses 22a,b. If no communication error has occurred, the program 150 proceeds to step 154 to determine whether any status messages from the I/O modules 30 have been received. If a status message has been received from an I/O module 30 (indicating that the I/O module 30 has detected a communication error, but that no drivers 60 have been determined to have failed), then the program 150 determines that a receiver 62 in the I/O module 30 may have failed (e.g. shorted). In step 156, the primary controller module 50a sends a notification of this

error (and identifying the affected I/O module 30) to the operator workstation 58, where it may be displayed on the GUI.

[0029] If in step 152, the program 150 determines that a communication error on a particular bus 22a,b has occurred, the program 150 proceeds to step 158 to determine whether it has received an error message from one of the I/O modules 30 or if the module detection program of the primary controller module 50a has determined that one of its drivers 60 has failed. If no error message has been received and the module detection program of the primary controller module 50a has determined that none of its drivers 60 have failed, then the program 150 proceeds to step 160, where the program 150 determines whether any status messages have been received. If one or more status messages have been received, the program 150 determines that the particular bus 22a,b itself may have failed and sends a notification of this error in step 162 to the operator workstation 58, where it may be displayed on the GUI. If, in step 160, no status messages have been received, the program 150 determines that one of the receivers 62 of the primary controller module 50a may have failed. In step 164, the primary controller module 50a sends a notification of this error to the operator workstation 58, where it may be displayed on the GUI.

[0030] If in step 158, the program 150 determines it has received one or more error messages from the I/O modules 30 or the controller's own module detection program has determined that one or more of its drivers 60 have failed, then the program 150 proceeds to step 168, where the program 150 determines the module(s) having a failed driver 60. In stepl 70, the primary controller module 50a sends an error message identifying the module(s) having a failed driver 60 to the operator workstation 58, where it may be displayed on the GUI.

[0031] It is to be understood that the description of the foregoing exemplary embodiment(s) is (are) intended to be only illustrative, rather than exhaustive, of the present disclosure. Those of ordinary skill will be able to make certain additions, deletions, and/or modifications to the embodiment(s) of the disclosed subject matter without departing from the spirit of the disclosure or the scope of the appended claims. For example, each receiver 62 in the controller modules 50 and the I/O modules 30 may be provided with a power sense

circuit 44 and a ground sense circuit 46 for detecting current on the high and lows sides of the receiver 62, respectively. However, it has been determined that doing so is typically not needed because most communication errors are caused by a failure of a driver. Thus, a typical control system provided in accordance with this disclosure does not include sense circuits for the receivers in its modules.

What is claimed is:

1. A control system for controlling a process, the control system comprising:

a module bus over which information may be transmitted;

a controller module connected to communicate over the module bus, the controller module being programmed to perform operations for controlling the process using data transmitted over the module bus;

a plurality of I/O modules connected to communicate with the controller module over the module bus, each I/O module including:

a microprocessor with memory;

a driver for sending information to the module bus and having a high side connected to a voltage source and a low side connected to ground; and

a sense circuit for detecting current on the high side of the driver; and

wherein the microprocessor is operable to execute computer-executable instructions stored in the memory to perform an I/O module error detection method that comprises determining whether the current on the high side of the driver measured by the sense circuit is outside of a predetermined high range and, if so, determining that the driver has failed.

2. The control system of claim 1, wherein the I/O module error detection method further comprises determining whether a communication error has occurred on the module bus and, if so, then performing the step of determining whether the current on the high side of the driver measured by the sense circuit is outside of a predetermined high range.

3. The control system of claim 2, wherein the step of determining whether a communication error has occurred on the module bus is performed using a cyclical redundancy check function.

4. The control system of claim 1, wherein the sense circuit is a power sense circuit and wherein each I/O module further includes a ground sense circuit for detecting current on the low side of the driver, and wherein the I/O module error detection method further comprises determining whether the current on the low side of the driver measured by the ground sense circuit is outside a predetermined low range and, if so, determining that the driver has failed.

5. The control system of claim 4, wherein the I/O module error detection method further comprises determining whether a communication error has occurred on the module bus and, if so, then performing the steps of determining whether the current on the high side of the driver measured by the power sense circuit is outside a predetermined high range and whether the current on the low side of the driver measured by the ground sense circuit is outside a predetermined low range.

6. The control system of claim 1, wherein the module bus is a first module bus;

wherein the driver is a first driver for sending information to the first module bus and the sense circuit is a first sense circuit for detecting current on the high side of the first driver;

wherein the control system comprises a second module bus;

wherein the I/O modules each further comprise:

a second driver for interfacing with the second module bus, the second driver having a high side connected to the voltage source and a low side connected to ground;

a second sense circuit for detecting current on the high side of the second driver;

wherein the I/O module error detection method further comprises determining whether the current on the high side of the second driver measured by the second sense circuit is outside the predetermined high range and, if so, determining that the second driver has failed.

7. The control system of claim 6, wherein the I/O module error detection method further comprises:

sending an error message about the failure of the first driver over the second module bus to the controller module if the first driver is determined to have failed; and

sending an error message about the failure of the second driver over the first module bus to the controller module if the second driver is determined to have failed.

8. The control system of claim 6, wherein the first and second sense circuits are first and second power sense circuits and wherein each I/O module further includes first and second ground sense circuits for detecting current on the low side of the first and second drivers, respectively, and wherein the I/O module error detection method further comprises:

determining whether the current on the low side of the first driver measured by the first ground sense circuit is outside the predetermined low range and, if so, determining that the first driver has failed; and

determining whether the current on the low side of the second driver measured by the second ground sense circuit is outside the predetermined low range and, if so, determining that the second driver has failed.

9. The control system of claim 8, wherein the I/O module error detection method further comprises:

determining whether a communication error has occurred on the first module bus and, if so, then performing the steps of determining whether the current on the high side of the first driver measured by the first power sense circuit is outside the predetermined high range and whether the current on the low side of the first driver measured by the first ground sense circuit is outside the predetermined low range; and

determining whether a communication error has occurred on the second module bus and, if so, then performing the steps of determining whether the current on the high side of the second driver measured by the second power

sense circuit is outside the predetermined high range and whether the current on the low side of the second driver measured by the second ground sense circuit is outside the predetermined low range.

10. The control system of claim 9, wherein the controller comprises:

a microprocessor with memory;

first and second drivers for interfacing with the first and second module buses respectively, each of the first and second drivers having a high side connected to a voltage source and a low side connected to ground;

a first power sense circuit for detecting current on the high side of the first driver;

a ground sense circuit for detecting current on the low side of the driver; and

wherein the microprocessor is operable to execute computer-executable instructions stored in the memory to perform a controller module error detection method that comprises:

determining whether communication errors have occurred on the first and second buses, respectively;

determining whether the current on the high side of the first driver measured by the first power sense circuit is outside a predetermined high range if a communication error has occurred on the first bus;

determining whether the current on the low side of the first driver measured by the first ground sense circuit is outside a predetermined low range if a communication error has occurred on the first bus;

determining that the first driver has failed if either the current on the high side of the first driver is outside the predetermined high range or the current on the low side of the first driver is outside the predetermined low range;

determining whether the current on the high side of the second driver measured by the second power sense circuit is outside the predetermined high range if a communication error has occurred on the second bus;

determining whether the current on the low side of the second driver measured by the second ground sense circuit is outside the predetermined low

range if a communication error has occurred on the second bus; and

determining that the second driver has failed if either the current on the high side of the second driver is outside the predetermined high range or the current on the low side of the second driver is outside the predetermined low range.

11. The control system of claim 10, wherein the I/O module error detection method further comprises:

sending an error message about the failure of the first driver over the second module bus to the controller module if the first driver is determined to have failed; and

sending an error message about the failure of the second driver over the first module bus to the controller module if the second driver is determined to have failed.

12. A control system for controlling a process, the control system comprising:

first and second module buses over which information may be transmitted;

a controller module connected to communicate over the first and second module buses, the controller module being programmed to perform operations for controlling the process using data transmitted over one or more of the first and second module buses; and

a plurality of I/O modules connected to communicate with the controller module over the first and second module buses;

wherein the controller module and each of the I/O modules comprise:

a microprocessor with memory;

a driver for sending information to the first module bus and having a high side connected to a voltage source and a low side connected to ground; and

a power sense circuit for detecting current on the high side of the driver;

a ground sense circuit for detecting current on the low side of the driver; and

wherein the microprocessor is operable to execute computer-executable instructions stored in the memory to perform a module error detection method

that comprises:

determining whether a communication error has occurred on the first module bus;

if a communication error has occurred on the first module bus, determining whether the current on the high side of the driver measured by the power sense circuit is outside a predetermined high range and whether the current on the low side of the driver measured by the ground sense circuit is outside a predetermined low range; and

if either the current on the high side of the driver is determined to be outside the predetermined high range or the current on the low side of the driver is determined to be outside the predetermined low range, determining that the driver has failed.

13. The control system of claim 12, wherein the module error detection method in the I/O modules further comprises:

sending an error message to the controller module over the second module bus if the driver is determined to have failed; and

sending a status message to the controller module over the second module bus if the driver is determined not to have failed.

14. The control system of claim 13, further comprising a work station comprising a graphical user interface, and wherein the microprocessor in the controller module executes computer-executable instructions stored in the memory to perform a system error detection method that comprises:

determining whether a communication error has occurred on the first module bus;

determining whether any error messages have been received and whether the driver of the controller module is determined to have failed if a communication error is determined to have occurred;

determining whether any status messages have been received if it is

determined that no error messages have been received and the driver of the controller module has not failed;

determining that the first module bus has failed if it is determined that one or more status messages have been received;

sending a message to the work station that the module bus has been determined to have failed.

15. The control system of claim 14, wherein the controller module and the I/O modules each further comprise a receiver for receiving information from the first module bus, and wherein the system error detection method further comprises:

determining that the receiver of the I/O module has failed if it is determined that a communication error has not occurred and it is determined that a status message has been received from an I/O module; and

sending a message to the work station that the receiver of the I/O module has been determined to have failed.

16. The control system of claim 15, wherein the system error detection method further comprises:

sending a message to the work station that the driver of the I/O module has failed if it is determined that a communication error has occurred and an error message has been received from an I/O module.

17. A method of detecting errors in a process control system having a plurality of modules connected to communicate over first and second module buses, each module having a driver for sending information to the first module bus and having a high side connected to a voltage source and a low side connected to ground, the method comprising:

determining in each of the modules whether a communication error has occurred on the first module bus;

measuring the current on the high side of the driver in each of the modules where

a communication error has been determined to have occurred;

measuring the current on the low side of the driver in each of the modules where a communication error has been determined to have occurred;

comparing the measured current on the high side of the driver in each of the modules where a high side measurement has been made to a predetermined high range;

comparing the measured current on the low side of the driver in each of the modules where a low side measurement has been made to a predetermined low range; and

determining that the driver in one of the modules has failed if either the current on the high side of the driver is outside the predetermined high range or the current on the low side of the driver is outside the predetermined low range.

18. The method of claim 17, further comprising: in each of the modules, after a communication error is determined to have occurred, determining when a message is sent by the driver; and

wherein in each of the modules where a communication error has been determined to have occurred, the steps of measuring the currents on the high and low sides of the driver are performed when a message is determined to have been sent by the driver.

19. The control system of claim 18, further comprising:

if the driver in one of the modules is determined to have failed, displaying a notification of the failed driver on a graphical user interface of a work station of the control system.

20. The control system of claim 17, further comprising:

determining that the first module bus has failed if more than one of the modules detects a communication error on the first module bus and none of the drivers in the modules are determined to have failed.

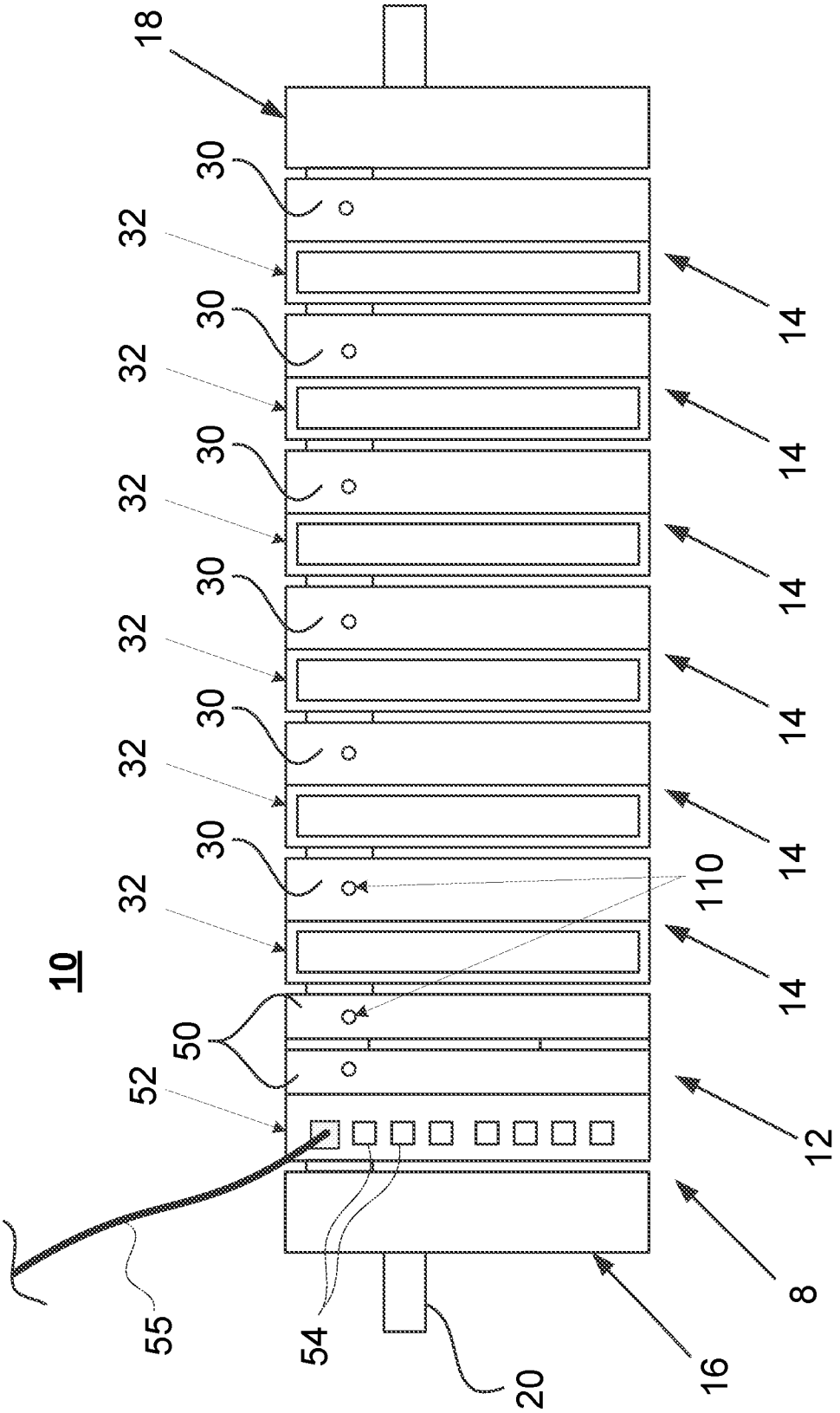

Fig. 1

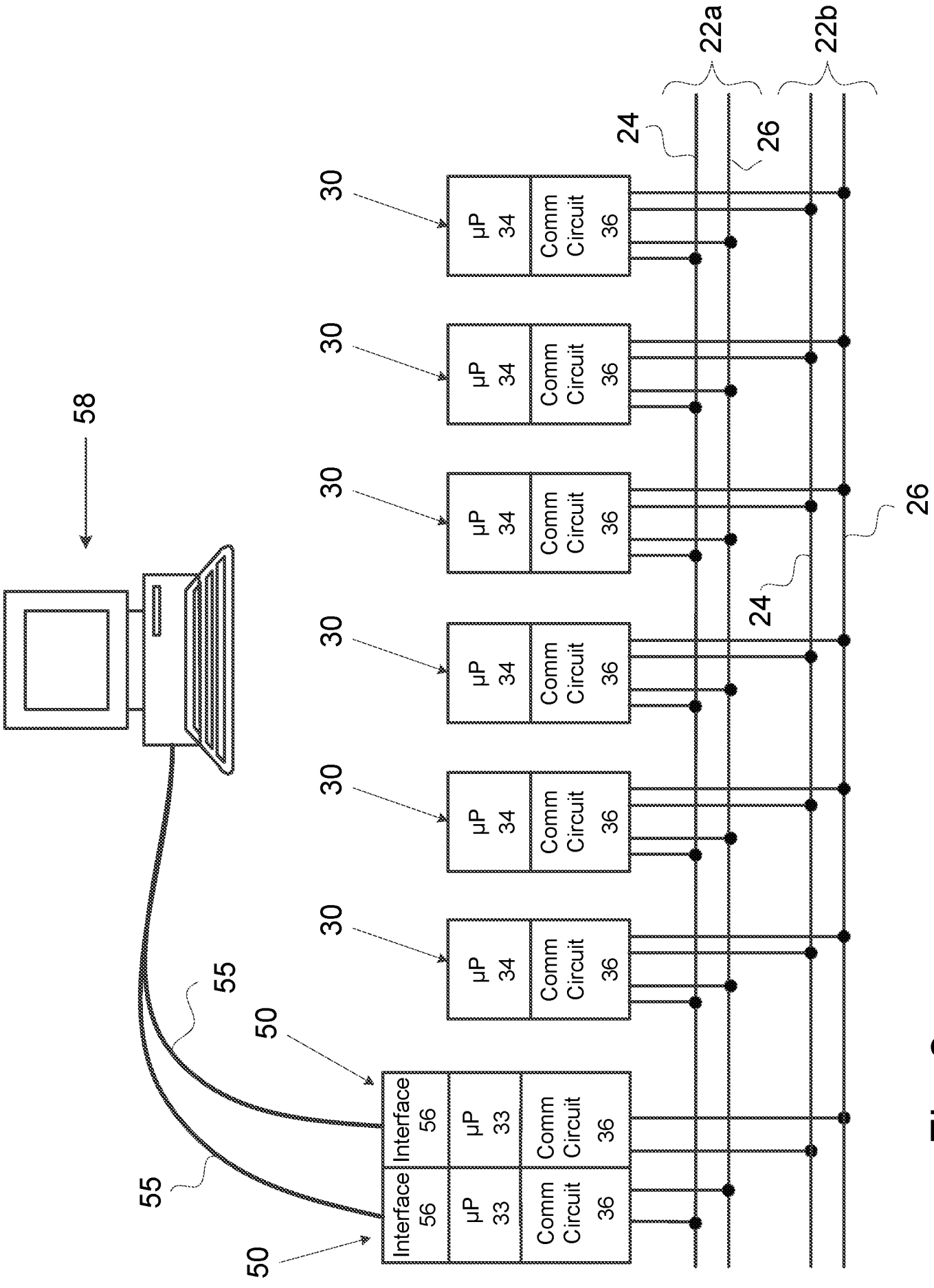
22a
22b
24
26
30
μP 34
Comm Circuit 36
58
55
50
Interface 56
μP 33
Comm Circuit 36

Fig. 2

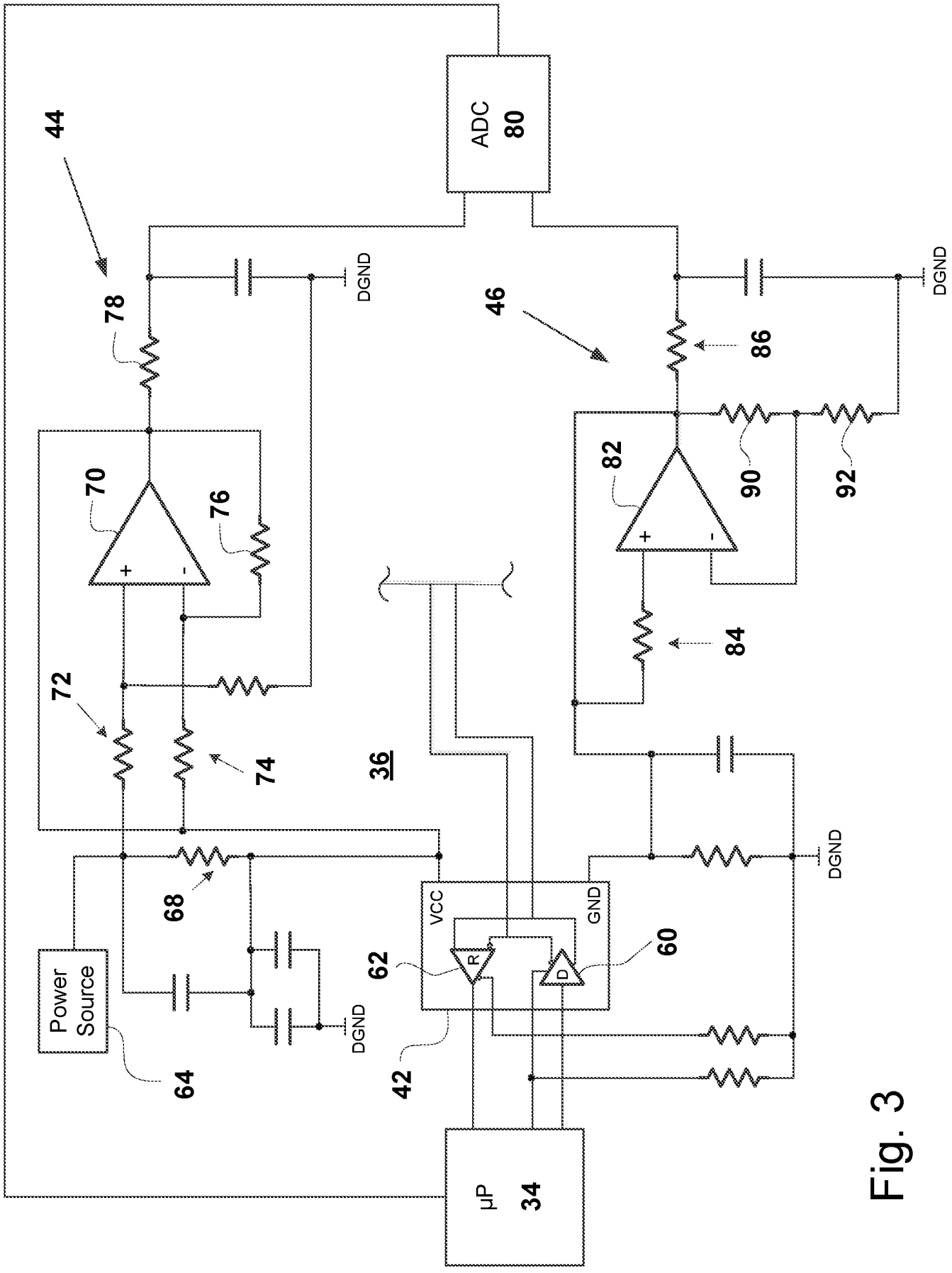
ADC
80
44
46
78
86
DGND
70
76
82
90
92
72
74
84
36
68
VCC
GND
R
D
62
60
Power Source
64
42
µP
34

Fig. 3

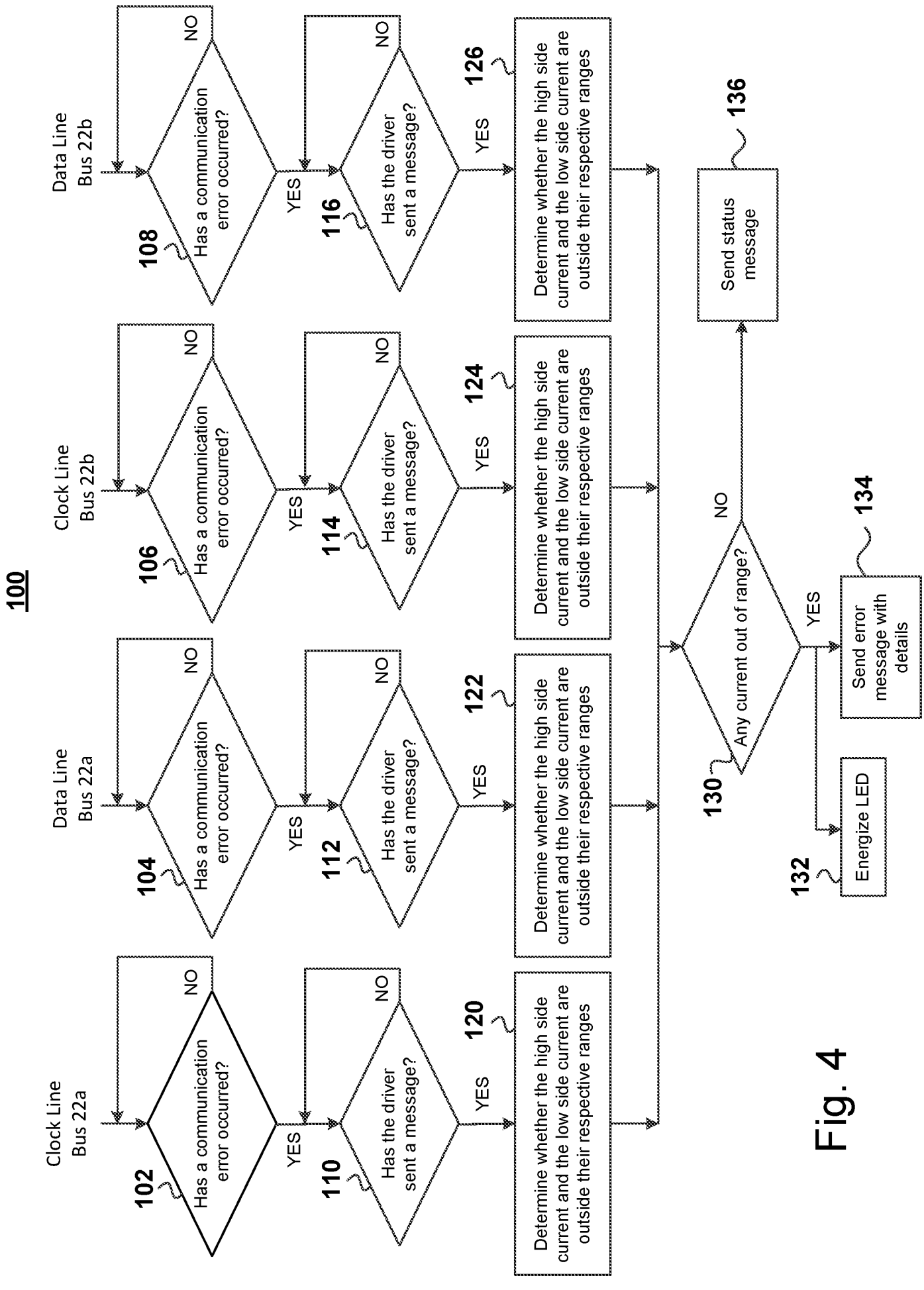
100
Clock Line Bus 22a
Data Line Bus 22a
Clock Line Bus 22b
Data Line Bus 22b
102 Has a communication error occurred?
104 Has a communication error occurred?
106 Has a communication error occurred?
108 Has a communication error occurred?
110 Has the driver sent a message?
112 Has the driver sent a message?
114 Has the driver sent a message?
116 Has the driver sent a message?
YES
NO
120 Determine whether the high side current and the low side current are outside their respective ranges
122 Determine whether the high side current and the low side current are outside their respective ranges
124 Determine whether the high side current and the low side current are outside their respective ranges
126 Determine whether the high side current and the low side current are outside their respective ranges
130 Any current out of range?
132 Energize LED
134 Send error message with details
136 Send status message

Fig. 4

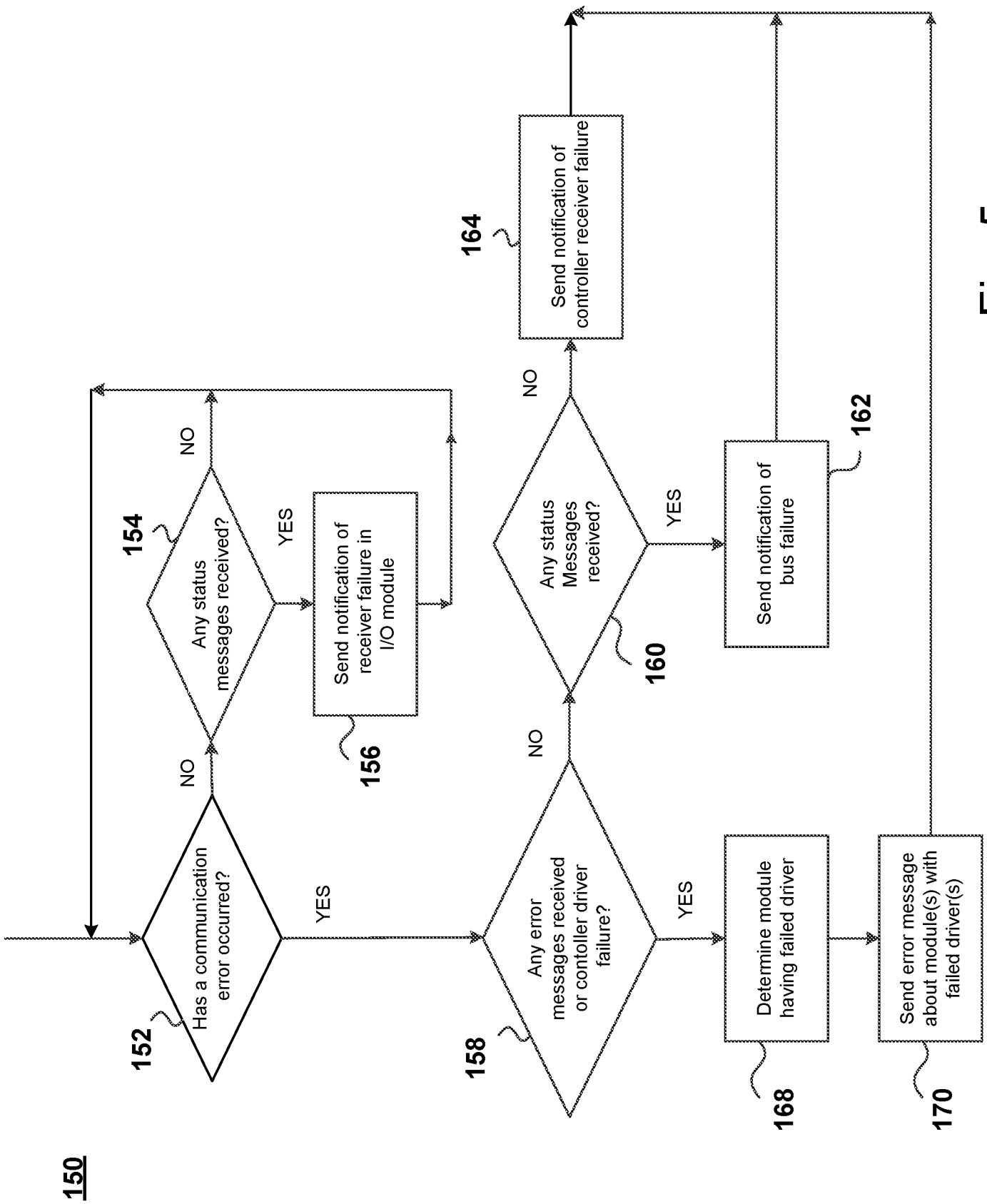
150
Has a communication error occurred?
152
NO
YES
Any status messages received?
154
NO
YES
Send notification of receiver failure in I/O module
156
Any error messages received or contoller driver failure?
158
NO
YES
Any status Messages received?
160
NO
YES
Send notification of bus failure
162
Send notification of controller receiver failure
164
Determine module having failed driver
168
Send error message about module(s) with failed driver(s)
170

Fig. 5

INTERNATIONAL SEARCH REPORT

Internationa l app licat ion No.
PCT/US 16/37837

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 11/00 (2016.01)
CPC - G06F1 1/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
CPC: G06F1 1/00; IPC(8): G06F 11/00 (2016.01); USPC: 714/48

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
CPC: G06F1 1/0793, G06F1 1/0709, H05K999/99, G06F1 1/0772, G06F1 1/0781 , G06F1 1/00; USPC: 714/763, 714/768, 714/718, 365/200, 365/201 , 714/48, 714/42, 714/774 (keyword limited; terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase; Google Scholar
Search Terms: I/O module bus controller microprocessor memory driver high side voltage low side ground measure detect communication error fail

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2013/0151919 A1 (HUYNH) 13 June 2013 (13.06.2013), entire document, especially abstract and para [0038], [0041]-[0045], [0047], [0061]-[0063], [0069]-[0073], [0084], [0087], [0090]-[0091], [01 12], [0123]-[01 24], Fig. 4A-4D, Fig. 18.	1-2, 4-12, 17-19 ---------- 3, 13-16, 20
Y	US 2014/0035481 A1 (PETING et al.) 06 February 2014 (06.02.2014), entire document, especially abstract and para [0053], [0147].	3
Y	US 2008/0086250 A1 (KUIVENHOVEN) 10 April 2008 (10.04.2008), entire document, especially abstract and para [0010]-[001 1], [0053], [0064].	13-16, *20*
A	US 2014/0301005 A1 (GENOVA et al.) 09 October 2014 (09.10.2014), entire document.	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 August 2016 (08.08.2016)	OR SEP 2016

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 2231 3-1450 Facsimile No. 571-273-8300	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774