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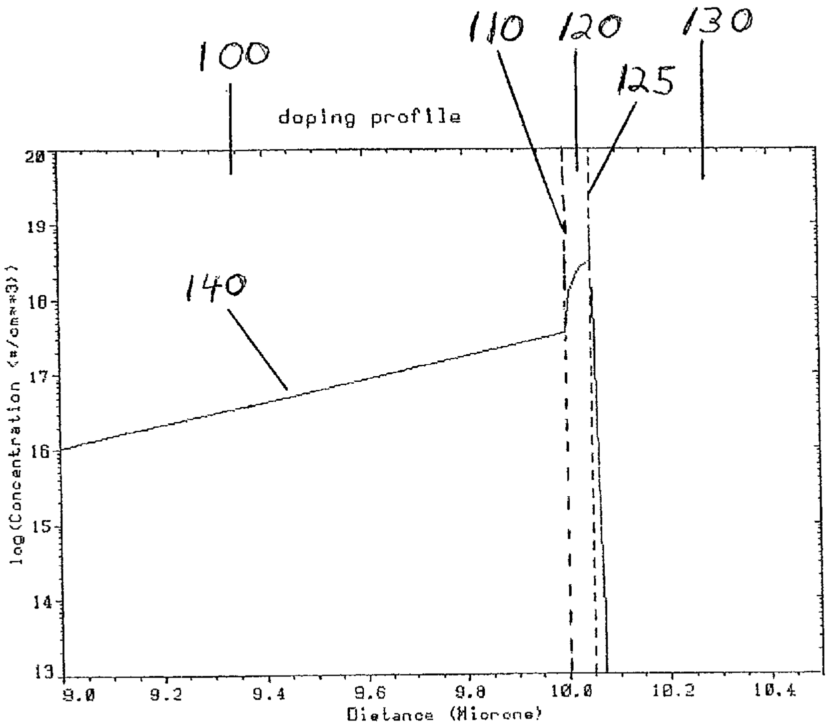
(54) **Title:** BACK-ILLUMINATED IMAGING DEVICE AND METHOD OF FABRICATING SAME



(57) **Abstract:** A method for fabricating a back-illuminated semiconductor imaging device on a thin semiconductor-on-insulator substrate, and resulting imaging device. Resulting device has a monotonically varying doping profile which provides a desired electric field and eliminates a dead band proximate to the backside surface.

WO 2006/086644 A2

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BACK-ILLUMINATED IMAGING DEVICE AND METHOD OF FABRICATING SAME

FIELD OF THE INVENTION

The field of invention is semiconductor device fabrication and device structure. More specifically, the field is fabrication and structure of back-illuminated semiconductor imaging devices.

BACKGROUND OF THE INVENTION

Thinned, back illuminated, semiconductor imaging devices are advantageous over front-illuminated imagers for high fill factor and better overall efficiency of charge carrier generation and collection. A desire for such devices is that the charge carriers generated by light or other emanation incident on the backside should be driven to the front side quickly to avoid any horizontal drift, which may smear the image. It is also desirable to minimize the recombination of the generated carriers before they reach the front side, since such recombination reduces overall efficiency and sensitivity of the device.

These desires may be achieved by providing a thin semiconductor layer and a high electric field within this layer. The field should extend to the back surface, so that the generated carriers, such as electrons or holes, can be driven quickly to the front side. This requires additional treatment at the backside of the device, which adds to complexity of the fabrication process. One current technique includes chemical thinning of semiconductor wafers and deposition of a "flash gate" at the backside after thinning. This requires critical thickness control of the backside flash gate. Another technique involves growth of a thin dopant layer on a wafer back using molecular beam epitaxy (MBE). Still another known method used to provide a desired electric field is to create a gradient of doping inside the thinned semiconductor layer by backside implant of the layer followed by appropriate heat treatment for annealing and activation.

These methods can not be easily included in conventional semiconductor foundry processing, and require more expensive custom processing. They are therefore often not cost-effective and not suitable for commercial manufacturing.

Back-illuminated imaging devices may be designed to operate at wavelengths ranging from less than 100 nanometers (deep ultraviolet) to more than 3000 nanometers (far infrared). An important factor that affects the sensitivity of back illuminated imagers is the absorption depth of radiation in the semiconductor bulk. In general, the radiation will be absorbed within a region close to the back surface of the device. For maximum device efficiency, all charge carriers generated in this region must reach optical detection components situated on the opposing front side of the device. A general method that is employed to increase the sensitivity of a thinned back-illuminated imager is to implant p-type or n-type dopant at the backside and, with later heat treatments, create a dopant concentration profile which decreases in the direction toward the front side of the thin substrate. In the case of p-type doping, such doping concentration gradient gives rise to an electric field tending to drive light-generated electrons toward the front side. In the case of n-type doping, such doping concentration gradient gives rise to an electric field tending to drive light-generated holes toward the front side.

For silicon imaging devices designed to operate in the deep ultraviolet (UV) wavelength range, the problem of getting the majority of generated carriers from the backside to the front side may be especially challenging, since the radiation is absorbed, and the carriers generated, within about 20 nanometers (nm) of the back surface. Careful tailoring of the electric field within a thin semiconductor layer may be particularly desirable for back-illuminated imaging devices in this wavelength range. This may be accomplished by introducing dopants to generate a desired internal electric field, as described above. When introducing the dopant by implantation, however, the doping concentration profile may have a maximum within about 20 nm from the back surface. The doping concentration will then be lower than the maximum in the first 20 nm or so from the back surface and this will cause the semiconductor electron energy bands to be lower near the surface, causing a "dead band". Stated another way, the electric field in the region within the first 20 nm or so of the back surface will tend to drive light-generated electrons toward the back surface, and trap them in that vicinity. Since, in silicon, most of the UV radiation is absorbed within the same approximately 20 nm region near the back surface, most of the generated electrons may be trapped in this dead band, resulting in poor sensitivity.

SUMMARY OF THE INVENTION

Disclosed is a method and resulting back-illuminated imaging device employing ultra-thin Semiconductor-on-insulator (UTSOI) substrates. The method is compatible with conventional semiconductor foundry processing. Starting with a UTSOI substrate, a semiconductor layer having a graded doping profile is created before front-side component fabrication.

A goal of inventive process is to create a desired dopant profile and a resulting electric field within a sufficiently thin semiconductor layer. The layer will include the region within which the radiation being detected is absorbed. Another goal of inventive process is to effectively eliminate a backside dead band by creating a desired dopant gradient within a sufficiently thin semiconductor layer.

SUMMARY DESCRIPTION OF THE DRAWINGS

Figures 1A, 1B, 1C, and 1D show an embodiment of process for fabricating a back-illuminated imaging device on a UTSOI substrate.

Figure 2 shows an initial doping profile in a semiconductor substrate.

Figure 3 shows a doping profile following growth of an epitaxial layer.

Figure 4 shows the doping profile of Figure 3 on a larger distance scale.

Figure 5 shows a complete device structure and associated doping profile resulting from an embodiment of process.

Figure 6 shows an actual doping profile, obtained by SIMS.

DETAILED DESCRIPTION OF THE INVENTION

The following embodiments are intended as exemplary, and not limiting. In keeping with common practice, figures are not necessarily drawn to scale.

Figures 1A, 1B, 1C, and 1D illustrate an embodiment of a process and a resulting structure. Figure 1A illustrates initial substrate 10 sometimes referred to in the art as an ultra-thin semiconductor-on-insulator (UTSOI) substrate. Figure 1B illustrates the state of process embodiment following growth of epitaxial layer 30. Figure 1C illustrates the state of process embodiment following a step of fabrication of imaging components 45 on and in epitaxial layer 30. As part of this step, one or more electrical junctions, or "pn-junctions" 40 are formed in epitaxial layer 30. Figure 1D illustrates a completed state of the process and the resulting imaging device. Details of each step follow.

Starting UTSOI substrate 10, shown in Figure 1A, is composed of mechanical substrate 25 to provide mechanical support during processing, insulator layer 20, and semiconductor substrate 15. In this embodiment mechanical substrate 25 may be a standard silicon wafer used in fabricating integrated circuits. Alternatively, mechanical substrate 25 may be any sufficiently rigid substrate composed of a material which is compatible with the steps of the method disclosed here. Insulator layer 20 may comprise an oxide of silicon with a thickness of about 1 micrometer in this embodiment. Among other embodiments, thickness of insulator layer 20 may fall in a range from about 10 nm to about 5000 nm. Semiconductor substrate 15 may be comprised of crystalline silicon having a thickness from about 5 nanometers to about 100 nanometers.

UTSOI substrates are available commercially and are manufactured by various known methods. In one method, thermal silicon oxide is grown on silicon wafers. Two such wafers are joined with oxidized faces in contact and raised to a high temperature. In some variations, an electric potential difference is applied across the two wafers and the oxides. The effect of these treatments is to cause the oxide layers on the two wafers to flow into each other, forming a monolithic bond between the wafers. Once the bonding is complete, the silicon on one side is lapped and polished to the desired thickness of semiconductor substrate 15, while the silicon on the opposite side of the oxide forms mechanical substrate 25. The oxide forms insulator layer 20.

Another method of fabricating a UTSOI substrate begins with obtaining a more standard semiconductor-on-insulator (SOI) wafer in which the semiconductor substrate (corresponding to 15 in Figure 1A) has a thickness in the range from about 100 nm to about 1000 nm. A thermal oxide is grown on the semiconductor substrate, using known methods. As the oxide layer grows, semiconductor material of the semiconductor substrate is consumed. Then the oxide layer is selectively etched off, leaving a thinned semiconductor substrate having a desired UTSOI thickness.

UTSOI substrates manufactured by an alternative method, known as Smart Cut™, are sold by Soitec, S.A.

Semiconductor substrate 15 may comprise silicon (Si), Germanium (Ge), SiGe alloy, a III-V semiconductor, a II-VI semiconductor, or any other semiconductor material suitable for the fabrication of optoelectronic devices.

Before further processing, semiconductor substrate 15 is doped. The purpose of this doping is to provide a source of at least one dopant which will form a desired dopant profile in later processing steps, as explained below. This initial doping may be accomplished in several known ways, such as diffusion from a gas, applying dopant directly to a surface of a semiconductor, or incorporating dopants during the formation of an ingot which is then cut into wafers. In addition, doping of semiconductor substrate 15 may be carried at any of various stages of making substrate 10. As one example, one or more dopants may be introduced during the formation of the ingot from which the wafer used to make semiconductor substrate 15 is cut. Alternatively, dopants could be introduced to that wafer after it is cut from the ingot.

In another alternative, depicted in Figure 1A, one or more dopants are introduced to semiconductor substrate 15 after this substrate is formed. This alternative is shown schematically in Figure 1A. Dopants 95 may be introduced into semiconductor substrate 15 by applying them through a face 57 opposite the interface 50 of semiconductor substrate 15 and insulator layer 20. Dopants 95 may be applied to face 57 by any of several known methods. As one example, dopants 95 may be diffused into semiconductor substrate 15 by immersing the entire starting substrate 10 in a furnace containing ambient gas which contains dopant. Alternatively, dopants 95 may be applied to face 57 in the form of a doped glass. A heat treatment then drives dopant from the glass into semiconductor substrate 15. The glass is then removed. In yet another example, dopants are implanted into semiconductor substrate 15 and then driven and activated by a heat treatment.

Dopants 95 are introduced into semiconductor substrate 15 in sufficient concentration to produce a desired net doping profile, as will be explained in more detail below. The initial net doping concentration in semiconductor substrate 15 may be on the order of 10^{17} charge carriers per cubic centimeter or higher, and may be either p-type or n-type. Common dopants include boron, phosphorous, antimony, and arsenic.

Referring to Figure 1B, epitaxial layer 30 is then grown on top of doped semiconductor substrate 15, using semiconductor substrate 15 as the template. Depending on the material of semiconductor substrate 15, epitaxial layer may comprise silicon (Si), Germanium (Ge), SiGe alloy, a III-V semiconductor, a II-VI semiconductor, or any other semiconductor material suitable for the fabrication of optoelectronic devices. Epitaxial layer 30 may have a thickness from about 1 micrometer to about 400 micrometers (depending on the wavelength or other properties of the radiation being detected), and provides a layer for fabricating front side components (45 in Figures 1C, 1D) which complete the overall imaging device. Still referring to Figure 1B, during the growth of epitaxial layer 30, dopants previously introduced into semiconductor substrate 15 diffuse into epitaxial layer 30. In one embodiment, disclosed in detail below in connection with Figures 2-4, epitaxial layer 30 is grown at a temperature at or above 1000 °C. At the conclusion of the growth, the net doping profile is very close to the desired profile, in that at each distance from interface 50, within the semiconductor substrate 15 and epitaxial layer 30, the net carrier concentration is close to its final desired value. All remaining steps in the process are then carried out at lower temperatures, so that relatively little diffusion of dopants takes place, and the profile is essentially unchanged at the end of the process. In an alternative embodiment, the profile immediately after growth of epitaxial layer 30 is significantly different from the desired one, but significant diffusion of dopants in later process steps results in the desired profile at the end of the process.

A goal of the exemplary process is the creation of a final net dopant concentration profile in semiconductor substrate 15 and epitaxial layer 30 which has a maximum value at interface 50 of semiconductor substrate 15 and insulator layer 20. It is also a goal that a final net dopant concentration profile desirably decreases monotonically with increasing distance from interface 50 within a portion of semiconductor substrate 15 and epitaxial layer 30 between interface 50 and junctions 40 shown in Figures 1C and 1D. (Junctions 40 are created during fabrication of front-side components 45, shown in Figures 1C and 1D.) Such a profile will give rise to an electric field within semiconductor substrate 15 and epitaxial layer 30 tending to drive photo-generated electrons toward the front side imaging components 45 and minimizing the trapping of these electrons near the backside.

It has been found that in back-illuminated devices having doping concentrations of the magnitude disclosed here (below) at the interface 50 of the semiconductor substrate and the insulator layer, the quantum efficiency of the device is more stable with respect to time and incident flux than in other similar imaging devices. This may be because essentially all charge-trapping states in the interface are initially filled from the dopant and remain filled, rather than becoming gradually filled over time while the device is illuminated. Quantum efficiency may be defined as the average number of charge carriers generated and imaged in the device for each incident photon or particle detected.

Referring to Figure 1C, once epitaxial layer 30 is grown, with the simultaneous formation of a desired dopant profile, one or more imaging components 45 may be fabricated using known methods of semiconductor fabrication These imaging components may include charge-coupled device (CCD) components, CMOS imaging components, photodiodes, avalanche photodiodes, phototransistors, or other optoelectronic devices, in any combination. Components 45 may include both CCD and CMOS components fabricated in separate areas of epitaxial layer 30 using known masking methods. Also included may be other electronic components such as CMOS transistors, (not shown) bipolar transistors (not shown), capacitors (not shown), or resistors (not shown). One or more p-n junctions 40 of various depths may be formed during the fabrication of imaging components 45.

Referring to Figure 1D, the last steps of the process include removal of mechanical substrate 25. Once the fabrication of components 45 is complete, substrate 25 is no longer needed to provide mechanical stability. Removal of mechanical substrate 25 may also be desirable in order to allow the emanation being detected to reach the backside semiconductor. Removal of mechanical substrate 25 may be accomplished by such methods as chemical etching, mechanical grinding, or a combination of these methods. With chemical etching, mechanical substrate 25 may be removed selectively, without removing insulator layer 20.

Alternatively, at least a portion of mechanical substrate 25 may be left in place (not removed) if the remaining portion at least partially transmits the radiation or particles being detected and imaged.

If mechanical substrate 25 is entirely removed, insulator layer 20 may be removed, either partially or entirely, by chemical or physical methods or a combination of the two. Figure 1D shows partially removed insulator layer 22. In one embodiment, insulator layer 22 is made to act as an anti-reflection coating for electromagnetic waves having wavelengths in a predetermined range, thereby allowing more photons to reach, and be absorbed in, the semiconductor layers 15, 30. This may be accomplished by reducing thickness of insulator layer 20 to a thickness which minimizes reflection in the predetermined wavelength range. The thickness may be determined by the wavelength range and the index of refraction of the material of layer 20 in this wavelength range. Explanations of how to do this may be found in any reference on the optics of thin films.

In one embodiment, imaging components 45 and antireflection coating 22 may be designed to operate in an ultraviolet region of the electromagnetic spectrum, for example in the wavelength range from about 100 to 400 nanometers. Alternatively, components 45 may be designed to operate in other regions of the electromagnetic spectrum, such as the x-ray, gamma ray, or visible region. In still another embodiment, components 45 may be designed to detect charged particles, such as electrons. Imaging components 45 may be designed to detect any form of emanation capable of interacting with solid matter and producing charge carriers within semiconductor regions 15 and 30.

Processing parameters such as doping levels, initial doping profiles, and temperatures are chosen to give a desired doping profile, as described above. As is common in semiconductor processing, choices of values of processing parameters, such as epitaxial growth temperature, may be guided by performing computer simulations of processes and the resulting dopant profiles and internal electric fields. Such simulations may be carried out using process simulation software such as SUPREM, available from Technology Modeling Associates, Inc. Figures 2 through 4 show the results of computer simulations of desired net doping profiles for an embodiment of inventive process. In these figures, various regions correspond to regions of the structures shown in Figure 1, as follows:

Region 150 corresponds to mechanical substrate 25. Region 130 corresponds insulator layer 20, comprising an oxide of silicon in this embodiment. Region 120 corresponds to semiconductor substrate 15, comprising silicon in this embodiment. Region 100 corresponds to epitaxial layer 30, comprising silicon in this embodiment. Number 125 corresponds to interface 50. Number 110 corresponds to interface 35.

Figure 2 shows an initial doping profile 135 in semiconductor substrate 120, before growth of epitaxial layer. In this embodiment boron is used as the dopant, and it may be introduced into semiconductor substrate 120 by any of the methods for introducing dopants described above. Initial profile 135 is created by boron doping (or, equivalently, net p-type doping) with a net p-type concentration of about 3×10^{18} carriers per cubic centimeter, assumed uniform through semiconductor substrate 120.

Figure 3 shows a net final doping profile 140 after growth of epitaxial layer 100. The net profile 140 in this embodiment is p-type; alternatively it could be n-type. Boron atoms starting in the semiconductor substrate 120 diffuse into epitaxial layer 100 during growth of that layer to produce what will become essentially final profile 140, as discussed above. Profile 140 in this simulated process embodiment has desired features: it has a maximum value at interface 125 of the semiconductor substrate and the insulator layer and decreases monotonically with increasing distance from interface 125 within semiconductor substrate 120 and epitaxial layer 100.

Figure 4 shows the same doping profile as Figure 3 on a larger scale of distance, in order to show essentially the entire profile. At some distance from interface 125 the monotonically decreasing portion 140 of the profile meets the background doping level 145 in the epitaxial layer 100. The doping level remains at this value 145 all the way to the junctions 40 (not shown in Figure 4). As long as net doping concentration 140, 145 does not increase with distance away from interface 125, carriers generated in the semiconductor substrate 120 or epitaxial layer 100 by waves or particles incident on the backside 60 will tend to be driven toward imaging components 45 and not in the opposite direction.

Figure 6 shows an actual doping profile obtained using Secondary Ion Mass Spectroscopy (SIMS). Two curves (300, 320) are shown. Curve 300 shows boron doping concentration variation with distance. Boron concentration is indicated on the left vertical axis. Curve 320, linked to the right vertical axis, is an indication of oxygen concentration, and serves to establish the locations corresponding to a silicon mechanical substrate 150A, a silicon oxide insulator layer 130A, and a silicon epitaxial layer 100A. As in Figures 2-4, vertical dashed lines indicate boundaries between these regions.

Figure 5 shows an embodiment of a complete laminated imaging device 250, with anti-reflection coating 22. For thin devices a sufficiently rigid lamination layer 340 may be added to provide mechanical stability. In the embodiment shown in Figure 5 a lamination layer 340 is shown on the front side of the device. Lamination layer 340 may be bonded to the front side of the wafer with a cement after concluding the fabrication of imaging components 45 and other front-side components. Alternatively, the lamination layer may be bonded to the back of the device. If the lamination layer is bonded to the back of a back illuminated device, lamination layer material, any cement used to bond the lamination layer, and any other materials between the lamination layer and the back of the device must be transparent to, and not degraded by, detected radiation 200.

Waves or particles 200 are incident on face 60 of the anti-reflection coating opposite to the face of epitaxial layer 30 where the imaging components 45 are fabricated. Figure 5 thus depicts a back-illuminated device. On the right side of Figure 5 is a reproduction of doping profile 140, 145 shown in Figure 4, thus indicating the doping concentration in semiconductor substrate 15 and epitaxial layer 30.

Although the invention is illustrated and described herein with reference to specific embodiments, the invention is not intended to be limited to the details shown. Rather, various modifications may be made in the details within the scope and range of equivalents of the claims and without departing from the invention.

What is claimed:

1. A method for fabricating a back-illuminated semiconductor imaging device, comprising the steps of:

growing an epitaxial layer on a substrate, the substrate comprising:

a mechanical substrate,

an insulator layer, and

a doped semiconductor substrate,

the epitaxial layer being grown on the doped semiconductor substrate, whereby the epitaxial growth process causes dopants from the doped semiconductor substrate to diffuse into the epitaxial layer, and;

fabricating one or more imaging components in the epitaxial layer.

2. The method of Claim 1, further comprising the step of removing at least a portion of the mechanical substrate.

3. The method of Claim 1, wherein the step of fabricating one or more imaging components in the epitaxial layer includes one or more steps of fabricating junctions in proximity to a face of the epitaxial layer, the face of the epitaxial layer being opposite a boundary between the semiconductor substrate and the epitaxial layer.

4. The method of Claim 3, further comprising the step of introducing one or more dopants in a semiconductor substrate to form the doped semiconductor substrate such that, upon completion of the step of fabricating one or more imaging components in the epitaxial layer, a net dopant concentration profile in the semiconductor substrate and the epitaxial layer results, the profile having a maximum value at an interface of the doped semiconductor substrate and the insulator layer and decreasing monotonically with increasing distance from the interface within a portion of the doped semiconductor substrate and the epitaxial layer between the interface and the junctions.

5. The method of Claim 4, wherein the step of introducing one or more dopants includes the step of applying dopants to the semiconductor substrate through a face of the semiconductor substrate opposite an interface of the semiconductor substrate and the insulator layer, the dopants being applied in sufficient concentration and over a sufficient distance within the doped semiconductor substrate such that, upon completion of the step of fabricating one or more imaging components in the epitaxial layer, a net dopant concentration profile in the doped semiconductor substrate and the

epitaxial layer results, the profile having a maximum value at the interface of the semiconductor substrate and the insulator layer and decreasing monotonically with increasing distance from the interface within a portion of the doped semiconductor substrate and the epitaxial layer between the interface and the junctions.

6. The method of Claim 2 further comprising the step of:

removing at least a portion of the insulator layer following complete removal of the mechanical substrate.

7. The method of Claim 6, wherein the step of removing at least a portion of the insulator layer results in a remaining insulator layer having a thickness such that the remaining insulator layer functions as an anti-reflection coating for electromagnetic radiation over a predetermined range of wavelengths.

8. A back-illuminated semiconductor imaging device configured to operate over a predetermined range of wavelengths, comprising:

an insulator layer;

a semiconductor substrate, having an interface with the insulator layer;

an epitaxial layer grown on the semiconductor substrate by epitaxial growth; and

one or more imaging components in the epitaxial layer in proximity to a face of the epitaxial layer, the face being opposite the interface of the semiconductor substrate and the insulator layer, the imaging components comprising junctions within the epitaxial layer;

wherein the semiconductor substrate and the epitaxial layer exhibit a net doping concentration having a maximum value at the interface of the semiconductor substrate and the insulator layer and decreasing monotonically with increasing distance from the interface within a portion of the semiconductor substrate and the epitaxial layer between the interface and the junctions.

9. The imaging device of Claim 8, wherein a doping concentration at the interface of the semiconductor substrate and the insulator layer is high enough to stabilize a quantum efficiency of the device with respect to time and incident flux.

10. The imaging device of Claim 8, wherein the insulator layer has a thickness selected to function as an anti-reflection coating over the predetermined range of wavelengths.

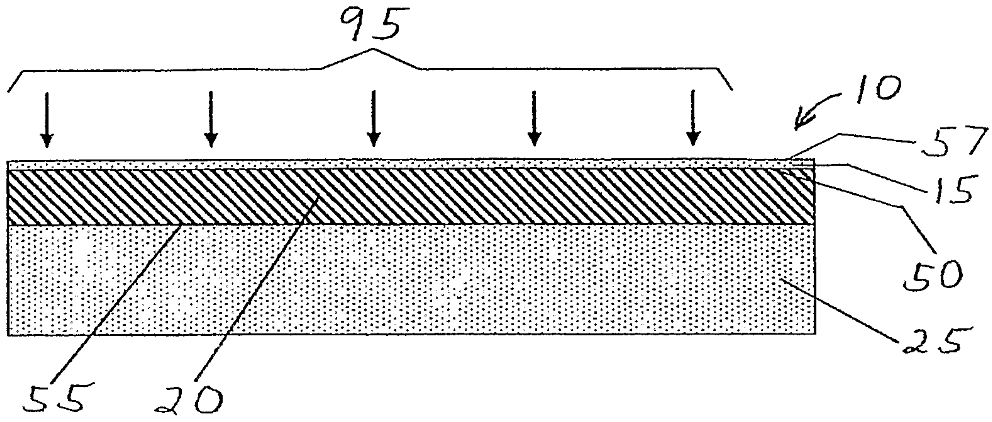


Fig. 1A

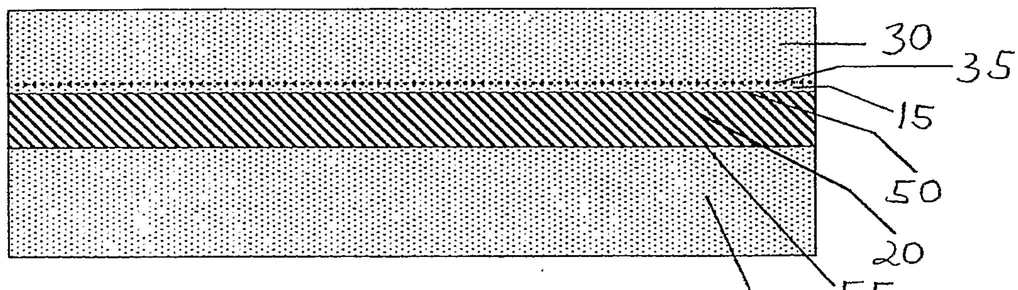


Fig 1B

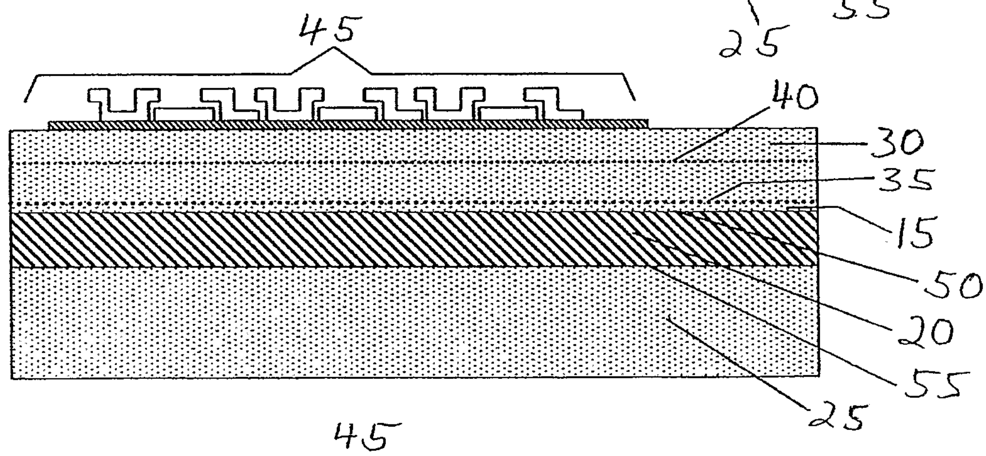


Fig. 1C

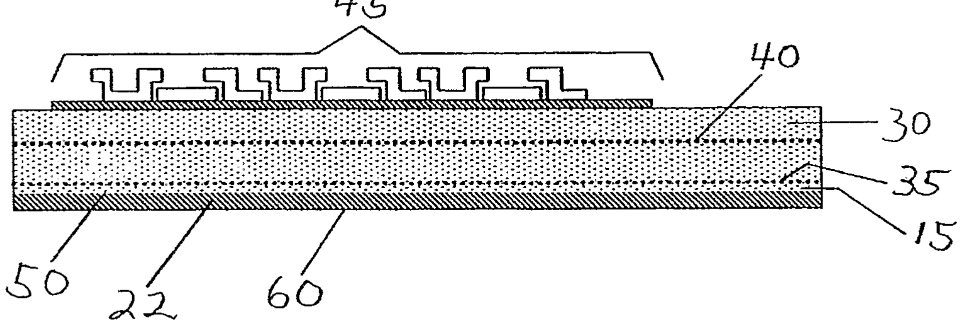
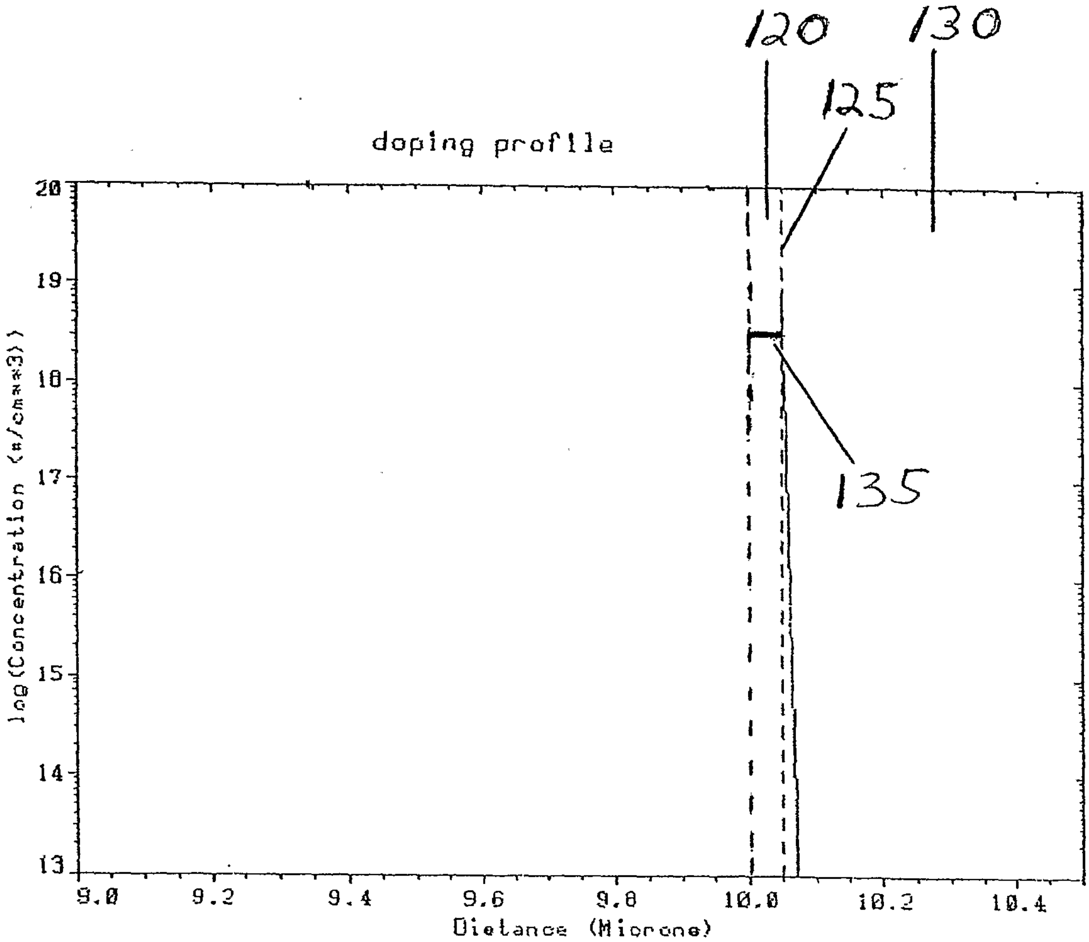


Fig. 1D


120
130
125
doping profile
135
20
19
18
17
16
15
14
13
log(Concentration (#/cm**3))
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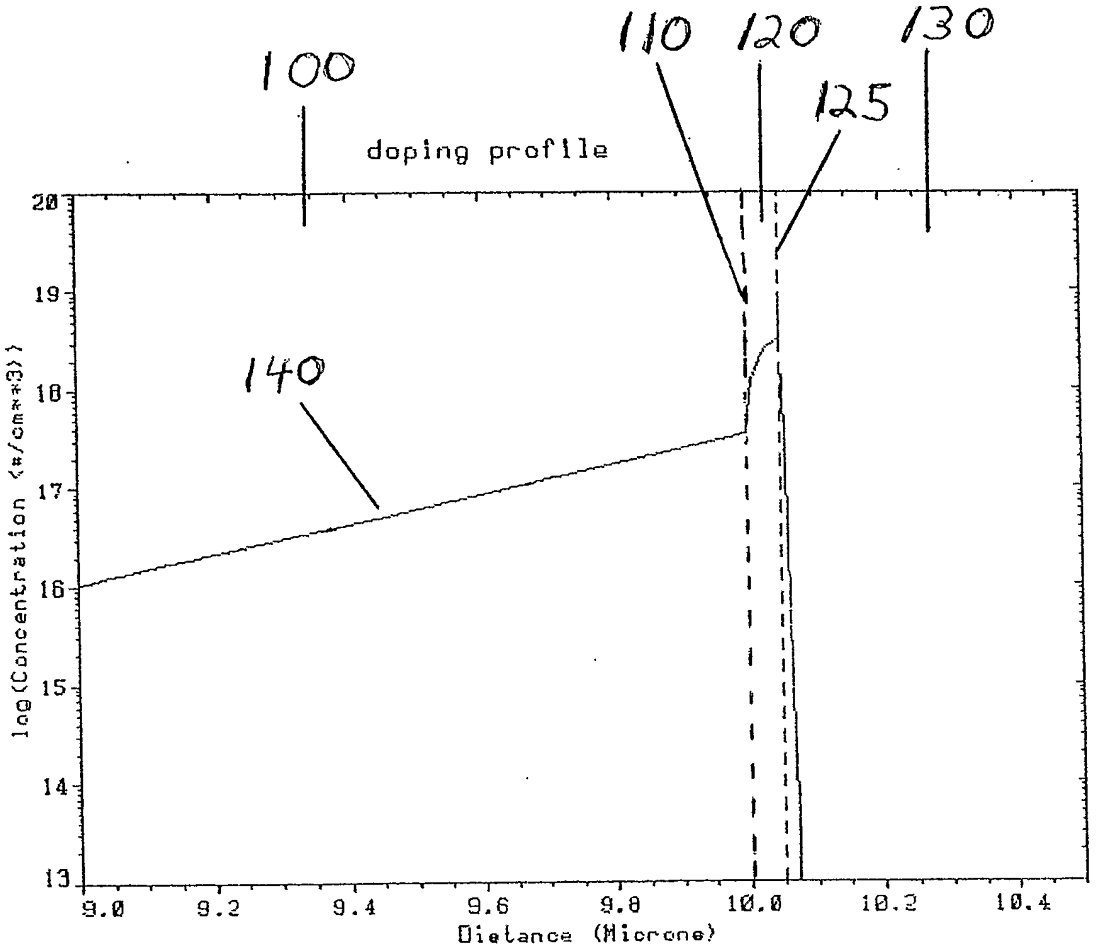
9.2
9.4
9.6
9.8
10.0
10.2
10.4
Distance (Microns)

Fig. 2


100
110
120
130
125
140
doping profile
log(Concentration (#/cm**3))
Distance (Microns)
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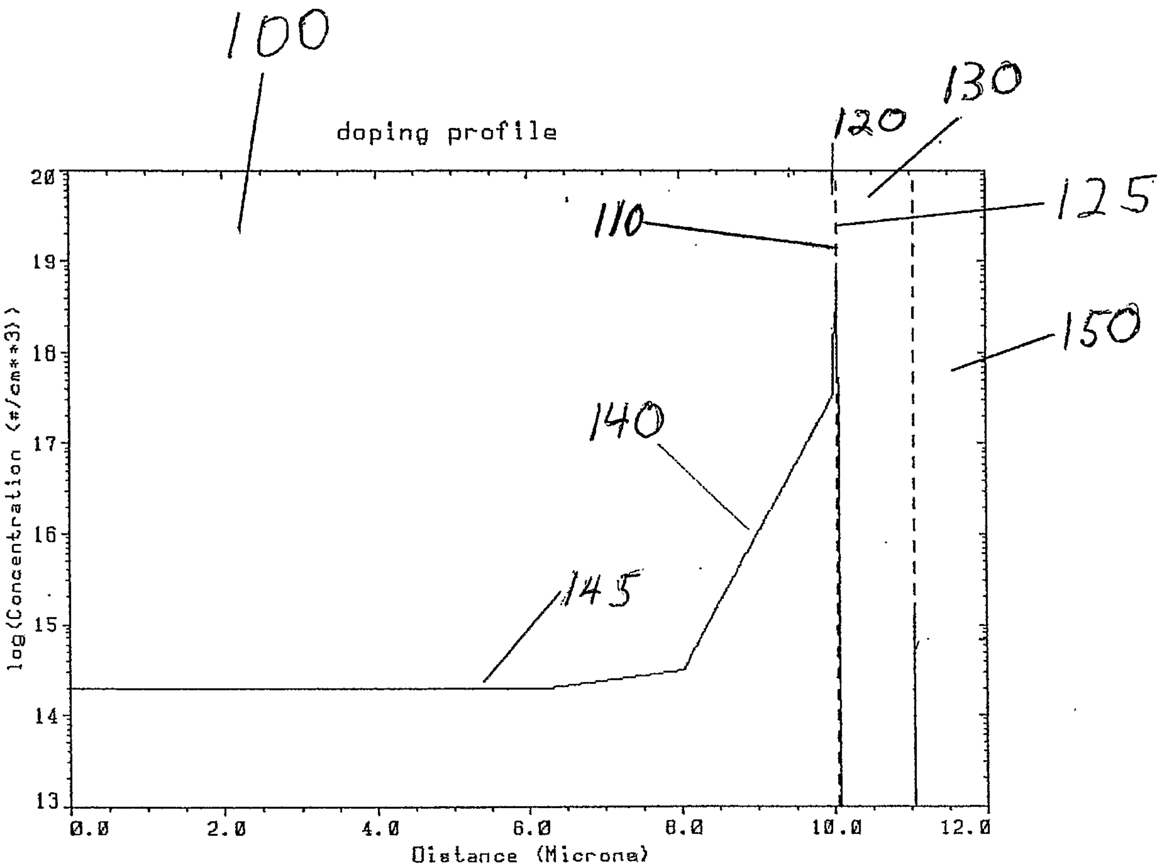
19
18
17
16
15
14
13
9.0
9.2
9.4
9.6
9.8
10.0
10.2
10.4

Fig. 3


100
doping profile
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130
125
110
150
140
145
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19
18
17
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12.0
Distance (Microns)

Fig. 4

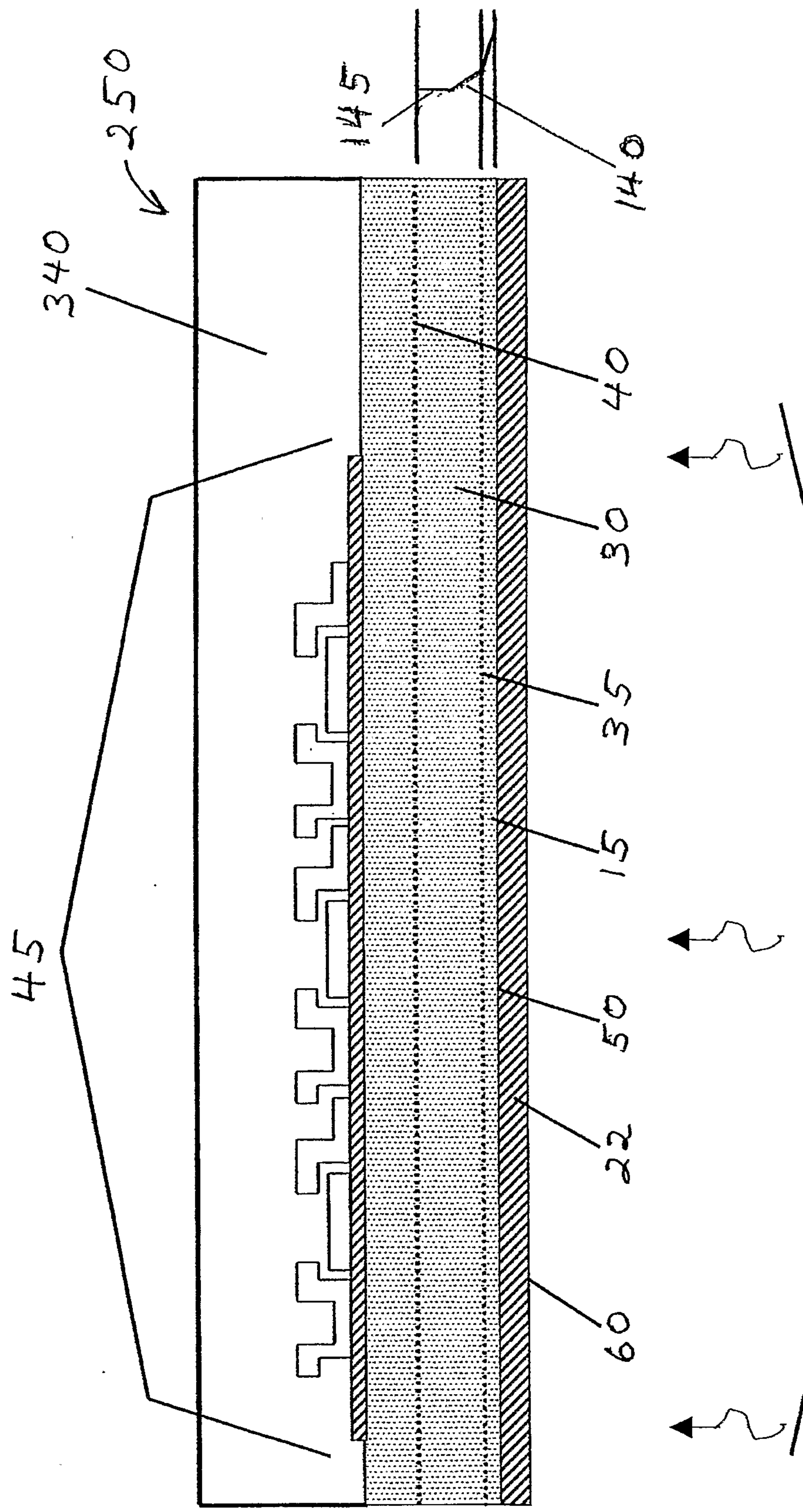
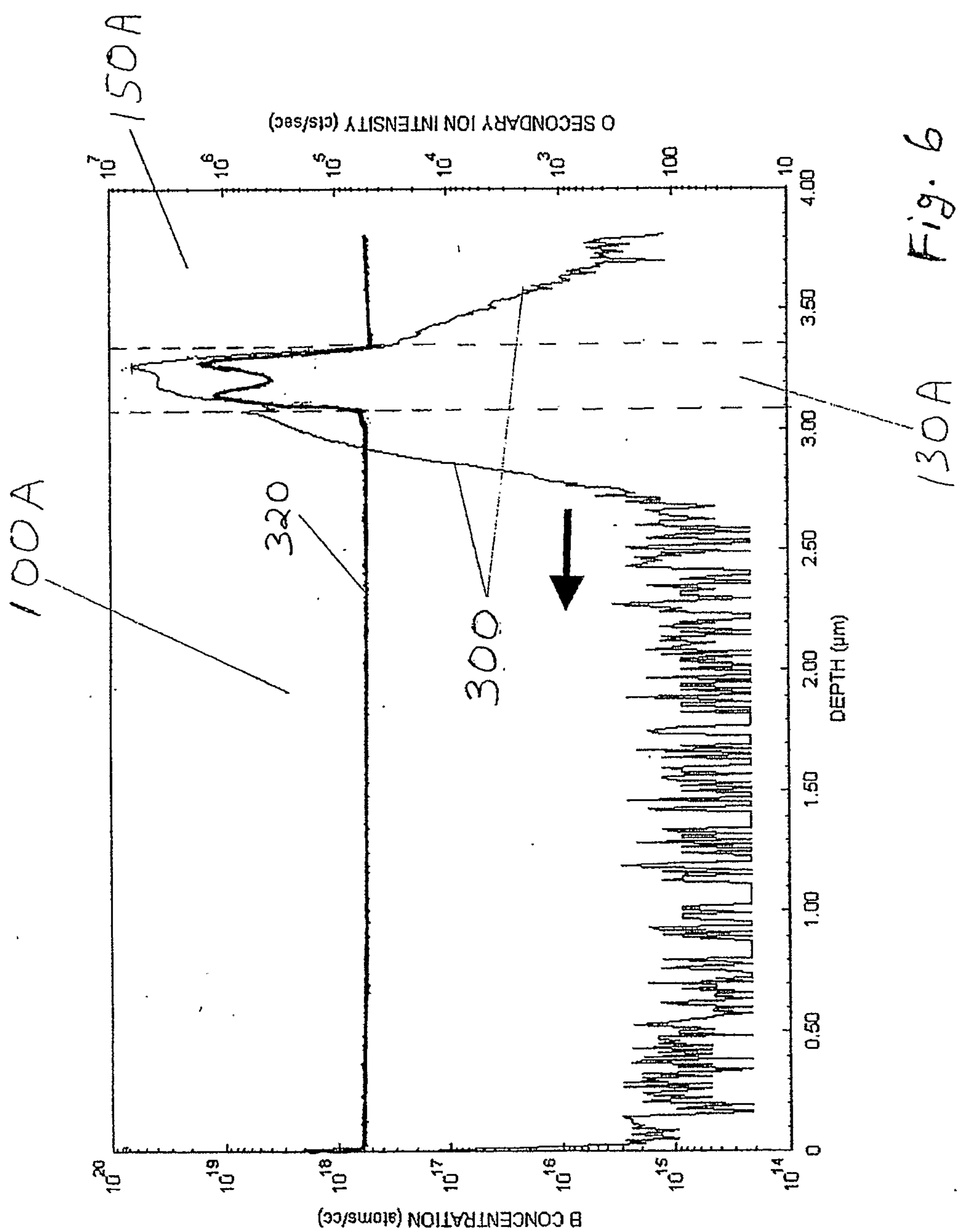


Fig. 5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B CONCENTRATION (atoms/cc)
DEPTH (μm)
100A
150A
130A
320
300

Fig. 6