(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 May 2013 (10.05.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/067118 A1

(51) International Patent Classification: ***H04L 25/02*** (2006.01)

(21) International Application Number: PCT/US2012/062965

(22) International Filing Date: 1 November 2012 (01.11.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/554,223 1 November 2011 (01.11.2011) US

(71) Applicant: NEWLANS, INC. [US/US]; 43 Nagog Park, Suite 215, Acton, MA 01720 (US).

(72) Inventor: GUPTA, Dev, V.; 356 Mattison Drive, Concord, MA 01742 (US).

(74) Agents: MEAGHER, Timothy, J. et al.; Hamilton, Brook, Smith & Reynolds, P.C., 530 Virginia Rd, P.O. Box 9133, Concord, MA 01742-9133 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- *with international search report (Art. 21(3))*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: WIDEBAND SIGNAL PROCESSING

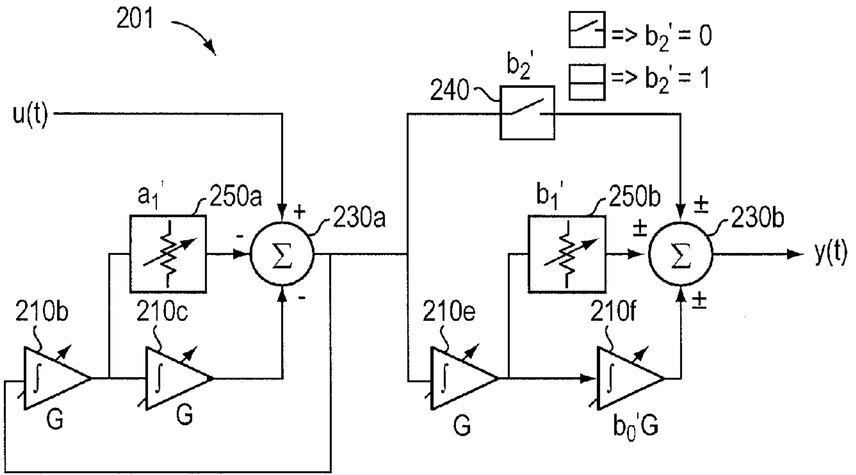


FIG. 21

(57) Abstract: A biquad wideband signal processing circuit can operate over bandwidths of 50 MHz to 20 GHz or more. The biquad circuit employs a configuration of integrators (transconductors), buffers, and scalable summers that can be implemented using deep sub-micron CMOS technology. Combining this scaling with high gain/high bandwidth enables implementation of feedback and programmability for broadband analog signal processing. A biquad circuit implementing a number of parallel integrator lines having adjustable gain provides greater accuracy, stability, and bandwidth, and allows for control of process variations and temperature variation in real-time.

WIDEBAND SIGNAL PROCESSING

RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 61/554,223, filed on November 1, 2011. The entire teachings of the above application are incorporated herein by reference.

BACKGROUND

Increases in signal bandwidth and data rates have prompted the development of new signal processing techniques to solve challenges associated with wideband signals. Increased signal bandwidth has also made new applications possible, including ultrawideband (UWB) technology-based active radio-frequency (RF) identification (ID) in heterogeneous environments. In addition, increasing signal bandwidth improves ranging accuracy, making wideband technologies especially attractive for radar, imaging, and other applications.

Unfortunately, fundamental scaling limits on clock speed, switching, heat dissipation, and difficulty of fault recovery make digital logic unsuitable for wideband signal processing. For example, today’s DSP technology cannot process the wideband signals required for emerging applications such as high-definition TV, software-defined radio, cognitive radio, 4-G handheld services, white spaces, UWB-based services, and real-time GHz/THz medical imaging. Beyond the need for greater speed and bandwidth processing capability, methods for reducing power consumption also have huge appeal and utility in many signal processing applications. For example, a huge premium is placed on power consumption in mobile devices; high-speed DSPs are a huge drain on the battery life of cell-phones and PDAs.

For wideband applications, the Nyquist rate is in the multiple giga-samples per second (GSPS) range and, hence, only relatively simple signal processing can be implemented and often requires highly pipelined and parallel processing architectures. Going forward, DSP technology is unlikely to reach the capabilities required by these applications because the limits of CMOS-based digital signal processing structures are not expanding according to Moore's Law any more. In fact, deep sub-micron CMOS gates have widths measured in molecules, suggesting that transistor sizes (and switching speeds) are nearing their fundamental limits. In other words, there is little room to increase the bandwidth processing ability of DSP technology because transistor switching speed, which is inversely related to transistor size, cannot get much faster.

Analog logic, in turn, has its own limitations. Because analog circuits are not formed of truly independent blocks, changing one block of analog logic can force changes in every other block in the circuit. In addition, advances in process technology occur so quickly that application-specific designs often become obsolete before they are fabricated. Finally, analog circuits are neither fully reconfigurable nor fully programmable.

SUMMARY

Example embodiments of the present invention include a biquad circuit for processing a wideband signal, operable (for example) over bandwidths of 50 MHz to 20 GHz or more. The circuit may include a first stage and a second stage, where the first stage includes a first summing circuit and a first plurality of integrator lines. The first summing circuit receives an input signal (e.g., a wideband signal to be processed), as well as an output of each of the first plurality of integrator lines. Each of the integrator lines includes one or more integrator circuits coupled in series, and receives an output of the first summing circuit. The second stage includes a second summing circuit and a second plurality of integrator lines. The second plurality of integrator lines each include at least one integrator circuit, and receive the output of the first summing circuit. The second summing circuit receives an output of each of the second plurality of integrator lines, and generates an output signal of the biquad circuit.

In further embodiments, the second stage may include a switch configured to selectively connect the output of the first summing circuit to the input of the second summing circuit. One or more of the integrator circuits of the integrator lines may include an adjustable gain to cause an adjustment of the biquad output signal. The first plurality of integrator lines may be connected to a common input node. Likewise, the second plurality of integrator lines may be connected to a common input node. The output of each of the first plurality of integrator lines may be inverted at the first summing circuit. Similarly, the output of each of the second plurality of integrator lines may be selectively inverted at the second summing circuit.

In still further embodiments, a loss pad may be implemented in place of one or more integrator circuits of the first and second integrator lines. The loss pad may be configured in a manner comparable to an integrator circuit as described above. In particular, the loss pad may be connected in parallel with an integrator line, connected to a common node, and may provide an input to a summing circuit that is inverted or selectively inverted.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing will be apparent from the following more particular description of example embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating embodiments of the present invention.

FIG. 1 is a block diagram of a biquad circuit.

FIG. 2 is a circuit diagram of an integrator circuit that may be implemented in an embodiment of the invention.

FIG. 3 is a chart illustrating a frequency response of the integrator circuit of Fig. 2.

FIG. 4 is a circuit diagram of an integrator circuit implementing a voltage-controlled resistor.

FIG. 5 is a circuit diagram of an integrator circuit in a further embodiment.

FIGs. 6(a)-(c) are circuit diagrams of integrator circuits in still further embodiments.

FIG. 7 is a circuit diagram of an integrator circuit configured with a tuner circuit.

FIG. 8 is a block diagram illustrating an input and output of an attenuator circuit.

FIG. 9 is a circuit diagram of an attenuator circuit.

FIG. 10 is a circuit diagram of an attenuator circuit that may be implemented in an embodiment of the invention.

FIG. 11 is a circuit diagram of an attenuator circuit in a further embodiment.

FIG. 12 is a chart illustrating distribution of attenuation values.

FIG. 13 is a circuit diagram of an attenuator circuit in a further embodiment.

FIG. 14 is a chart illustrating distribution of attenuation values corresponding to various configurations of an attenuator circuit.

FIG. 15 is a chart illustrating magnitude and phase of an attenuator circuit.

FIG. 16 is a circuit diagram of a summer circuit that may be implemented in an embodiment of the invention.

FIG. 17 is a circuit diagram of a circuit configured to measure output characteristics.

FIG. 18 is a chart illustrating frequency response of a summer circuit.

FIG. 19 is a block diagram of a configuration of biquad circuits in which embodiments of the invention may be implemented.

FIG. 20 is a block diagram of a biquad circuit in one embodiment.

FIG. 21 is a block diagram of a biquad circuit in a further embodiment.

DETAILED DESCRIPTION

A description of example embodiments of the invention follows.

Embodiments of the present invention include methods and apparatuses for wideband signal processing as described in U.S. Application No. 12/921,987 to Dev V. Gupta and Divi Gupta, published as U.S. Patent Pub. 2011/0051782, incorporated herein by reference in its entirety. Embodiments of the radio-frequency broadband analog component blocks may be constructed according to International Application No. PCT/US2011/024542 to Dev V. Gupta and Zhiguo Lai, incorporated herein by reference in its entirety.

Wideband Signal Processing (WiSP) is analog signal processing technology; that is, it implements programmable and executable analog computing over bandwidths from 50 MHz to 20 GHz or more. The underlying basis of WiSP is state variable theory, which, when combined with CMOS deep sub-micron technology, makes it possible to extend low-frequency signal processing techniques to micron and millimeter wavelengths. WiSP may be realized in complementary-metal-oxide-semiconductor (CMOS), silicon germanium (SiGe) technology, and silicon-on-insulator (SOI) technology.

WiSP is highly accurate because parameters of the state variable machines can be set to 10 bits of accuracy. WiSP is also frequency agile, as changing state variable parameters, such as gain, makes it possible to span the whole frequency band. For example, a state variable machine that is centered about a frequency of 1 GHz may be shifted to a frequency of 10 GHz just by changing the gain parameters. WiSP technology is suitable for both linear time invariant signal processing and time variant signal processing. State variable systems can be used in single input/output mode and in multiple input/multiple output (MIMO) mode—for example, in mimicking a MIMO wireless antenna system.

Conventional, low-frequency analog design is a relatively easy and exact science mostly because the components, such as capacitors, resistors, etc., and the traces that connect them on a printed circuit board (PCB) are so small compared to the wavelength of the signals being processed. There is no distributed effect, so the components may be treated as lumped elements. Also, low-frequency analog components typically have bandwidths that are larger than (e.g., at least ten times) the signal bandwidth. This relatively high bandwidth allows the use of feedback to simplify design, to stabilize systems, to improve system performance, to make them more accurate, etc. Feedback also allows implementation of programmable hardware; for instance, op-amps with some programmable resistors can be used to build programmable gain devices. Therefore, such programmability allows one to create complex systems using a programmable approach.

Unfortunately, conventional high-frequency design does not allow for the same advantages because the wavelengths of high-frequency signals are comparable to the size of the circuit elements. The traces connecting elements on PCBs are comparable in size to the wavelength of high-frequency signals. In conventional high-frequency design, traces are treated as transmission lines and designed with the levels and dimensions necessary to prevent reflection, etc., on the PCB. In general, such designs are very power hungry, and the materials of the PCB limit the bandwidth. Also, limits on the accuracy of the printed traces may prevent these distributed elements from interacting with each other. Further, conventional high-frequency designs do not permit use of the feedback that enables very accurate designs.

Making broadband analog devices on CMOS substrates rather than PCBs enables the use of low-frequency designs because the ratio of CMOS trace size to high-frequency wavelength is about the same as the ratio of PCB trace size to low-frequency wavelength. In fact, the small trace sizes using deep sub-micron CMOS technology is on the scale of nanometers, and at nanometers scales, everything may be treated as an element; in effect, the distributed nature of the circuits can be ignored. So on a CMOS substrate, high-frequency design is the same thing as low-frequency design on a PCB except for the fact that feedback is still unavailable because component bandwidth is not high enough.

Embodiments disclosed herein offer the high-gain and extra high bandwidth necessary to enable high-frequency CMOS designs with feedback. The underlying basic elements are transconductors that have very high gain, e.g., greater than 80 dB, and up to 100 dB or 120 dB, and bandwidths in the 200 GHz range. These transconductors also may be used to build an attenuator that is accurate to one least significant bit (LSB). These attenuators can be digitally programmed with 10-bit accuracy, or about 1 part in 1,000. Such accuracy allows us to build programmable analog hardware.

Combining transconductors and attenuators with broadband scaling information allows fabrication of biquads, which are basic building blocks for building broadband analog processors. In particular, the transconductors, attenuators, and scalable summers disclosed herein can be used to create programmable biquad structures that are frequency agile and/or time-variant. These biquads may be cascaded to form programmable transfer function synthesizers, as described in PCT/US2009/001512 to Gupta *et al.*, filed March 10, 2009, published as WO2009/114123, and incorporated herein by reference in its entirety. Biquad-based circuits can be used to make agile filters, equalizers, delay lines, etc., for end uses ranging from radar to cognitive radio to radio-frequency identification.

Fig. 1 is a block diagram of a biquad circuit 100. The biquad circuit 100 includes, as components, one or more integrators 110, attenuators 120 and summers 130. The characteristics of the biquad output $y(t)$ can be changed by altering the transfer function, $T(s)$, of the biquad 100. This is achieved by changing the values of the attenuators 120, which are comprised of a_0, a_1, b_o, b_1 and b_2. The center frequency of the transfer function is swept by changing the gain G of the integrators 110. The values of the attenuators 120 and the gain of the integrators 110 may be digitally controlled by a Serial Peripheral Interface (SPI), which has 12-bit accuracy.

Fig. 2 illustrates an integrator circuit 200 that may be implemented in the biquad circuit 100 of Fig. 1. The integrator 200 is a broadband self-tuned integrator using feedforward-regulated topology. The integrator 200 has a high bandwidth, high linearity and low intermodulation distortion which make it suitable especially for applications at microwave frequencies.

Small signal analysis shows that the transfer function of this circuit is of the form:

$$T(s) = \frac{\Omega_0 \cdot (s/z_1 - 1) \cdot (s/z_2 - 1)}{s \cdot (s/p + 1) + a_0}$$

where

$$z_1 = \frac{g_{m1}}{C_{gd1}}$$

$$z_2 = \frac{(g_{m3} + 1/R)}{C_{gd3}}$$

$$\Omega_0 = \frac{g_{m1} \cdot (g_{m3} + 1/R)}{(C_{gs3} + C_{gd3} + C_{gd1} + C_{ds1}) \cdot (g_{ds3} + 1/R) + (C_{gd3} + C_{ds3}) \cdot (g_{ds1} + 1/R) + C_{gd3} \cdot (g_{m3} + 2/R)}$$

$$p = \frac{(C_{gs3} + C_{gd3} + C_{gd1} + C_{ds1}) \cdot (g_{ds3} + 1/R) + (C_{gd3} + C_{ds3}) \cdot (g_{ds1} + 1/R) + C_{gd3} \cdot (g_{m3} + 2/R)}{(C_{gs3} + C_{gd3} + C_{gd1} + C_{ds1}) \cdot (C_{gd3} + C_{ds3}) - C_{gd3}^2}$$

$$a_0 = \frac{\left(g_{ds1} + 1/R\right)\cdot\left(g_{ds3} + 1/R\right) - \left(g_{m3} + 1/R\right)/R}{\left(C_{gs3} + C_{gd3} + C_{gd1} + C_{ds1}\right)\cdot\left(g_{ds3} + 1/R\right) + \left(C_{gd3} + C_{ds3}\right)\cdot\left(g_{ds1} + 1/R\right) + C_{gd3}\cdot\left(g_{m3} + 2/R\right)}$$

The resistor R is usually chosen to be small compared to $1/g_{m1}$, $1/g_{m3}$, $1/g_{ds1}$, and $1/g_{ds3}$. For deep submicron CMOS technology (for example 130 nm or below), it is usually true that C_{gs} dominates all the parasitic capacitance. In view of this, we have:

$$z_1 > \frac{g_{m1}}{C_{gs1}} \approx 2\pi \cdot f_T$$

$$z_2 > \frac{1}{R \cdot C_{gd3}}$$

$$p \approx \frac{1}{R \cdot C_{gd3}}$$

with f_T being the unity gain frequency which is usually large. For small R, z_2 and p are usually very large. The transfer function can hence be approximated as

$$T(s) \approx \frac{\Omega_0}{s + a_0}$$

Note that $a_0 = 0$ if R is chosen to be

$$R = \frac{g_{m3} - g_{ds1} - g_{ds3}}{g_{ds1} \cdot g_{ds3}}$$

This further simplifies the transfer function to

$$T(s) \approx \frac{\Omega_0}{s}$$

which is exactly the response of a perfect integrator. Note that the transistors are usually chosen such that $g_{m1} > g_{m3}$ hence

$$\Omega_0 \approx \frac{g_{m1}}{C_{gs3}} > \frac{g_{m3}}{C_{gs3}} \approx 2\pi \cdot f_T$$

This implies that the unity gain frequency of the integrator 200 is approximately the same as that of the technology.

Fig. 3 illustrates the frequency response of the integrator 200 as implemented in TSMC's 65 nm CMOS. The unity frequency is about 60 GHz. The magnitude has 20 dB/dec of roll off from about 10 MHz to 60 GHz while the phase is approximately -90° (within ±10°) from 50 MHz to 10 GHz.

Embodiments of an integrator circuit 200 as shown in Fig. 2 may be modified in a number of ways. As shown in the integrator circuit 400 of Fig. 4, the middle resistor R in Fig. 2 may be implemented using a transistor whose gate is connected to a voltage source. The resistance value (hence the value of a0 in the transfer function) can be varied simply by varying the voltage. This enables users to tune the integrator through a feedback control circuit as will be explained in the next section.

Fig. 5 illustrates a further embodiment of an integrator circuit 500, wherein the resistance of M2 (and M5) in Fig. 4 is controlled by the voltage VcR. Usually the resistance decreases as VcR increases. In order to prevent VcR to become too large, a fixed resistor can be added in parallel with M2 (and M5).

Figs. 6(a)-(c) illustrate still further embodiments of integrator circuit 601, 602, 603. In order to further improve the linearity, two source degeneration resistors can be added on top as shown in the integrator circuit 601 Figure 6(a). A slightly different approach is to split the current source into two identical ones and a single source degeneration resistor can be added between the two branches as shown in the integrator circuit 602 of Figure 6(b). In Figure 6(c), an integrator circuit 603 includes both top and bottom source degeneration resistors.

Fig. 7 illustrates an integrator circuit 701 (such as the integrator circuits described above with reference to Figs. 2 and 4-6) configured with an tuning circuit 702 to form an integrator tuning circuit 700. As described above, the voltage VcR must be chosen correctly in order to achieve a perfect integrator. This selection is done through the tuning circuit 702. The complete tuning circuit includes two parts, namely, DC calibration and gain control. In order for the DC calibration to work, two identical buffers (for example, source followers) are inserted in front of the integrator. One buffer is biased with a fixed voltage Vfix while the other one is controlled through a feedback loop which is simply an integration circuit that takes the differential outputs of the integrator as its inputs. The DC calibration circuit ensures the differential outputs of the integrator having approximately the same bias voltage. This eventually ensures the integrator to have a high common mode rejection when it is tuned.

As VcR varies, the DC-calibrated integrator may have significant phase variations at low frequencies and the phase varies monotonously with the VcR. The gain control circuit is hence essentially a phase detector that drives the DC-calibrated integrator to have the desired phase response at a given low frequency. As shown in Fig. 7, the oscillator generates a 200 kHz signal, which is fed to the integrator whose output is then amplified. The same 200 kHz signal is also fed to a phase shifter (PS) and a single-to-differential converter (S2D) and then amplified (using the same amplifier). Both amplified signals are fed to a multiplier. The DC component of the multiplier indicates the phase difference between the two amplified signals. More specifically, the DC value is maximized when they are in phase and is zero when the phase is 90 degrees out of phase. With a properly chosen phase value for the phase shifter, the integration circuit following the multiplier drives the integrator to have the desired phase response at 200 kHz, hence the desired VcR value.

Fig. 8 illustrates an attenuator circuit 800 with respective input and output signals. Attenuators reduce a signal in proportion to a given binary number specified by a processor or DSP. Attenuators are designed to be either “linear in voltage” or “linear in dB.” The attenuator 800 is a “liner in voltage” attenuator. A “linear in dB” attenuator is similar except the attenuation is carried out in dBs.

Applications of attenuators include signal processing elements in cellular networks, cable modems, digital subscriber loops, imaging systems, adaptive filters and equalizers used in diverse applications. Tens of millions of attenuators are sold in the microwave components markets and many times more are incorporated in VLSIs designs.

Fig. 9 illustrates a typical attenuator 900 employing a R/2R ladder. Typical attenuator designs use multistage resistive ladders to implement the attenuator function. There are as many stages as there are bits in the binary bits controlling the attenuation. As the desired accuracy grows the numbers of stages grow and the tolerances get worse. This limits the realizable dynamic range. In CMOS design this limits the usefulness of this structure to 6 to 8 bits and a dynamic range of 64 to 256. Higher accuracy is achievable with laser trimming, but this increases the cost. Also, each stage has an intrinsic bandwidth and as many stages are cascaded, the bandwidth decreases. Hence, if a low cost, broadband attenuator with 10 or more bits accuracy is desired this multistage resistive ladder architecture will not be useable.

Fig. 10 illustrates an attenuator circuit 1000 that may be implemented in embodiments of the invention, and that overcomes the limitations described above using a stochastic design technique. Here, a single stage attenuator 1000 consists of a group of resistors R that can be switched into the series arm (between the source and the output) or into the load arm (between the output and ground). Each resistor is either in the series arm or otherwise in the load arm.

If the resistors are arranged in the ratio R, 2R, 4R,…,(2N)R, then it is easy to show that we have a N-bit attenuator. Since the switches, which are either on or off FETs, typically have capacitance, we can expect that the larger resistors will create bandwidth problems. The smallest resistor has to be significantly bigger than the switches on impedance, so the largest resistor will be really big for N>9. This is a real problem for broadband performance. Also the largest resistor will become really big and this will use up a lot of silicon area. Accuracy will be compromised particularly with temperature since different families of resistors (with different thermal coefficients) will have to be used to accommodate the large range of resistor values, one family not having enough range.

The bandwidth problem can be mitigated by selecting FET switch sizes inversely proportional to the resistor size so the RC time constant of each arm is the same. Theoretically, this should give infinite bandwidth. However the ratio of the largest to smallest FET will become very large and there will be layout and silicon size problems because the smallest FET would have to be large enough to have mismatch related variance be small relative to the smallest resistor.

The attenuator 1000 uses N resistors to provide 2^N values of attenuation. Such an attenuator has N degrees of freedom since the designer can only set N values. If the attenuator is ideal, it will provide 2^N equally spaced points of attenuation on the number line going from 0 to 1. The distribution of attenuation values will thus be uniform (subject to 1/2^N binning) over the interval [0, 1]. In a non-ideal situation many bins will be empty and many bins will have multiple values. With laser trimming one can try to change the distribution to move the attenuation values to have a value present in every bin. But this is difficult and expensive.

Fig. 11 illustrates an attenuator circuit 1100 in a further embodiment. In some embodiments, there are M degrees of freedom (number of resistors) where $M > N$. One can create 2M points along the interval [0, 1]. By choosing the M resistors properly, one can create a distribution with multiple points in each of the 2^N bins. One can then do a Monte Carlo simulation with resistor/FET tolerances included to verify that a large percentage of results will still yield a distribution with at least one point in every bin. The finished product can then be calibrated by running through the 2^M points to determine the control M bit combinations that correspond to the 2^N desired values. This table can be stored in memory of size 2^N words each M bit long. When the N address lines are set up to the desired attenuation value, the memory puts out (on the data bus) the corresponding M bit value to the attenuator which then leads to the desired attenuation. If one desires N* bit accuracy with $N < N^* < M$ but is willing to put up with a few missing codes (e.g. near the 0 or 1 corner), then that program can be put into memory of size 2^N* words of size M. Such an embodiment is illustrated in the attenuator circuit 1100 of Fig. 11.

Fig. 12(a) illustrates a distribution of the achieved attenuation for an attenuator circuit having N-bit accuracy, M-degrees of freedom network with resistors R, 2R, …, (2N)R. Now if one dithers (changes) the values of each resistor by a uniformly distributed random variable lying in the interval (1 - x/100, 1 + x/100, i.e., an error of x percent), a typical realization for the same control bit pattern is shown in Figure 12(b). As can be seen, the distribution now has a spread around the values shown in Figure 12(a). This method can be used to fill in empty bins around some populated bins, especially in the middle of multiple populated bins. This result may be referred to as “smoothing the distribution.”

Fig. 13 shows a M bit (in this example $M = 24$) attenuator 1300 with N bit (in this example $N = 12$) accuracy. The maximum resistor (and hence FET switch) ratio is approximately 64. We begin with resistors R, 2R, 4R, 8R, 16R, 32R, 64R and add resistors of value 59R, 53R, 47R, 43R, 41R, 37R, 31R where the numbers 59, 47, 43, 41, 37, 31 are prime to the numbers 2, 4, 8, 16, 32, and 64. The resulting distribution is dithered to get the best possible distribution (maximum range of fill) in the 2N bins using x=5%. We then fill with resistors of value R until we have M resistors (here we add 10 resistors of value R).

Fig. 14 illustrates a distribution that results for N=10 to N=14 bins. A Monte Carlo simulation shows that FETs and resistors have approximately 1.5% variation under mismatch in 65 nm CMOS technology when minimum resistors of size R = 100 Ω and minimum FETs of size 0.12 μm are used. The simulations are configured with x set at 2%, and a long run shows that 500 out of 500 designs meet the requirement that for N=12, all but the two extreme bins 0 and 1023 of this 212 bins in the range [0, 1] have at least one element.

Fig. 15 illustrates the frequency domain performance of the attenuator 1300 for a specific loss pattern. In general, the attenuator exhibits greater than 10 GHz of bandwidth at all other attenuation values.

To calibrate a specific attenuator, one starts with the nominal design. One creates a table of bins and up to 10 control bit combinations distributed across each bin. Of course bins that have less than ten control bit combinations have all their elements listed.

For the attenuator being calibrated, one starts with bin i, (1 ≤ i ≤ = 2N), and the nominal control bit pattern for that bin. One measures the actual attenuation achieved and computes the error. The error is multiplied by 2N to determine how many bins to move to correct the error. The direction of movement depends on the polarity of the error. If the measured value is too high one moves in the direction of lower bin values and vice versa. The new control bit pattern is determined (some control pattern in the selected bin may give better values than others, here we retain the best) and the process repeated until the desired accuracy is achieved. In practice it has been found that one gets the desired accuracy in 2 to 3 steps.

The entire process is repeated for all the bins until one gets the entire table of 2N bin values and corresponding control bit patterns.

The methods described above provide a highly accurate, low cost, high bandwidth, high yield CMOS attenuator. For a desired N bit accuracy, we begin with M (M > N) resistors and switches. By choosing M sufficiently larger than N we get enough accuracy to statistically “guarantee” that a large percentage of attenuators will meet the N bit accuracy in spite of component tolerances. No laser trimming is required in the manufacturing process.

Further, methods for choosing the resistors for optimal distributions have been described. A method to calibrate a specific realization of the attenuator has been described. Although the example embodiments described above provide a “linear in voltage” attenuator, one of skilled in the art may apply the same methods to create a “linear in dB” attenuator.

Fig. 16 illustrates a summer circuit 1600 that may be implemented in the biquad circuit 100 described above with reference to Fig. 1, and in the biquad circuits 200, 201 described below with reference to Figs. 20 and 21. The summing circuit 1600 comprises a single resistor R and N transistors. The summer 1600 can be used in circuit topologies that require broadband analog signal processing. The number of transistors N is determined by the number of input signals that will be summed.

The summer receives input signals V_1, V_2, …, V_N, and provides output signal V_{out}, all of which contain the DC and the AC terms. The resistor R sets the DC current through the summing network and contributes to the overall gain of the summing block. By using superposition and therefore taking into account one transistor at the time, we are left to analyze a common source (CS) amplifier. By ignoring the DC bias term at the output and focusing only on the AC term, the output for CS amplifier is given by

$$v_o = -g_m v_{in} (R||r_o) . \qquad \text{Equation 1}$$

In Equation 1, term g_m is the gain of the transistor (*i.e.*, transconductance) and r_o is the output resistance of the transistor. Assuming that $r_o \gg R$ the overall output of the circuit in Figure 1 is given by

$$v_{out} = -(g_{m1} v_1 + g_{m2} v_2 + \cdots + g_{mN} v_N)R \qquad \text{Equation 2}$$

In Equation 2, the g_m terms that accompany the input signals can be viewed as the summing coefficients. Because the resistor R is fixed, we can adjust the summing coefficients by changing the transistor gain g_m. The transistor gain g_m can be expressed in terms of the transistor width W,

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN}) . \qquad \text{Equation 3}$$

According to Equation 3, the transistor gain is directly proportional to the transistor width and therefore by varying the transistor width we can adjust the summing coefficients.

The bandwidth of the summing circuit 1600 is determined by the CS amplifier bandwidth. Fig. 17 illustrates an equivalent small-signal circuit model 1700 that is commonly used in analyzing the high-frequency behavior of the CS amplifier. Resistor R_T is given by $R||r_o$ and capacitor C_T is the total capacitance between the output node and ground of the transistor (*i.e.*, load capacitance, internal parasitic capacitance of the transistor, and the input capacitance of the subsequent stages).

For applications where R_S is relatively large and C_T is relatively small the bandwidth of the CS amplifier.

$$f_{3dB} = \frac{1}{2\pi\left(C_{gs} + C_{gd}(1 + g_m R_T)\right)R_S} . \qquad \text{Equation 4}$$

For applications where R_S is small the bandwidth of the CS amplifier.

$$f_{3dB} = \frac{1}{2\pi(C_L + C_{gd})R_T} \qquad \text{Equation 5}$$

From above equation, it is shown that high bandwidth can be achieved with small R (since R_T is given by $R//r_0$) . This usually results in a loss. In order to reduce the loss or to get some gain, R needs to be increased, which usually compromises the bandwidth.

A 3-input summing circuit was constructed in Cadence using TSMC's 65 nm process. Fig. 18 shows the frequency response for the given circuit with the source resistance R_S set to 10 Ω. The solid lines correspond to the case with R = 26 Ω. The circuit has 5.4 dB of loss but has a 3-dB bandwidth of approximately 200 GHz. The dashed lines corresponds to the case with R = 60 Ω. The circuit has approximately 0 dB of loss and the 3-dB bandwidth is reduced to 90 GHz.

Fig. 19 illustrates a series of biquad circuits 1900 in which embodiments of the integrators, attenuators and summers described above may be implemented. The biquad configuration is a second order state variable structure. $2N^{th}$ order transfer function $T(s)$' is obtained by cascading N biquads.

The transfer functions shown in Fig. 19 also describe a single input single output (SISO) field programmable analog array (FPAA). By varying the values of the attenuators and the integrator gains, one can obtain an assortment of adaptive filter and delay line characteristics. The ability to work in the analog domain offers engineers a powerful tool to process wideband signals.

Turning again to Fig. 1, the biquad circuit 100 described above implements a second-order state variable structure that comprises two integration/gain stages, with variable gain attenuators operating within each stage. A combined signal based on a wideband input is fed to the first integration/gain stage, which, in turn, provides an input to the second integration/gain stage. Variable gain attenuators feeds signals forward (b's) and backward (a's) from the input and output of each of the two integrators. These signals terminate in a first summing block that combines feedback signals and second summing block that combines feed-forward signals. Example second-order state variable filters may also include fractional gain blocks and additional summers. Varying gains of the variable gain blocks changes a center frequency of the embodiment second-order state variable filters. The transfer function coefficients of a wideband signal processing filter constructed from the biquad circuit 100 are determined by the variable attenuator values.

Fig. 20 illustrates biquad circuit 200 in an example embodiment. The biquad circuit 200 implements a second-order state variable structure that comprise two integration/gain stages, each of which includes three variable gain integrators 210a-f, two of which are operably coupled to a summing block 230a-b. In particular, the first stage includes two integrator lines that are connected in parallel to the summer 230a, where one integrator line includes integrator 210a and another integrator line includes integrators 210b and 210c connected in series. Both integrator lines are connected to receive an output of the summer 230a at a common node, and to provide an output (which may be inverted) to the summer 230a. Similarly, the second stage includes two integrator lines that are connected in parallel to the summer 230b, where one integrator line includes integrator 210d and another integrator line includes integrators 210e and 210f connected in series. Further, a switch 240 selectively couples the output of the first summer to the input of the second summer 230b, thereby providing a third, binary-valued signal to the second stage summer 230b. Both integrator lines are connected to receive an output of the summer 230b at a common node, and to provide an output (which may be selectively inverted) to the summer 230a.

In operation, a combined signal *u(t)*, based on a wideband input, is provided to the first integration/gain stage, which, in turn, provides an input to the second integration/gain stage. Example second-order state variable filters may also include fractional gain blocks and additional summers (not shown). Varying gains of the variable gain blocks changes a center frequency of the embodiment second-order state variable filters. The transfer function *T(s)*, shown in Fig. 20, defines the transfer function of the biquad circuit 200. The coefficients of the transfer function *T(s)* are determined by the integrator gain values.

Fig. 21 illustrates biquad circuit 201 in an further embodiment, and comprises a second-order state variable structure including two integration/gain stages, each of which includes one tunable loss pad 250a-b and two integrators 210b-c, 210ef. A combined signal based on a wideband input is fed to the first integration/gain stage, which, in turn, provides an input to the second integration/gain stage. In particular, the first stage includes a single integrator line comprising integrators 210b and 210c connected in series. The integrator line is connected to receive an output of the summer 230a and provide an output (which may be inverted) to the summer 230a. The tunable loss pad 250a is configured to receive an output of the integrator 210b and provide an output to the summer 230a. The second stage includes a single integrator line comprising integrators 210e and 210f connected in series. The integrator line is connected to receive an output of the summer 230b and provide an output (which may be selectively inverted) to the summer 230b. The tunable loss pad 250b is configured to receive an output of the integrator 210b and provide an output to the summer 230a. Further, a switch 240 selectively couples the output of the first summer 230a to the input of the second summer 230b, thereby providing a third, binary-valued signal to the second stage summer 230b.

In further embodiments, the biquad circuit 201 may include additional second-order state variable filters, such as fractional gain blocks and additional summers (not shown). Adjusting a gain value of the variable gain blocks (e.g., integrators 210b-c, 210e-f) in turn alters a center frequency of the second-order state variable filters. The transfer function coefficients of a wideband signal processing filter provided by the biquad circuit 201 are determined by the tunable loss pads and integrator gain values.

The biquad circuits 200, 201 described above are distinct from the biquad circuit 100 shown in Fig. 1 in a number of ways. Specifically, the biquad circuits 200, 201 benefit from the elimination of the attenuators, programmability of the integrators, and global control (tuning) of the integrators. By eliminating the attenuators, the biquad circuits 200, 201 provide increased accuracy, stability, and bandwidth. Further, the programmable integrators (e.g., integrators 210a-f) enable control of the transfer function in response to process variations and temperature variation in real-time, creating what can be considered a "control plane." Such control is distinct from the "user plane," which follows the path from input *u(t)* to output *y(t)*. An SPI bus implements a management plane, through which integrators and the switch instantiating b2' are controlled. By providing global control rather than individual tuning of integrators, much of the tuning circuit overhead can be removed and scalability of the biquad may be increased dramatically. Fore example, a density of 10+ biquads per square millimeter of silicon may be achievable.

Further, the biquad circuit 200 of Fig. 20 is distinct from the biquad circuit 201 of Fig. 21 in that two programmable integrators 210a-b are replaced with two tunable loss pads 250a-b, which are connected to the output of an integrator (210b, 210e). In some embodiments, implementing tunable loss pads in place of integrators may reduce circuit complexity and size without sacrificing performance.

The teachings of all patents, published applications and references cited herein are incorporated by reference in their entirety.

While this invention has been particularly shown and described with references to example embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

CLAIMS

What is claimed is:

1. A circuit for processing a wideband signal, comprising:

    a first stage comprising:

        a first summing circuit configured to receive an input signal, and

        a first plurality of integrator lines configured to receive an output of the summing circuit, each of the first plurality of integrator lines including at least one integrator circuit, the first summing circuit configured to receive an output of each of the first plurality of integrator lines; and

    a second stage comprising:

        a second plurality of integrator lines configured to receive the output of the first summing circuit, each of the second plurality of integrator lines including at least one integrator circuit, and

        a second summing circuit configured to receive an output of each of the second plurality of integrator lines, the second summing circuit further configured to output an output signal.

2. The circuit of claim 1, wherein the second stage further comprises a switch configured to selectively connect the output of the first summing circuit to the input of the second summing circuit.

3. The circuit of claim 1, wherein the at least one integrator circuit of the first and second plurality of integrator lines has an adjustable gain.

4. The circuit of claim 1, wherein the first and second plurality of integrator lines each include a plurality of integrator circuits having an adjustable gain.

5. The circuit of claim 1, wherein at least one integrator line of the first and second plurality of integrator lines includes a plurality of integrator circuits.

6. The circuit of claim 5, wherein at least one of the plurality of integrator circuits has an adjustable gain.

7. The circuit of claim 1, wherein the first plurality of integrator lines is connected to a common input node.

8. The circuit of claim 1, wherein the second plurality of integrator lines is connected to a common input node.

9. The circuit of claim 1, wherein the output of each of the first plurality of integrator lines is inverted at the first summing circuit.

10. The circuit of claim 1, wherein the output of each of the second plurality of integrator lines is selectively inverted at the second summing circuit.

11. A circuit for processing a wideband signal, comprising:

a first stage comprising:

a first summing circuit configured to receive an input signal,

a first integrator line configured to receive an output of the summing circuit, the first integrator line including at least one integrator circuit, the first summing circuit configured to receive an output the first integrator line, and

a first loss pad having an input coupled to the first integrator line, the first summing circuit configured to receive an output of the first loss pad; and

a second stage comprising:

a second integrator line configured to receive the output of the first summing circuit, the second integrator line including at least one integrator circuit, a second loss pad having an input coupled to the second integrator line, and

a second summing circuit configured to receive an output of each of the second integrator line and the second loss pad, the second summing circuit further configured to output an output signal.

12. The circuit of claim 11, wherein the second stage further comprises a switch configured to selectively connect the output of the first summing circuit to the input of the second summing circuit.

13. The circuit of claim 11, wherein the at least one integrator circuit of the first and second integrator lines has an adjustable gain.

14. The circuit of claim 11, wherein the first and second integrator lines each include a plurality of integrator circuits having an adjustable gain.

15. The circuit of claim 11, wherein at least one of the first and second integrator lines includes a plurality of integrator circuits.

16. The circuit of claim 15, wherein at least one of the plurality of integrator circuits has an adjustable gain.

17. The circuit of claim 11, wherein the input of the first loss pad is connected to a node coupled to an output of a first integrator circuit and an input of a second integrator circuit of the first integrator line.

18. The circuit of claim 11, wherein the input of the second loss pad is connected to a node coupled to an output of a first integrator circuit and an input of a second integrator circuit of the second integrator line.

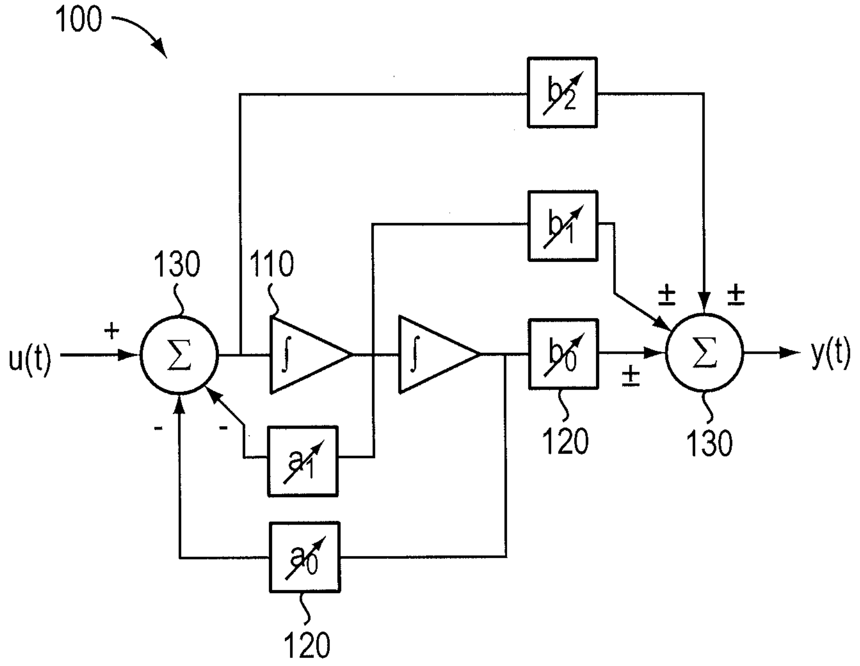
19. The circuit of claim 11, wherein at least one of the first and second loss pads has an adjustable loss value.

20. The circuit of claim 11, wherein the output of the first integrator line is inverted at the first summing circuit.

21. The circuit of claim 11, wherein the output of the first loss pad is inverted at the first summing circuit.

22. The circuit of claim 11, wherein the output of the second integrator line is selectively inverted at the second summing circuit.

23. The circuit of claim 11, wherein the output of the second loss pad is selectively inverted at the second summing circuit.



$$T(s) = \frac{b_2 s^2 + b_1 s + b_0}{s^2 + a_1 s + a_0}$$

FIG. 1

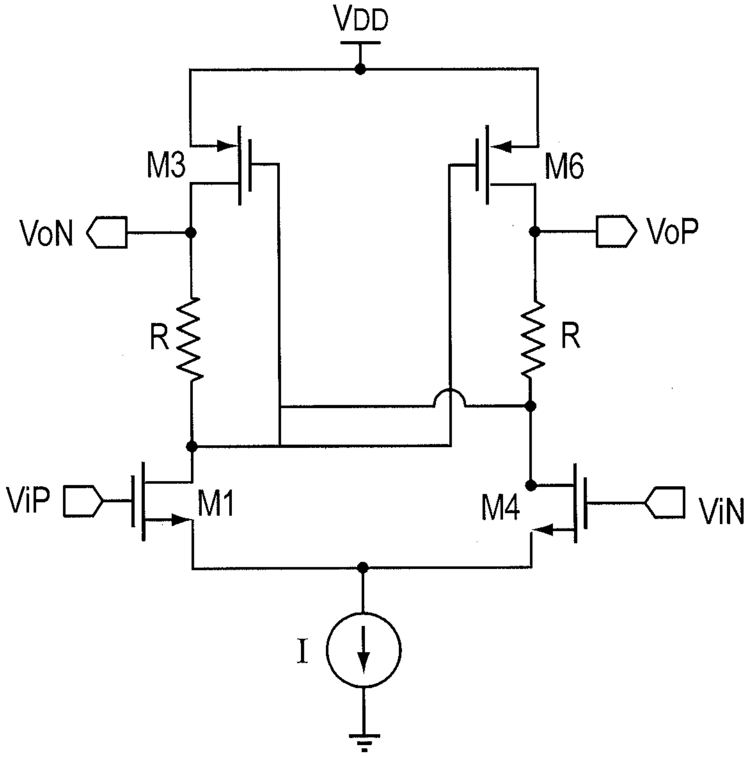


FIG. 2

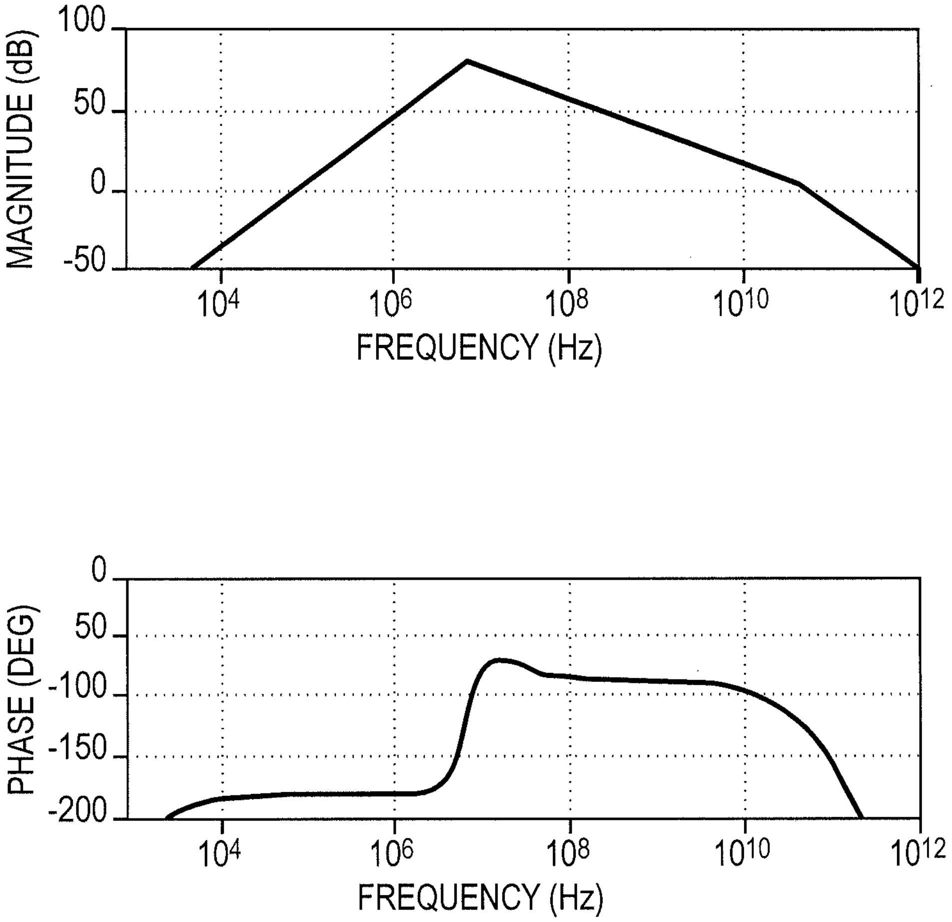

100
50
0
-50
MAGNITUDE (dB)
10^4
10^6
10^8
10^{10}
10^{12}
FREQUENCY (Hz)
0
50
-100
-150
-200
PHASE (DEG)
10^4
10^6
10^8
10^{10}
10^{12}
FREQUENCY (Hz)

FIG. 3

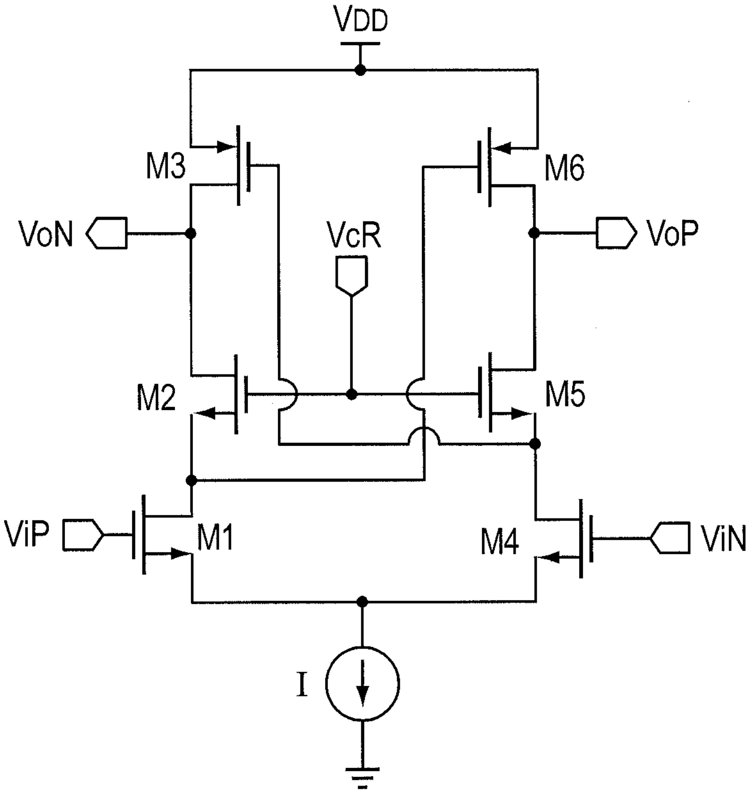


FIG. 4

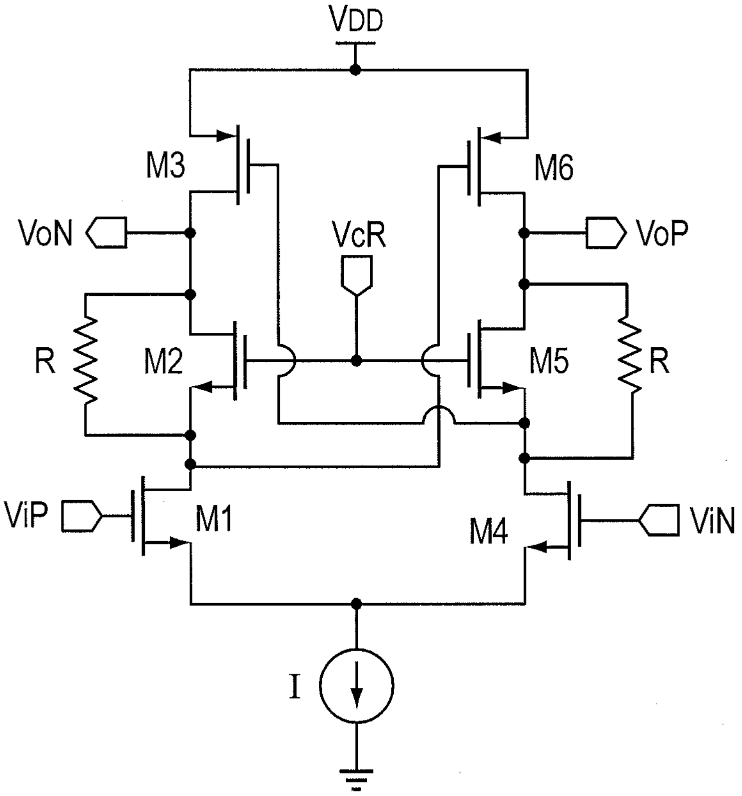


FIG. 5

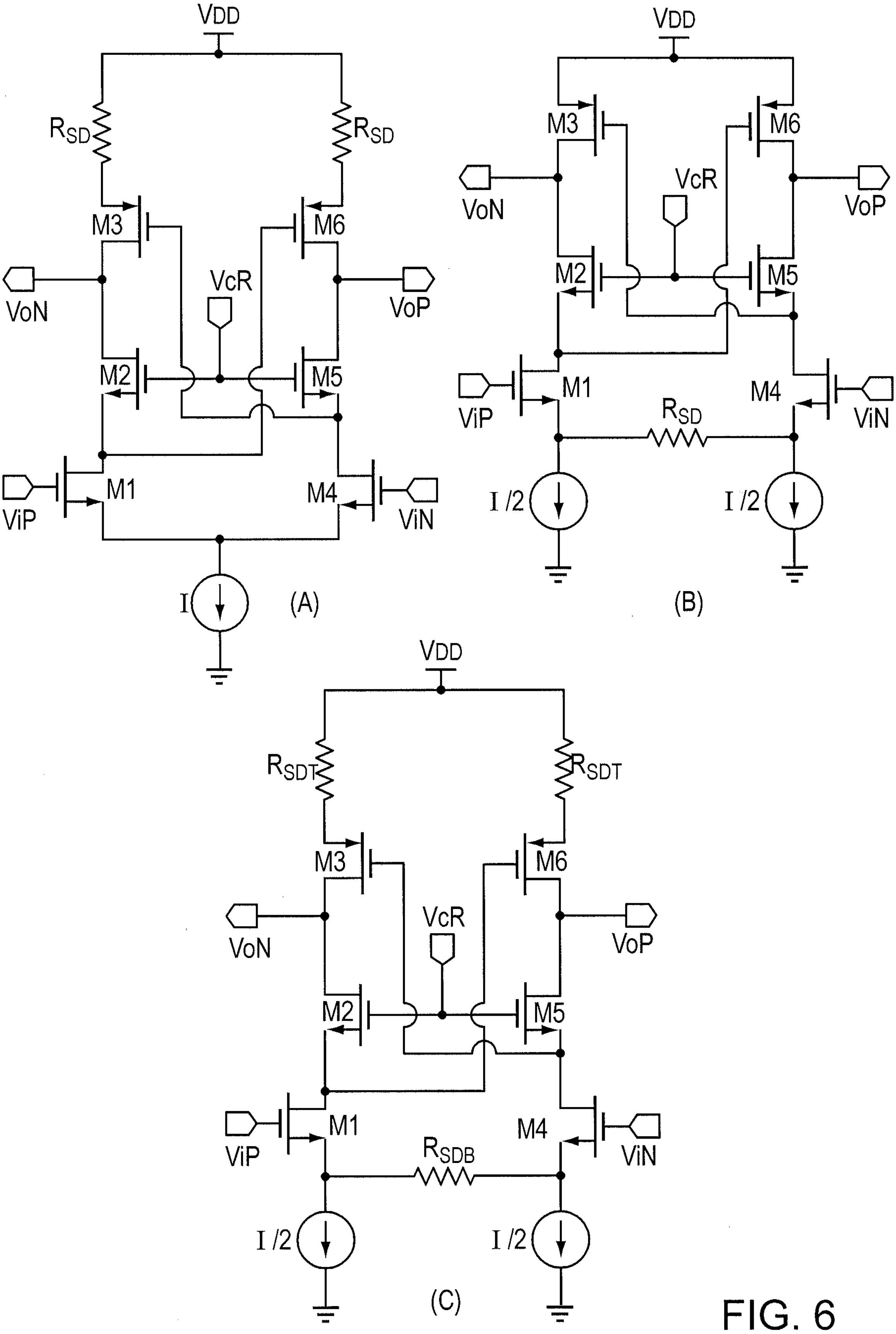

VDD
RSD
RSD
M3
M6
VoN
VcR
VoP
M2
M5
ViP
M1
M4
ViN
I
(A)
VDD
M3
M6
VcR
VoN
VoP
M2
M5
ViP
M1
RSD
M4
ViN
I /2
I /2
(B)
VDD
RSDT
RSDT
M3
M6
VcR
VoN
VoP
M2
M5
ViP
M1
M4
RSDB
ViN
I /2
I /2
(C)

FIG. 6

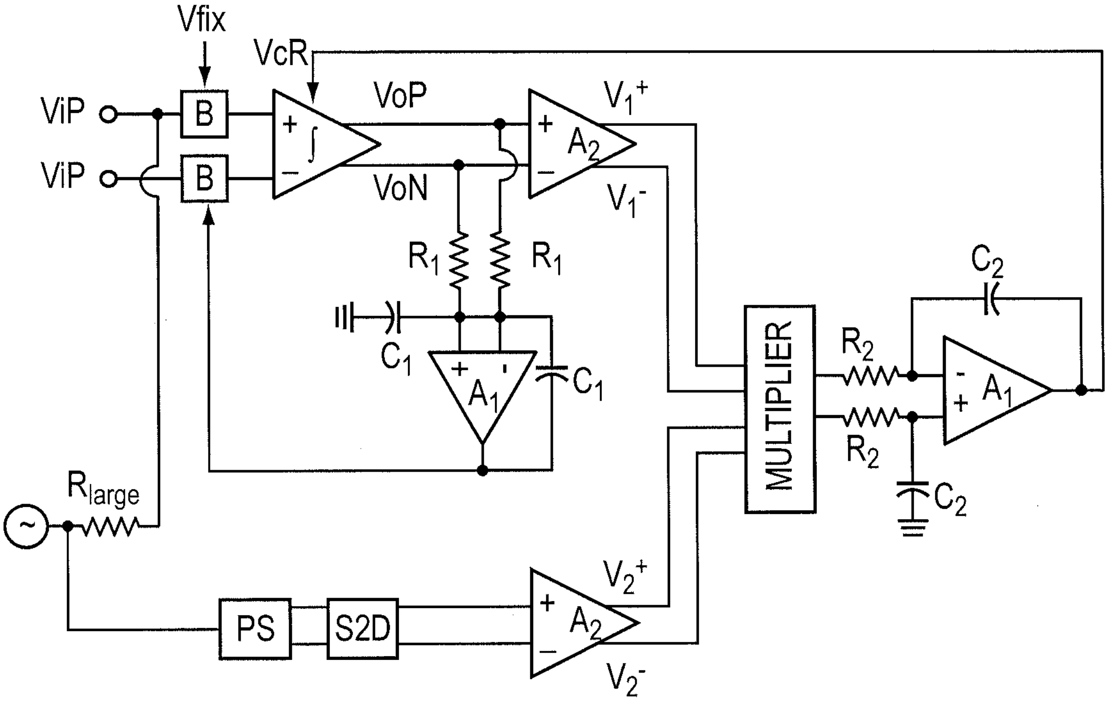

Vfix
VcR
ViP
ViP
B
B
∫
VoP
VoN
A_2
V_1^+
V_1^-
R_1
R_1
C_1
A_1
C_1
C_2
R_2
R_2
MULTIPLIER
A_1
C_2
R_{large}
PS
S2D
A_2
V_2^+
V_2^-

FIG. 7

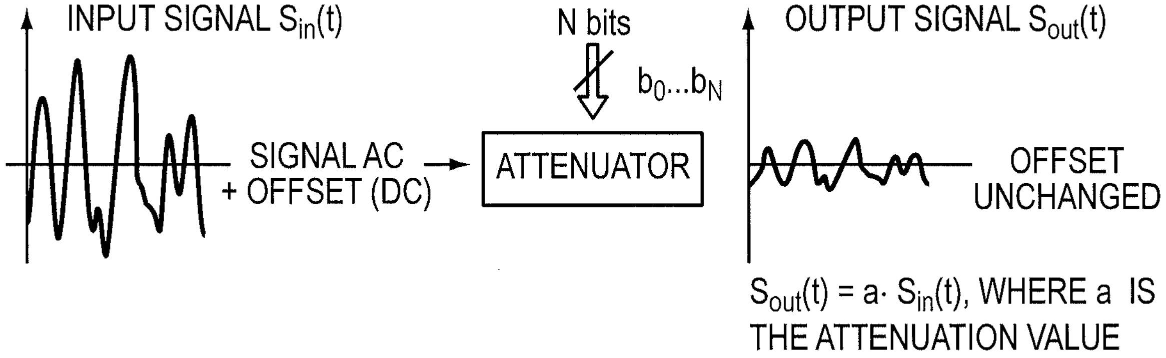

INPUT SIGNAL $S_{in}(t)$
SIGNAL AC + OFFSET (DC)
N bits
$b_0 \ldots b_N$
ATTENUATOR
OUTPUT SIGNAL $S_{out}(t)$
OFFSET UNCHANGED
$S_{out}(t) = a \cdot S_{in}(t)$, WHERE a IS THE ATTENUATION VALUE

FIG. 8

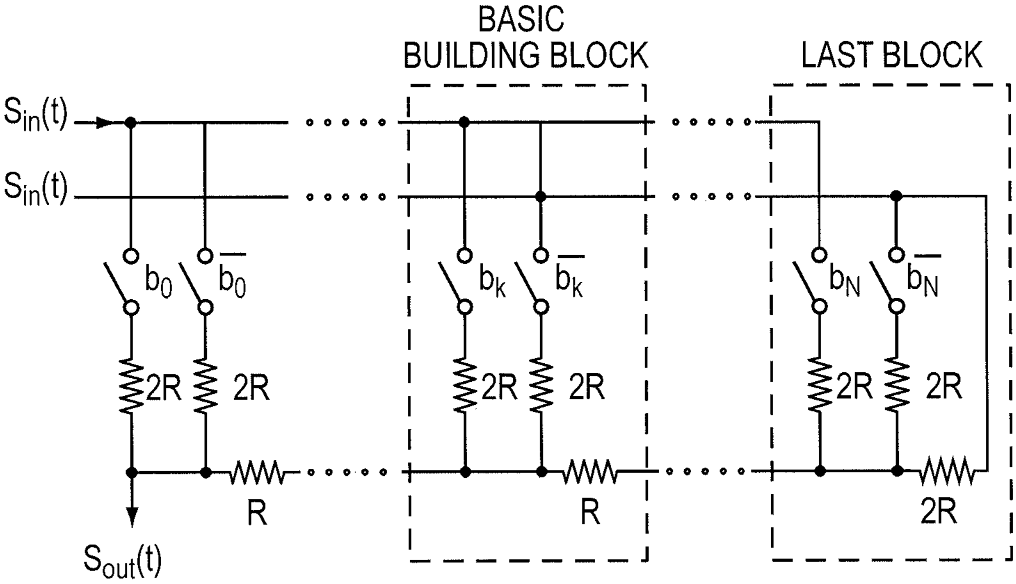
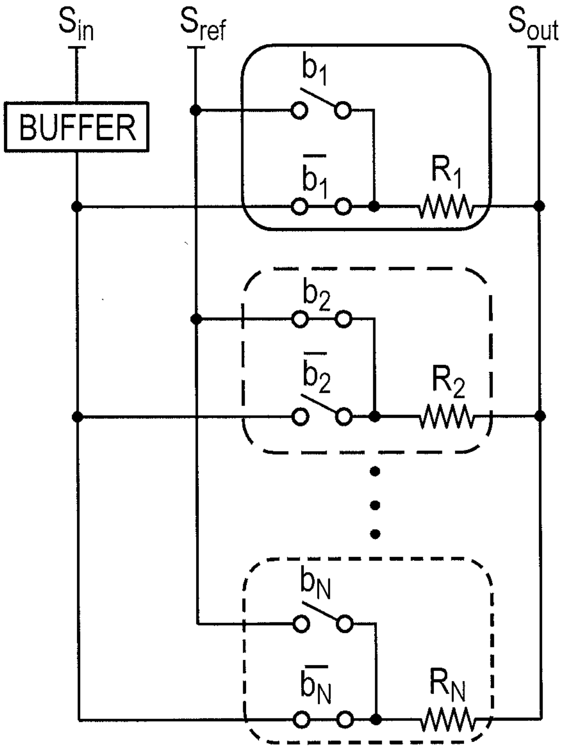

BASIC BUILDING BLOCK
LAST BLOCK
$S_{in}(t)$
$S_{in}(t)$
b_0
$\overline{b_0}$
b_k
$\overline{b_k}$
b_N
$\overline{b_N}$
2R
2R
2R
2R
2R
2R
R
R
2R
$S_{out}(t)$

FIG. 9



OFFERS 2^N ATTENUATION VALUES

FIG. 10

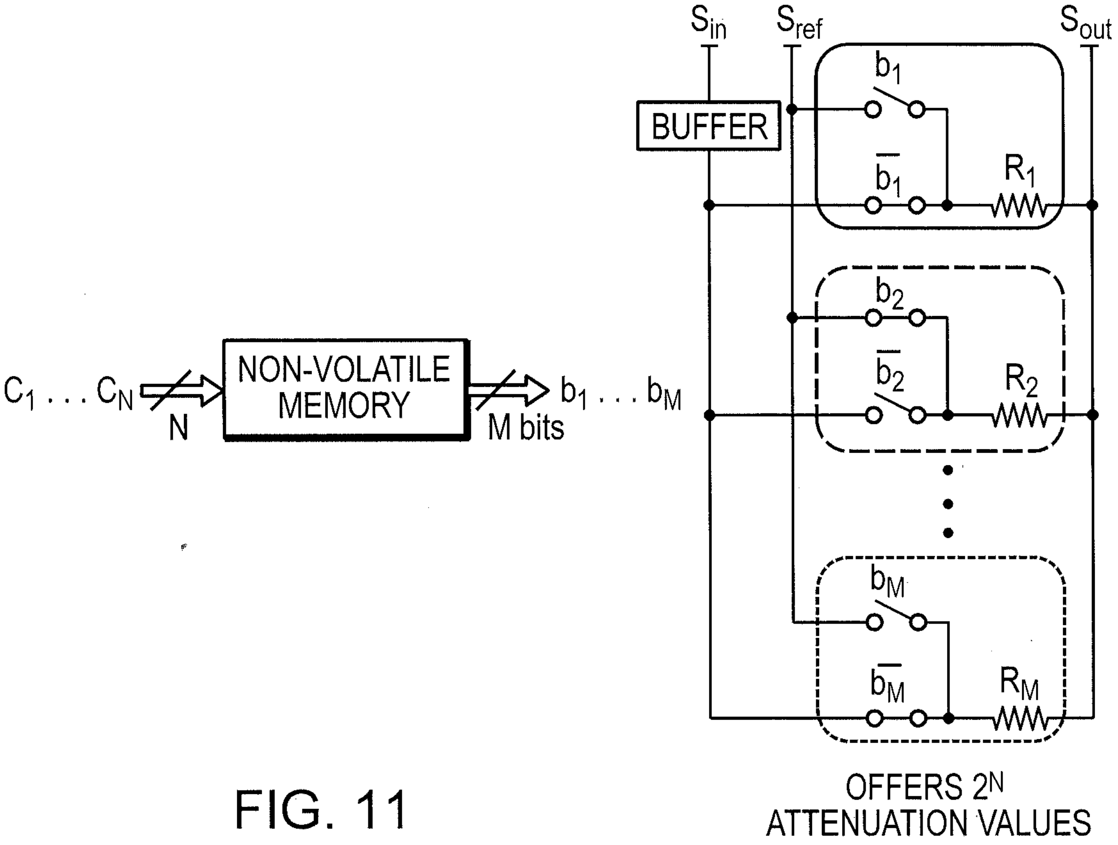

$C_1 \dots C_N$
N
NON-VOLATILE MEMORY
M bits
$b_1 \dots b_M$
S_{in}
S_{ref}
S_{out}
BUFFER
b_1
$\overline{b_1}$
R_1
b_2
$\overline{b_2}$
R_2
b_M
$\overline{b_M}$
R_M
OFFERS 2^N ATTENUATION VALUES

FIG. 11

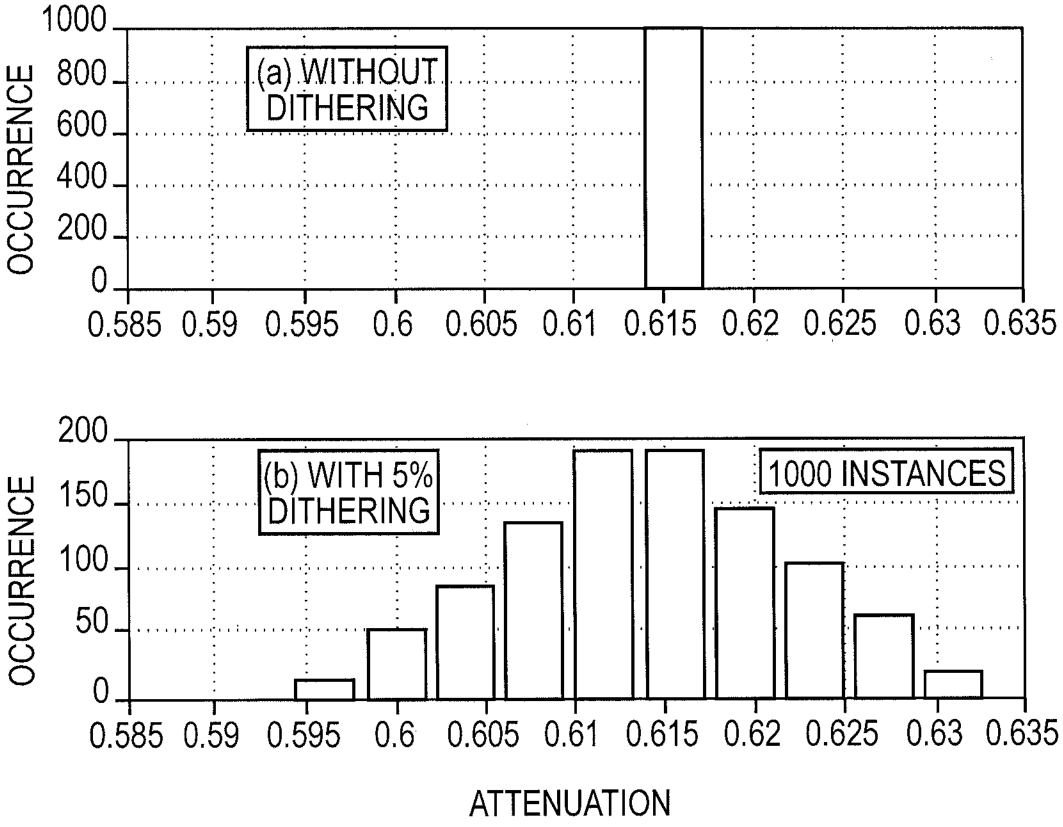

1000
800
600
400
200
0
OCCURRENCE
(a) WITHOUT DITHERING
0.585
0.59
0.595
0.6
0.605
0.61
0.615
0.62
0.625
0.63
0.635
200
150
100
50
0
OCCURRENCE
(b) WITH 5% DITHERING
1000 INSTANCES
0.585
0.59
0.595
0.6
0.605
0.61
0.615
0.62
0.625
0.63
0.635
ATTENUATION

FIG. 12

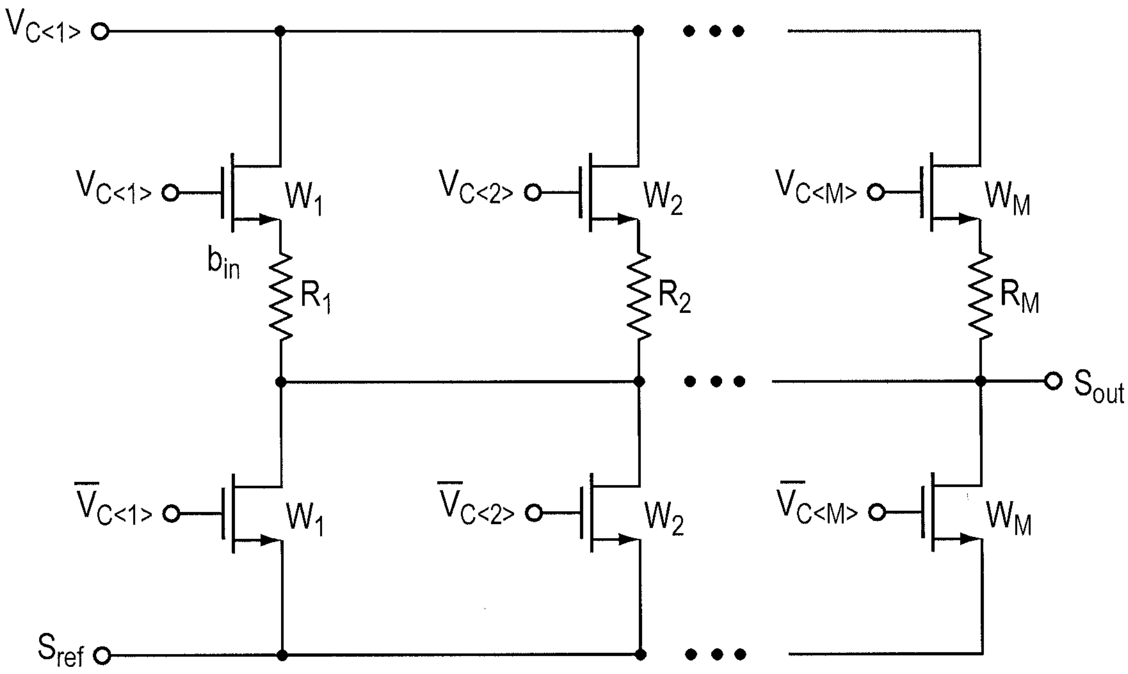
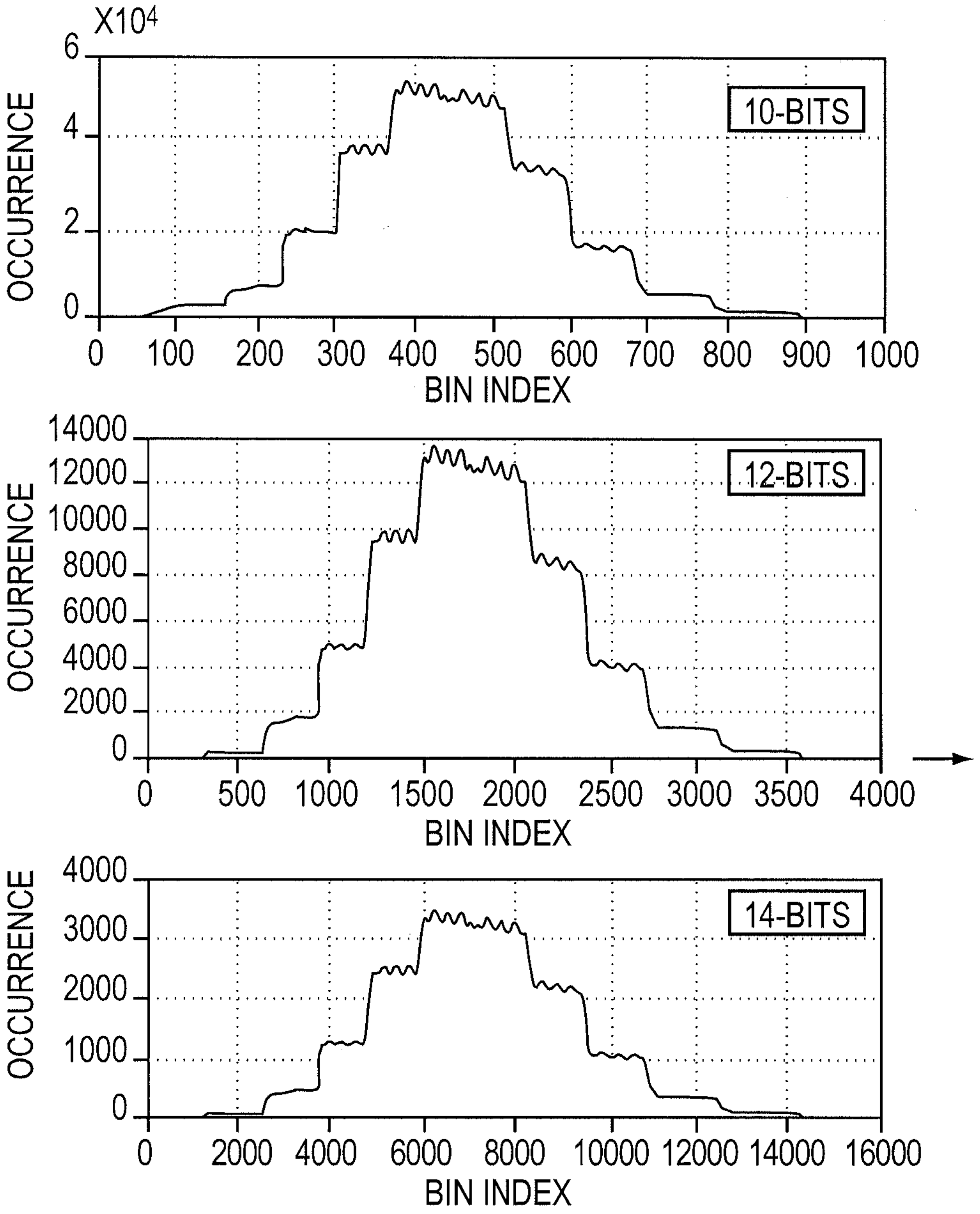

$V_{C<1>}$
$V_{C<1>}$
W_1
b_{in}
R_1
$V_{C<2>}$
W_2
R_2
$V_{C<M>}$
W_M
R_M
S_{out}
$\overline{V}_{C<1>}$
W_1
$\overline{V}_{C<2>}$
W_2
$\overline{V}_{C<M>}$
W_M
S_{ref}

FIG. 13



CONTINUOUS COVERAGE

Bits	LOW BIN NUMBER[A]	HIGH BIN NUMBER[B]	DYNAMIC RANGE	STEP SIZE
10	1	1, 022	60dB	0.000977
12	5	4, 079	58dB	0.000244
14	62	14,489	47dB	0.000061

NUMBER OF BINS

2^{10} = 1,024
2^{12} = 4,096
2^{14} = 16,384

[A] LOWEST BIN NUMBER WITH AT LEAST ONE ATTENUATION VALUE PRESENT

[B] HIGHEST BIN NUMBER WITH AT LEAST ONE ATTENUATION VALUE PRESENT

FIG. 14

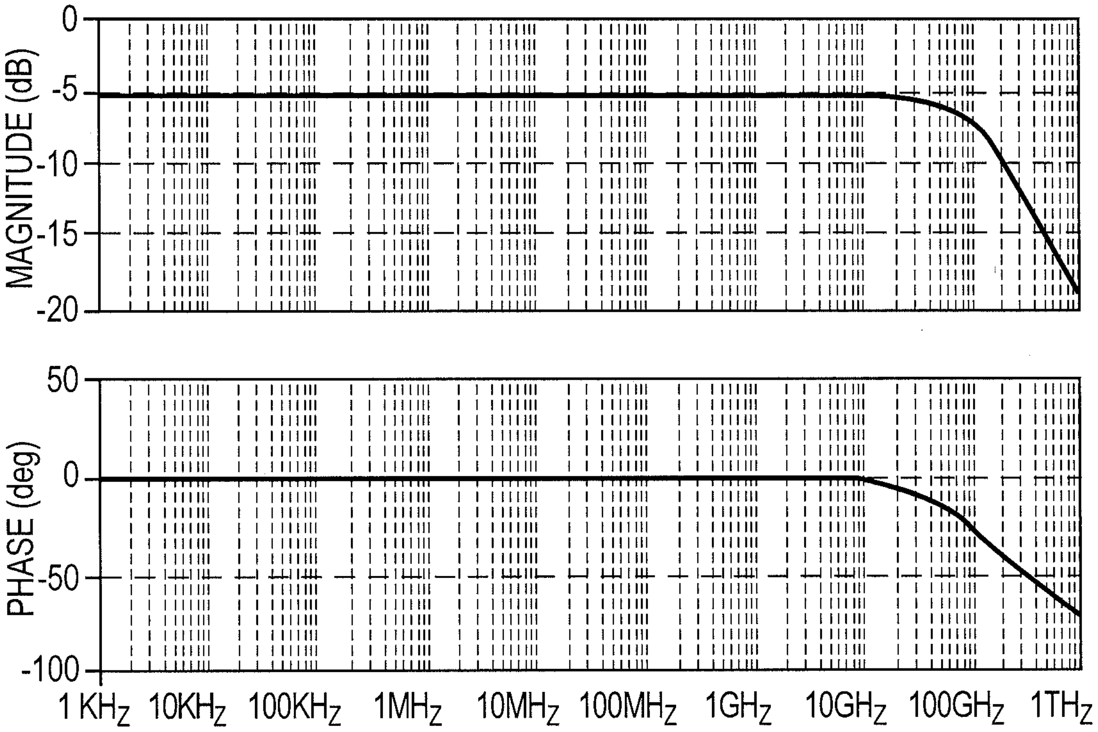

0
-5
-10
-15
-20
MAGNITUDE (dB)
50
0
-50
-100
PHASE (deg)
1 KHz
10KHz
100KHz
1MHz
10MHz
100MHz
1GHz
10GHz
100GHz
1THz

FIG. 15

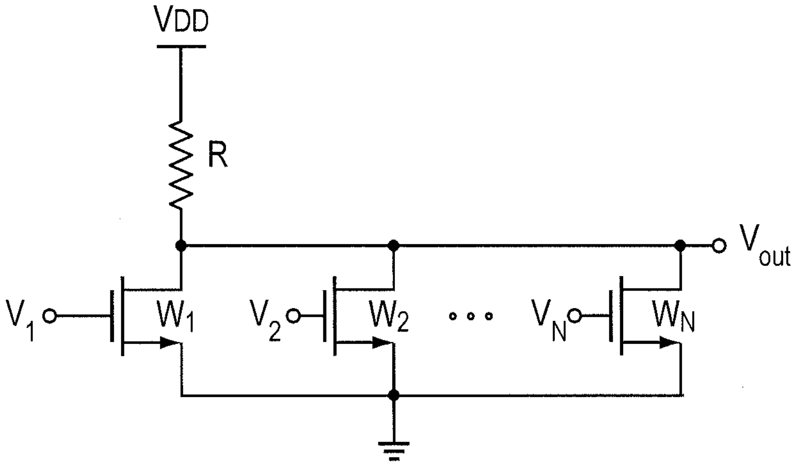


FIG.16

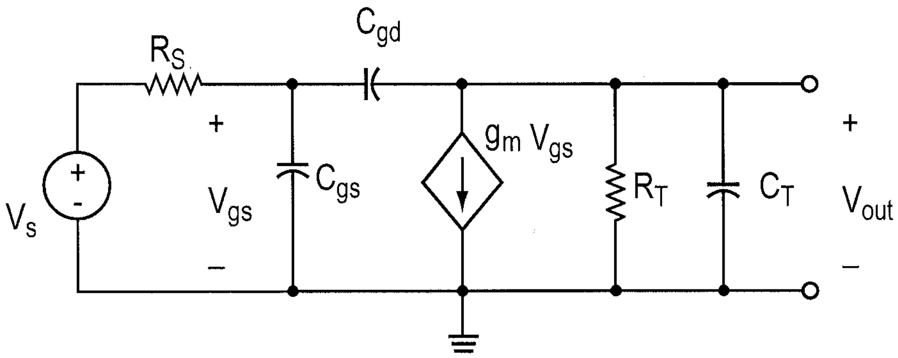


FIG. 17

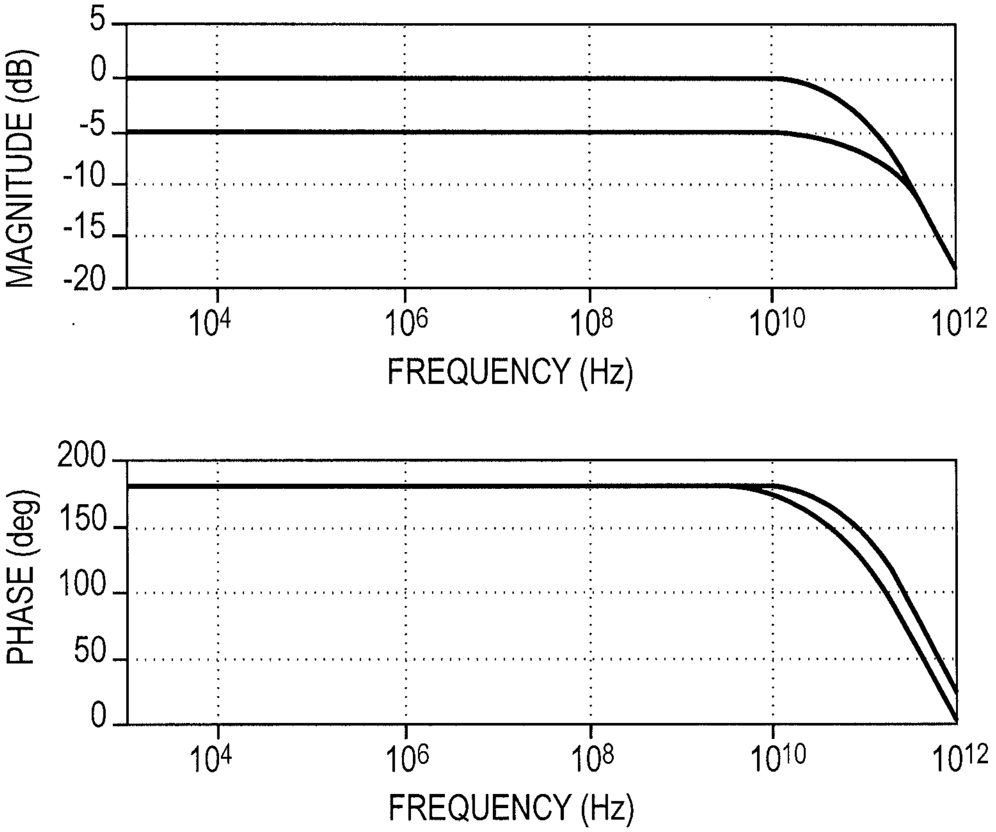

5
0
-5
-10
-15
-20
MAGNITUDE (dB)
10^4
10^6
10^8
10^{10}
10^{12}
FREQUENCY (Hz)
200
150
100
50
0
PHASE (deg)
10^4
10^6
10^8
10^{10}
10^{12}
FREQUENCY (Hz)

FIG. 18

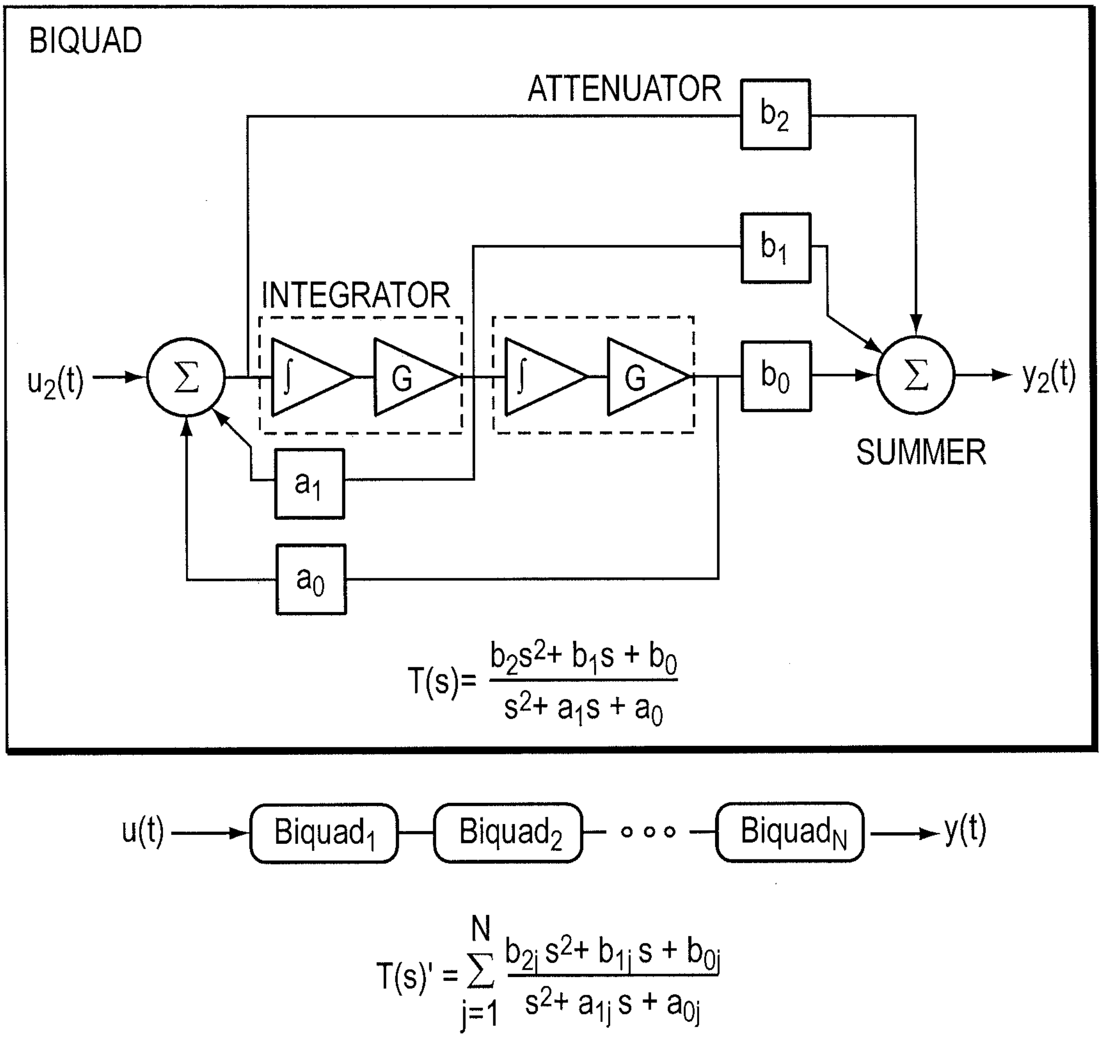
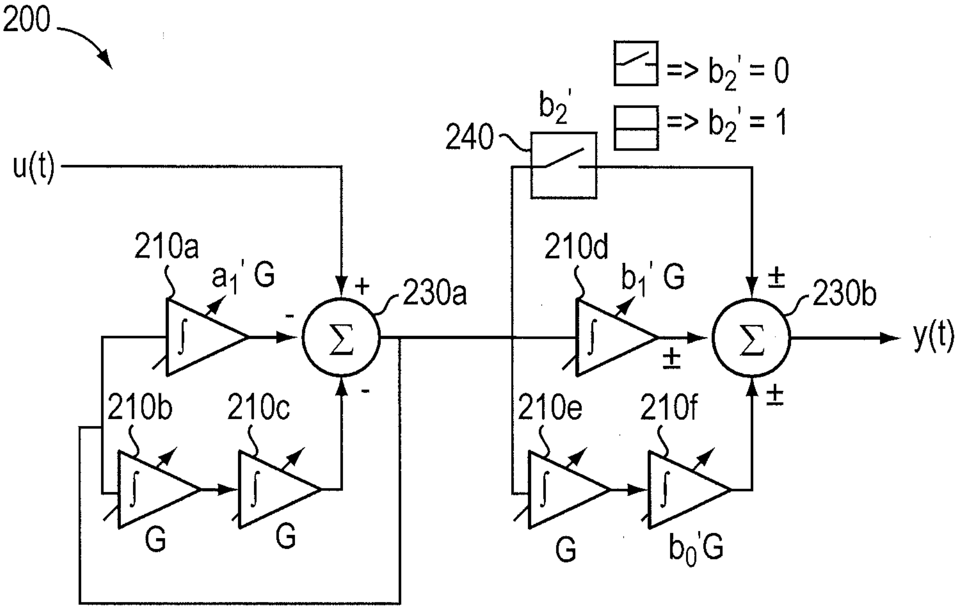

BIQUAD
ATTENUATOR
b_2
b_1
INTEGRATOR
$u_2(t)$
Σ
$\int$
G
$\int$
G
b_0
Σ
$y_2(t)$
SUMMER
a_1
a_0
$T(s)=\frac{b_2s^2+b_1s+b_0}{s^2+a_1s+a_0}$
$u(t)$
Biquad_1
Biquad_2
Biquad_N
$y(t)$
$T(s)'=\sum_{j=1}^{N}\frac{b_{2j}s^2+b_{1j}s+b_{0j}}{s^2+a_{1j}s+a_{0j}}$

FIG. 19



$$T(s) = \frac{b_2' + b_1'\,G/s + b_0'\,G^2/s^2}{1 + a_1'\,G/s + G^2/s^2}$$

WHERE $a_1' = a_1/s$

$b_0' = b_0/s^2$

$b_1' = b_1/s$

$b_2' = b_2^2$

FIG. 20

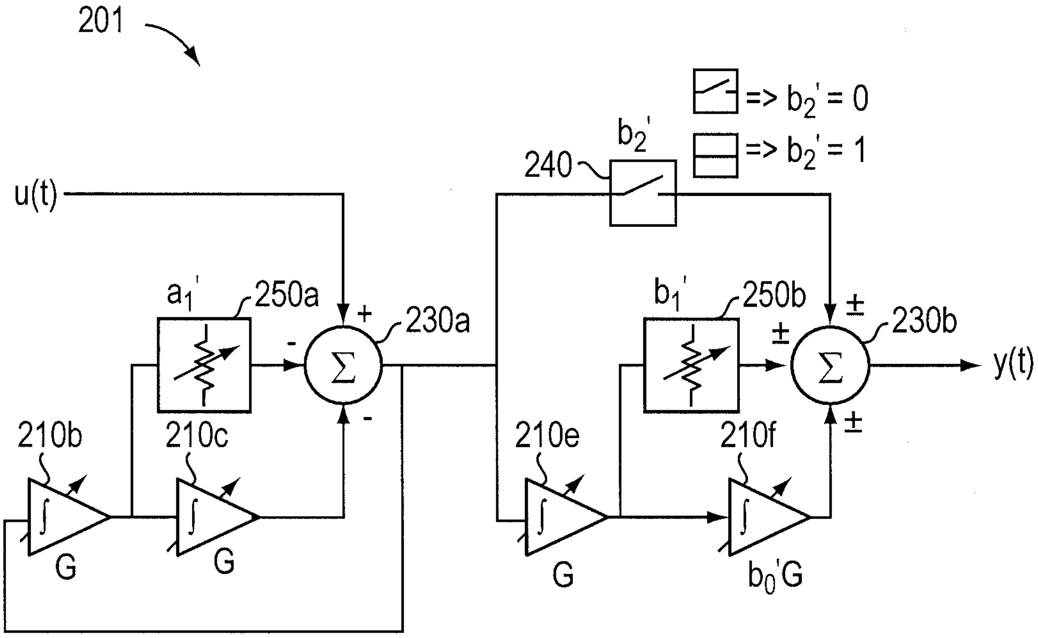

201
=> b2' = 0
=> b2' = 1
b2'
240
u(t)
a1'
250a
+
230a
-
-
b1'
250b
±
230b
±
y(t)
±
210b
210c
210e
210f
G
G
G
b0'G

FIG. 21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/062965

A. CLASSIFICATION OF SUBJECT MATTER

H04L 25/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L 25/02; H01L 51/50

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: wideband signal, summing circuit, integrator line, loss pad

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2006-131565 A1 (EM MICROELECTRONIC-MARIN SA) 14 December 2006 See the Abstract; Figs. 4-5; pages 1-4; Claims 1-11.	1-23
A	US 2009-0184769 A1 (LEE WEI-YANG et al.) 23 July 2009 See the Abstract; Figs. 1, 2; Paragraph [0007]-[0009]; Claims 1-25.	1-23
A	US 06118794A A (CORNFIELD; PAUL SIMON et al.) 12 September 2000 See the Abstract; Figs. 5, 6; column 2-5; Claims 1-16.	1-23
A	JP 2008-122408 A (LOCKHEED MARTIN CORP) 29 May 2008 See the Abstract; Figs. 2-4; Paragraph [0009]-[0016]; Claims 1-32.	1-23

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search 26 FEBRUARY 2013 (26.02.2013)	Date of mailing of the international search report **26 FEBRUARY 2013 (26.02.2013)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer Park, Sung Woong Telephone No. 82-42-481-8596

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2012/062965

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2006-131565 A1	14.12.2006	CN 101194379 A0	04.06.2008
		CN 101194379 B	19.05.2010
		EP 1894262 A1	05.03.2008
		JP 2008-543102 A	27.11.2008
		JP 2008-543102 T	27.11.2008
		KR 10-2008-0012926 A	12.02.2008
		US 2009-0096354 A1	16.04.2009
US 2009-0184769 A1	23.07.2009	None	
US 06118794A A	12.09.2000	None	
JP 2008-122408 A	29.05.2008	None	