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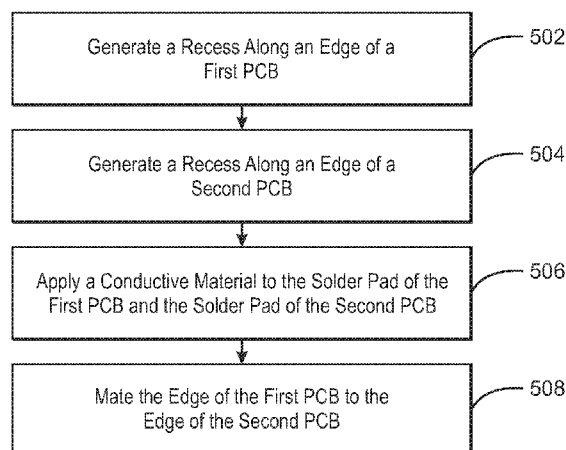
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[Continued on next page]

(54) **Title:** BOARD TO BOARD INTERCONNECT



(57) **Abstract:** A system for board-to-board interconnect is described herein. The system includes a first printed circuit board (PCB) having a first recess along a first edge of the first PCB that exposes a first solder pad on a layer of the first PCB. The system also includes a second PCB having a second recess along a second edge of the second PCB that exposes a second solder pad on a layer of the second PCB. The second recess is complementary to the first recess to allow the first PCB to mate with the second PCB. The first solder pad is aligned with the second solder pad when the first PCB is mated with the second PCB. The system additionally includes an assembly configured to electronically couple the first solder pad with the second solder pad.

500
FIG. 5



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BOARD TO BOARD INTERCONNECT

CROSS REFERENCE TO RELATED APPLICATION

[0001] The present application claims the benefit of the filing date of United States Patent Application Serial No. 14/757,984, by Wong, et al., entitled “BOARD TO BOARD INTERCONNECT” filed December 26, 2015, and is incorporated herein by reference.

TECHNICAL FIELD

[0002] This disclosure relates generally to interconnects. Specifically, this disclosure relates to board to board interconnects.

BACKGROUND

[0003] Printed circuit boards (PCBs) typically include solder at various layers to interconnect with other PCBs. However, the connector that is used to interconnect PCBs is usually placed on top of the PCBs. Unfortunately, this adds height to the layered PCBs, which increases the size of the devices that the PCBs are placed in. These include smart devices, such as phones, tablets, watches and other wearable computing devices, and system in package devices. A System in Package is a single module that encloses a number of integrated circuits, and may be used in small form computing devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figs. 1A-1C are block diagrams of example PCBs for on-cavity board-to-board interconnect;

[0005] Figs. 2A-2B are diagrams of example on-cavity interconnected boards in fixed and removable assemblies;

[0006] Fig. 3 is a diagram of an example stack of PCBs for on-cavity board-to-board interconnect;

[0007] Fig. 4 is a diagram of stacked PCBs for on-cavity board-to-board interconnects with horizontally expanded solder pads;

[0008] Fig. 5 is a process flow diagram of a method for manufacturing PCBs for on-cavity board-to-board interconnect;

[0009] Fig. 6 is a diagram of example sections of System in Package (SIP) and corresponding input-output (IO) board for an on-cavity board-to-board interconnect; and

[0010] Fig. 7 is a diagram of an example on-cavity board-to-board interconnect between a System in Package and an IO board.

[0011] In some cases, the same numbers are used throughout the disclosure and the figures to reference like components and features. Numbers in the 100 series refer to features originally found in Fig. 1; numbers in the 200 series refer to features originally found in Fig. 2; and so on.

DESCRIPTION OF THE EMBODIMENTS

[0012] In one embodiment of the present techniques, board-to-board interconnects may be provided without a connector. Instead, an on-cavity board-to-board interconnect is used. An on-cavity board-to-board interconnect is the connection of two PCBs, where a cavity has been excavated in each PCB to expose solder contact points. The PCBs are then combined, placing the exposed solder of each of the PCBs in electrical contact with each other. Because the electrical contact is made in the space where a cavity has been created, these are called on-cavity board-to-board interconnects. In this way, PCBs may be interconnected without the added z-height of a connector, which is advantageous for incorporating interconnected PCBs into small form factor devices and System in Package devices. The z-height refers to the vertical height of layers of PCBs. Typically, the connector sits on top of the PCBs, thus increasing the z-height, which increases the minimum height of what are designed to be small, in some cases, wearable devices.

[0013] In the following description, numerous specific details are set forth, such as examples of specific types of processors and system configurations, specific hardware structures, specific architectural and micro architectural details, specific register configurations, specific instruction types, specific system components, specific measurements or heights, specific processor pipeline stages and operation, etc., in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that these specific details need not be employed to practice the present invention. In other instances, well known components or methods, such as specific and alternative processor architectures, specific logic circuits or code for described algorithms, specific

firmware code, specific interconnect operation, specific logic configurations, specific manufacturing techniques and materials, specific compiler implementations, specific expression of algorithms in code, specific power down and gating techniques or logic and other specific operational details of computer system have not been described in detail in order to avoid unnecessarily obscuring the present invention.

[0014] Although the following embodiments may be described with reference to energy conservation and energy efficiency in specific integrated circuits, such as in computing platforms or microprocessors, other embodiments are applicable to other types of integrated circuits and logic devices. Similar techniques and teachings of embodiments described herein may be applied to other types of circuits or semiconductor devices that may also benefit from better energy efficiency and energy conservation. For example, the disclosed embodiments are not limited to smart rings, and may be also used in other devices, such as wearable and handheld devices, systems on a chip (SOC) devices, and embedded applications. Some examples of handheld devices include cellular phones, Internet protocol devices, digital cameras, and handheld PCs. Embedded applications typically include a microcontroller, a digital signal processor (DSP), a system on a chip, network computers (NetPC), or any other system that can perform the functions and operations taught below. Moreover, the apparatuses, methods, and systems described herein are not limited to physical computing devices, but may also relate to software optimizations for energy conservation and efficiency. As will become readily apparent in the description below, the embodiments of methods, apparatuses, and systems described herein (whether in reference to hardware, firmware, software, or a combination thereof) are vital to a 'green technology' future balanced with performance considerations.

[0015] Figs. 1A-1C are block diagrams of example PCBs 102, 104 for on-cavity board-to-board interconnect. In Fig. 1A, the PCB 102 is shown with a first layer ground 106, dielectric 108, signal traces 110, and exposed solder pads 112. With the use of semi-rigid board recess or other board cavity technology, it is possible to create a recess at the edge of PCB 102 to expose the solder pads 112 as shown. In semi-rigid board recess technology, the PCB is manufactured, with solder pads 112 incorporated within dielectric material. Additionally, the PCB typically includes a first layer ground 106. To create the recess, or cavity, the first metal layer, ground 106, and the first dielectric layers are removed from the

edge of the PCB 102, thus exposing the solder pads 112. The physical material, e.g., the metal in the first layer ground 106, and the dielectric material, is cut away mechanically, such as with a high precision router, such as, a laser router. In one embodiment of the present techniques, once the solder pads 112 are exposed by the creation of the cavity, the solder pads 112 may be coated with solder paste to provide a strong solder joint formation. Besides using conventional solder paste for the solder joint, an anisotropic conductive film (ACF) may be used. In some embodiments such as System in Package, some or all of the edges of PCB 102 can be recessed to expose solder pads along multiple edges of PCT 102.

[0016] In Fig. 1B, a similar procedure is performed for PCB 104. The PCB 104 is cut as described above. However, the PCB 104 is cut in a complementary way to the PCB 102. In this way, the PCBs 102, 104 can be combined. Thus, with the solder pads of both boards 102, 104 exposed, an interconnect can be created by making electrical contact with the exposed solder pads of both boards 102, 104. In some embodiments, PCT 102 and 104 can be cut in manner which allows PCB 102 and PCB 104 to be mated together. As shown in FIG. 1B the overall height (or Z-dimension) of PCB 102 and 104 when combined can be substantially the same height as when separated.

[0017] Fig. 1C is a side view of an on-cavity board-to-board interconnect between PCBs 102 and 104. As shown, the z-height of the PCB 102 and 104, when combined, remains substantially unchanged. In some embodiments, PCB 102 and 104 can be substantially the same height individually and also when combined. By connecting the PCBs in this way, the extra z-height typically taken up by a connector is avoided. In some circumstances layer misregistration may occur during PCB manufacturing. Layer misregistration occurs when a contact mask becomes misaligned. Contact masks are the end point of a signal line or solder pad at the edge of a PCB. To account for the possibility of layer misregistration occurring between the two PCBs 102, 104, the pad size on both PCBs may be enlarged. For small pitch design, a guide pin may be used to overcome the misalignment.

[0018] Figs. 2A-2B are diagrams of example on-cavity interconnected boards 202, 204 in fixed and removable assemblies, respectively. In a fixed assembly, the PCBs 202, 204 may be bonded together by soldering the exposed solder pads 206 together permanently. Alternatively, as shown in Fig. 2A, an adhesive and conductive film 208 is used, such as anisotropic conductive film (ACF) adhesive bonding. Advantageously, the ACF bonding

provides quick and easy assembly without stepped or 3D stencilling to apply the solder paste to the pads in the cavity. The film's adhesive properties create a permanent bond between the boards 202, 204 at their exposed solder pads 206. Additionally, the film 208 is conductive, as to provide an electrical contact between the exposed solder pads 206. As shown, the fixed assembly does not increase the z-height.

[0019] Fig. 2B is a diagram of a removable assembly. Instead of an adhesive film as used in the fixed assembly, a material 210, such as metallized particle interconnect, or an elastomer, may be placed between the exposed solder pads, to make electrical contact. The metallized particle interconnect is an elastomer with structured metal parts arranged within that provide an electrical contact through the elastomer. In addition to providing electrical contact between the solder pads 206, the metallized particle interconnect provides the flexibility to be able to remove and re-attach the boards without need to raise the external temperature to loosen the bonding. Additionally, a clamping mechanism 212 may be used to physically hold the PCBs 202, 204 together. The clamping mechanism 212 may be a screw, or an external clamping socket. As shown, the removable assembly can slightly increase the z-height due to the height of the ends of clamping mechanism 212. However, the z-height remains substantially the same as the z-height of the combined PCBs 202, 204. In one embodiment of the present techniques, the PCBs 202, 204 include an opening to house a securing mechanism for securing the PCBs 202, 204.

[0020] The fixed assembly, provides an advantage over the removable assembly in that the z-height is limited to the combined z-height of the PCBs 202, 204 and the adhesive film. The removable assembly, however, provides the advantage of being able to replace one or both of the combined PCBs. This is advantageous where the computing device incorporating the PCBs is designed to be upgradeable, or scalable.

[0021] Advantageously, the on-cavity board-to-board interconnect described herein eliminates the traditional connector from the assembly of interconnected PCBs. This is useful in developing small form factor systems. Additionally, the input-output pin density of the traditional connector is preserved with the on-cavity board-to-board interconnect described herein. The input-output pin density represents the pin map that typically exist on standard connectors. Another advantage is that the on-cavity board-to-board interconnect described herein is electrically better than the traditional connector.

[0022] The traditional connector is a lossy interconnect that creates impedance discontinuity. A lossy interconnect is a connector that dissipates some of the electrical energy being passed between electrical contacts. To account for the amount of energy lost to lossy interconnects, a loss budget is built into the design of an electrical system. The loss budget dictates how much electrical energy can be lost, and still provide the designed functionality. However, the improved electrical contact of the on-cavity board-to-board interconnect is not lossy. Accordingly, the loss budget that would have been allocated to traditional connectors can instead be allocated to PCB routing such for additional length or tighter routing density. The loss budget from connector can thus be used to route a longer PCB length.

[0023] Additionally, there are fewer impedance discontinuities with the on-cavity board-to-board interconnect than with the traditional connector. Impedance discontinuities are distortions in electrical signals that occur due to some of the signals reflecting backwards instead of towards their destination. On-cavity board-to-board interconnects reduce impedance discontinuities by optimizing the interconnect impedance to match to the system impedance. This can be achieved by tuning the pad, stack-up and reference plane dimensions to yield the required impedance range. Impedance tuning was traditionally hard to tune on a standard connector, due to large physical size.

[0024] Another advantage is that the on-cavity board-to-board interconnect reduces crosstalk between adjacent signal lines. By using a direct connection, instead of one that runs through the z-height of the PCBs, there is less potential for cross-talk because of a shorter coupled electrical length and close vicinity to the reference plane. Further, the on-cavity board-to-board interconnect described herein can also be expanded to stacks of PCBs, with multiple layers of on-cavity board-to-board interconnects. With added pin density introduced by multiple layers of on-cavity board-to-board interconnects, we can introduce more gnd pin to provide better crosstalk shielding for noise sensitive signals.

[0025] Fig. 3 is a diagram of an example stack 302 of PCBs for on-cavity board-to-board interconnect. The stack 302 includes a ground at the first layer 304, stacked connections of solder pads at the second layer 306, and stacked connections of solder pads at the third layer 308. As shown, two or more layers of solder pads can be exposed for high density input-output. On the second layer, a cavity is created at the edge of the PCB, exposing the solder

pads. Similarly, at the third layer, a cavity is cut out of the second layer to expose the solder pads. Both solder pads are designed in larger size to ensure good electrical contact as well as to cater for the potential misalignment between board-to-board. Further, in addition to being expanded vertically, the solder pads can be expanded horizontally.

[0026] Fig. 4 is a diagram of stacked PCBs for on-cavity board-to-board interconnects with horizontally expanded solder pads. As shown, the stack 402 includes a ground at the first layer 404, stacked connections at a second layer 406, and stack connections at a third layer 408. As shown, the stacked connections at the second layer 406 and stack connections at the third layer 408 are vertically and horizontally displaced from each other. This displacement creates shielding of the electrical traces with the dielectric material placed in-between. In this way, shielding of the electrical signals is provided that reduces crosstalk input-output between the two groups of stacked connections. Crosstalk is the tendency of electrical traces that are close to each other having their electrical signals migrate into neighboring lines. With the dielectric material between horizontally and vertical displaced connections, the potential for crosstalk is reduced. In one embodiment of the present techniques, such on-cavity board-to-board interconnects are suitable for crosstalk-sensitive input-output. The horizontal displacement can also act as mechanical stopper, and minimize misalignment between boards, especially for removable assemblies.

[0027] Fig. 5 is a process flow diagram of a method 500 for manufacturing PCBs for on-cavity board-to-board interconnect. The process flow diagram is not intended to represent a sequence of performing the method 500. The method 500 begins at block 502, where a recess is generated along an edge of a first PCB. The first recess exposes a first solder pad on a layer of the first PCB. Generating the recess may be accomplished using a combination of laser and mechanical techniques. Additionally, a laser stop may be used to prevent excavation of the solder material. For a PCB stack, multiple layers of the stack may be removed to expose the solder pads at a specified layer. In one embodiment, the recess may be a notch in a first layer of the first PCB that exposes the solder pad at a second layer of the first PCB.

[0028] At block 504, a recess is generated along an edge of a second PCB. The recess along the edge of the second PCB is complementary to the recess along the edge of the first PCB. Additionally, the recess exposes a solder pad on a layer of the second PCB.

[0029] At block 506, a conductive material is applied to the solder pad of the first PCB and the solder pad of the second PCB. In the case of a fixed assembly, a solder paste or an anisotropic conductive adhesive may be applied. In the case of a removable assembly, metallized particle interconnect or an elastomer may be applied.

[0030] At block 508, the edge of the first PCB is mated to the edge of the second PCB such that the solder pad of the first PCB is electronically coupled to the solder pad of the second PCB via the conductive material. In the case of a fixed assembly, the PCBs are pressed together at the contact points of the corresponding solder pads in either PCB. In the case of a removable assembly, a clamping mechanism is applied, such as shown in Fig. 2B.

[0031] Alternatively, a sequential lamination method may be used. In the sequential lamination method, a PCB stack is built up using 2 separate laminates. The PCB stack is built up using the first laminate. The built up PCB stack is cut to the desired layer, and laminated using the second laminate, which provides the solder pads.

[0032] Fig. 6 is a diagram of example sections of System in Package (SIP) 602 and corresponding input-output (IO) board 604 for an on-cavity board-to-board interconnect. The SIP 602 is an 8-layer PCB stack that includes blocks 606, 608, 610, 612. Each block 606, 608, 610, 612 is cut to a different layer of the PCB stack, and corresponds to one of the blocks 614 on the IO board 604. For example, blocks 606, 610 have layers one and two removed, to expose solder pads on layer 3. The corresponding blocks 614 on the IO board 604 have layers 4 through 8 removed, to expose the solder pads at layer 3. Similarly, blocks 608, 612 have layers 1 through 5 removed to expose solder pads at layer 6. The corresponding blocks 614 on the IO board 604 have layers 7 and 8 removed to expose the solder pads at layer 6. Thus, the SIP 602 and IO board 604 can be combined to form on-cavity board-to-board interconnects that can interlock. The blocks 608, 610, 612 can be repeated along the edge of a SIP. As shown, the blocks along an edge of SIP 602 can be configured to have two alternating heights. In other words, a first block along an edge of SIP 602 can have a first height of X while a subsequent block along the same edge of SIP 602 can have a second height of Y, followed by a third block along the same edge having a first height of X. This configuration can allow SIP 602 and IO board 604 to mate or interlock with one another. In other embodiments, the blocks along an edge of SIP 602 can be

configured to have different heights which serve to guide SIP 602 into a preferred coupling configuration with IP board 604.

[0033] Fig. 7 is a diagram of an example on-cavity board-to-board interconnect 702 between a System in Package 704 and an IO board 706. The on-cavity board-to-board interconnect 702 represents the edges of the SIP 704 and IO board 706, i.e., blocks 606, 608, 610, 612, 614 described with reference to Fig. 6. Referring back to Fig. 7, in this way, SIP 704 may be placed within a cavity of IO board 702 so that the four edges of SIP 704 (i.e., the boundary of SIP 704) mates with a cavity of IO board 706. In one example, the z-height of the combined system is substantially the same as the z-height of the IO board 702. Furthermore, on-cavity board-to-board interconnect provides an increased IO density over traditional techniques. Screws 706 may be used to secure the SIP 704 and the IO board 706 together. Advantageously, using a removable assembly like screws 706, allows for the use of multiple, replaceable SIPs 704. Alternatively, the SIP 704 and IO board 706 may be soldered down, or combined using an anisotropic conductive adhesive.

[0034] EXAMPLES

[0035] Example 1 is a system. The system includes a first printed circuit board (PCB) having a first recess along a first edge of the first PCB that exposes a first solder pad on a layer of the first PCB; a second PCB having a second recess along a second edge of the second PCB that exposes a second solder pad on a layer of the second PCB, the second recess being complementary to the first recess to allow the first PCB to mate with the second PCB, wherein the first solder pad is aligned with the second solder pad when the first PCB is mated with the second PCB; and an assembly configured to electronically couple the first solder pad with the second solder pad.

[0036] Example 2 includes the system of example 1, including or excluding optional features. In this example, the first PCB is a system in package (SIP) and the second PCB is an IO board. Optionally, the IO board includes a cavity to house the first PCB.

[0037] Example 3 includes the system of any one of examples 1 to 2, including or excluding optional features. In this example, a z-height of the first PCB is substantially the same as the z-height of the system.

[0038] Example 4 includes the system of any one of examples 1 to 3, including or excluding optional features. In this example, the assembly includes a conductive material comprising an anisotropic conductive adhesive.

[0039] Example 5 includes the system of any one of examples 1 to 3, including or excluding optional features. In this example, the assembly includes a conductive material to apply to the first solder pad and the second solder pad and a removable clamping mechanism.

[0040] Example 6 includes the system of example 5, including or excluding optional features. In this example, the first recess exposes at least two layers of the first PCB. Optionally, the first recess includes a plurality of alternating blocks, wherein a first set of blocks expose solder pads on a first layer of the first PCB and a second set of blocks expose solder pads on a second layer of the first PCB.

[0041] Example 7 is a method for interconnecting two PCBs. The method includes generating a first recess along a first edge of a first PCB, the first recess exposing a first solder pad on a layer of the first PCB; generating a second recess along a second edge of a second PCB, the second recess being complementary to the first recess and having a second solder pad on the layer of the second PCB; applying a conductive material to the first solder pad and the second solder pad; and mating the first edge of the first PCB to the second edge of the second PCB such that the first solder pad is electronically coupled to the second solder pad via the conductive material.

[0042] Example 8 includes the method of example 7, including or excluding optional features. In this example, the first PCB is a SIP and the second PCB is an IO board. Optionally, the IO board includes a cavity to house the SIP.

[0043] Example 9 includes the method of any one of examples 7 to 8, including or excluding optional features. In this example, generating the first recess comprises generating a first plurality of alternating blocks, wherein the first set of blocks expose solder pads on a first layer of the first PCB and a second set of blocks expose solder pads on a second layer of the first PCB. Optionally, generating the second recess comprises generating a second plurality of alternating blocks that are complementary to the first plurality of alternating blocks.

[0044] Example 10 includes the method of any one of examples 7 to 9, including or excluding optional features. In this example, mating the first edge of the first PCB to the

second edge of the second PCB comprises applying a removable clamping mechanism to clamp the first PCB to the second PCB.

[0045] Example 11 is an apparatus. The apparatus includes a printed circuit board (PCB) including: a first layer to ground the PCB and a second layer below the first layer having a first plurality of solder pads exposed along an edge of the PCB; and an arrangement of conductive material to cover the first plurality of solder pads.

[0046] Example 12 includes the apparatus of example 11, including or excluding optional features. In this example, the conductive material includes an anisotropic conductive adhesive to fix the PCB to another PCB.

[0047] Example 13 includes the apparatus of any one of examples 11 to 12, including or excluding optional features. In this example, the PCB further includes an opening to house a securing mechanism for securing the PCB to another PCB.

[0048] Example 14 includes the apparatus of any one of examples 11 to 13, including or excluding optional features. In this example, the PCB further includes: a notch within the first layer to expose the at least one solder pad of the second layer.

[0049] Example 15 includes the apparatus of any one of examples 11 to 14, including or excluding optional features. In this example, the PCB further includes: a third layer below the second layer having a second plurality of solder pads.

[0050] Example 16 includes the apparatus of any one of examples 11 to 15, including or excluding optional features. In this example, the second plurality of solder pads are exposed along the edge of the PCB.

[0051] Example 17 includes the apparatus of any one of examples 11 to 16, including or excluding optional features. In this example, the second plurality of solder pads are exposed parallel to the first plurality of solder pads.

[0052] Example 18 is a method. The method includes generating a first notch through a first set of layers of a printed circuit board (PCB) to form a first recess exposing a first plurality of solder pads along a first edge of the PCB; and applying a conductive material to the first plurality of solder pads, the conductive material being configured to electronically couple the PCB to another PCB.

[0053] Example 19 includes the method of example 18, including or excluding optional features. In this example, the method includes generating a second notch through a

second set of layers of the PCB to form a second recess exposing a second plurality of solder pads, the second set of layers being different than the first set. Optionally, the second plurality of solder pads are exposed along the first edge of the PCB.

[0054] Example 20 includes the method of any one of examples 18 to 19, including or excluding optional features. In this example, the second plurality of solder pads are parallel to the first plurality of solder pads.

[0055] Example 21 includes the method of any one of examples 18 to 20, including or excluding optional features. In this example, the method includes generating an opening in the PCB to house a securing mechanism to secure the PCB to the another PCB.

[0056] Example 22 is a system for interconnecting two PCBs. The system includes means to generate a first recess along a first edge of a first PCB, the first recess exposing a first solder pad on a layer of the first PCB; means to generate a second recess along a second edge of a second PCB, the second recess being complementary to the first recess and having a second solder pad on the layer of the second PCB; means to apply a conductive material to the first solder pad and the second solder pad; and means to mate the first edge of the first PCB to the second edge of the second PCB such that the first solder pad is electronically coupled to the second solder pad via the conductive material.

[0057] Example 23 includes the system of example 22, including or excluding optional features. In this example, the first PCB is a SIP and the second PCB is an IO board. Optionally, the IO board includes a cavity to house the SIP.

[0058] Example 24 includes the system of any one of examples 22 to 23, including or excluding optional features. In this example, the means to generate the first recess comprises means to generate a first plurality of alternating blocks, wherein the first set of blocks expose solder pads on a first layer of the first PCB and a second set of blocks expose solder pads on a second layer of the first PCB. Optionally, the means to generate the second recess comprises means to generate a second plurality of alternating blocks that are complementary to the first plurality of alternating blocks.

[0059] Example 25 includes the system of any one of examples 22 to 24, including or excluding optional features. In this example, the means to mate the first edge of the first PCB to the second edge of the second PCB comprises means to apply a removable clamping mechanism to clamp the first PCB to the second PCB.

[0060] Not all components, features, structures, characteristics, etc., described and illustrated herein need be included in a particular embodiment or embodiments. If the specification states a component, feature, structure, or characteristic “may”, “might”, “can” or “could” be included, for example, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to “a” or “an” element, that does not mean there is only one of the element. If the specification or claims refer to “an additional” element, that does not preclude there being more than one of the additional element.

[0061] It is to be noted that, although some embodiments have been described in reference to particular implementations, other implementations are possible according to some embodiments. Additionally, the arrangement and/or order of circuit elements or other features illustrated in the drawings and/or described herein need not be arranged in the particular way illustrated and described. Many other arrangements are possible according to some embodiments.

[0062] In each system shown in a figure, the elements in some cases may each have a same reference number or a different reference number to suggest that the elements represented could be different and/or similar. However, an element may be flexible enough to have different implementations and work with some or all of the systems shown or described herein. The various elements shown in the figures may be the same or different. Which one is referred to as a first element and which is called a second element is arbitrary.

[0063] It is to be understood that specifics in the aforementioned examples may be used anywhere in one or more embodiments. For instance, all optional features of the computing device described above may also be implemented with respect to either of the methods or the computer-readable medium described herein. Furthermore, although flow diagrams and/or state diagrams may have been used herein to describe embodiments, the techniques are not limited to those diagrams or to corresponding descriptions herein. For example, flow need not move through each illustrated box or state or in exactly the same order as illustrated and described herein.

[0064] The present techniques are not restricted to the particular details listed herein. Indeed, those skilled in the art having the benefit of this disclosure will appreciate that many other variations from the foregoing description and drawings may be made within the scope

of the present techniques. Accordingly, it is the following claims including any amendments thereto that define the scope of the present techniques.

CLAIMS

What is claimed is:

1. An apparatus for manufacturing printed circuit board for board-to-board interconnect, comprising logic, at least partially including hardware logic, to:
generate a first printed circuit board comprising first solder pads;
generate a second printed circuit board comprising second solder pads;
cut the first printed circuit board to expose the first solder pads; and
cut the second printed circuit board to expose the second solder pads.
2. The apparatus of claim 1, comprising logic to place a relief film on the first solder pads and the second solder pads, wherein the relief film eases exposing the first solder pads and the second solder pads.
3. The apparatus of claims 1 or 2, comprising logic to apply a conductive material to the exposed first solder pads, and the exposed second solder pads.
4. The apparatus of claim 3, wherein the conductive material comprises anisotropic conductive adhesive.
5. The apparatus of claim 4, comprising logic to combine the first printed circuit board and the second printed circuit board at the exposed first solder pads and the exposed second solder pads.
6. The apparatus of claim 3, wherein the conductive material comprises metallized particle interconnect.
7. The apparatus of claim 6, comprising logic to combine the first printed circuit board and the second printed circuit board at the exposed first solder pads and the exposed second solder pads using a removable clamping mechanism.

8. The apparatus of claim 1 to 7, wherein generating the first printed circuit board comprises using a sequential lamination method.

9. The apparatus of claim 8, wherein the sequential lamination method comprises building up the first printed circuit board using as first laminate.

10. The apparatus of claim 9, wherein the sequential lamination method comprises:

cutting the first printed circuit board to a desired layer; and
laminating the cut first printed circuit board using a second laminate that provides the first solder pads.

11. A method for manufacturing printed circuit board for board-to-board interconnect, comprising:

generating a first printed circuit board comprising first solder pads;
generating a second printed circuit board comprising second solder pads;
cutting the first printed circuit board to expose the first solder pads; and
cutting the second printed circuit board to expose the second solder pads.

12. The method of claim 11, comprising placing a relief film on the first solder pads and the second solder pads, wherein the relief film eases exposing the first solder pads and the second solder pads.

13. The method of claims 11 or 12, comprising applying a conductive material to the exposed first solder pads, and the exposed second solder pads.

14. The method of claim 13, wherein the conductive material comprises anisotropic conductive adhesive.

15. The method of claim 14, comprising combining the first printed circuit board and the second printed circuit board at the exposed first solder pads and the exposed second solder pads.

16. The method of claim 13, wherein the conductive material comprises metallized particle interconnect.

17. The method of claim 16, comprising combining the first printed circuit board and the second printed circuit board at the exposed first solder pads and the exposed second solder pads using a removable clamping mechanism.

18. The method of claim 11 to 17, wherein generating the first printed circuit board comprises using a sequential lamination method.

19. The method of claim 18, wherein the sequential lamination method comprises building up the first printed circuit board using a first laminate.

20. An apparatus for interconnecting printed circuit boards, comprising:
a first printed circuit board layer comprising first solder pads, wherein the first printed circuit board layer is cut to expose the first solder pads; and
a conductive film, applied to the exposed first solder pads to enable an interconnection between the first solder pads and second solder pads of a second printed circuit board layer.

21. The apparatus of claim 20, comprising a second printed circuit board layer cut to expose the second solder pads, wherein the second printed circuit board layer is combined with the first printed circuit board layer to form a board-to-board interconnect.

22. A system for manufacturing printed circuit board for board-to-board interconnect, comprising:

means for generating a first printed circuit board comprising first solder pads;
means for generating a second printed circuit board comprising second solder pads;
means for cutting the first printed circuit board to expose the first solder pads; and
means for cutting the second printed circuit board to expose the second solder pads.

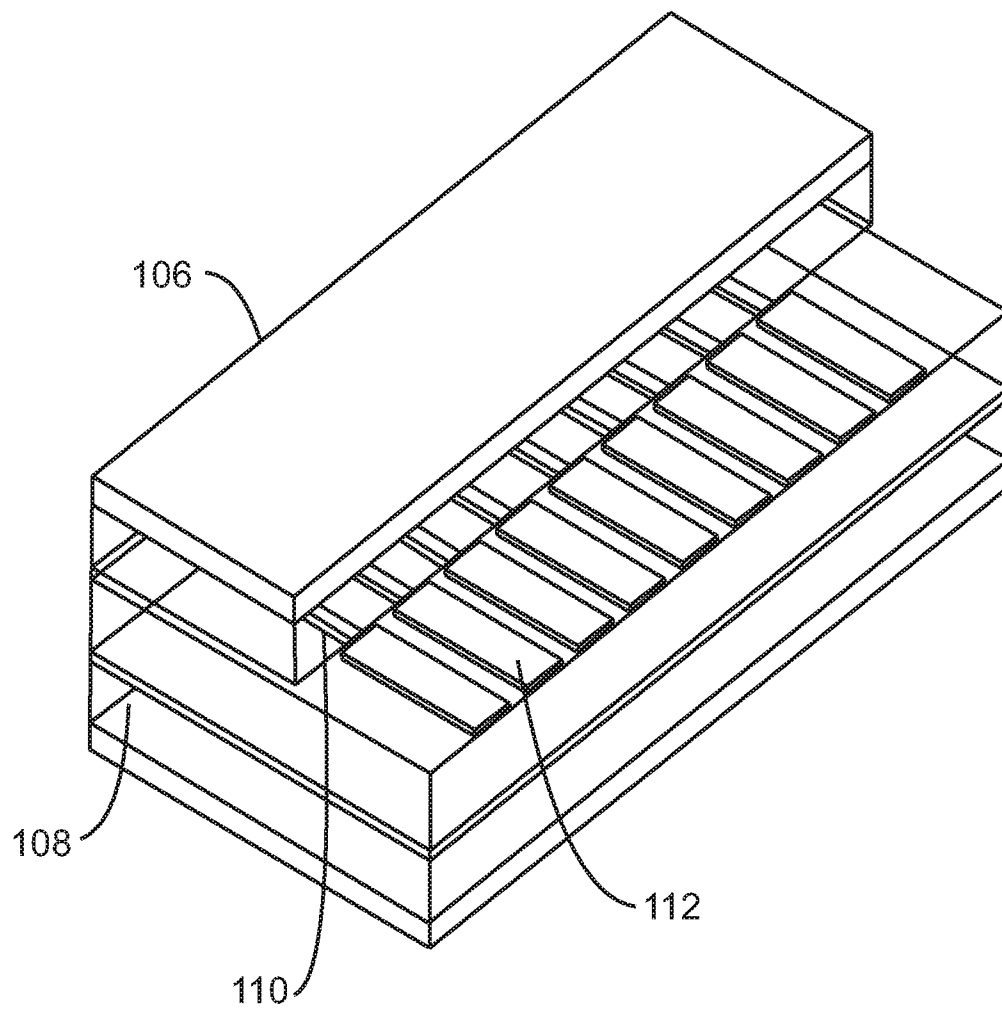
23. The system of claim 22, comprising means for placing a relief film on the first solder pads and the second solder pads, wherein the relief film eases exposing the first solder pads and the second solder pads.

24. A computer-readable medium for manufacturing printed circuit board for board-to-board interconnect, the medium having instructions stored therein that, in response to being executed on a processor, cause the processor to:

generate a first printed circuit board comprising first solder pads;
generate a second printed circuit board comprising second solder pads;
cut the first printed circuit board to expose the first solder pads; and
cut the second printed circuit board to expose the second solder pads.

25. The computer-readable medium of claim 24, wherein the instructions cause the processor to place a relief film on the first solder pads and the second solder pads, wherein the relief film eases exposing the first solder pads and the second solder pads.

1/9



102
FIG. 1A

2/9

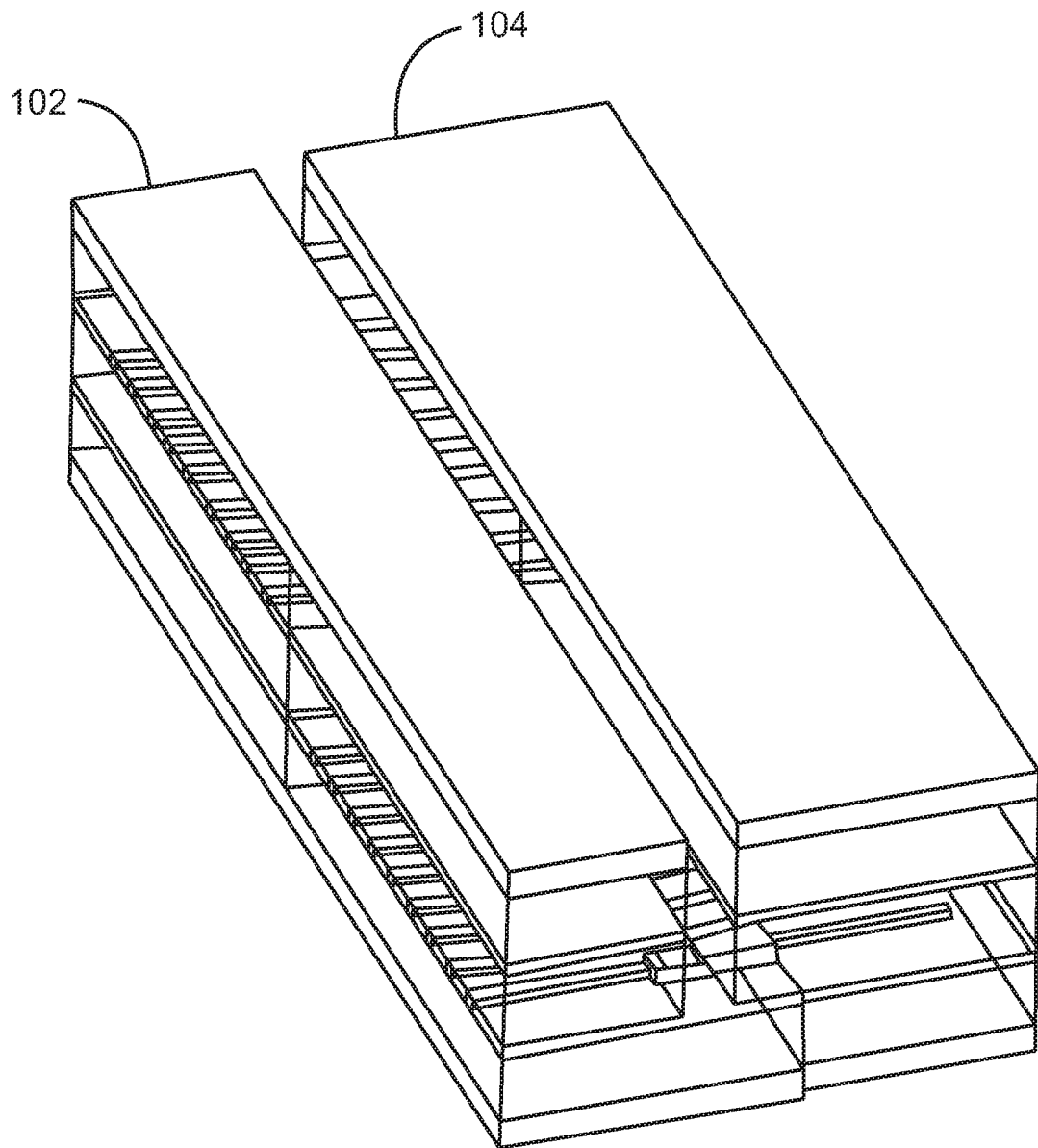


FIG. 1B

3/9

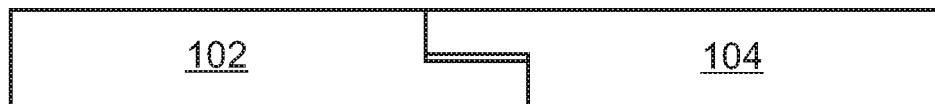


FIG. 1C

4/9

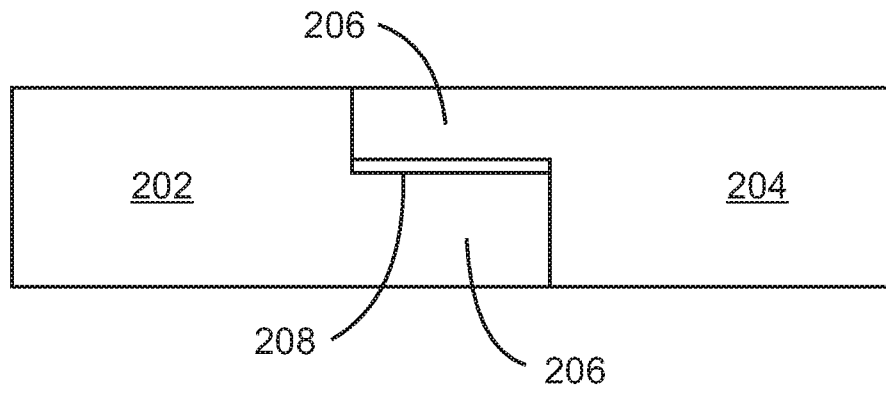


FIG. 2A

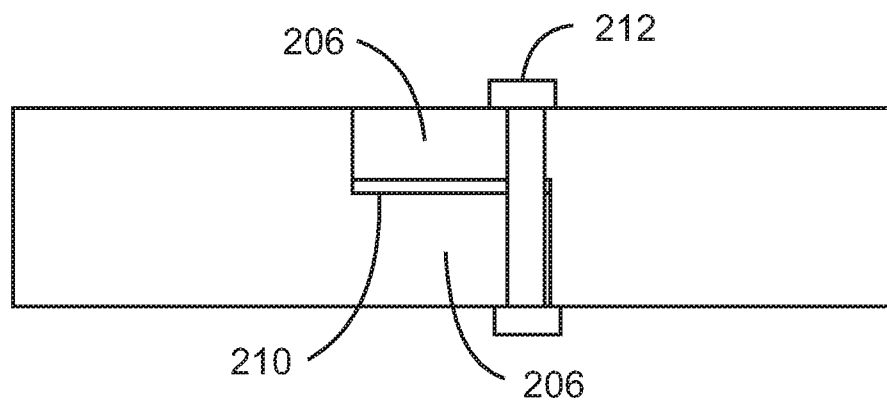
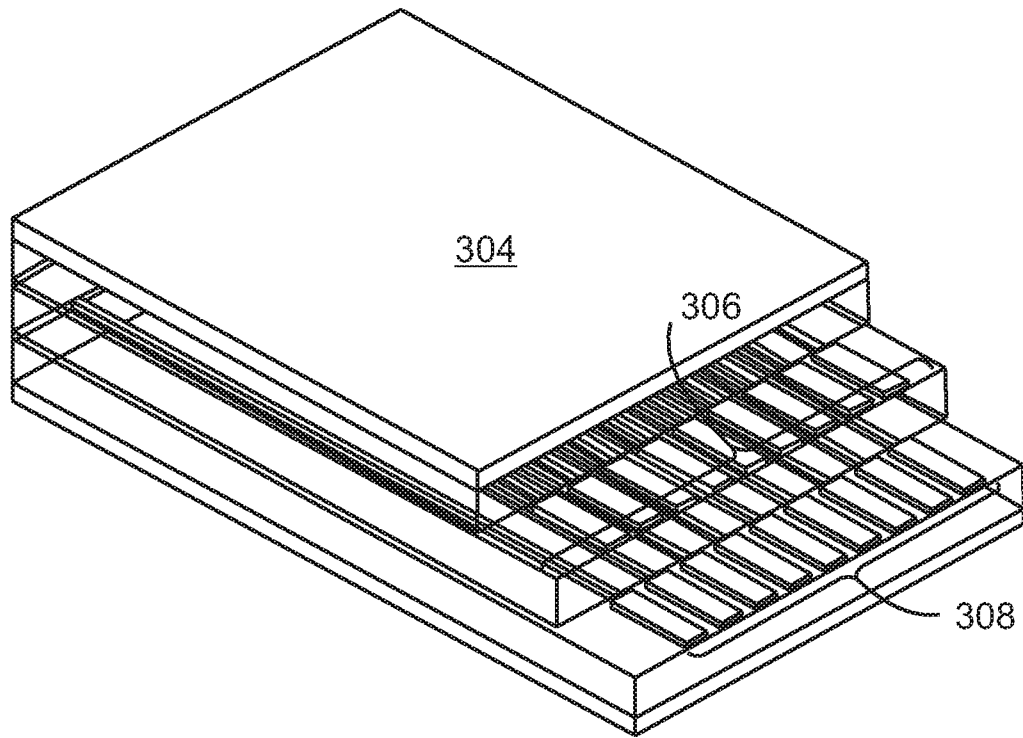


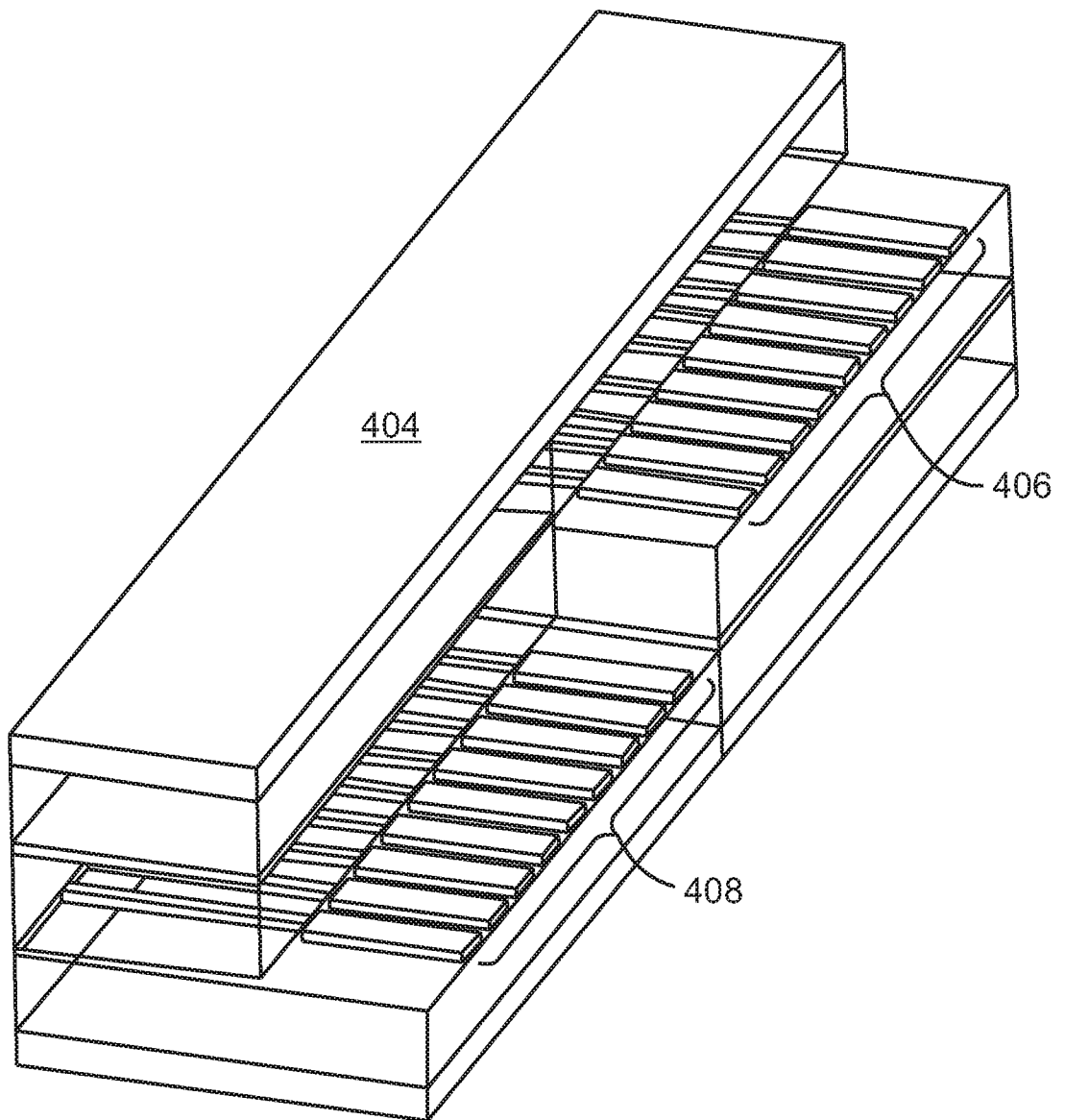
FIG. 2B

5/9



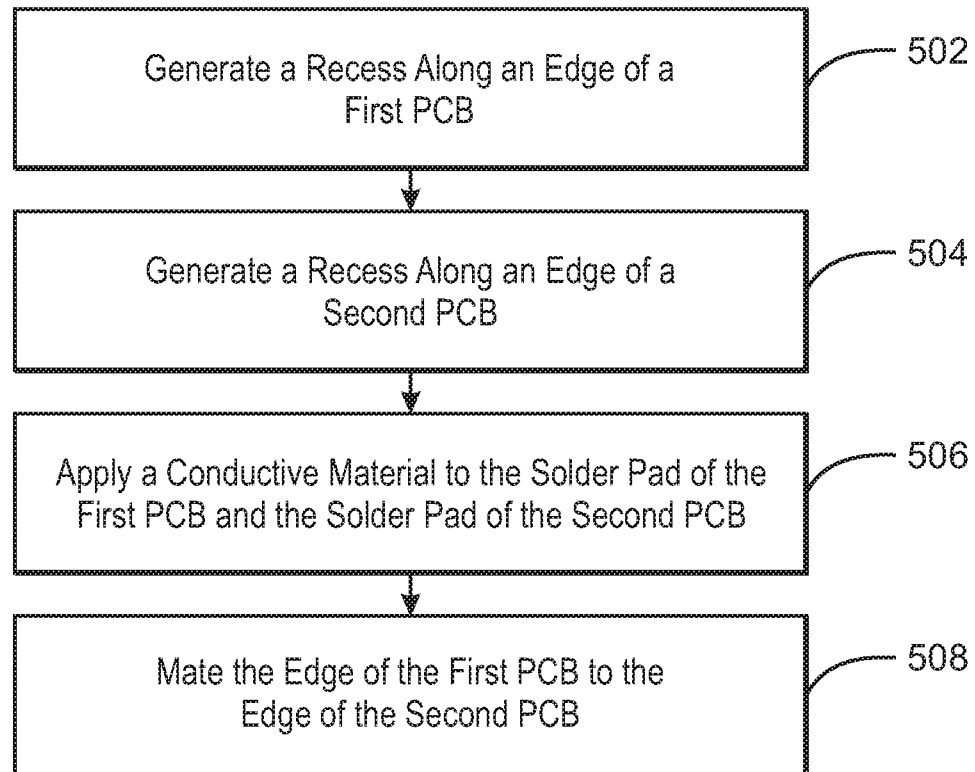
300
FIG. 3

6/9



402
FIG. 4

7/9



500
FIG. 5

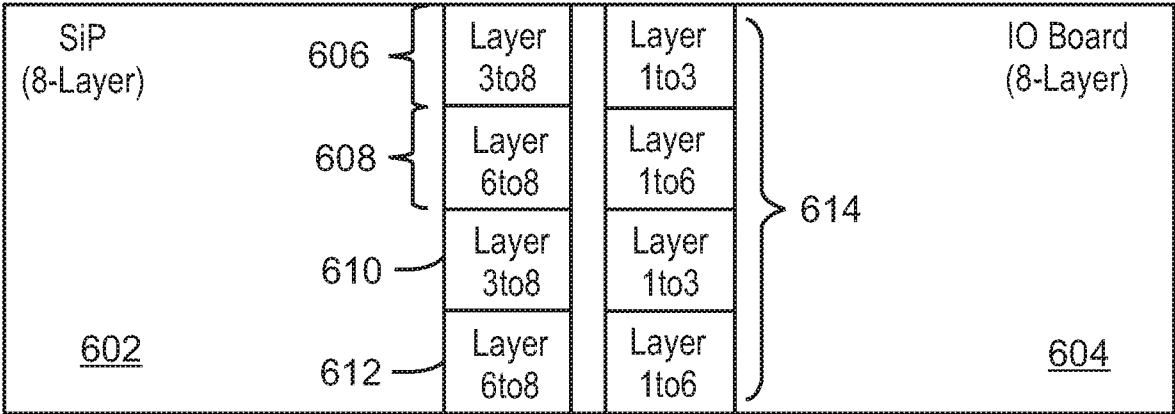


FIG. 6

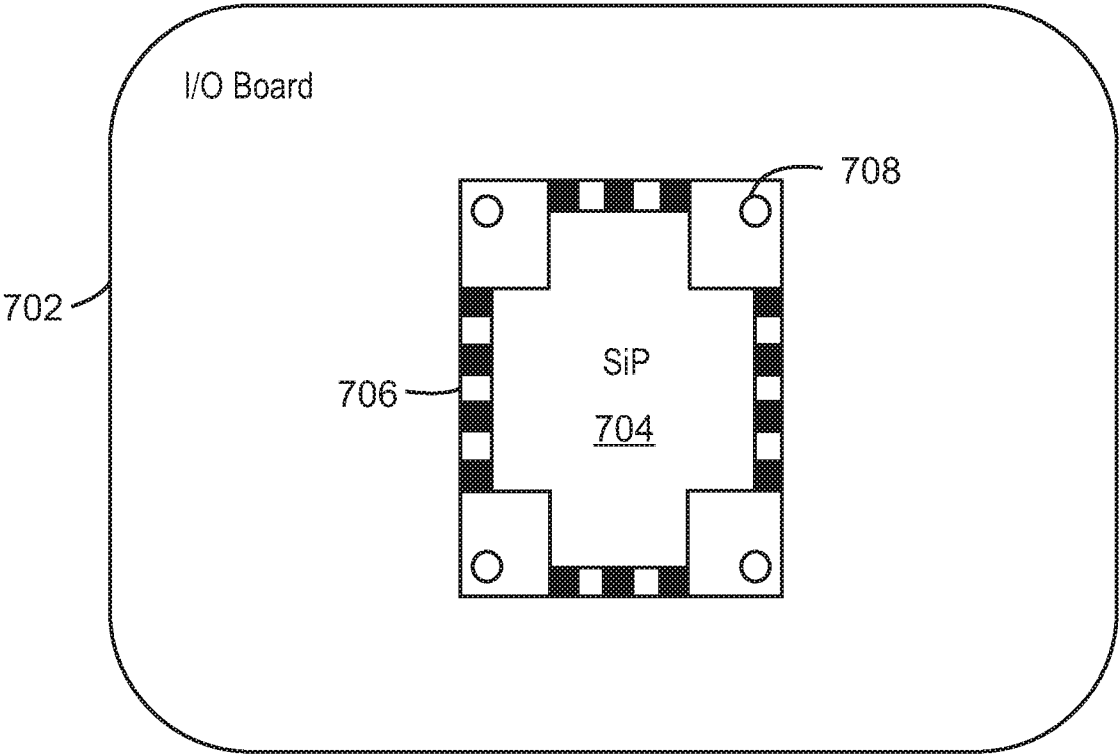


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/059252**A. CLASSIFICATION OF SUBJECT MATTER****H05K 3/40(2006.01)i, H05K 1/11(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H05K 3/40; H05K 3/36; H05K 1/14; H05K 1/11; H01L 21/762; H01L 23/498; H05K 1/02; B29C 65/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: interconnect, board to board, printed circuit board, solder pad

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0069696 A1 (APPLE INC.) 13 March 2014 See paragraphs [0028]-[0031], [0037]-[0042] and figures 1-3, 7, 9-10.	1-5, 11-15, 20-25
Y		6-7, 16-17
Y	JP 2006-237334 A (FUJI PHOTO FILM CO., LTD.) 07 September 2006 See paragraphs [0023]-[0026] and figure 4.	6-7, 16-17
A	KR 10-0483399 B1 (SAMSUNG ELECTRONICS CO., LTD.) 10 August 2005 See claims 1-6, 10 and figures 4-8.	1-7, 11-17, 20-25
A	WO 2015-166222 A1 (FLEXENABLE LIMITED) 05 November 2015 See pages 7, line 20 - page 11, line 17 and figures 1a-2.	1-7, 11-17, 20-25
A	US 2014-0084454 A1 (APPLE INC.) 27 March 2014 See paragraphs [0027]-[0032] and figures 3A-4.	1-7, 11-17, 20-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

09 January 2017 (09.01.2017)

Date of mailing of the international search report

10 January 2017 (10.01.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



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INTERNATIONAL SEARCH REPORTInternational application No.
PCT/US2016/059252**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 9-10, 19
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claims 9-10, 19 are regarded to be unclear because the claims refer to multiple dependent claims which do not comply with PCT Rule 6.4(a).
3. ☒ Claims Nos.: 8, 18
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/059252

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0069696 A1	13/03/2014	CN 103676249 A CN 103676249 B	26/03/2014 10/08/2016
JP 2006-237334 A	07/09/2006	None	
KR 10-0483399 B1	10/08/2005	KR 10-1999-0024909 A	06/04/1999
WO 2015-166222 A1	05/11/2015	GB 2525605 A	04/11/2015
US 2014-0084454 A1	27/03/2014	US 9117873 B2	25/08/2015