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(54) Title: METHOD FOR FABRICATING THREE DIMENSIONAL DEVICE

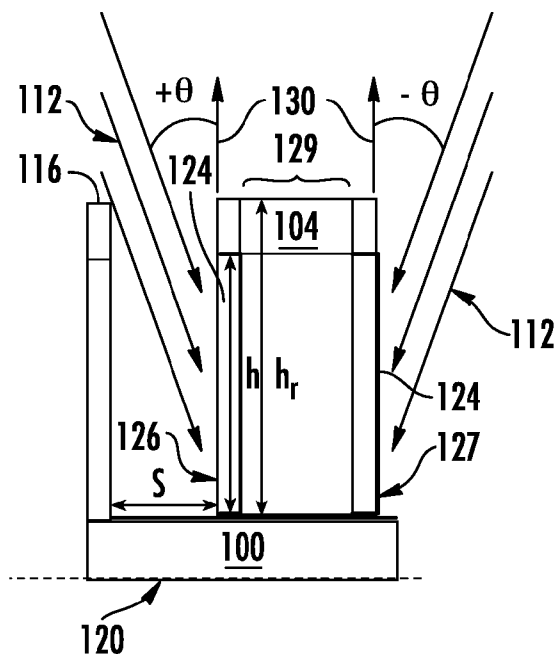


FIG. 1C

(57) Abstract: A method for forming a three dimensional device. The method may include directing ions to an end surface of an extension region of a fin structure, the fin structure extending perpendicularly from a substrate plane and having a fin axis parallel to the substrate plane, wherein the ions have trajectories extending in a plane perpendicular to the substrate plane and parallel to the fin axis, wherein a portion of the fin structure is covered by a gate structure defining a channel region, and wherein the end surface is not covered by the gate structure.



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SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

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— *with international search report (Art. 21(3))*

## **METHOD FOR FABRICATING THREE DIMENSIONAL DEVICE**

### **Field**

[0001] The present embodiments relate to three dimensional device structures, and more particularly, to techniques for doping three dimensional devices.

### **Background**

[0002] In the present day, three dimensional transistor devices are used to provide increased performance over planar transistors. Devices such as finFET devices and horizontal-Gate-All-Around (hGAA) FETs are formed from fin-shaped semiconductor regions extending perpendicularly from a substrate plane, such as the plane of a silicon wafer. Adjacent fins in such devices may be packed close to one another where a ratio of fin structure height: fin structure spacing may approach 10:1 at certain stages in processing, accounting for extra layers including polysilicon and masking layers. Under these circumstances implanting source/drain or source/drain extension regions of the fin structures may be difficult because ions directed to a surface of a given fin structure are shadowed by and adjacent fin or adjacent fins.

[0003] With respect to these and other considerations the present disclosure is provided.

### **Summary**

[0004] In one embodiment, a method for forming a three dimensional device may include directing ions to an end surface of an extension region of a fin structure, the fin structure extending perpendicularly from a substrate plane and having a fin axis parallel to the substrate plane, wherein the ions have trajectories extending in a plane perpendicular to the substrate plane and parallel to the fin axis, wherein a portion of the

fin structure is covered by a gate structure defining a channel region, and wherein the end surface is not covered by the gate structure.

**[0005]** In another embodiment, a method for forming a three dimensional device may include providing a plurality of fin structures extending perpendicularly from a substrate plane, the fin-type structures being parallel to one another and having a fin axis parallel to the substrate plane; providing a gate structure covering a portion of the fin structures, wherein the gate structure defines an exposed region of a given fin structure; removing at least a portion of the exposed region, wherein an extension region of the fin structures is formed having an end surface not covered by the gate structure; and directing ions to the end surface, the ions having trajectories extending in a plane perpendicular to the substrate plane and parallel to the fin axis.

**[0006]** In a further embodiment, a method of forming a source/drain region in a multigate transistor may include providing a plurality of fin structures extending perpendicularly from a substrate plane, the fin structures being parallel to one another and having a fin axis parallel to the substrate plane, wherein the fin structures comprise at least monocrystalline silicon. The method may further include providing a gate structure covering a portion of the fin structures, wherein the gate structure defines an exposed region of a given fin structure. The method may also include, before the performing a source/drain extension implant, removing at least a portion of the exposed region, wherein an extension region of the fin structures is formed having an end surface not covered by the gate structure.

**Brief Description of the Drawings**

[0007] **FIGs. 1A to 1C** illustrate a side view of a device during different stages of fabrication according to embodiments of the disclosure;

[0008] **FIG. 1D** depicts an end perspective view of the device of FIGs. 1A-1C during the stage depicted in FIG. 1C;

[0009] **FIGs. 2A to 2C** illustrates a side view of another device during different stages of fabrication according to additional embodiments of the disclosure;

[0010] **FIG. 2D** depicts an end perspective view of the device of FIGs. 2A-2C during the stage depicted in FIG. 2C;

[0011] **FIG. 3** depicts an exemplary process flow for fabricating a device according to various embodiments of the disclosure;

[0012] **FIG. 4** depicts another exemplary process flow according to further embodiments of the disclosure.

**Detailed Description**

[0013] The present embodiments will now be described more fully hereinafter with reference to the accompanying drawings, where some embodiments are shown. The subject matter of the present disclosure may be embodied in many different forms and are not to be construed as limited to the embodiments set forth herein. These embodiments are provided so this disclosure will be thorough and complete, and will fully convey the scope of the subject matter to those skilled in the art. In the drawings, like numbers refer to like elements throughout.

[0014] The embodiments described herein provide novel processing and device

structures for forming three dimensional devices including multigate metal oxide semiconductor field effect transistors (MOSFETs). The terms "multigate transistor" or "multigate MOSFET" refer to a type of three dimensional device where channel regions of the transistor extend from a substrate surface to present multiple sides for contacting by a gate. Examples of multigate MOSFETs include finFET devices or hGAA FET devices, as well as vertical channel FET devices. A characteristic of multigate MOSFETs is a given gate structure forming on various different sides of a semiconductor channel, where the semiconductor channel may be formed within a fin structure. Thus, the gate structure may act to gate the channel from various sides, as opposed to a planar MOSFET, where gating takes place from just a top side of a channel. Various embodiments facilitate improved doping of transistor features such as source/drain extension (SDE) regions, source/drain (S/D) and adjacent regions of a three dimensional field effect transistor.

**[0015]**        **FIGs. 1A to 1C** illustrate a side view of a device 120 during different stages of fabrication according to embodiments of the disclosure. **FIG. 1D** depicts an end perspective view of the device of FIGs. 1A-1C during the stage depicted in FIG. 1C. As illustrated in FIG. 1A a fin structure 102 is disposed on a substrate 100. The fin structure 102 may in some examples constitute a crystalline material such as monocrystalline silicon. The fin structure 102 extends perpendicularly from the substrate plane (X-Y plane) of substrate 100. At the stage of formation shown in FIG. 1A, a gate structure 104 is also disposed over the fin structure 102. In some cases, the gate structure 104 may be a dummy gate to be replaced at later stages of processing. As more clearly illustrated in FIG. 1D, a plurality of fin structures 102 may be arranged parallel to one another and may have a fin axis extending parallel to the X-axis (and parallel to the substrate plane P) in the Cartesian coordinate system shown. The fin axis may be parallel

to a direction of current flow between S/D regions in a transistor device to be formed. As further shown in FIG. 1A, sidewalls 106 may be formed along the gate structure 104, where the gate structure 104 (and sidewalls 106) cover the fin structure 102 in a manner leaving an exposed region 118.

[0016] In known device fabrication techniques, S/D regions and SDE regions may be implanted with ions to introduce a target level of dopants for forming source regions and drain regions on opposite sides of a channel. The channel (not shown) may be formed in a portion of a fin structure covered by at least a portion of the gate structure 104. In order to introduce dopants into such S/D or SDE regions known techniques may implant ions into a device structure such as shown in FIG. 1A, where the ion trajectories lie within the Y-Z plane. In this known approach, the ions are implanted at a low angle of incidence with respect to the Z-axis in order to impact the sides 122 of fin structures 102 lying in the X-Z plane. Because of the height of the fin structures 102 along the Z-direction and close spacing of fin structures 102 along the Y-direction, ions are directed toward the sides 122 at angles of approximately 7 degrees or less with respect to the Z-axis in some known techniques.

[0017] According to various embodiments of the disclosure an innovative technique provides improvements on the aforementioned approach. An example of this novel and innovative technique is illustrated in FIG. 1B and FIG. 1C. In FIG 1B a portion of the exposed region 118 is removed from the fin structure 102. In this example the fin structure 102 may be etched at least to the substrate 100. The embodiments are not limited in this context.

**[0018]** When the fin structure 102 is etched as shown in FIG. 1B, an extension region 124 is formed presenting an end surface 126. A portion of the fin structure 102 is covered by the gate structure 104, defining a channel region 129.

**[0019]** The end surface 126 forms an end surface of the fin structure 102 at this stage of processing, and represents a surface not covered by the gate structure 104 or the sidewalls 106. Likewise, on an opposite end of the fin structure 102, a second extension region, also designated as extension region 124, is formed. On this opposite end of the fin structure 102, the extension region has an end surface 127, also not covered by the gate structure 104 or sidewalls 106. As illustrated, the end surface 126 and end surface 127 may lie parallel to the Y-Z plane.

**[0020]** Turning now to FIG. 1C, after the exposed region 118 is etched forming the extension region 124, ions 112 may be directed to the extension regions 124. In particular, the ions 112 may be directed to the end surface 126 and the end surface 127. The ions 112 may be implanted into an extension region 124 in one implant process or a plurality of implant processes, to act as a source/drain extension (SDE) doping implant, and may additionally act as ions for "halo" doping, for example. In this embodiment, the ions 112 may be directed along trajectories lying within the X-Z plane, where the X-Z plane is perpendicular to a substrate plane P lying parallel to the X-Y plane. The end surface 126 and end surface 127 may lie parallel to the Y-Z plane. Accordingly, the trajectories of ions 122 may lie within a plane perpendicular to a plane of the end surface 126 and a plane of the end surface 127. The ions 112 may have trajectories also forming a non-zero angle of incidence, shown as an angle of incidence  $\theta$  with respect to a perpendicular 130 to the substrate plane P. As illustrated in FIG. C, ions 112 may be directed in one implant process at an angle of  $+\theta$  to the end surface 126 and in a second

implant process at an angle of  $-\theta$  to the end surface 127. In one example where the ions 112 are dopant ions, the ions may form a first source/drain extension when implanted through the end surface 126 and a second source/drain extension when implanted through the end surface 127. The two source/drain extensions may form two junctions defining opposite ends of a channel extending along the X-axis through the fin structure 102. Subsequently to the operations depicted in FIGs. 1A-1C, a source/drain region may be regrown into the exposed region 118. Notably, the angle  $-\theta$  and angle  $+\theta$  may have the same magnitude or different magnitude.

**[0021]** An advantage of the approach depicted in FIGs. 1A-1C is the ability to provide ions 112 at an angle of incidence  $\theta$  greater than in known processing of finFET structures or hGAA FET structures. In the known approaches, SDE implantation may take place into a device structure at the stage illustrated in FIG. 1A, for example. The maximum tilt-angle may be defined as an angle,  $\theta_{crit}$ , where an incident ion 112 is able to reach the bottom of the end surface 126 while not being blocked by the top of adjacent structure 116. The maximum tilt angle can be calculated as  $\theta_{crit} = \arctan(<\text{distance } S \text{ along X axis between adjacent structure 116 and the gate structure 104 including sidewall 106}> / <\text{height } h_T, \text{ the total gate height from the bottom of the fin structure 102 to the top of the gate structure 104}>)$ , or more simply,  $(S/h_T)$ . This distance  $S$  as shown in FIG. 1C represents the distance along the X-axis between the end surface 126 and the adjacent structure 116. Notably, in the approach shown in FIGs. 1A-1C, the adjacent structure 116 is located on the same fin string as the fin structure 102 located under gate structure 104, and hence is of the same polarity. Accordingly, the adjacent structure 116 does not have a mask such as resist when ion implantation is performed into the extension region 124. By way of comparison, for known approaches, where the SDE implant takes place into

the sides 122 of a fin structure 102, ions 112 now incident with a tilt in the Y-Z plane have to clear adjacent fin structures 102 (see FIG. 1D). Frequently, adjacent fin structures 102 are of opposite polarity to one another so a first fin is protected by a mask (not shown in the FIGS.) when an adjacent fin is implanted. The thickness of this mask has to be taken into account by adding to the denominator in the aforementioned formula for  $\theta_{\text{crit}}$ , making  $\theta_{\text{crit}}$  smaller for known implantation approaches where ions have a tilt in the Y-Z plane and are implanted into the sides 122 of a fin structure 102. In one particular example, for a 7 nm technology node, ions 112 may be directed to the end surfaces 126 at an angle of incidence of 10 degrees to 12 degrees, and in particular at an angle of incidence of 12 degrees with respect to the direction 130. In comparison a maximum angle for ions when directed at sides of fin structures according to known techniques for the same technology node is 7 degrees.

**[0022]** By way of comparison, for a given tilt-angle, ions implanted using a known approach, being tilted in plane Y-Z and incident into the sides 122 of the fin structure 102, also implant the top surface 132 of a fin structure 102 in the exposed region 118. The incident angle for the top surface 132 is given by the tilt-angle  $\theta$ , as regards the sides 122 of the fin structures 102, the incidence angle may be expressed as  $90 - \theta$ . This difference results in a much larger effective dose to be implanted into the top surface 132 than the sides 122 of the fin structure 102, leading to much higher dopant volume concentration and more lateral penetration of dopant into the channel during implant and during subsequent thermal treatment at the top region of the fin. In contrast, directing the ions 112 with a tilt in the X-Z plane into the end surface 126 gives the same incident angle irrespective of where the ions impinge along the height,  $h$ , of end surface 126, leading to better junction planarity.

[0023] FIGs. 2A to 2C illustrate a side view of a device 220 during different stages of fabrication according to additional embodiments of the disclosure. FIG. 2D depicts an end perspective view of the device of FIGs. 2A-2C during the stage depicted in FIG. 2C. As illustrated in FIG. 2A a fin structure 200 is disposed on a substrate 100. The fin structure 200 may in some examples constitute a plurality of different semiconductor layers, such as at least three layers. In some cases at least one layer may comprise a first semiconductor material and at least one layer may comprise a second semiconductor material. In one example, a first semiconductor layer 202 may alternate with a second semiconductor layer 204. The first semiconductor layer 202 may be monocrystalline silicon and the second semiconductor layer 204 may be monocrystalline silicon:germanium in one example. The fin structure 200 may serve as the basis to form a horizontal-gate-all-around device structure (hGAA FET structure) by selectively etching the layer 202 or the layer 204 with respect to respective layers, layer 204 or layer 202, as known in the art. In other respects processing of the fin structure 200 may proceed as described above with respect to FIGs. 1A-1D. Accordingly, the end surface 226 and end surface 227 of extension regions 224 may be implanted by ions 112 at a greater angle of incidence  $\theta$  than is achievable by known techniques where ions are directed toward sides of fin structures 200 within the Y-Z plane.

[0024] In the embodiments of FIG. 1A to FIG. 2C, the ability to direct ions into end surfaces of a fin structure may provide more uniform doping as opposed to the approach of known techniques of directing ions into sidewalls of a fin structure. Simulations have been carried source/drain extension implants are performed upon fin structures using the approach generally illustrated by the FIGs. 1A-2C (where ions lie in the X-Z plane) and a conventional source/drain extension ion implantation process of

directing ions into fin sidewalls (where ions lie in the Y-Z plane). Results show junctions between the source/drain extension region formed by the techniques of the present embodiments are more uniform as compared to the conventional approach. Additionally, the variation in effective channel length ( $L_{eff}$ ) within a device is smaller according to the present embodiments as compared to the conventional approach. This may in part arise from the implanting of ions directly into the end surface 126 or end surface 127, where the end surfaces lie parallel (in the Y-Z plane) to the target junctions to be created by the source/drain extension implants. In this manner, the ions being implanted may be distributed uniformly over the end surface 126 and end surface 127, and may be implanted at a more uniform depth with respect to end surface 126 and end surface 127.

[0025] **FIG. 3** depicts an exemplary process flow 350 for fabricating a device according to various embodiments of the disclosure. The exemplary process flow 350 may represent a portion of operations employed to fabricate an hGAA transistor, for example. In a first operation 290 polysilicon deposition may be followed by chemical-mechanical polishing (CMP). In the operation 292 lithography may be applied to the deposited polysilicon to define a gate pattern. At operation 294, etching may be performed to define gate structures. In the subsequent operations shown in FIG. 3, a conventional sequence may be represented by: the operation 300, SDE spacer deposition and etch; operation 302, SDE implant/halo implant; operation 304, epitaxial spacer deposition and etch; operation 306, recess etch; and operation 308, raised source/drain epitaxial deposition. Such a conventional sequence may entail for operation 302, the directing of ions at the sidewalls of fin structures at relatively lower angles, such as 7 degrees, as noted above. Subsequently, during the recess etch of operation 306, an exposed region of the fin may be etched away to allow for growth of the raised

source/drain, in operation 308. In accordance with an embodiment of the disclosure, the operation 302 may be moved so the new sequence of operations proceeds as: operation 300, operation 304, operation 306, operation 302, and operation 308. Additionally the operation 302 may entail direction ions toward the end surface of fin structures at relatively larger angles, such as 12 degrees, as discussed above.

[0026] **FIG. 4** depicts another exemplary process flow 400 according to additional embodiments of the disclosure. At block 402, a plurality of fin structures are provided, extending perpendicularly from a substrate plane, where the fin-type structures are parallel to one another and have a fin axis. In different embodiments the fin structures may be formed from monocrystalline silicon or from a plurality of different semiconductor layers. In one example, a first semiconductor layer of the fin structure may alternate with a second semiconductor layer. The first semiconductor layer may be monocrystalline silicon and the second semiconductor layer may be a monocrystalline silicon:germanium alloy in one example.

[0027] At block 404, a gate structure is provided, covering a portion of the fin structures, wherein the gate structure defines an exposed region of a given fin structure.

[0028] At block 406, a portion of the exposed region is removed, wherein an extension region is formed having an end surface not covered by the gate structure.

[0029] At block 408 ions are directed to the extension region, where the ions have trajectories extending in a plane perpendicular to the substrate plane, perpendicular to a plane of the end surface, and parallel to the fin axis.

[0030] Advantages provided by the present embodiments include the ability to implant ions into a fin structure for source/drain extension doping at a greater angle of

incidence with respect to a fin surface being implanted in comparison to known approaches. For example, because implantation may be performed along a given fin string where adjacent structures have a same polarity, resist is not present on a structure adjacent to the fin structure on the same fin string being implanted. This allows ions to penetrate more uniformly into a fin surface as opposed to more grazing angles of incidence employed by conventional approaches, such as 7 degrees. Another advantage is the ability to direct dopants into a fin structure in a more uniform manner, since dopants may implant into an entire end surface representing a cross-section of a fin structure where the ions uniformly "illuminate" this cross-section. As a result, the present embodiments may generate a more planar junction as opposed to conventional approaches.

[0031] The present disclosure is not to be limited in scope by the specific embodiments described herein. Indeed, other various embodiments of and modifications to the present disclosure, in addition to those described herein, will be apparent to those of ordinary skill in the art from the foregoing description and accompanying drawings. Thus, such other embodiments and modifications are intended to fall within the scope of the present disclosure. Furthermore, the present disclosure has been described herein in the context of a particular implementation in a particular environment for a particular purpose. Those of ordinary skill in the art will recognize the usefulness is not limited thereto and the present disclosure may be beneficially implemented in any number of environments for any number of purposes. Thus, the claims set forth below are to be construed in view of the full breadth and spirit of the present disclosure as described herein.

**What is claimed is:**

1. A method for forming a three dimensional device, comprising:  
  
directing ions to an end surface of an extension region of a fin structure, the fin structure extending perpendicularly from a substrate plane and having a fin axis parallel to the substrate plane,  
  
wherein the ions have trajectories extending in a plane perpendicular to the substrate plane and parallel to the fin axis,  
  
wherein a portion of the fin structure is covered by a gate structure defining a channel region, and  
  
wherein the end surface is not covered by the gate structure.
2. The method of claim 1, wherein the fin structure comprises monocrystalline silicon.
3. The method of claim 1, wherein the fin structure comprise at least three layers, wherein at least one layer comprises silicon and at least one layer comprises a silicon:germanium alloy.
4. The method of claim 1, wherein the trajectories form an angle of incidence of 10 degrees to 12 degrees with respect to a perpendicular to the substrate plane.
5. The method of claim 1 wherein the ions are provided as a source/drain extension implant.

6. The method of claim 1, further comprising forming a raised source/drain on the extension region after the directing the ions into the end surface.

7. The method of claim 1, wherein the gate structure defines an exposed region of the fin structure, the method further comprising removing a portion of the exposed region, wherein the extension region of the fin structure is formed.

8. A method for forming a three dimensional device, comprising:

providing a plurality of fin structures extending perpendicularly from a substrate plane, the fin structures being parallel to one another and having a fin axis parallel to the substrate plane;

providing a gate structure covering a portion of the fin structures, wherein the gate structure defines an exposed region of a given fin structure;

removing at least a portion of the exposed region, wherein an extension region of the fin structures is formed having an end surface not covered by the gate structure; and

directing ions to the end surface, the ions having trajectories extending in a plane perpendicular to the substrate plane and parallel to the fin axis.

9. The method of claim 8, wherein the plurality of fin structures comprises monocrystalline silicon.

10. The method of claim 8, wherein the plurality of fin structures comprise at least three layers, wherein at least one layer comprises silicon and at least one layer comprises

a silicon:germanium alloy, wherein the fin structure comprises a portion of a horizontal-gate-all-around device structure.

11. The method of claim 8, wherein the trajectories form an angle of incidence of 10 degrees to 12 degrees with respect to a perpendicular to the substrate plane.

12. The method of claim 8, wherein three dimensional device comprises a plurality of fin strings, wherein a given fin string includes a given fin structure and an adjacent structure separated from the end surface of the fin structure by a distance  $S$ , wherein the gate structure is defined by a height  $h_T$ , and wherein the ions are directed at an angle of incidence defined by  $\arctan(S/h_T)$ .

13. The method of claim 8, wherein the plurality of fin structures comprise portions of a finFET device or portions of a horizontal-gate-all-around device.

14. A method of forming a multigate transistor, comprising:

providing a plurality of fin structures extending perpendicularly from a substrate plane, the fin structures being parallel to one another and having a fin axis parallel to the substrate plane, wherein the fin structures comprise at least monocrystalline silicon;

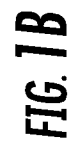
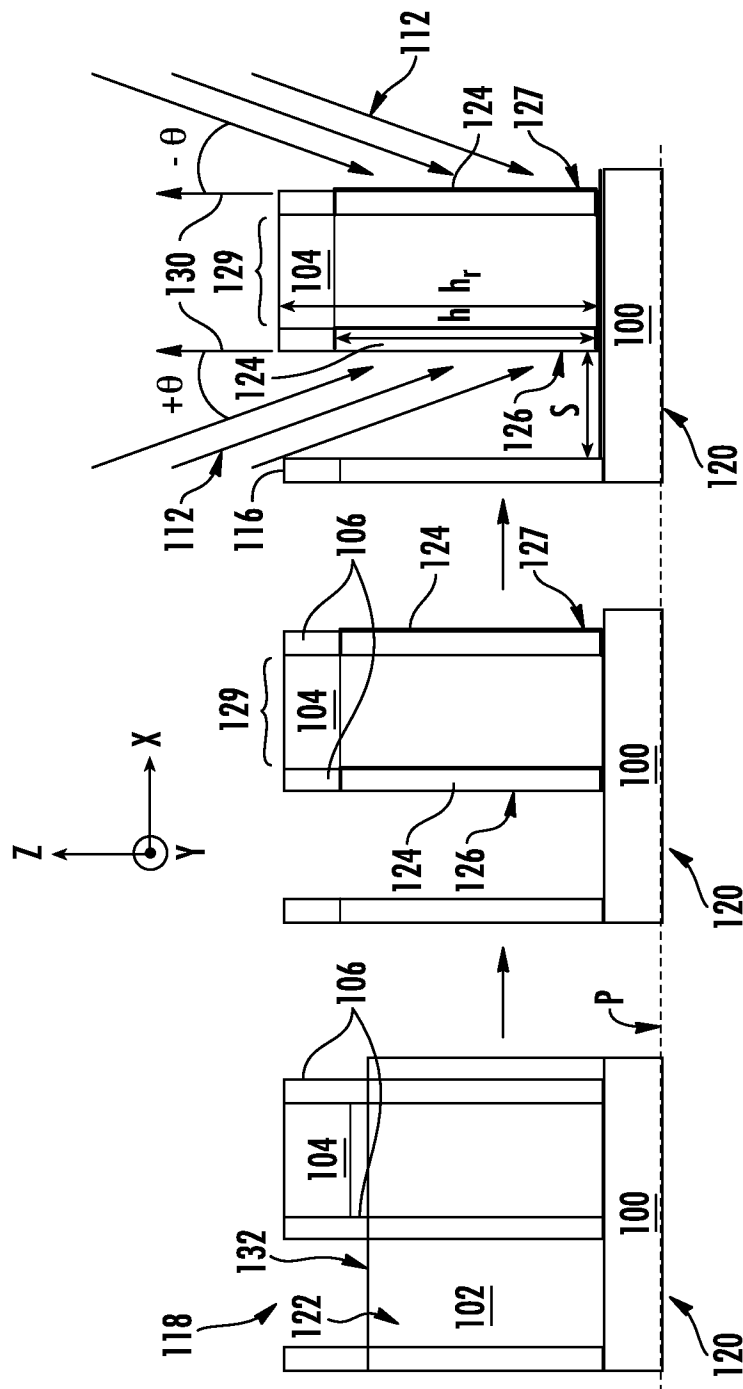
providing a gate structure covering a portion of the fin structures, wherein the gate structure defines an exposed region of a given fin structure; and

before the performing a source/drain extension implant, removing at least a portion of the exposed region,

wherein an extension region of the fin structures is formed having an end surface

not covered by the gate structure.

15. The method of claim 14, wherein the performing the source/drain extension implant comprises: directing dopant ions to the end surface, the dopant ions having trajectories extending in a plane perpendicular to the substrate plane and parallel to the fin axis, wherein the trajectories form a non-zero angle of incidence with respect to a perpendicular to the substrate plane, wherein the dopant ions form a source/drain extension within the fin structure.



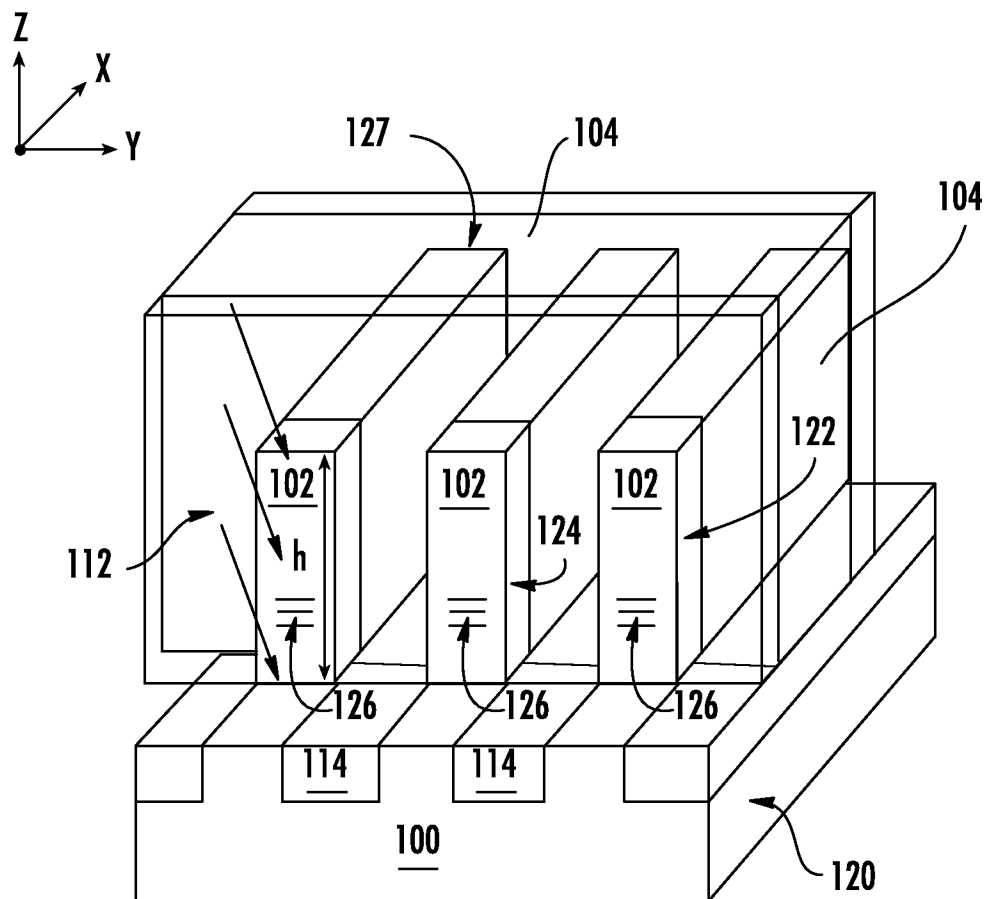


**FIG. 1D**

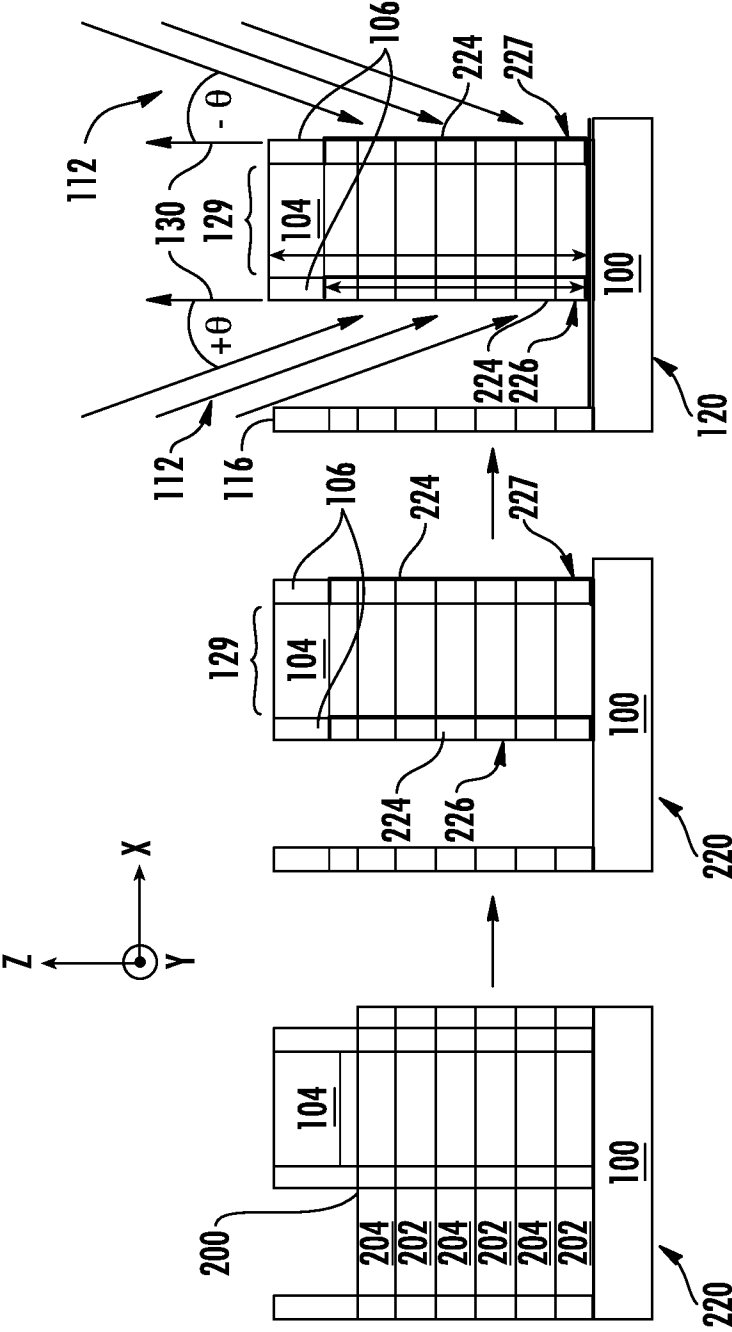


FIG. 2C

FIG. 2B

FIG. 2A

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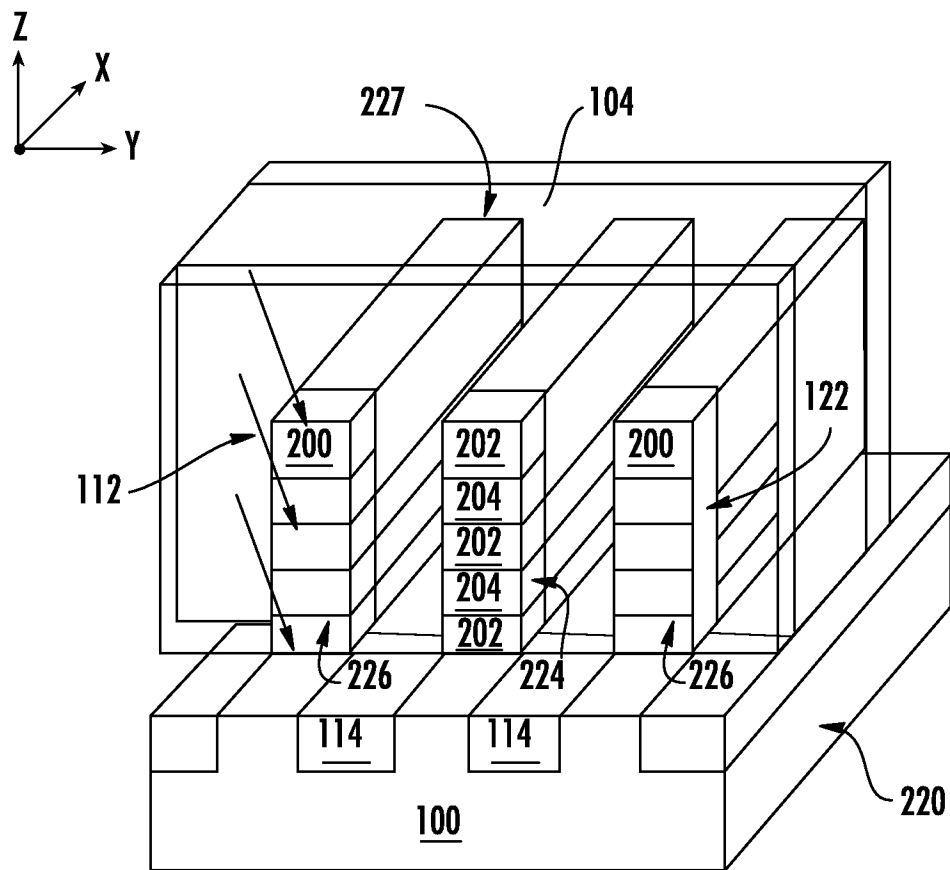
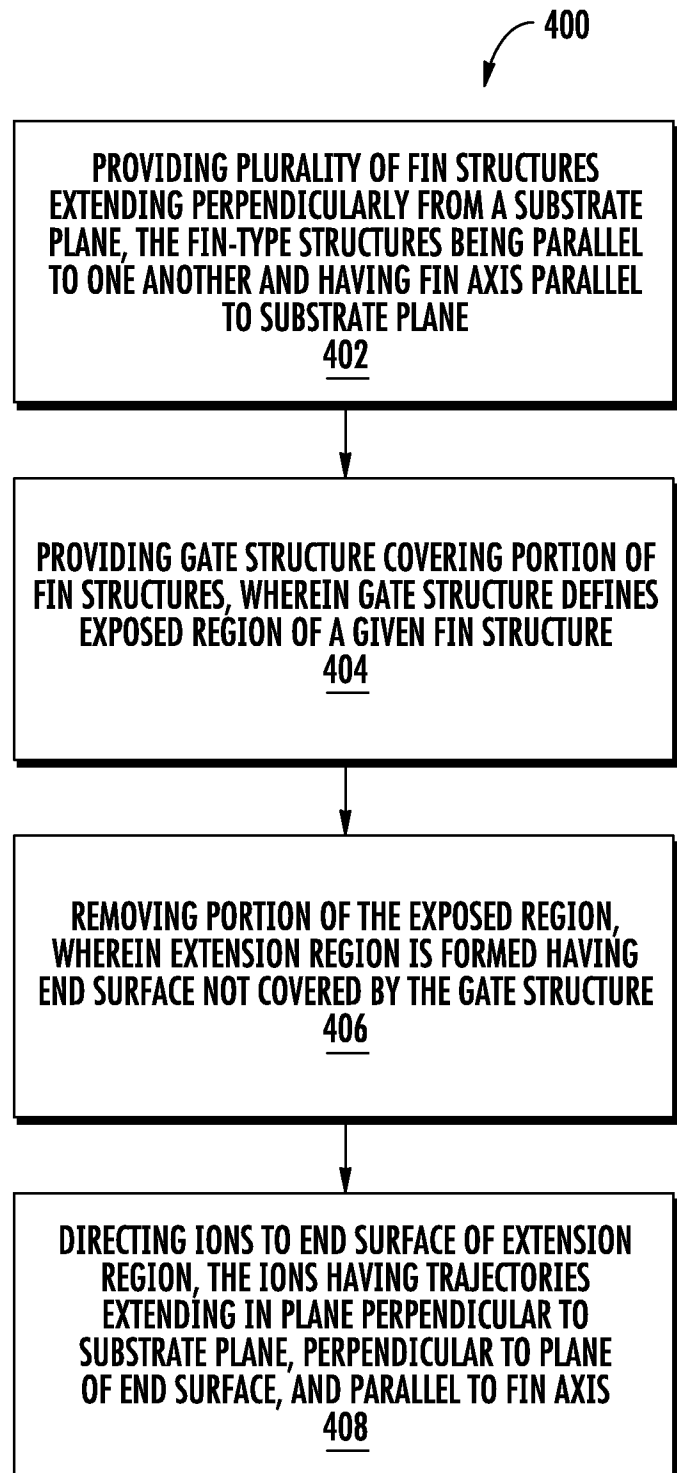


FIG. 2D

5/5

290 POLY DEPOSITION/CMP  
292 POLY LITHOGRAPHY  
294 POLY ETCH  
300 SDE SPACER DEPOSITION/ETCH  
304 EPI SPACER DEPOSITION/ETCH  
306 RECESS ETCH  
302 SDE IMPLANTATION/HALO IMPLANTATION  
308 RSD EPI DEPOSITION

350

**FIG. 3****FIG. 4**

**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/336(2006.01)i, H01L 29/78(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/336; H01L 29/00; H01L 21/8236; H01L 29/78; H01L 29/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: fin, gate, ion, angle

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                              | Relevant to claim No. |
|-----------|---------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| X         | US 2013-0187207 A1 (DANIEL TANG et al.) 25 July 2013<br>See abstract, paragraphs [0030]-[0068] and figures 3-18.                | 1-15                  |
| A         | US 2013-0146942 A1 (HUILONG ZHU et al.) 13 June 2013<br>See abstract, paragraphs [0015]-[0032] and figures 1-10.                | 1-15                  |
| A         | US 2008-0265321 A1 (CHEN-HUA YU et al.) 30 October 2008<br>See abstract, paragraphs [0016]-[0029] and figures 1a-1d.            | 1-15                  |
| A         | US 2015-0035061 A1 (SAMSUNG ELECTRONICS CO., LTD.) 05 February 2015<br>See abstract, paragraphs [0026]-[0063] and figures 1-16. | 1-15                  |
| A         | US 2009-0302402 A1 (BRENT A. ANDERSON et al.) 10 December 2009<br>See abstract, paragraphs [0048]-[0089] and figures 1A-8B.     | 1-15                  |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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