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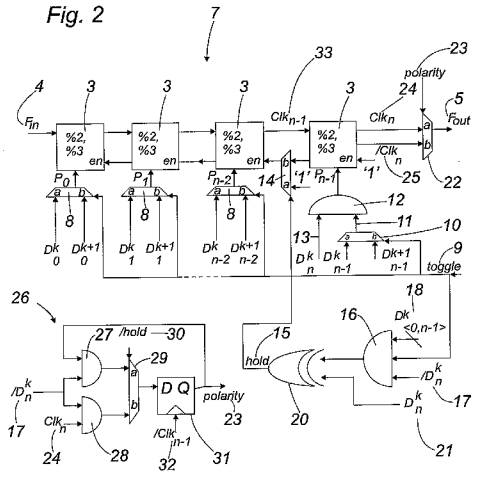
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(54) Title: FRACTIONAL FREQUENCY DIVIDER

Fig. 2



(57) Abstract: A fractional-n frequency divider that overcomes the presence of so-called dead zones in known frequency divider circuits, n divider cells (3) are connected so as to form a ripple counter (n being an integer greater than or equal to two) and an output multiplexer (22) is provided with a clock signal (24) and an inverted clock signal (25) by the nth divider cell. A polarity circuit (26) generates a polarity signal (23) which clocks the output multiplexer (22) so as to controllably combine the clock signal and the inverted clock signal to produce an output signal (5). A toggle signal (9) toggles between a first and a second integer division configuration so as to provide for fractional divisional outputs therebetween. With n 2/3 divider cells (3) the division ratio therefore can take any fractional value that satisfies the following inequality 2 (n-1) less than or equal to division ratio less than or equal to 2 (n+1) - 1.

WO 2009/133380 A3

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A. CLASSIFICATION OF SUBJECT MATTER
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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/063699 A1 (WELDON PAUL J [DK] ET AL) 3 April 2003 (2003-04-03) paragraphs [0017] - [0029]; figures 2,3	1-25
A	US 2007/147571 A1 (YU SHIH-AN [TW] ET AL) 28 June 2007 (2007-06-28) paragraphs [0073] - [0083]; figures 5-13	1-24

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Date of the actual completion of the international search	Date of mailing of the international search report
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CICERO S VAUCHER ET AL: "A Family of Low-Power Truly Modular Programmable Dividers in Standard 0.35-m CMOS Technology" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 35, no. 7, 1 July 2000 (2000-07-01), XP011061290 ISSN: 0018-9200 cited in the application paragraph [0III]; figures 2,3 -----	1,20
A	ROGERS, J. W. M. ET AL: "A Multiband Delta Sigma Fractional-N Frequency Synthesizer for a MIMO WLAN Transceiver RFIC" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 40, no. 3, 1 March 2005 (2005-03-01), pages 678-689, XP011128275 ISSN: 0018-9200 cited in the application paragraph [000V]; figures 4,5 -----	1,20

INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003063699 A1	03-04-2003	NONE	
US 2007147571 A1	28-06-2007	NONE	