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[Continued on next page]

(54) Title: A MULTI STRING CONTROLLER WITH INDEPENDENT CURRENT SETTING FOR EACH STRING

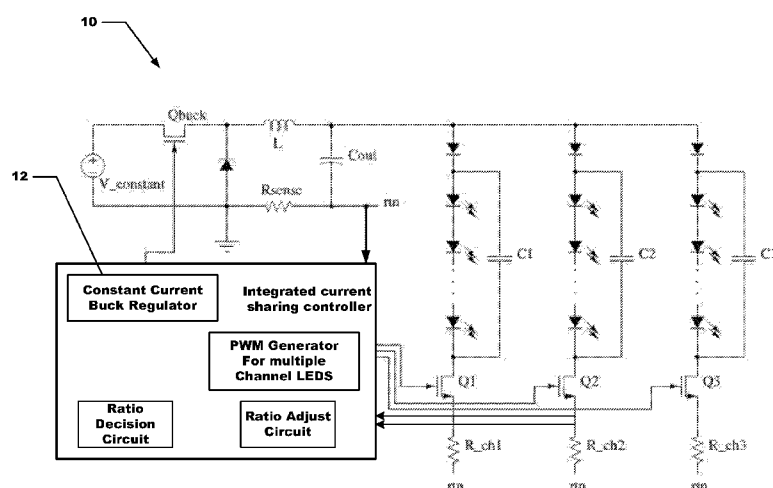


Figure 1

(57) Abstract: A multi string controller with independent current setting for each string is designed for solid state lighting applications. This controller can regulate multiple channels of LEDs. Each string may have a different forward voltage and current setting. A constant buck regulator is also integrated inside this controller to regulate the total current, which is fed into the LED output channels. The circuit also contains a feedback loop in order to precisely control the current passing through each string and is immune to transient conditions.

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## A MULTI STRING CONTROLLER WITH INDEPENDENT CURRENT SETTING FOR EACH STRING

### CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is an international application and claims priority to, and the benefit of, United States Provisional Patent Application No. 62/265,967, filed on December 10, 2015, and United States Provisional Patent Application No. 62/270,949, filed on December 22, 2015, the entire contents of both of which are hereby incorporated by reference.

### TECHNICAL FIELD

[0002] The present invention relates to electronics, and more specifically, to controller circuits and controllers.

### BACKGROUND

[0003] In the past two decades, solid-state lighting technology has grown rapidly. Due to its high efficacy, long lifetime, and good color quality, the light-emitting diode (LED) has been used in both indoor and outdoor lighting applications. As the power of LED fixtures increases, more and more diodes are put onto a single LED light engine. Moreover, in order to generate high CRI (color rendering index) and high efficacy (lm/W) white light, multi-spectral LEDs clusters, which include both phosphor-converted white LEDs and single-color diodes, are used. The main reason for using multi-spectral LED clusters is that phosphor-converted white LEDs with high correlated color temperature (CCT, ~5000K) show good efficacy compared to those with a lower CCT (~2700K), but the color rendering index of the higher CCT LED is worse than that of the lower CCT LED. The high CCT phosphor-converted white LED lacks high wavelength energy in its spectrum; therefore, in order to compensate for this weakness while still maintaining high efficacy, a red LED can be added into the light engine to improve color rendering. There are several challenges to driving LED light engines containing diodes of different color. First, the forward

voltages of the LEDs having different colors are not the same. GaN material is used to make phosphor-converted white LEDs, while red or orange LEDs are usually made from AlGaInP. The material bandgap for these two types of semiconductor are different. It is very difficult to maintain forward voltage balancing while driving these LEDs in different chains without regulation. Second, for a color-mixing LED light engine, not all LEDs will be driven at the same current. In order to achieve a certain color temperature as well as maintain high efficacy, the current pass through the phosphor-converted white LED will need to be larger than the current pass through other single-color diodes.

[0004] A multi-channel LED driver is required to solve these challenges. Much work has been done in the past on multi-channel drivers, both in academia and industry. Among these designs, in order to drive multiple channel outputs the power converter either requires all the output channels to share the same regulation, which means every output channel has an identical output current; or each output channel requires a subpower conversion system to regulate the output current separately, in which, for example, three output channels require three sets of power inductors, power diodes, and capacitors. For a color-mixing light engine design, it is required to have separate current regulation for each LED chain, but considering the cost efficiency it is much better for the design to eliminate as many power-conversion components as possible while still maintaining the independent current regulation among each output channel. In this study, a current-sharing topology was used. Table 2 compares the existing design methodologies with the topology presented in this study.

## SUMMARY

[0005] Conventional mechanisms, such as those explained above, suffer from a variety of deficiencies. The current-sharing topology of the presently described multiple channel current sharing circuit is similar to some of the existing multichannel solutions, namely that the current passing through the LED strings is from one common constant current source. However, among those designs, the

control MOSFET/Transistor is operated in the linear region, which will lead to lower efficiency compared to a switch mode power supply.

[0006] A multiple channel current sharing controller is designed for LED lighting application. This controller can regulate three channels of LEDs. Each LED string may have a different forward voltage and current setting. A constant buck regulator is also integrated inside this controller to regulate the total current, which is fed into three LED output channels. The circuit also contains a feedback loop in order to precisely control the current passing through each LED string and is immune to transient conditions. The start-up procedure is designed to ensure both acceptable overshooting of output current and that the turn on time is as short as possible. In the final simulation, the maximum output current overshooting and ripple under transient condition do not exceed 20% of the nominal value. The output current buildup time is less than 25ms for all three channels.

[0007] In an embodiment, there is provided a [insert prose-ification of the claims here].

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The foregoing and other objects, features and advantages disclosed herein will be apparent from the following description of particular embodiments disclosed herein, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles disclosed herein.

[0009] FIG. 1 shows a [what FIG. 1 shows] according to embodiments disclosed herein.

[0010] Figure 1 depicts a schematic diagram of a multiple channel current sharing circuit in accordance with embodiments of the present invention.

[0011] Figures 2A – 2C depict schematics showing operation mode for each channel in accordance with embodiments of the present invention.

[0012] Figure 3 depicts a schematic diagram of a PWM generator cell in accordance with embodiments of the present invention.

[0013] Figure 4 depicts a schematic of a three PWM generation circuit in accordance with embodiments of the present invention.

[0014] Figure 5 depicts a schematic of a charging network in accordance with embodiments of the present invention.

[0015] Figure 6 depicts a schematic of a circuit that senses the LED current and also generates the charging/discharging current in accordance with embodiments of the present invention.

[0016] Figure 7 depicts a schematic of the feedback circuit in accordance with embodiments of the present invention.

[0017] Figure 8 depicts a schematic diagram of the integrated buck regulator in accordance with embodiments of the present invention.

[0018] Figure 9 depicts graphs showing the channel LED currents in accordance with embodiments of the present invention.

[0019] Figures 10A and 10B depict graphs showing the voltage across channel charging capacitors and PWM signals for channel LEDs in accordance with embodiments of the present invention.

[0020] Figure 11 depict a graph showing the channel LED currents in accordance with embodiments of the present invention.

[0021] Figure 12 depicts a schematic of a second embodiment of a multiple channel current sharing circuit in accordance with embodiments of the present invention.

[0022] Figure 13 depicts a schematic of a buck circuit in accordance with embodiments of the present invention.

[0023] Figure 14 depicts a schematic of a buck hysteresis comparator in accordance with embodiments of the present invention.

[0024] Figure 15 depicts a schematic of three buck hysteresis comparators connected in parallel in accordance with embodiments of the present invention.

[0025] Figure 16 depicts a graph showing the current passing through the buck inductor in accordance with embodiments of the present invention.

[0026] Figure 17 depicts a graph showing the current passing through each LED string in accordance with embodiments of the present invention.

## DETAILED DESCRIPTION

[0027] Referring to Figure 1, a schematic of a circuit 10 incorporating a current sharing controller 12 is shown. The control MOSFETs (Q1, Q2 and Q3) of each LED string, act as switches. Compared to a linear regulator, the loss is much smaller. From Figure 1 it can be seen that three channels of LEDs share the same constant current from an integrated buck regulator 14. While three channels of LEDs are shown, it should be appreciated that any number of channels of LEDs could be used. The present description uses three channels as an example only, and is not intended to be limited to three channels. Each channel of LED is controlled separately; each channel can have different forward voltages as well as different current. The operation mode of each channel of LEDs is presented in Figure 2. When the switching is on, the main current will pass through the LED and charge the capacitor in parallel connection with the load. The other two channels of LEDs are powered by the discharging current of the capacitors next to them. Unlike most commercial designs, the constant buck regulator 14 is also integrated inside the circuit. This integration improves the overall start-up performance and also reduces the cost compared to multi-chip solutions. Moreover, as presented in Figure 2, although there are three output LED strings, the whole system requires only one set of power inductor L, Cout, and freewheeling diode D1. Compared to traditional multi-channel designs, the current-sharing topology is cost efficient. The overall efficiency will increase with the load current. Generally speaking, for a constant buck regulator the best efficiency will occur at maximum allowable load voltage with maximum load current. This rule applies to this design as well. The current ratio between each channel and the forward voltage of each LED string will also affect the overall efficiency value.

[0028] The design of output capacitor C1, C2, and C3 should consider switching frequency, hold up time, and power consumption of the LED load connected in parallel with it. As described before, when one of the three channels is connected to the main constant current buck output, the other two strings will be powered by these capacitors only, and moreover, the LED is also very sensitive to forward voltage. If the capacitance is too small in reference to the load size and switching

frequency, the voltage will drop greatly and cause large output current ripple. Equations 1 and 2 explain the relationship. Although independent leds strings have a ripple current limit this will not be a requirement if all led strings are in the same fixture and are switching above 2K Hz. In this case C1,2,3 can be eliminated.

$$W_{hold\_up} = \frac{1}{2} (V_{forward\_nominal}^2 - V_{drop\_target}^2) \cdot C_{1,2,or3} \quad (1)$$

$$C_{1,2,or3} = \frac{2 \cdot P_{1,2,or3} \cdot D'}{f_{sw} \cdot (V_{forward\_nominal}^2 - V_{drop\_target}^2)} \quad (2)$$

[0029] Where:

[0030] Whold\_up: energy required to hold up the LED forward voltage and also provide load current; Vforward\_nominal: LED nominal forward voltage;

Vdrop\_target: target voltage of load forward voltage drop under worst condition;

P1, 2, or 3: channel 1, 2, or 3 nominal output power; D': off duty cycle of channel 1, 2, or 3.

[0031] In order to make three channels of LEDs with different forward voltages to have independent current control, the on-time for Q1, Q2, and Q3 should not have any overlap. As a result, the current ratio between each channel depends on the on-time of each MOSFET; moreover, considering the situation in which one channel has the largest number of LEDs (maximum forward voltage), the power MOSFET for this LED channel can be eliminated. For example, if the third LED channel has the largest forward voltage, Q3 can be eliminated. When Q1 is on while Q2 is off, since the forward voltage of the LEDs of the first channel is less than that of the third channel, all the current from the buck regulator will pass through channel one.

[0032] Figures 2A-2C show the operation mode of each LED string. When a channel is on (channel 1 in Figure 2A, channel 2 in Figure 2B and channel 3 in Figure 2C), the buck drives the LEDs and charges the capacitor. For the channels that are not on the LEDs are not driven. The switches are controlled to turn a channel on or off, and are controlled in a manner wherein there is no overlap in on time between the channels.

[0033] The single PWM generator cell 30 is presented in Figure 3. When the charging switch S1 is turned on, the current Charge\_I will charge the capacitor C\_charge until its voltage reaches V\_H. Comparator 32 will then trigger the reset input on the flip flop 36, the QB port of SR flip flop 36 will be set to high and the Discharge\_I will discharge the capacitor until V\_L is achieved which will cause comparator 34 to trigger the set input of flip flop 36 and then start another cycle. The duty cycle of this PWM generator cell depends on the charging current, discharging current, and the value of the capacitor. In order to generate a three-channel PWM signal without any overlap, three PWM generator cells should be used. Each PWM signal has a different duty cycle, which means the charge current should be varied by the channel as well. The charging network and three PWM generation circuit are presented in Figure 4 and Figure 5.

[0034] As shown in Figure 4, when the system 40 is powered up, signal phi 1 will be set to high after the circuit initialization ready is true; then current source Ch1\_dutycap\_charge will charge the Ch1\_dutycap while signals phi 2 and phi 3 remain low. When voltage across Ch1\_dutycap reaches V\_H, Ch1\_high will become true and phi 2 signal will be pulled up high when phi 1 signal changes to low.

[0035] Because phi 1, phi 2, and phi 3 will be set to high in a continuous sequence without overlap, the duty cycle ratio of these signals totally depends on the charging current when all three charge capacitors have the same value. The circuit 50 in Figure 5 will generate three different charging currents with certain ratio. It can be seen from Figure 5 that U1, Q1-Q3, and R\_total\_ind will generate the reference current to present unit 1 or 100%. U2, Q4-Q8, and R\_ch1\_ind will generate current to the charge capacitor of channel 1, which will be used for the phi 1 signal. The value of this charging current should be less than the reference current. U3, Q9-Q13, and R\_ch2\_ind will generate channel 2's capacitor charging current. The summary of I\_charge\_ch1 and I\_charge\_ch2 should be less than the reference current as well. Q17-Q27 comprise the current deduction circuit to generate the charging current for the capacitor of channel 3. Q14-Q17 is a current mirror that copies the reference current. Q18-Q19 and Q22-Q23 copy the charge current of both channel 1 and

channel 2. The duty cycle of each of these three PWM signals is presented in Equation 3 to Equation 8.

$$V_{Ch1duty\text{cap}} = \frac{I_{Ch1duty\text{capcharge}}}{C_{Ch1duty\text{cap}}} \cdot t_{\text{phi1on}} \quad (3)$$

$$t_{\text{phi1on}} = \frac{V_{Ch1duty\text{cap}} \cdot C_{Ch1duty\text{cap}}}{I_{Ch1duty\text{capcharge}}} \quad (4)$$

$$D_{\text{phi1}} = \frac{t_{\text{phi1on}}}{t_{\text{phi1on}} + t_{\text{phi2on}} + t_{\text{phi3on}}} \quad (5)$$

$$C_{Ch1duty\text{cap}} = C_{Ch2duty\text{cap}} = C_{Ch3duty\text{cap}} = C \quad (6)$$

$$D_{\text{phi1}} = \frac{\frac{1}{I_{Ch1duty\text{capcharge}}}}{\frac{1}{I_{Ch1duty\text{capcharge}}} + \frac{1}{I_{Ch2duty\text{capcharge}}} + \frac{1}{I_{Ch3duty\text{capcharge}}}} \quad (7)$$

$$I_{LED-channel1} = D_{\text{phi1}} \cdot I_{total} \quad (8)$$

[0036] Equation 8 shows that the ratio between the current passing through each LED channel depends on the duty cycle of these three PWM generators. The duty cycle of phi 1, phi 2, or phi 3 is decided by the charging current. Figure 5, which presents the method of generating these charging currents, shows the port-to-connect feedback system. When the system is powered up, the charging current is set by the on-chip reference voltage  $V_{ref}$  and the off-chip resistors ( $R_{ch1\_ind}$  and  $R_{ch2\_ind}$ ). The arbitrary setup will provide a fast turn-on of each LED channel with the desired current ratio. However, because MOSFET mismatch exists in the current mirror circuit, the charging capacitors are not exactly identical in the three PWM generator systems, nor is the tolerance of the off-chip resistors identical. This preset charging current ratio may lead the current pass through each LED channel to deviate from the target value. In this case, a feedback circuit is required to correct

these errors. Moreover, a feedback circuit will also improve the transient response of the current passing through each output channel. The feedback circuit 50 is presented in Figure 5.

[0037] From Figure 5, it can be seen that the feedback signal generator contains two parts. Figure 6 shows the circuit 60 that senses the LED current and also generates the charging/discharging current for the circuit in Figure 7. The low pass RC filter and type I compensation amplifier circuit are presented in Figure 6 as well. In this design, all the low pass filters are RC circuit. Although a resistor will be greatly affected by PVT (process, voltage, and temperature), around 30% tolerance will be good enough for the purpose used in this design. As presented in both Figure 5 and equation 7, the larger the charging current for the Channel<sub>x</sub>\_dutycap, the smaller the duty cycle will be, leading to a smaller current passing through this channel. In Figure 6 and Figure 7, the LED current of a certain channel is sensed by the Channel<sub>x</sub> current sensing resistor (R<sub>x</sub>), and through one low-pass filter and compensation network, the voltage is used to create current called IFB\_V\_charge<sub>x</sub>. The larger the current sensing signal is compared to the reference voltage, the bigger the IFB\_V\_charge<sub>x</sub> will be. The IFB\_V\_discharge<sub>x</sub> is generated through a current deduction circuit. When the LED current is less than the target value, the IFB\_V\_charge<sub>x</sub> will increase and the IFB\_V\_discharge<sub>x</sub> will decrease. This will reduce the charging time of Feedback\_C (C<sub>fb</sub>). Under this condition, the on-time of the Q port will become smaller, which will cause the Feedback\_signal to reduce. With a smaller Feedback\_signal value, the IChannel<sub>x</sub>\_dutycap\_charge will decrease, causing the duty cycle of this channel to increase and finally boost up the LED current. Equations 9 through 17 present the feedback signal calculation.

$$V_{sns\_x} = I_x \cdot R_x \cdot \frac{1}{1 + \frac{s}{\omega_0}} \cdot \frac{\omega_1}{s} \cdot A_p \quad (9)$$

$$\frac{V_{sns\_x}}{R_{fb}} = I_{FB\_V\_charge\_x} \quad (10)$$

$$\frac{V_{set}}{R_{set}} = I_{FB\_V\_charge\_x} + I_{FB\_V\_discharge\_x} \quad (11)$$

$$I_{FB\_V\_discharge} = \frac{V_{set}}{R_{set}} - \frac{V_{sns\_x}}{R_{fb}} \quad (12)$$

$$t_{on\_fb} = \frac{V_H \cdot C_{fb}}{I_{FB\_V\_charge\_x}} \quad (13)$$

$$t_{off\_fb} = \frac{V_H \cdot C_{fb}}{I_{FB\_V\_discharge\_x}} \quad (14)$$

$$T_{fb} = t_{on\_fb} + t_{off\_fb} \quad (15)$$

$$V_{FB\_signal\_x} = \frac{t_{on\_fb}}{T_{fb}} \cdot V_{ref\_bus} \quad (16)$$

$$I_{Ch\_x\_dutycharge} = \frac{V_{FB\_signal\_x}}{R_{ch\_x\_ind}} \quad (17)$$

[0038] Where:

[0039]  $I_x$ : LED forward current passing through channel x;  $R_x$ : channel x current sensing resistance;  $V_{sns\_x}$ : voltage sent to the compensation network;  $V_{set}$ ,  $R_{set}$ : voltage and resistor used to set reference main current;  $R_{fb}$ : based on  $V_{sns\_x}$  define the current charging feedback capacitor  $C_{fb}$ ;  $I_{FB\_V\_Charge\_x}$ : current charging feedback capacitor  $C_{fb}$ ;  $I_{FB\_V\_discharge\_x}$ : current discharging feedback capacitor  $C_{fb}$ ;  $t_{on\_fb}$ : on-time of feedback capacitor;  $t_{off\_fb}$ : off-time of feedback capacitor

[0040] For a three-channel current-sharing circuit design, only two channels require a feedback system. The last channel will take over whatever current remains from the total output of the constant current buck regulator.

[0041] In order to improve the system's start-up performance, the buck regulator is designed as part of this control IC. The system schematic 80 for this integrated buck regulator is shown in Figure 8.

[0042] As presented in Figure 8, the voltage on the current sensing resistor will first pass through a low-pass filter and then be amplified before reaching the compensation network. For the reference voltage, when the unit starts up, a small value will be used in order to improve the start-up performance, then a final value will be used for the steady-state operation.

[0043] A simulation was conducted for this circuit. In the simulation, both channel 1 and channel 2 have 21V forward voltage, and channel 3 has 32V forward voltage. As channel 3 has the largest forward voltage, the MOSFET of channel 3 can be eliminated. The current ratio of each channel is set to 4:2:3, and the total current from the buck regulator is set to 1200mA. The off-chip power train components are listed in Table 3 and the results are presented in Figure 9.

[0044] Figure 9 shows the Channel 1 LED current 90; the Channel 2 LED current 92 and the Channel 3 LED current 94. From Figure 9, it can be seen that the LED current started to build up at 9ms. There was current passing through both channel 1's and channel 2's LEDs at the same time. The LEDs on channel 3 started at almost 15ms. The difference in the turn-on time was due to the LED forward voltage. Because the LED chain of channel 3 had the largest forward voltage, it required a longer time for the current to charge up the voltage of C3 (shown in Figure 1) to achieve the threshold voltage. Figure 9 also shows output current disturbance when the feedback regulation kicked in; due to the integrated buck regulator applying a smaller reference voltage during start-up, the overshooting of the output current caused by the feedback system was lower than the nominal output current.

[0045] Figures 10A – 10B presents the PWM signal of all three output channels and the voltage across each Chx\_dutycap. From Figure 10A and Figure 10B, it can be seen that the three PWM signals 102, 106 and 110 do not have any overlap.

[0046] In Figure 10A and 10B, waveform 100 represents the voltage across channel 1 charging capacitor and signal 102 the PWM signal for channel 1 LED; waveform 104 represents the voltage across channel 2 charging capacitor and signal 206 the PWM signal for channel 2 LED; and waveform 108 represents the voltage across channel 3 charging capacitor and signal 110 the PWM signal for channel 3 LED.

[0047] The perturbation condition was also simulated to test the feedback circuit. One of the channels with feedback regulation was set to have 500mA current, then a step change in the input current with the step level being 125% nominal target value. The result is presented in Figure 11. As presented in the result 115, the maximum current perturbation reaches 595mA, which is 19% over the nominal output current; the minimum current dip is 420mA, which is 16% below the target value.

[0048] The current-sharing topology can be very useful for a multi-channel LED lighting application. Different channels can drive different numbers of LEDs with different current. Moreover, compared to a traditional multi-channel LED driver, a current-sharing topology can greatly reduce the number of power components needed, such as power inductors, freewheeling diodes, and even MOSFET if powering LEDs with unbalanced forward voltage.

[0049] In this embodiment, a controller regulating a three-channel current-sharing topology-based LED driver was described. This design shows quick start-up performance; moreover, due to the buck regulator being integrated inside the controller, the output current start-up overshooting is below the nominal value. The feedback circuit can control the output current well, and the maximum and minimum values of perturbation are less than 30% of the target value.

[0050] In this embodiment, if a duty cycle of one channel is changed, the duty cycles of the other channels would also change in order to maintain a unity total duty cycle. The current is fixed and the duty cycle is adjustable.

[0051] In a second embodiment a multi-channel current sharing circuit incorporates a buck operating at a multilevel output current. Each channel operates at a fixed frequency and a fixed and equal duty cycle. Each channel has a same switching frequency and a same duty cycle. For example, if the number of channels were three, the three corresponding PWM signals would have 120 degrees difference with no overlap. When a particular channel is on, the buck is controlled to be three times the channel nominal current.

[0052] As opposed to the shared duty cycle of the first embodiment, this embodiment the duty cycles are fixed. There is no feedback in this embodiment. The PWM is fixed and the current is variable. Referring to Figure 12, a schematic 120

is shown which includes a multiple channel current sharing circuit 122. The circuit 122 includes a Buck circuit having a current level set for multiple channels that are synchronized to a selected channel. Also shown is a non-overlapping three phase PWM having a fixed frequency and a fixed duty cycle. A buck hysteresis comparator is also shown.

[0053] Figure 13 shows a schematic 130 of the buck circuit. Figure 14 shows a schematic 140 of the buck hysteresis comparator which uses the inductor current sensing voltage from the buck circuit to define a PWM output using hysteresis as the control mechanism. This serves to limit the peak current level and limit the minimum current level. Also, feedback is not required for the hysteresis control mechanism.

[0054] Figure 15 shows the buck current control methodology. In this example three buck hysteresis comparators are connected in parallel to produce the waveform shown in Figure 16. The waveform 160 is the current passing through the buck inductor. There are three level differences. One for each channel and having the same duration. Further, with no feedback required, regulation is fast. Figure 17 shows the current passing through each LED string. It should be noted that only high current ripple exists.

[0055] The methods and systems described herein are not limited to a particular hardware or software configuration, and may find applicability in many computing or processing environments. The methods and systems may be implemented in hardware or software, or a combination of hardware and software. The methods and systems may be implemented in one or more computer programs, where a computer program may be understood to include one or more processor executable instructions. The computer program(s) may execute on one or more programmable processors, and may be stored on one or more storage medium readable by the processor (including volatile and non-volatile memory and/or storage elements), one or more input devices, and/or one or more output devices. The processor thus may access one or more input devices to obtain input data, and may access one or more output devices to communicate output data. The input and/or output devices may include one or more of the following: Random Access Memory (RAM),

Redundant Array of Independent Disks (RAID), floppy drive, CD, DVD, magnetic disk, internal hard drive, external hard drive, memory stick, or other storage device capable of being accessed by a processor as provided herein, where such aforementioned examples are not exhaustive, and are for illustration and not limitation.

[0056] The computer program(s) may be implemented using one or more high level procedural or object-oriented programming languages to communicate with a computer system; however, the program(s) may be implemented in assembly or machine language, if desired. The language may be compiled or interpreted.

[0057] As provided herein, the processor(s) may thus be embedded in one or more devices that may be operated independently or together in a networked environment, where the network may include, for example, a Local Area Network (LAN), wide area network (WAN), and/or may include an intranet and/or the internet and/or another network. The network(s) may be wired or wireless or a combination thereof and may use one or more communications protocols to facilitate communications between the different processors. The processors may be configured for distributed processing and may utilize, in some embodiments, a client-server model as needed. Accordingly, the methods and systems may utilize multiple processors and/or processor devices, and the processor instructions may be divided amongst such single- or multiple-processor/devices.

[0058] The device(s) or computer systems that integrate with the processor(s) may include, for example, a personal computer(s), workstation(s) (e.g., Sun, HP), personal digital assistant(s) (PDA(s)), handheld device(s) such as cellular telephone(s) or smart cellphone(s), laptop(s), handheld computer(s), or another device(s) capable of being integrated with a processor(s) that may operate as provided herein.

Accordingly, the devices provided herein are not exhaustive and are provided for illustration and not limitation.

[0059] References to "a microprocessor" and "a processor", or "the microprocessor" and "the processor," may be understood to include one or more microprocessors that may communicate in a stand-alone and/or a distributed environment(s), and may thus be configured to communicate via wired or wireless communications with

other processors, where such one or more processor may be configured to operate on one or more processor-controlled devices that may be similar or different devices.

Use of such "microprocessor" or "processor" terminology may thus also be understood to include a central processing unit, an arithmetic logic unit, an application-specific integrated circuit (IC), and/or a task engine, with such examples provided for illustration and not limitation.

[0060] Furthermore, references to memory, unless otherwise specified, may include one or more processor-readable and accessible memory elements and/or components that may be internal to the processor-controlled device, external to the processor-controlled device, and/or may be accessed via a wired or wireless network using a variety of communications protocols, and unless otherwise specified, may be arranged to include a combination of external and internal memory devices, where such memory may be contiguous and/or partitioned based on the application. Accordingly, references to a database may be understood to include one or more memory associations, where such references may include commercially available database products (e.g., SQL, Informix, Oracle) and also proprietary databases, and may also include other structures for associating memory such as links, queues, graphs, trees, with such structures provided for illustration and not limitation.

[0061] References to a network, unless provided otherwise, may include one or more intranets and/or the internet. References herein to microprocessor instructions or microprocessor-executable instructions, in accordance with the above, may be understood to include programmable hardware.

[0062] Unless otherwise stated, use of the word "substantially" may be construed to include a precise relationship, condition, arrangement, orientation, and/or other characteristic, and deviations thereof as understood by one of ordinary skill in the art, to the extent that such deviations do not materially affect the disclosed methods and systems.

[0063] Throughout the entirety of the present disclosure, use of the articles "a" and/or "an" and/or "the" to modify a noun may be understood to be used for convenience and to include one, or more than one, of the modified noun, unless

otherwise specifically stated. The terms "comprising", "including" and "having" are intended to be inclusive and mean that there may be additional elements other than the listed elements.

**[0064]** Elements, components, modules, and/or parts thereof that are described and/or otherwise portrayed through the figures to communicate with, be associated with, and/or be based on, something else, may be understood to so communicate, be associated with, and or be based on in a direct and/or indirect manner, unless otherwise stipulated herein.

**[0065]** Although the methods and systems have been described relative to a specific embodiment thereof, they are not so limited. Obviously many modifications and variations may become apparent in light of the above teachings. Many additional changes in the details, materials, and arrangement of parts, herein described and illustrated, may be made by those skilled in the art.

What is claimed is:

1. A multi LED string controller with independent current setting for each string comprising:

- at least one of a constant current buck or linear generator, having an output;
- a pulse width modulation (PWM) generator providing a plurality of PWM outputs;

- a ratio decision circuit in communication with the PWM generator;

- a ratio adjust circuit in communication with the PWM generator and having a plurality of inputs; and

wherein the current sharing controller circuit provides a fixed total current with a non-overlapping variable duty cycle at the plurality of PWM outputs, the plurality of PWM outputs driving a plurality of channels, each channel including a plurality of LEDs and the ratio adjust circuit plurality of inputs provide feedback from the plurality of channels.

2. The multi LED string controller circuit of claim 1, wherein the constant current buck generator comprises:

- a low pass filter (LPF) having an input and an output;

- an amplifier circuit having an input coupled to the output of the LPF and having an output;

- a compensation circuit having a first input coupled to the output of the amplifier circuit, having a second input, and having an output;

- a first switch having a first lead coupled to the second input of the compensation circuit, a second lead coupled to an initial reference voltage source, and a control for selectively coupling the voltage from the initial reference voltage source to the first lead;

- a second switch having a first lead coupled to the second input of the compensation circuit, a second lead coupled to a steady state reference voltage source, and a control for selectively coupling the voltage from the steady state reference voltage source to the first lead;

a comparator having a first input coupled to the output of the compensation circuit, a second input coupled to a reference waveform generator, and an output; and

an offchip gate driver having an input coupled to the output of the comparator and having an output.

3. The multi LED string controller circuit of claim 2, wherein the amplifier circuit comprises:

a first operational amplifier (op-amp) having a first input coupled to the amplifier circuit input, a second input, and an output coupled to the amplifier circuit output;

a first resistor having a first lead coupled to the first op-amp output and a second lead coupled to the first op-amp second input; and

a second resistor having a first lead coupled to the first op-amp second input and having a second lead coupled to a ground.

4. The multi LED string controller circuit of claim 2, wherein the compensation circuit comprises:

a third resistor having a first lead coupled to the compensation circuit first input, and a second lead;

a second op-amp having a first input coupled to the first lead of the third resistor a second lead coupled to the second input of the compensation circuit and an output coupled to the compensation circuit output; and

a compensation element having a first lead coupled to the first input of the second op-amp and a second lead coupled to the output of the second op-amp.

5. The multi LED string controller circuit of claim 1, wherein the PWM generator comprises a plurality of PWM cells, each PWM cell comprising:

a first switch having a first lead coupled to a charging circuit, a second lead, and a control;

a second switch having a first lead coupled to the second lead of the first switch, a second lead coupled to a discharging circuit, and a control;

a charging capacitor having a first lead coupled to the first lead of the second switch and a second lead coupled to ground;

a first comparator having a first input coupled to the first lead of the charging capacitor, having a second lead coupled to a first reference voltage, and having an output;

a second comparator having a first input coupled to the first lead of the charging capacitor, having a second lead coupled to a second reference voltage, and having an output; and

a flip flop having a set input coupled to the output of the second comparator, having a reset input coupled to the output of the first comparator, having a first output coupled to the control of the first switch, and having a second output coupled to the control of the second switch.

6. The multi LED string controller of claim 1, wherein the constant current buck regulator is capable of driving a buck circuit and of controlling a plurality of channels of LEDs.

7. The current sharing controller of claim 6, wherein the buck controller comprises:

a voltage source having a first lead and having a second lead coupled to a ground;

a buck circuit switch having a source coupled to a first lead of the voltage source, a gate coupled to the output of the constant current buck regulator, and a drain;

a diode having an anode connected to ground and a cathode coupled to the drain of the buck circuit switch;

an inductor having a first lead coupled to the cathode of the diode and a second lead comprising a buck circuit output;

an output capacitor having a first lead connected to the second lead of the inductor and a second lead connected to a return output; and

a sense resistor having a first lead connected to ground and a second lead connected to the second lead of the output capacitor.

8. The multi LED string controller of claim 6, wherein each channel of the plurality of channels of LEDs comprises:

a plurality of LEDs connected serially;

a channel capacitor having a first lead coupled to a cathode of a first one of the plurality of LEDs connected serially and a second lead coupled to a cathode of a last one of the plurality of LEDs connected serially;

a channel switch having a source connected to the second lead of the channel capacitor; a gate couple to one of the PWM generator outputs, and a drain; and

a channel resistor having a first lead coupled to the drain of the channel switch and a second lead coupled to a second lead of the output capacitor.

9. The multi LED string controller of claim 1, wherein the PWM is analog derived.

10. The multi LED string controller of claim 1, wherein the PWM is digitally derived.

11. A multi LED string controller circuit comprising:

a buck current level circuit having a plurality of outputs and a plurality of inputs;

a pulse width modulation (PWM) generator providing a plurality of PWM outputs and in communication with the buck current level circuit; and

a buck hysteresis comparator having an output and in communication with the buck current level circuit;

wherein the current sharing controller circuit provides a fixed frequency and fixed duty cycle signal with a non-overlapping duty cycle at the plurality of PWM outputs, the plurality of PWM outputs driving a plurality of channels, each channel including a plurality of LEDs.

12. The multi LED string controller of claim 11, wherein the buck hysteresis comparator comprises:

a first hysteresis comparator having a first input coupled to an inductor current sensing voltage, a second input coupled to a first voltage reference, a first positive threshold value input, a first negative threshold value input and an output;

a second hysteresis comparator having a first input coupled to a second voltage reference, a second input coupled to the first hysteresis comparator first input, a first positive threshold value input, a first negative threshold value input and an output; and

a flip flop having a set input coupled to the output of the second hysteresis comparator, having a reset input coupled to the output of the first hysteresis comparator, and having a first output.

13. The multi LED string controller circuit of claim 12, wherein the circuit includes a plurality of buck hysteresis controller wherein a first buck hysteresis controller of the plurality of buck hysteresis controllers is coupled in parallel with at least one other buck hysteresis controller.

14. The multi LED string controller of 11, wherein the constant current buck regulator is capable of driving a buck circuit and of controlling a plurality of channels of LEDs.

15. The multi LED string controller of claim 14, wherein the buck controller comprises:

a buck circuit switch having a source coupled to a voltage source, a gate coupled to the output of the current sharing controller, and a drain;

a diode having an anode connected to ground and a cathode couples to the drain of the buck circuit switch;

an inductor having a first lead coupled to the cathode of the diode and a second lead comprising a buck circuit output;

an output capacitor having a first lead connected to the second lead of the inductor and a second lead connected to a return output; and

a sense resistor having a first lead connected to ground and a second lead connected to the second lead of the output capacitor.

16. The multi LED string controller of claim 14 wherein each channel of the plurality of channels of LEDs comprises:

a plurality of LEDs connected serially;

a channel capacitor having a first lead coupled to a cathode of a first one of the plurality of LEDs connected serially and a second lead coupled to a cathode of a last one of the plurality of LEDs connected serially;

a channel switch having a source connected to the second lead of the channel capacitor; a gate couple to one of the PWM outputs, and a drain; and

a channel resistor having a first lead coupled to the drain of the channel switch and a second lead coupled to a second lead of the output capacitor.

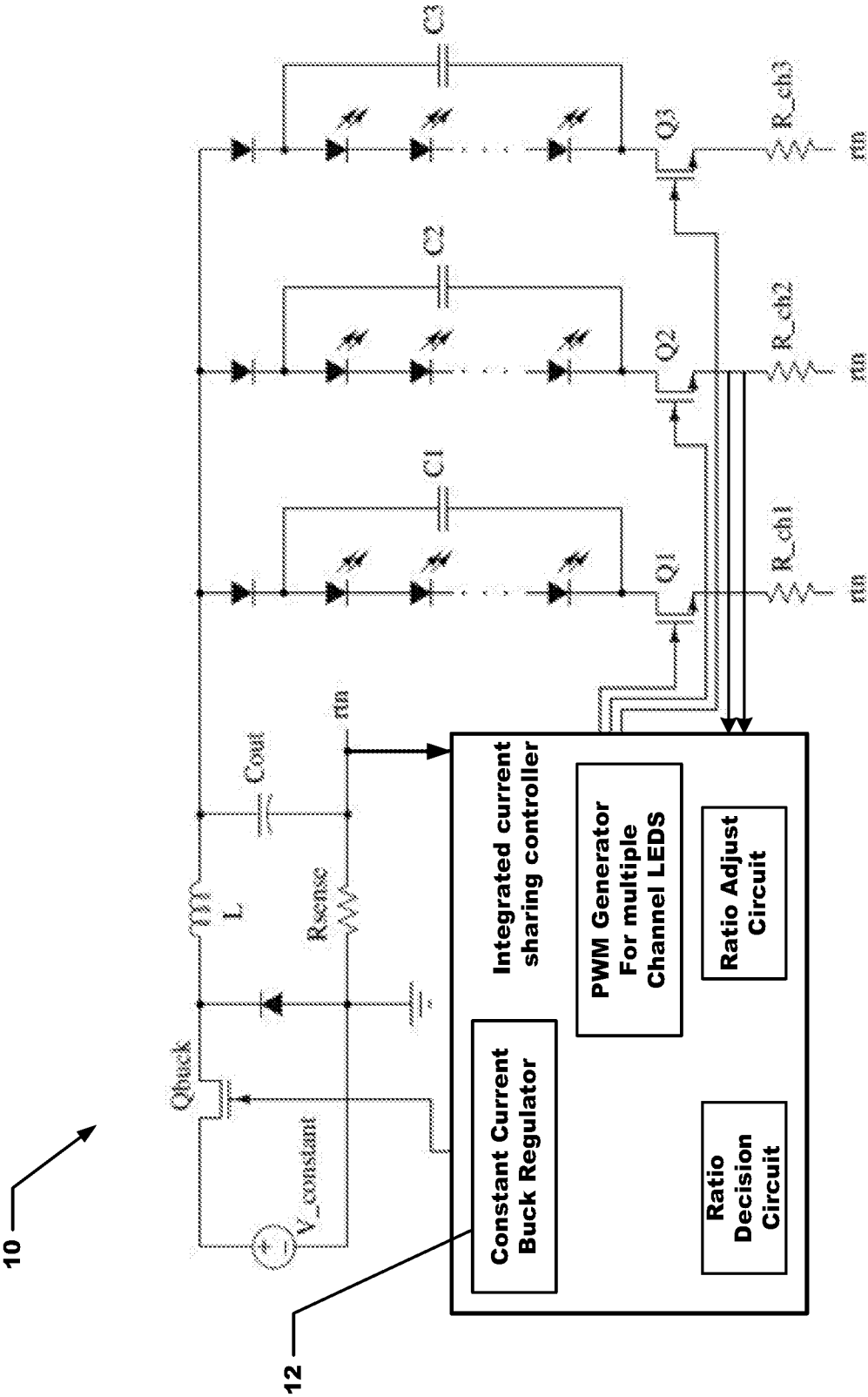


Figure 1

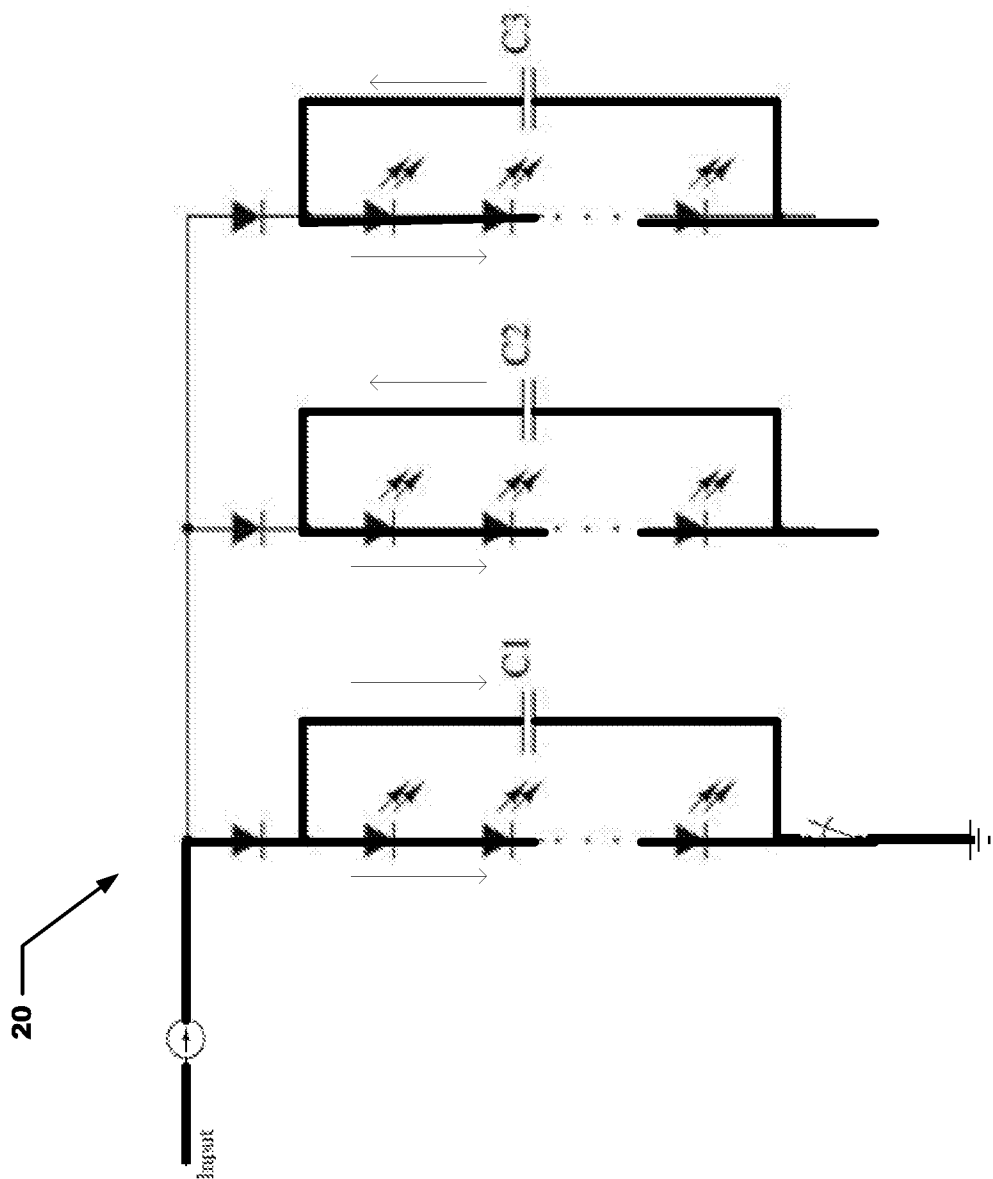


Figure 2A

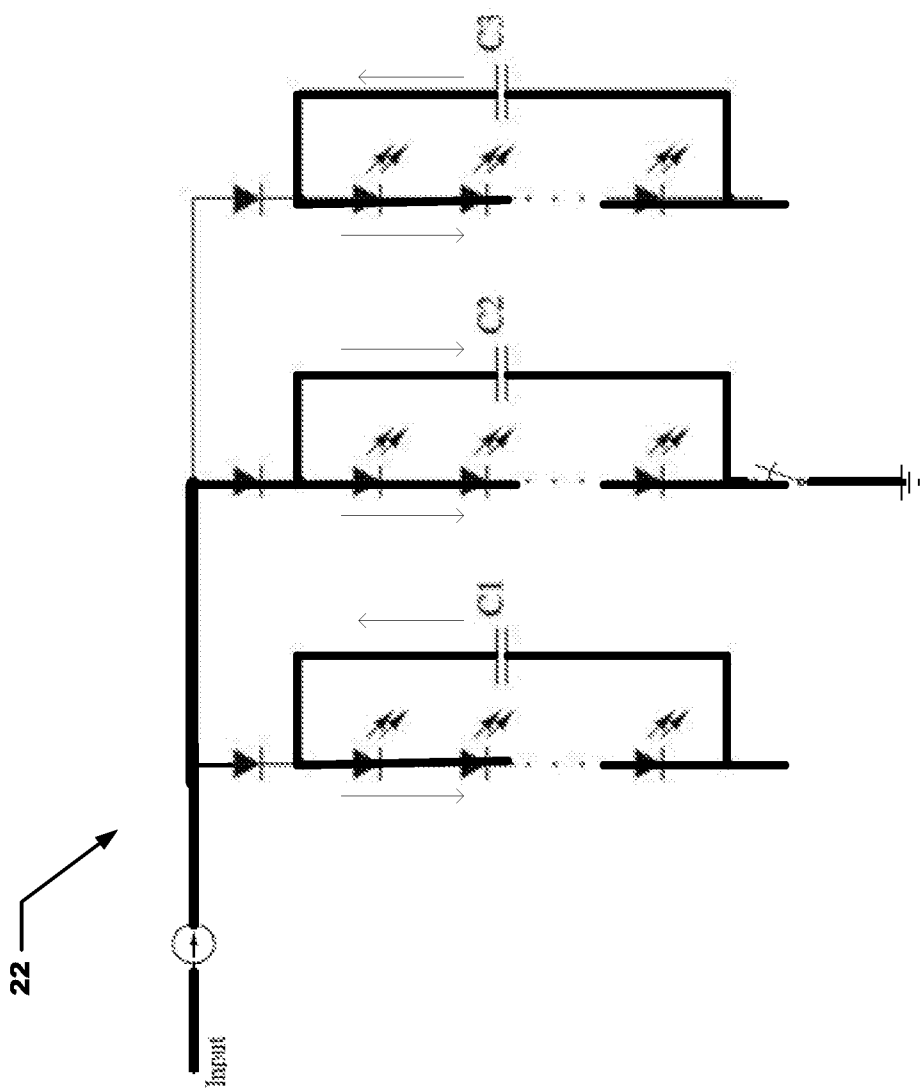


Figure 2B

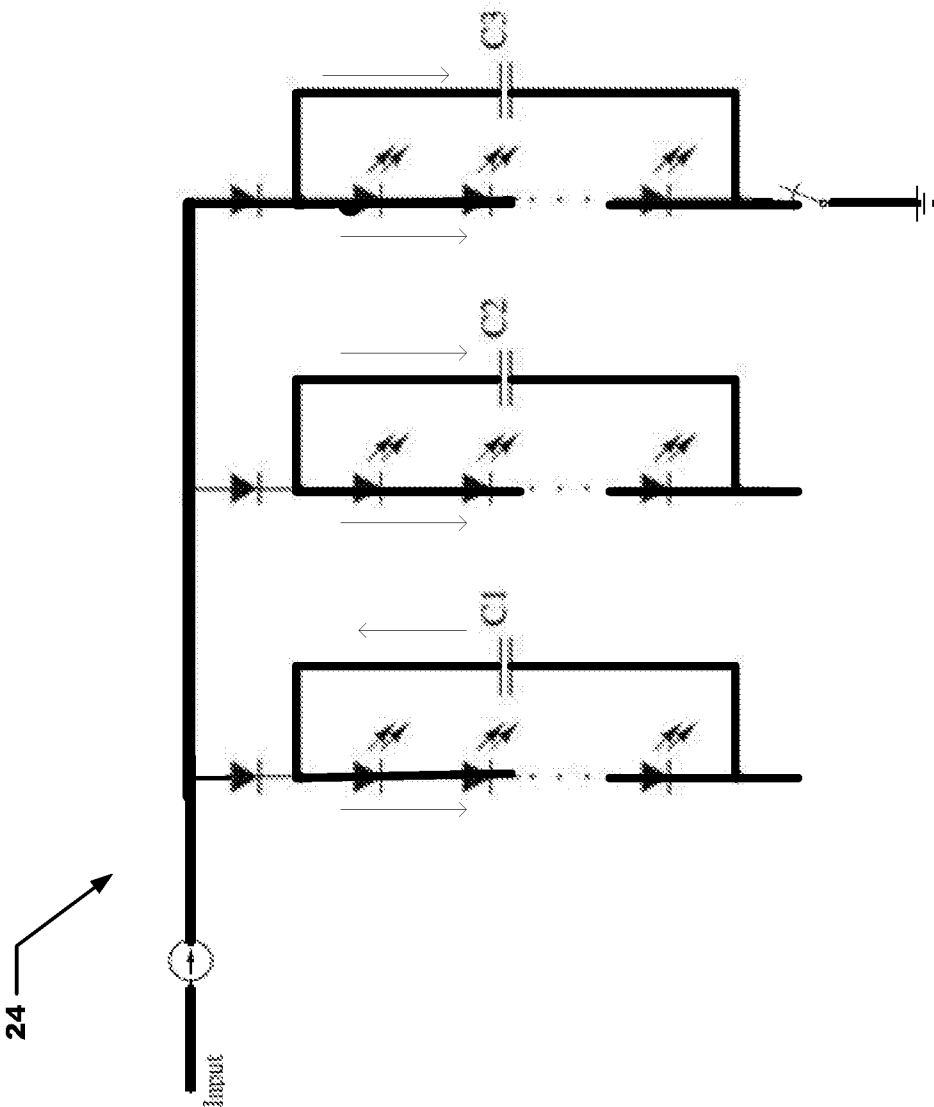


Figure 2C

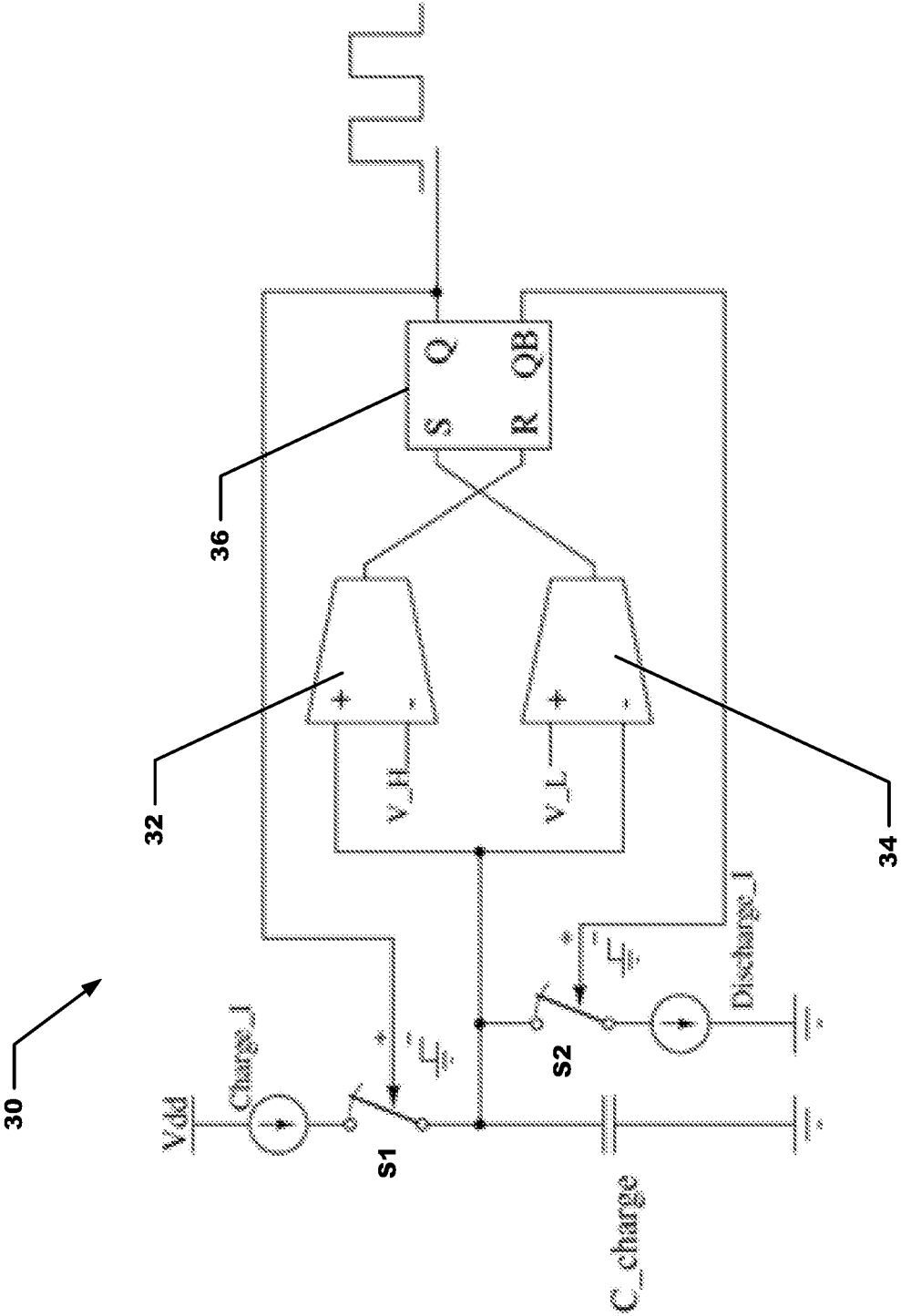


Figure 3

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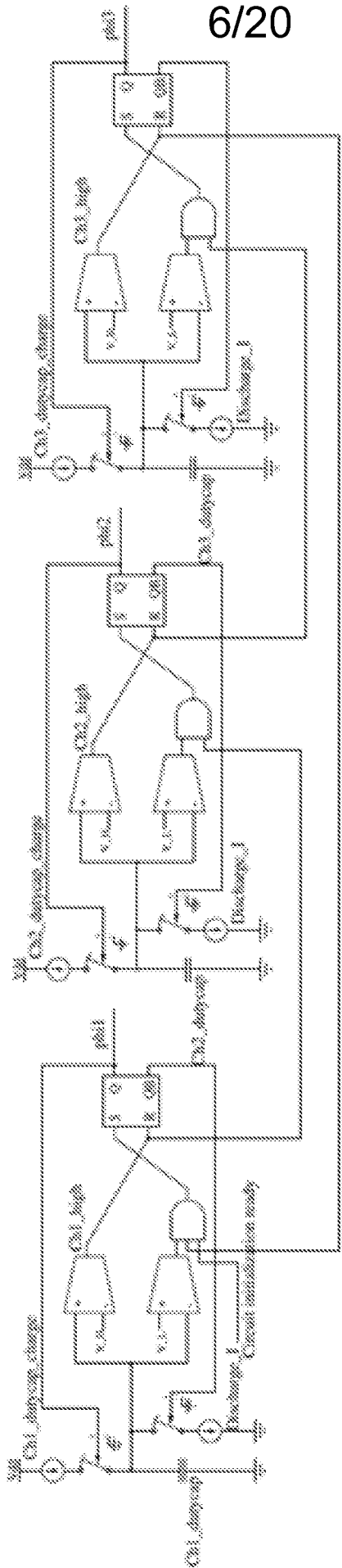


Figure 4

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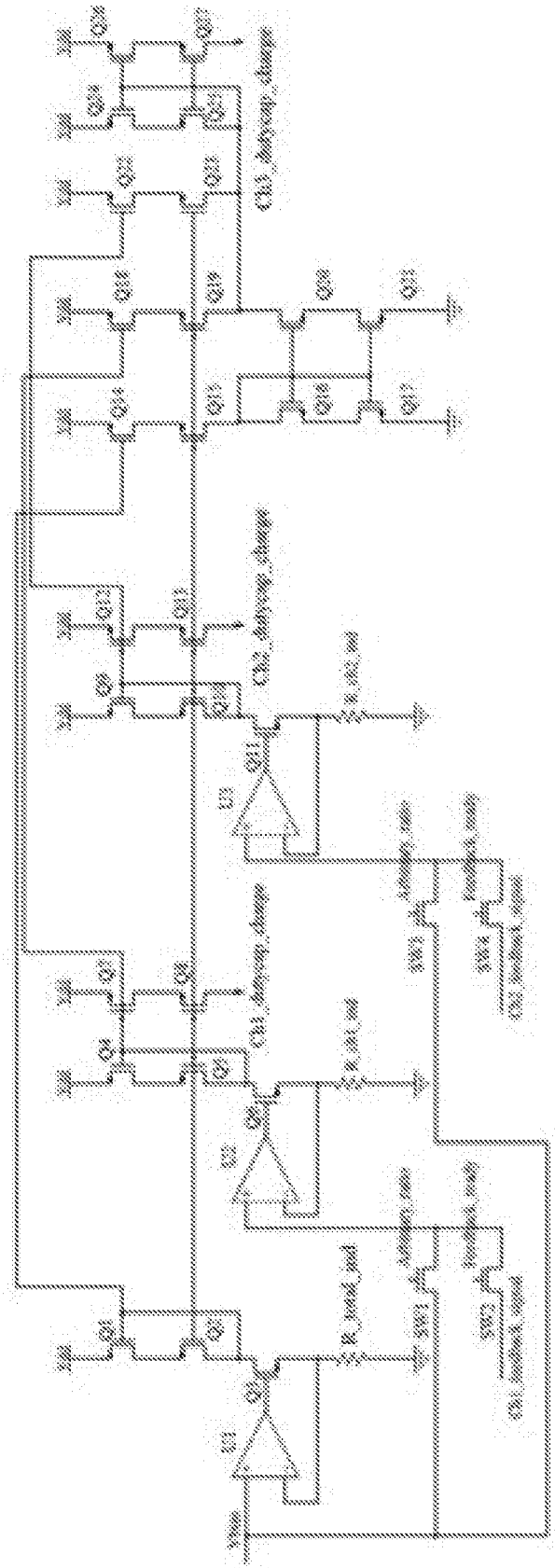
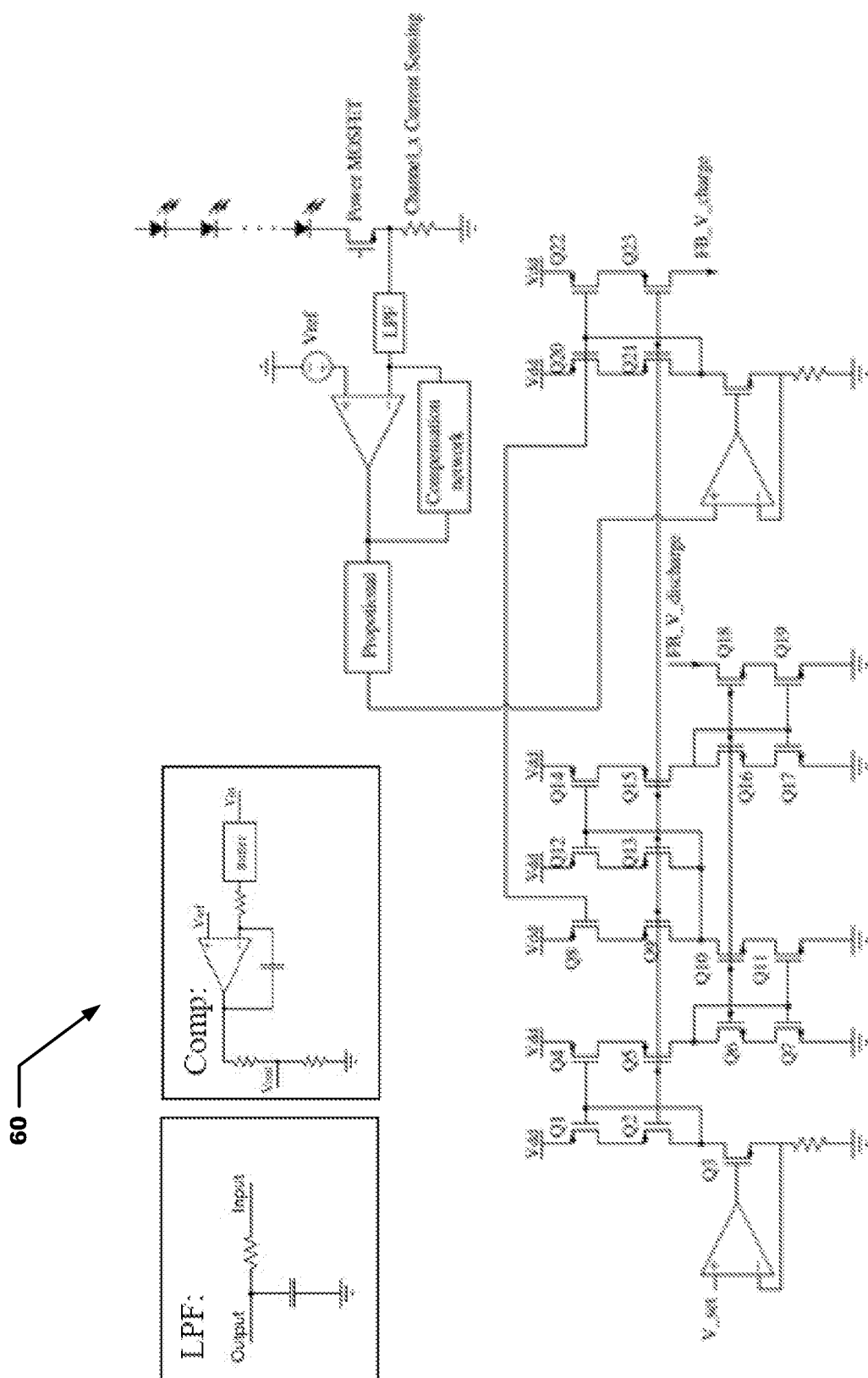
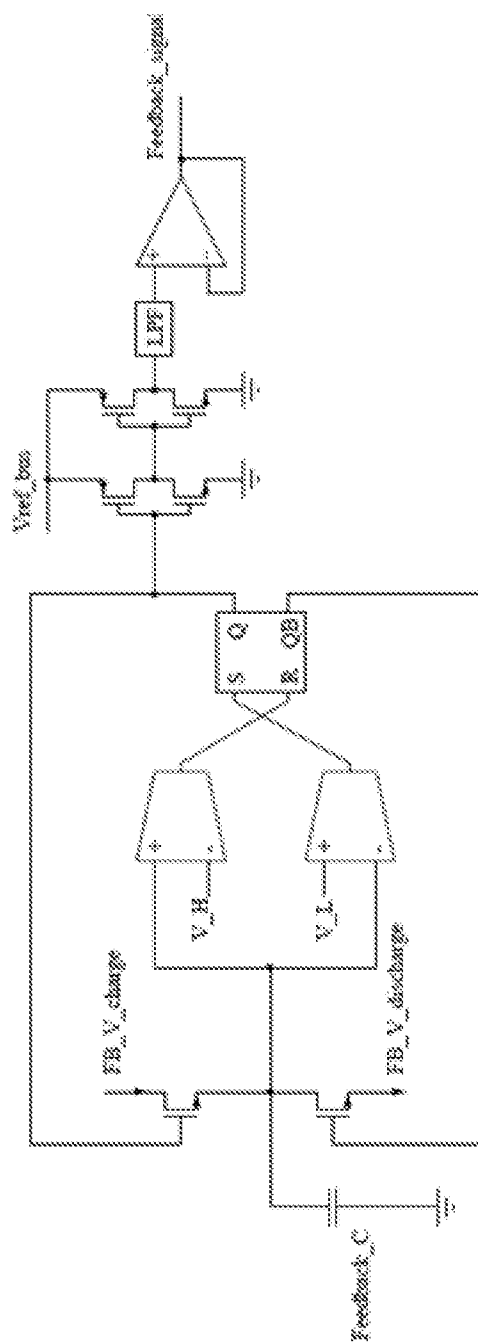


Figure 5



## Figure 6

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## Figure 7

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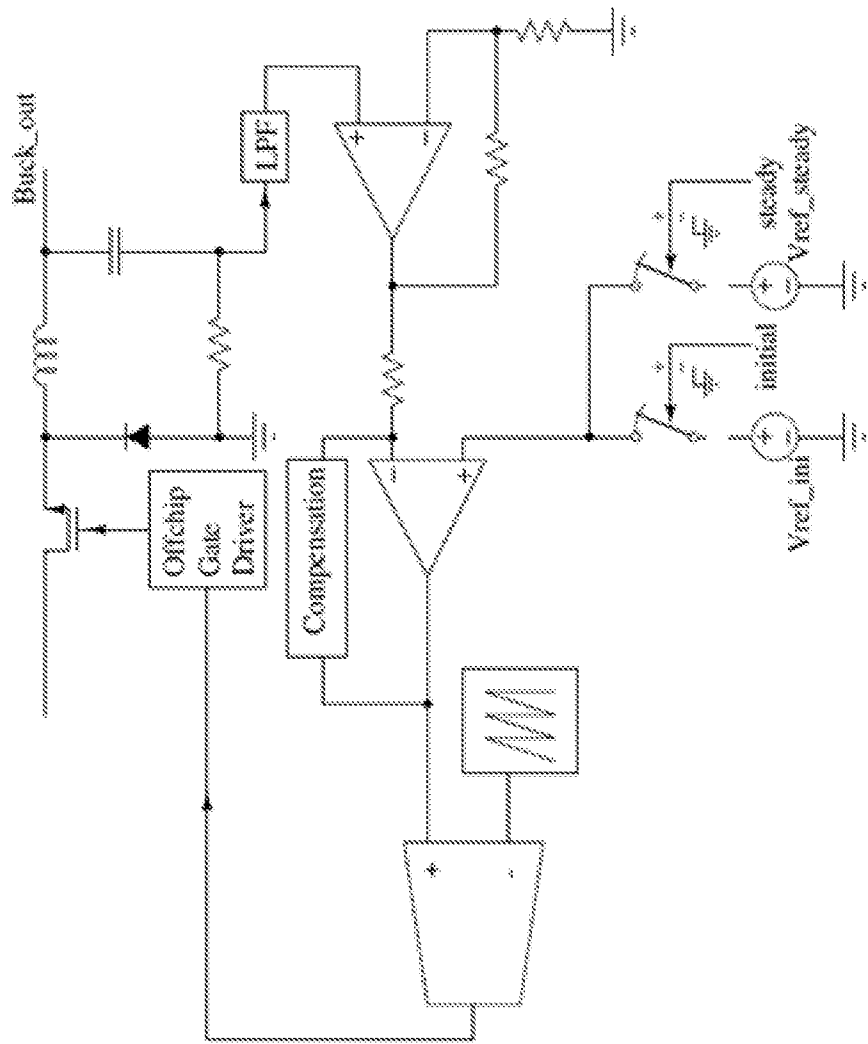


Figure 8

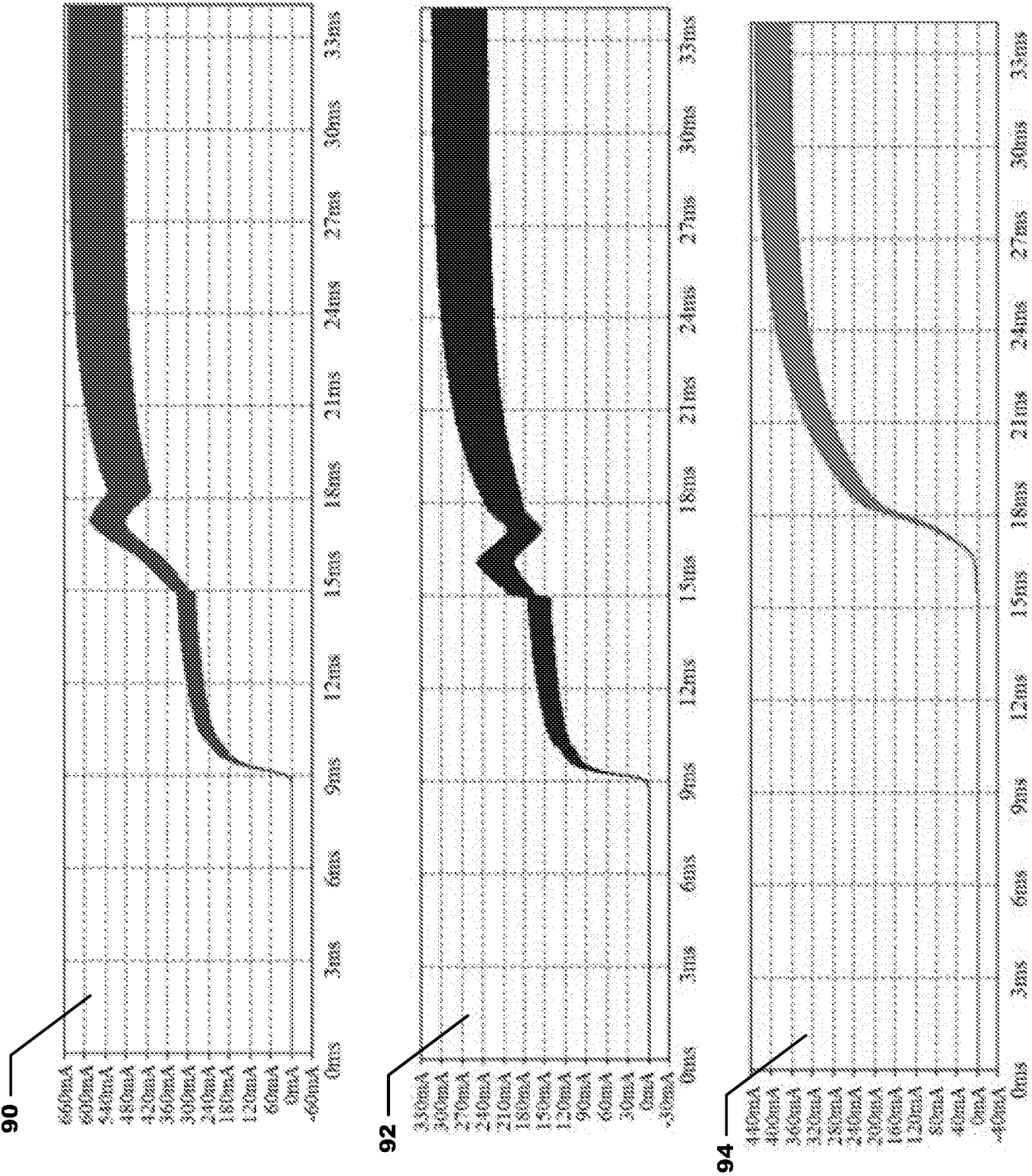


Figure 9

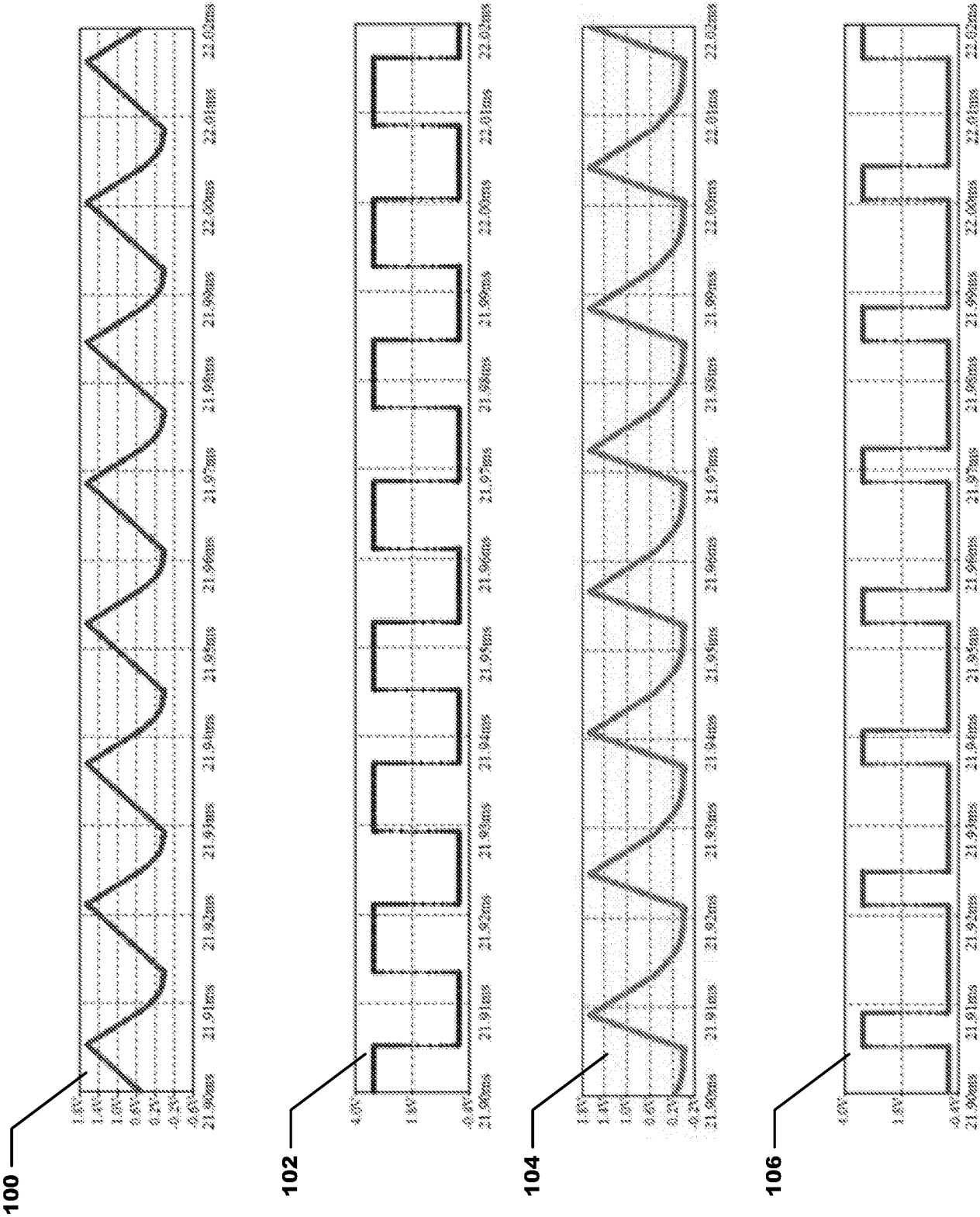


**Figure 10A**

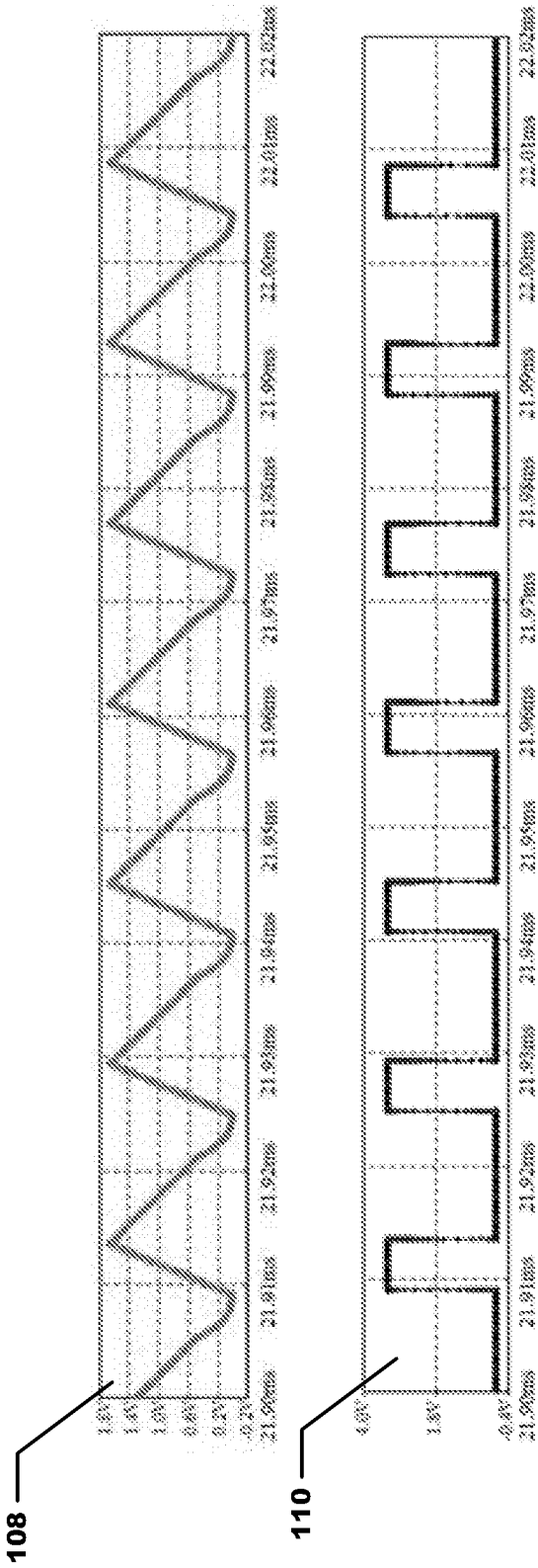


**Figure 10B**

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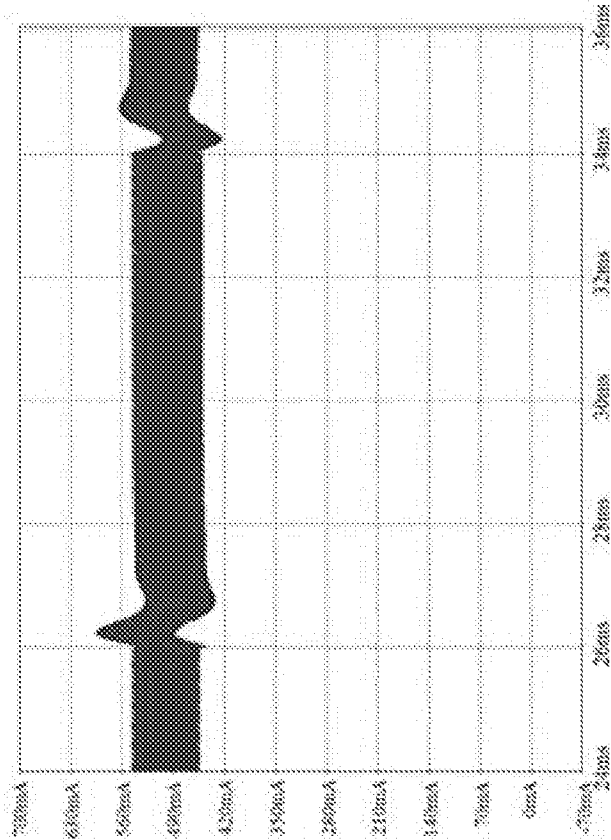
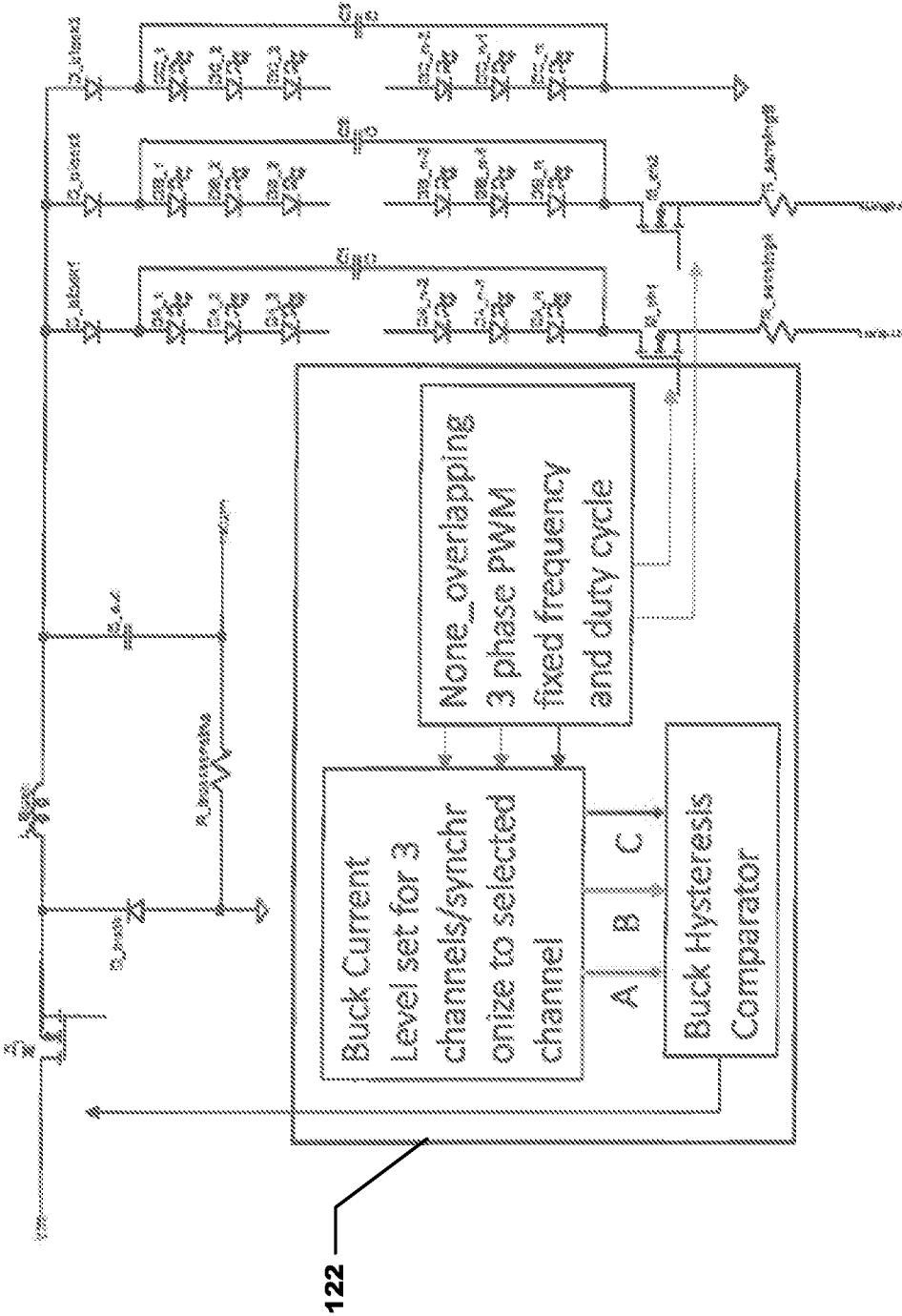


Figure 11

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Figure 12

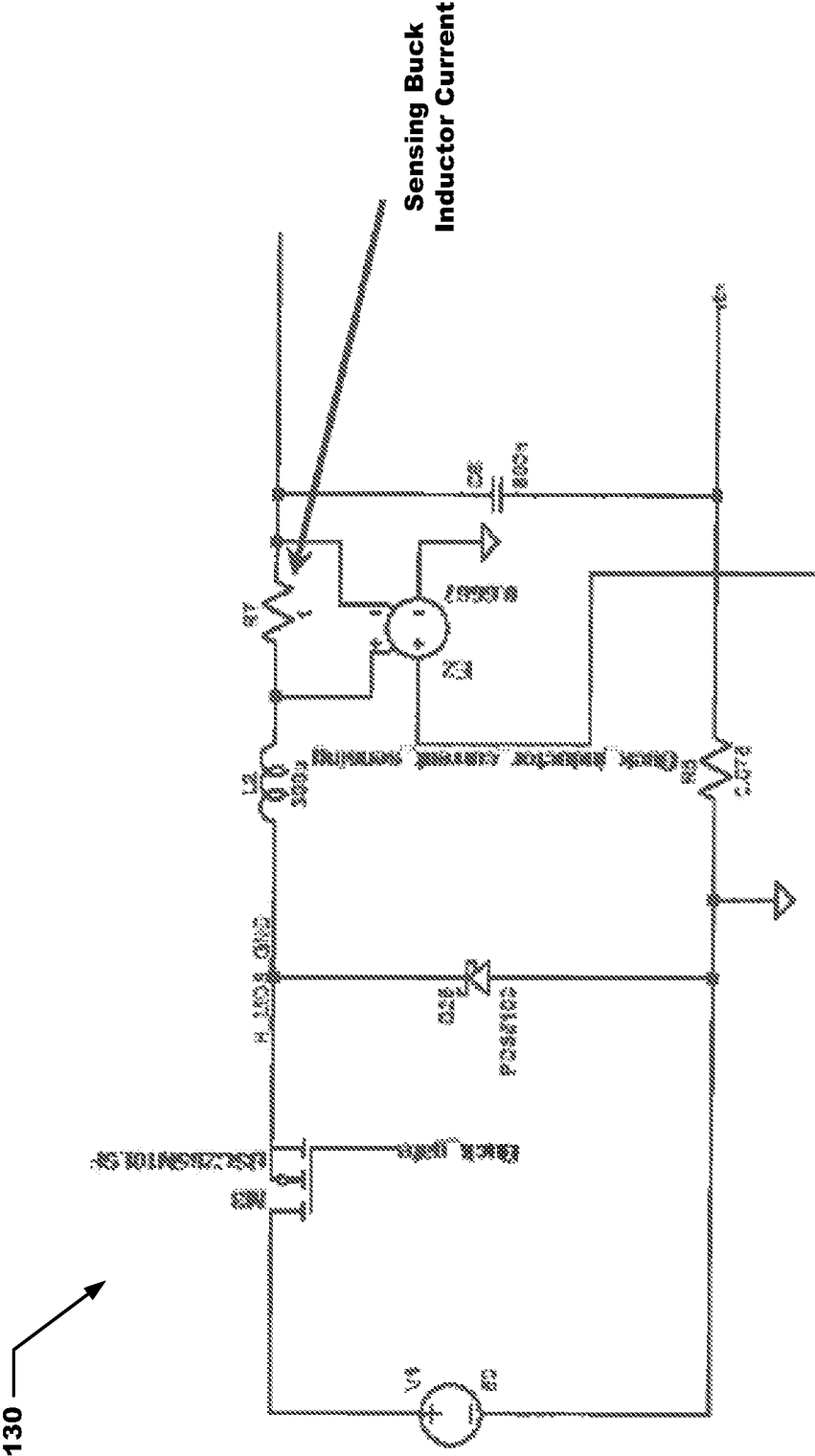


Figure 13

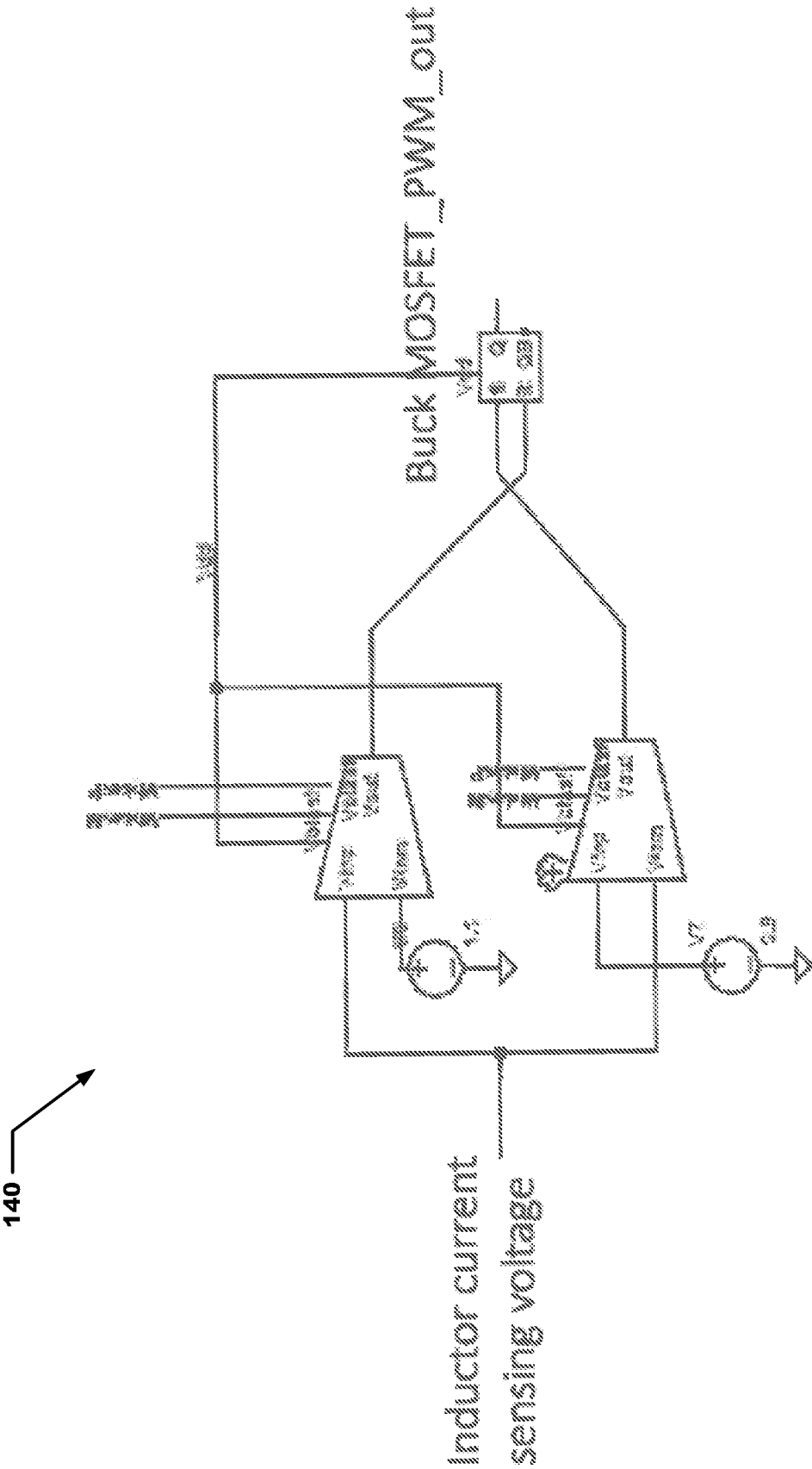


Figure 14

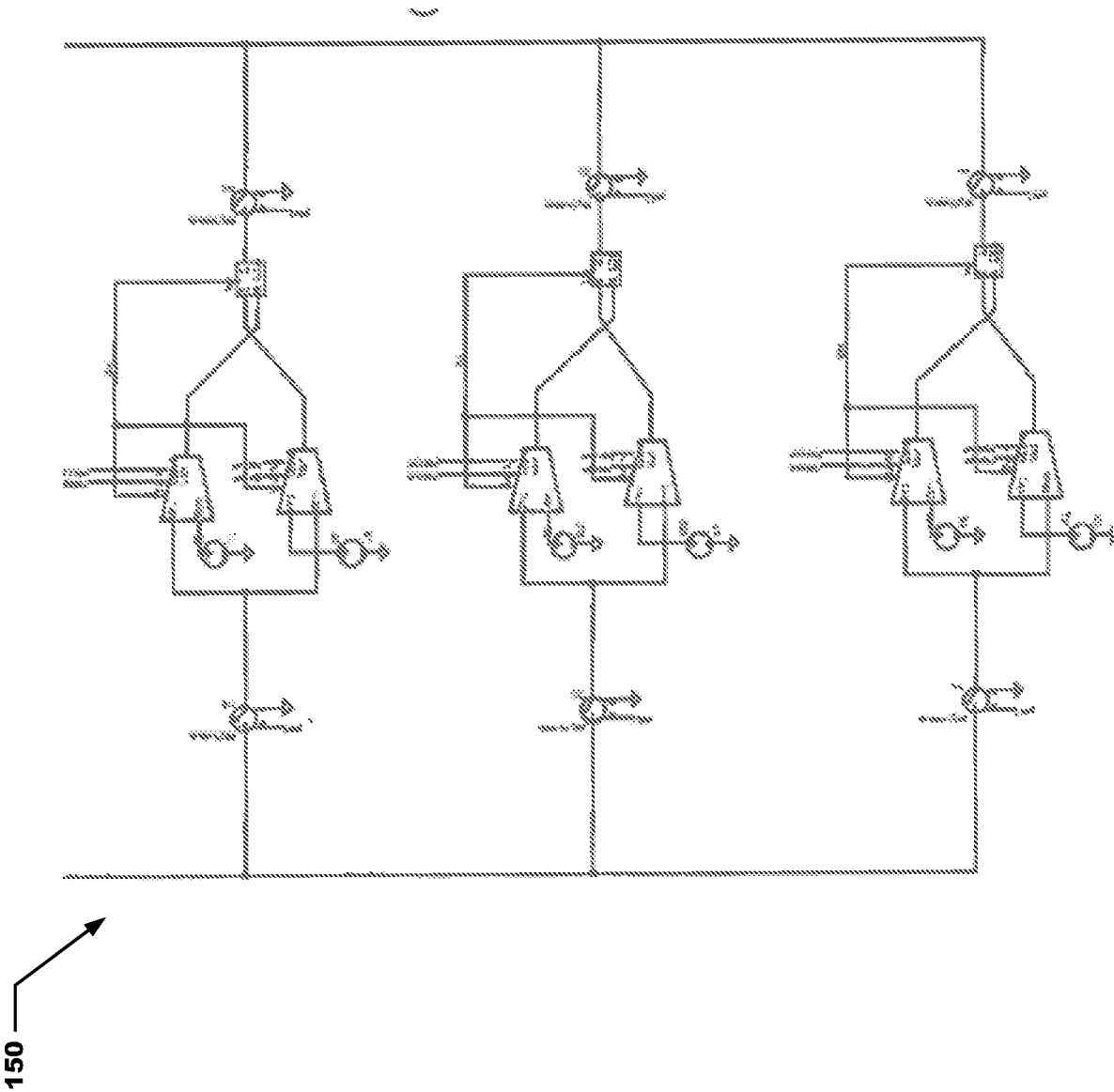


Figure 15

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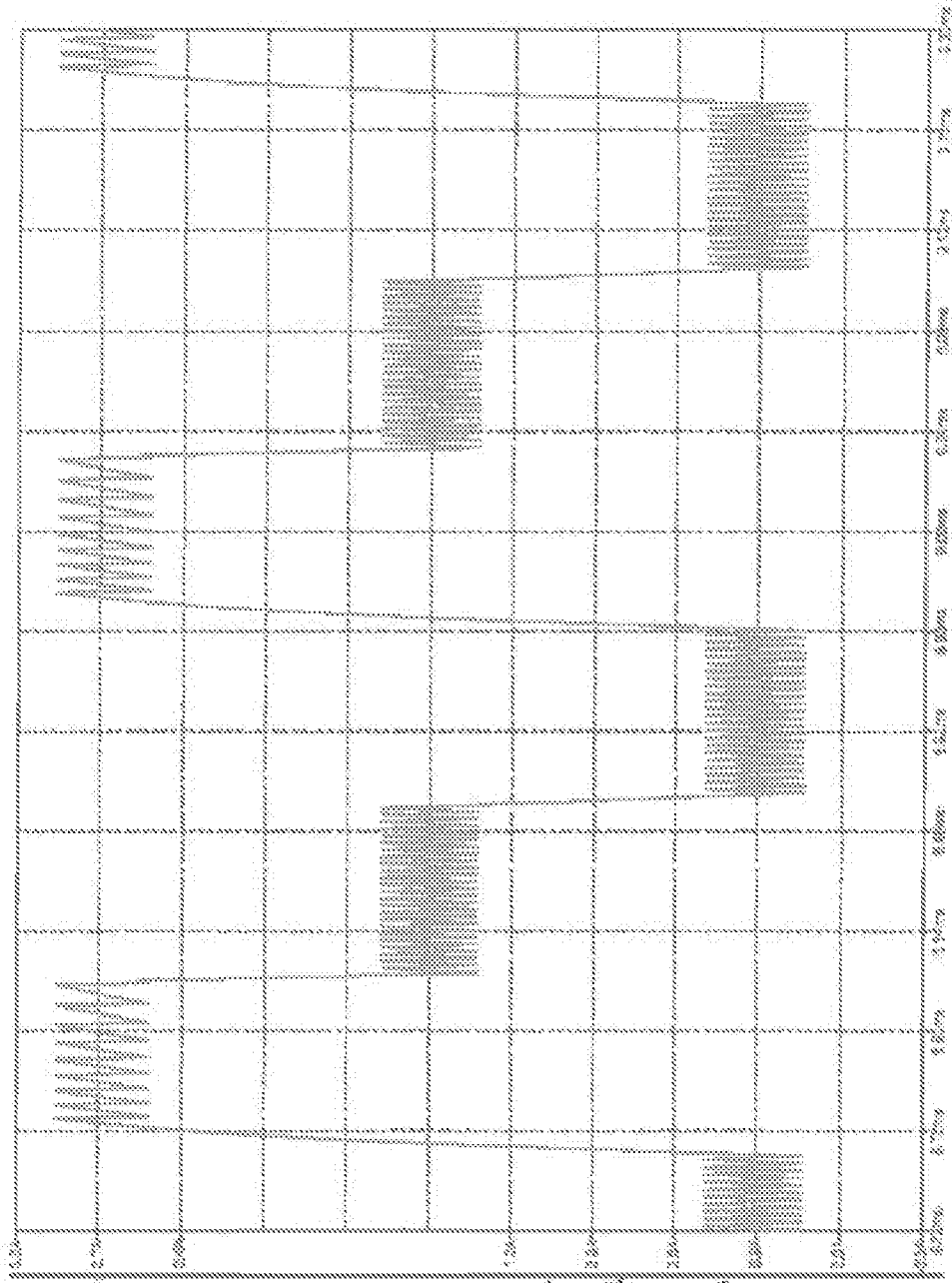


Figure 16

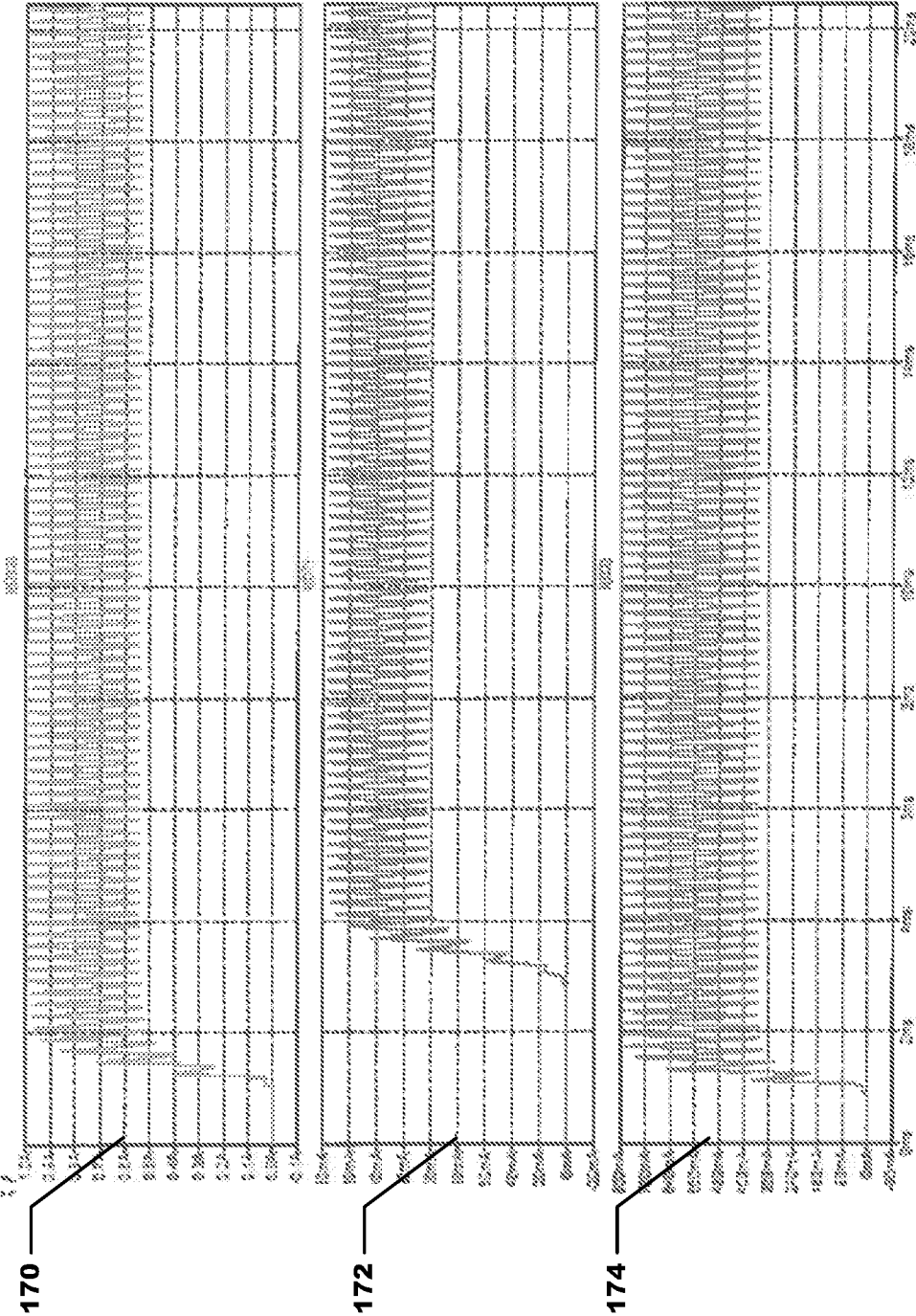


**Figure 17**

## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2016/066229

A. CLASSIFICATION OF SUBJECT MATTER  
 INV. H05B33/08  
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
 H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                 | Relevant to claim No. |
|-----------|----------------------------------------------------------------------------------------------------|-----------------------|
| X         | US 2008/116818 A1 (SHTEYNBERG ANATOLY [US]<br>ET AL) 22 May 2008 (2008-05-22)                      | 1,6,8,9               |
| Y         | figures 7,14                                                                                       | 2-5,7,10              |
| X         | -----<br>CN 102 821 526 B (UNIV ZHEJIANG)<br>9 September 2015 (2015-09-09)                         | 1                     |
| Y         | figure 5                                                                                           | 5-10                  |
| Y         | -----<br>DE 10 2007 047725 A1 (TEXAS INSTRUMENTS<br>DEUTSCHLAND [DE])<br>9 April 2009 (2009-04-09) | 2-4                   |
| Y         | figure 2                                                                                           |                       |
| Y         | -----<br>US 2003/025120 A1 (CHANG CHIN [US])<br>6 February 2003 (2003-02-06)                       | 5-8                   |
|           | figure 3                                                                                           |                       |
|           | -----<br>-/-                                                                                       |                       |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 March 2017

Date of mailing of the international search report

29/03/2017

Name and mailing address of the ISA/

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 NL - 2280 HV Rijswijk  
 Tel. (+31-70) 340-2040,  
 Fax: (+31-70) 340-3016

Authorized officer

Müller, Uta

## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2016/066229

| C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT |                                                                                                                                                 |                       |
|------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Category*                                            | Citation of document, with indication, where appropriate, of the relevant passages                                                              | Relevant to claim No. |
| Y                                                    | WO 2012/140634 A1 (KONINKL PHILIPS ELECTRONICS NV [NL]; KAHLMAN HENRICUS MARIUS JOSEPH MA)<br>18 October 2012 (2012-10-18)<br>figure 4<br>----- | 1-10                  |
| Y                                                    | DE 10 2011 055528 A1 (SAMSUNG ELECTRONICS CO LTD [KR]) 26 July 2012 (2012-07-26)<br>figure 18<br>-----                                          | 1-10                  |
| Y                                                    | WO 2015/039041 A1 (DIALOG SEMICONDUCTOR INC [US]) 19 March 2015 (2015-03-19)<br>figure 2b<br>-----                                              | 1-10                  |
| Y                                                    | WO 2013/027886 A1 (IDT INC [KR]; CHO HYUN MIN [KR]; LEE SEOUNG WOO [KR])<br>28 February 2013 (2013-02-28)<br>figure 3<br>-----                  | 11-16                 |
| X                                                    | US 2009/187925 A1 (HU YUEQUAN [US] ET AL)<br>23 July 2009 (2009-07-23)<br>figures 1-21,22,25<br>-----                                           | 1,6,7                 |
| Y                                                    | EP 1 691 580 A1 (ST MICROELECTRONICS SRL [IT]) 16 August 2006 (2006-08-16)<br>figure 3<br>-----                                                 | 2-5,8-16              |
| Y                                                    | US 2010/109563 A1 (GONG JUNG CHUL [KR] ET AL) 6 May 2010 (2010-05-06)<br>figure 1<br>-----                                                      | 11-16                 |
| Y                                                    | US 2011/032244 A1 (KATAOKA SHINICHIRO [JP]) 10 February 2011 (2011-02-10)<br>figure 6<br>-----                                                  | 11-16                 |
| Y                                                    | WO 2009/122488 A1 (NEC DISPLAY SOLUTIONS LTD [JP]; NAKANISHI SHUICHI [JP])<br>8 October 2009 (2009-10-08)<br>figure 10<br>-----                 | 11-16                 |
| Y                                                    | KR 101 028 860 B1 (GREEN C & C TECH CO LTD [KR]) 12 April 2011 (2011-04-12)<br>figures 1-4<br>-----                                             | 11-16                 |
| Y                                                    | WO 2004/100614 A1 (KONINKL PHILIPS ELECTRONICS NV [NL]; XU PENG [US])<br>18 November 2004 (2004-11-18)<br>figures 1,4<br>-----                  | 11-16                 |

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US2016/066229

## Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

## Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

### Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☒ No protest accompanied the payment of additional search fees.

**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-10

LED constant current controller for multichannel current sharing topology using an integrated buck converter providing a fixed current and variable PWM regulation of the respective LED string.

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2. claims: 11-16

LED constant current controller for multichannel current sharing topology using a buck converter providing a variable current and fixed duty cycle control of the respective LED string.

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# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2016/066229

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s)                                                                                         | Publication<br>date                                                              |
|-------------------------------------------|---------------------|--------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|
| US 2008116818 A1                          | 22-05-2008          | TW 200838358 A<br>US 2008116818 A1<br>US 2011187276 A1<br>US 2012306389 A1<br>US 2014055046 A1<br>WO 2008063454 A2 | 16-09-2008<br>22-05-2008<br>04-08-2011<br>06-12-2012<br>27-02-2014<br>29-05-2008 |
| CN 102821526 B                            | 09-09-2015          | NONE                                                                                                               |                                                                                  |
| DE 102007047725 A1                        | 09-04-2009          | NONE                                                                                                               |                                                                                  |
| US 2003025120 A1                          | 06-02-2003          | CN 1537403 A<br>EP 1421829 A1<br>JP 2004538653 A<br>KR 20040028976 A<br>US 2003025120 A1<br>WO 03015476 A1         | 13-10-2004<br>26-05-2004<br>24-12-2004<br>03-04-2004<br>06-02-2003<br>20-02-2003 |
| WO 2012140634 A1                          | 18-10-2012          | CN 103493590 A<br>TW 201247016 A<br>WO 2012140634 A1                                                               | 01-01-2014<br>16-11-2012<br>18-10-2012                                           |
| DE 102011055528 A1                        | 26-07-2012          | CN 102610195 A<br>DE 102011055528 A1<br>JP 2012151830 A<br>KR 20120084555 A<br>TW 201233065 A<br>US 2012187762 A1  | 25-07-2012<br>26-07-2012<br>09-08-2012<br>30-07-2012<br>01-08-2012<br>26-07-2012 |
| WO 2015039041 A1                          | 19-03-2015          | DE 112014004226 T5<br>US 2015076999 A1<br>WO 2015039041 A1                                                         | 21-07-2016<br>19-03-2015<br>19-03-2015                                           |
| WO 2013027886 A1                          | 28-02-2013          | KR 20130020326 A<br>WO 2013027886 A1                                                                               | 27-02-2013<br>28-02-2013                                                         |
| US 2009187925 A1                          | 23-07-2009          | NONE                                                                                                               |                                                                                  |
| EP 1691580 A1                             | 16-08-2006          | EP 1691580 A1<br>US 2006186827 A1<br>US 2010148684 A1                                                              | 16-08-2006<br>24-08-2006<br>17-06-2010                                           |
| US 2010109563 A1                          | 06-05-2010          | CN 101730339 A<br>KR 100956222 B1<br>US 2010109563 A1                                                              | 09-06-2010<br>04-05-2010<br>06-05-2010                                           |
| US 2011032244 A1                          | 10-02-2011          | JP 4657355 B2<br>JP 2011014616 A<br>US 2011032244 A1<br>WO 2011001563 A1                                           | 23-03-2011<br>20-01-2011<br>10-02-2011<br>06-01-2011                             |
| WO 2009122488 A1                          | 08-10-2009          | JP 5366221 B2<br>WO 2009122488 A1                                                                                  | 11-12-2013<br>08-10-2009                                                         |
| KR 101028860 B1                           | 12-04-2011          | NONE                                                                                                               |                                                                                  |
| WO 2004100614 A1                          | 18-11-2004          | AT 392792 T<br>CN 1784930 A                                                                                        | 15-05-2008<br>07-06-2006                                                         |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2016/066229

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s) | Publication<br>date |
|-------------------------------------------|---------------------|----------------------------|---------------------|
|                                           |                     | DE 602004013138 T2         | 07-05-2009          |
|                                           |                     | EP 1623604 A1              | 08-02-2006          |
|                                           |                     | JP 4959325 B2              | 20-06-2012          |
|                                           |                     | JP 2006525665 A            | 09-11-2006          |
|                                           |                     | KR 20060018829 A           | 02-03-2006          |
|                                           |                     | KR 20120018825 A           | 05-03-2012          |
|                                           |                     | US 2006267514 A1           | 30-11-2006          |
|                                           |                     | WO 2004100614 A1           | 18-11-2004          |
| -----                                     |                     |                            |                     |