Title: TRANSIENT TRIGGERED FINFET SILICON CONTROLLED RECTIFIER FOR ELECTROSTATIC DISCHARGE PROTECTION

Abstract: Described is an apparatus which comprises a first shallow trench isolation (STI) region; a first gated FinFET device including a source region of a first conductivity type; and a second gated FinFET device including a drain region of a second conductivity type, wherein the source region of the first gated FinFET device is adjacent to the drain region of the second gated FinFET device such that the source region of the first gated FinFET device is separated by the drain region of the second gated FinFET device via the first STI region.

Fig. 4
TRANSIENT TRIGGERED FINFET SILICON CONTROLLED RECTIFIER FOR ELECTROSTATIC DISCHARGE PROTECTION

BACKGROUND

[0001] Electrostatic discharge (ESD) is the sudden discharge of electric charge between two electrically charged nodes (e.g., Input-Output (IO) pins coupled to an Integrated Circuit (IC)). This sudden discharge typically produces a large current that passes through the IC in a short duration of time, which may result in damage or destruction of the IC, if not properly handled or protected. This large current is bypassed by circuits called ESD protection circuits. Typically, an ESD protection circuit provides a current path to ground and/or supply when an ESD event occurs so that the high current resulting from the ESD event bypasses the ESD sensitive circuitry in the IC.

[0002] Conventional ESD protection circuits for the IO pins of Radio-Frequency (RF) circuits suffer from challenges. For example, conventional ESD protection circuits trigger too slowly and exhibit transient voltage overshots causing damage to the ultra-thin gate oxides often used in RF receiver gates. Conventional ESD protection circuits cause too much capacitive loading for proper RF circuit functionality. Furthermore, RF circuit requirements often prohibit the usage of conventional dual-stage ESD circuits, as no series resistor in the signal path is allowed due to noise issues. These design requirements further challenge the design of ESD protection circuits for use with IO pins of RF circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0004] Fig. 1 illustrates a perspective view of a Fin Field Effect Transistor (FinFET) based Silicon Controlled Rectifier (SCR) device having a single gate electrode.

[0005] Fig. 2 shows a cross-sectional view of the FinFET SCR device of Fig. 1.

[0006] Fig. 3 shows a cross-sectional view of a FinFET SCR with two terminals where a gated diode is coupled in series to a Metal Oxide Semiconductor (MOS) transistor.

[0007] Fig. 4 illustrates a cross-sectional view of a power-supply transient-triggered FinFET (TT-FinFET) gated SCR, according to some embodiments of the disclosure.
[0008] Fig. 5 illustrates a cross-sectional view of a ground-supply TT-FinFET gated SCR, according to some embodiments of the disclosure.

[0009] Fig. 6 illustrates a circuit model of an Electro-Static Discharge (ESD) circuit with the power-supply TT-FinFET gated SCR and the ground-supply TT-FinFET gated SCR, according to some embodiments of the disclosure.

[0010] Fig. 7 illustrates a folded layout of a power-supply TT-FinFET gated SCR of Fig. 4, according to some embodiments of the disclosure.

[0011] Fig. 8 illustrates a smart device or a computer system or a SoC (System-on-Chip) having an ESD circuit with TT-FinFETs, according to some embodiments.

**Detailed Description**

[0012] Fig. 1 illustrates a perspective view of a Fin Field Effect Transistor (FinFET) based Silicon Controlled Rectifier (SCR) 100 having a single gate electrode. Fig. 2 shows a cross-sectional view of the FinFET SCR 200 of Fig. 1. Both Figs. 1-2 are described together. So, identifiers discussed and not indicated in Fig. 1 are in Fig. 2, and vice versa.

[0013] FinFET based SCR 100 includes a semiconductor fin 102, extending upwardly from an upper surface 104 of semiconductor substrate 106. Here, Shallow Trench Isolation (STI) region 108, which is made of a dielectric material (e.g., silicon dioxide), has an upper surface 110 that divides the semiconductor fin 102 into upper portion 102a and base portion 102b. STI region 108 laterally surrounds base fin portion 102b, while upper fin portion 102a remains above upper surface 110 of STI region 108. Unlike planar Complementary Metal Oxide Semiconductor (CMOS) transistors where the source, drain, and channel regions are formed in a planar substrate; in FinFETs the source, drain, and channel regions are formed in a thin slice of semiconductor material (i.e., a “fin”), which extends upward from the semiconductor substrate.

[0014] Upper fin portion 102a includes anode 112 having a first conductivity type (e.g., P+) and cathode 114 having a second conductivity type (e.g., N+). Anode 112 and cathode 114 are arranged at opposing ends of the fin 102. A current control element or trigger element 115 is arranged between anode 112 and cathode 114.

[0015] In Figs. 1-2, current control element 115 includes a conductive gate electrode 116. Here, conductive gate electrode 116 is arranged to traverse over fin 102 between anode 112 and cathode 114. An intrinsic upper fin region 118 can be arranged under gate electrode 116,
and gate dielectric 120 can electrically isolate the intrinsic upper fin region 118 from gate electrode 116. The conductive gate electrode 116 is often made of metal, and the substrate often has the first conductivity type (e.g., P+).

[0016] Base fin portion 102b includes a first doped base region 122 having the second conductivity type (e.g., N-) under anode 112. Under cathode 114, the base fin portion 102b includes a second doped base region 124 having the first conductivity type (e.g., P-). An intrinsic base fin region 126 can be arranged under gate electrode 116 between first and second base regions 122, 124. Often, the intrinsic base fin region 126 has a length, L\text{base} that is shorter than a length, L\text{upper}, of the intrinsic upper fin region 118. Because intrinsic silicon has a lower conductivity than doped silicon, this arrangement tends to promote current flow through the less resistive, base fin region 126; although some lesser amount of current can still flow in the more resistive, upper intrinsic fin region 118 as well.

[0017] During operation, current can flow from anode 112, through the base fin portion 102b and out the cathode 114 (depending on the biases applied to the SCR terminals). However, FinFET SCR 100/200 when used in Electrostatic Discharge (ESD) protection circuit, triggers too slowly and exhibits transient voltage overshoots causing damage to the ultra-thin gate oxides often used in RF receiver gates. Gates of FinFET SCR 100/200 do not act as means to enable/disable current flow, because there is no Metal Oxide Semiconductor (MOS) transistor. FinFET SCR 100/200 does not have a dedicated trigger mechanism, and rely on inner breakdown which creates a much too high trigger voltage causing damage to the gate oxides. As such, FinFET SCR 100/200 is not suitable for ESD protection of RF-IOs.

[0018] Fig. 3 shows a cross-sectional view of FinFET SCR 300 where a gated diode is in series to a MOS transistor. Metal Gate 1 is coupled to the Anode, Metal Gate 2 is coupled to resistor R and capacitor C, which provide the necessary time constant for tuning on and off the ESD circuit, while Metal Gate 3 is coupled to the Cathode (i.e., ground (VSS)). As such, Metal gate 2 behaves as a current control unit. In FinFET SCR 300, there is limited gate bias on Metal Gate 2 and thus limited MOS current (i.e., VDD is just floating during ESD). The capacitive loading at the Anode also slows the trigger speed. Further, the spacing between the Anode and the Cathode terminals is long, where the Anode terminal is coupled to a P+ source region while the Cathode terminal is coupled to the N+ drain region. As such, the current path by SCR 300, by the forward-biased diode and the RC triggered NMOS, is long.
[0019] The long Anode-to-Cathode distance of the SCR spacing makes the triggering process slow for FinFET SCR 300. FinFET SCR 300 is triggered by a built-in MOS transistor which may be ESD-efficient for large gate widths making it unsuitable for RF circuits due to the high parasitic capacitance from the large gate widths. This long Anode-to-Cathode path in FinFET SCR 300 leaves critical circuits coupled to the RF-IO open to the adverse stress from ESD for longer time. As such, both FinFET SCRs 100/200 and 300 are not suitable for providing ESD protection to RF-IOs.

[0020] Some embodiments describe an SCR structure for FinFET technology where the critical PN-junctions may also be formed under a gate and are thus without STI. In some embodiments, the SCR structure is also provided without gate and without STI. In some embodiments, the terminals of the SCR structure are configured for very fast turn-on during ESD events compared to the FinFET SCRs described with reference to Figs. 1-3.

[0021] In some embodiments, the conduction of current happens along two different paths for the different ESD stress events. In some embodiments, the first conduction path is via a built-in non-STI diode for Charge Device Model (CDM) ESD protection (i.e., short and very high current event but relatively low energy content). In some embodiments, the second conduction path through the actual SCR covers Human Body Model (HBM) ESD (i.e., still high current event but longer and higher energy content). In some embodiments, two complementary clamp devices are described that can effectively protect an RF-IO pad during different ESD stress modes. For example, the two complementary clamp devices can protect the RF-IO pad which may be stressed positively vs. VSS, stressed negatively vs. VSS, stressed positively vs. VDD, stressed negatively vs. VDD, etc.

[0022] In some embodiments, the SCR FinFET structure comprises a central anode region forming two devices at the same time—a diode and an SCR. In some embodiments, the anode of the diode is connected to a VDD line (i.e., power supply) which is floating and/or grounded during the ESD event. In some embodiments, the SCR is formed between the anode, an N-well region, a P-substrate, and an N+ cathode which is grounded.

[0023] In some embodiments, a cross-section of the FinFET SCR structure without STI in the diode path allows the best ratio between a high ESD current at low clamping voltage and a low parasitic capacitance. In some embodiments, this non-STI diode features an anode-cathode path length ("diode length") which is significantly shorter than with STI based SCR (as shown
with reference to Fig. 2) and at higher cross-section area for reduced current density, thus minimizing the transient voltage overshoot (i.e., forward recovery effect).

[0024] In some embodiments, the wiring of the SCR structure allows two clamping devices to be used in a complementary fashion for positive and negative ESD stress polarities at the IO pin to the supply lines VDD or VSS (i.e., ground). As such, each clamp covers two ESD discharge modes while capacitively loading the IO pin merely once, in accordance with some embodiments.

[0025] In some embodiments, the SCR is triggered transiently by a current through the first diode path which flows to the temporarily grounded VDD supply line. The current in the diode path then turns on the SCR path to VSS. In some embodiments, the SCR does not involve any junction to break down for triggering or any other trigger devices, and its snapback-free trigger characteristic leads to the minimum possible trigger voltage for best possible ESD clamping. In some embodiments, in addition to the diodes without STI, the FinFET SCR kernel itself may also be done without STI for further enhanced ESD turn-on characteristics.

[0026] There are many technical effects/benefits of various embodiments. For example, in some embodiments, the influence of the gate capacitance in the gated diode is reduced by the fact that the tip of the fin is depleted and the influence of the gate overlap capacitance is reduced by a resistive connection to VDD. The SCR of some embodiments has a shorter anode-cathode spacing and shorter trigger path (compared to the SCR FinFET of Fig. 3), both accomplished by the arrangement of the device structure and its wiring. Various embodiments can also provide adequate CDM and HBM ESD protection levels for ultra-sensitive RF-IO pins because the FinFET SCR structures of various embodiments trigger extremely fast so that the transient voltage overshoot is minimized and no series resistor and/or no secondary clamping stage in the signal path is needed (e.g. 50 Ohms per current ESD concepts). Other technical effects will be evident from the description of illustrations of various figures and embodiments.

[0027] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.
[0028] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0029] Throughout the specification, and in the claims, the term "connected" means a direct connection, such as electrical, mechanical, or magnetic connection between the things that are connected, without any intermediary devices. The term "coupled" means a direct or indirect connection, such as a direct electrical, mechanical, or magnetic connection between the things that are connected or an indirect connection, through one or more passive or active intermediary devices. The term "circuit" or “module” may refer to one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" may refer to at least one current signal, voltage signal, magnetic signal, or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0030] The term “scaling” generally refers to converting a design (schematic and layout) from one process technology to another process technology and subsequently being reduced in layout area. The term “scaling” generally also refers to downsizing layout and devices within the same technology node. The term “scaling” may also refer to adjusting (e.g., slowing down or speeding up – i.e. scaling down, or scaling up respectively) of a signal frequency relative to another parameter, for example, power supply level. The terms “substantially,” “close,” “approximately,” “near,” and “about,” generally refer to being within +/- 10% of a target value.

[0031] Unless otherwise specified the use of the ordinal adjectives “first,” “second,” and “third,” etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.
For the purposes of the present disclosure, phrases “A and/or B” and “A or B” mean (A), (B), or (A and B). For the purposes of the present disclosure, the phrase “A, B, and/or C” means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

For purposes of the embodiments, the transistors in some circuits and logic blocks described here are metal oxide semiconductor (MOS) transistors or their derivatives, where the MOS transistors include drain, source, gate, and bulk terminals. The transistors and/or the MOS transistor derivatives also include Tri-Gate and FinFET transistors, Gate All Around Cylindrical Transistors, Tunneling FET (TFET), Square Wire, or Rectangular Ribbon Transistors, ferroelectric FET (FeFETs), dynamic-VT FeFETs, dynamic-VT nanocrystal based FETs, or other devices implementing transistor functionality like carbon nanotubes or spintronic devices. MOSFET symmetrical source and drain terminals i.e., are identical terminals and are interchangeably used here. A TFET device, on the other hand, has asymmetric Source and Drain terminals. Those skilled in the art will appreciate that other transistors, for example, Bi-polar junction transistors—BJT PNP/NPN, BiCMOS, CMOS, eFET, etc., may be used without departing from the scope of the disclosure. The term “MN” indicates an n-type transistor (e.g., NMOS, NPN BJT, etc.) and the term “MP” indicates a p-type transistor (e.g., PMOS, PNP BJT, etc.).

Fig. 4 illustrates a cross-sectional view of a power-supply transient-triggered FinFET (TT-FinFET) gated SCR 400, according to some embodiments of the disclosure. It is pointed out that those elements of Fig. 4 having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

In some embodiments, TT-FinFET gated SCR 400 comprises gated diode 1 401, gated diode 2 402, resistors R1 and R2, and STIs 403a/b/c, where STI 403b separates gated diode 401 from gated diode 402. In some embodiments, gated diode 401 (also referred to as the first gated device) includes source region 405 (i.e., diffusion region) of a first conductivity type (i.e., P+ doped region in this example); drain region 404 (i.e., another diffusion region) of a second conductivity type (i.e., N+ doped region in this example); lightly doped region 406 of the second conductivity type (e.g., N- type Anti-Punch Through-doping (APT), N-well doping, etc.); Intrinsic Fin 407 (e.g., a fully depleted region), Metal Gate 1 408 (e.g., PMOS type gate), and Gate dielectric separating Metal Gate 408 from Intrinsic Fin 407.
[0036] In the various embodiments described here, the terms or labels for source regions and drain regions can be switched. For example, P+ diffusion region 405 can be labeled as the first drain region and N+ diffusion region 404 can be labeled as the first source region. As such, the embodiments are not limited to a certain labeling of the regions, which is why such labels are not inserted in the figures and used in the specification for ease of describing the various embodiments.

[0037] In some embodiments, source and drain regions 405/404 of first gated device 401 are partially separated by lightly doped region 406. In some embodiments, Intrinsic Fin 407 (also referred to as the first fully depleted region) forms a first channel region between source and drain regions 405/404 of first gated device 401.

[0038] In some embodiments, gated diode 402 (also referred to as the second gated device) includes drain region 409 (i.e., diffusion region) of the second conductivity type (e.g., N+ doped region in this example); source region 410 (i.e., another diffusion region) of the first conductivity type (i.e., P+ doped region in this example); lightly doped region 411 of the first conductivity type (e.g., P- type APT, or P-well); Intrinsic Fin 412 (e.g., a fully depleted region), Metal Gate 413 (e.g., NMOS type gate), and Gate dielectric separating Metal Gate 413 from Intrinsic Fin 412. In some embodiments, source and drain regions 410/409 of second gated device 402 are partially separated by lightly doped region 411. In some embodiments, Intrinsic Fin 412 (also referred to as the second fully depleted region) forms a second channel region between source and drain regions 410/409 of second gated diode 402. Although the various embodiments describe the gates as being formed of metal, the gate electrodes can be made from other materials such as classical poly-silicon.

[0039] So as not to obscure the embodiments, the materials used for these various regions are not discussed. Any suitable material used for making the gated diode and STIs may be used.

[0040] In some embodiments, source region 405 of first gated diode 401 is adjacent to drain region 409 of second gated device 402 such that source region 405 is separated by drain region 409 via STI region 403b (also referred to as first ST region 403b). In some embodiments, second STI region 403c is coupled to source region 410 of second gated device 402. In some embodiments, second STI region 403a is coupled to drain region 404 of first gated device 401. Here, Csti is the capacitance between source region 405 and drain region 409 with STI 403b acting as dielectric.
In some embodiments, TT-FinFET gated SCR 400 comprises substrate 414 underlying: first, second, and third STI regions (403b/c/a, respectively), lightly doped region 411, and lightly doped region 406. In some embodiments, substrate 414 is a P- substrate. In some embodiments, contacts are provided to couple the source, drain, and gate regions of gated diodes 401 and 402 to different nodes. Any suitable material may be used for forming the contacts. In this example, in some embodiments, source region 405 of gated diode 401 forms the Anode terminal of the TT-FinFET gated SCR 400 and is coupled to the RF-I/O pad. In some embodiments, drain region 409 of gated diode 402 forms the Cathode terminal of the TT-FinFET gated SCR 400 and is coupled to ground (i.e., VSS).

In some embodiments, an SCR current path is formed from source region 405 of first gated diode 401 through substrate 414 (and under STI 403b) to drain region 409 of second gated diode 402. In some embodiments, a substrate current path is formed from source region 405 of first gated diode 401 through substrate 414 to source region 410 of second gated diode 402. In some embodiments, a trigger current path is formed from source region 405 of first gated device 401 through first fully depleted fin region 407 to drain region 404 of first gated diode 401. The trigger current may flow deeper via the N-type APT region 406, in accordance with some embodiments.

In some embodiments, TT-FinFET SCR 400 provides very fast triggering while keeping the capacitive loading at the RF-IO pin low. Here, the gated diodes 401 and 402 are non-STI gated diodes such that first gated diode 401 from the Anode to VDD represents the trigger path and second gated diode 402 from the Cathode to ground is a regular substrate diode and may be a gated or regular STI diode, in accordance with some embodiments. In some embodiments, the SCR kernel is formed by an STI-bound junction between the N-well and the P-well (e.g., between N-type APT 406 and P-type APT 411). In some embodiments, the inner path length Lac between the Anode and Cathode is minimized to ensure fast turn-on of the SCR.

In some embodiments, the Anode is connected to the voltage-and capacitance-sensitive RF-IO pin. In some embodiments, the capacitive loading is dominated merely by the junction capacitance of the P+/Nwell region (Cj) and the capacitance Cstn of P+ region 405 to N+ region 409 via STI region 403b. In some embodiments, the overlap capacitance Covl,a to Metal Gate 408 at the Anode side provides very little effect to the capacitance seen at the RF-IO pin because the overlap capacitance Covl,a is coupled in series with the overlap capacitance.
Covl,v between Metal Gate 408 and VDD while the latter is coupled in parallel to a high ohmic resistor (e.g., greater than 1kOhm). Another reason for the overlap capacitance Covl,a to Metal Gate 408 at the Anode side Covl,a to provide very little effect to the capacitance seen at the RF-IO pin is that the capacitance of Metal Gate 408 to Intrinsic Fin 407 is highly ineffective due to the depleted fin, in accordance with some embodiments.

[0045] In some embodiments, the trigger speed of TT-FinFET SCR 400 is governed by fast gated diode to VDD and by shallow/short path via P- substrate 414 along shallow STI length Lac. So as not to obscure the embodiment of TT-FinFET SCR 400, dummy gates on either sides of the diodes (i.e., either sides of STI 403a/c) are not shown.

[0046] Fig. 5 illustrates a cross-sectional view of a ground-supply TT-FinFET gated SCR 500, according to some embodiments of the disclosure. It is pointed out that those elements of Fig. 5 having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. In some embodiments, TT-FinFET gated SCR 500 is a complementary version of TT-FinFET gated SCR 400.

[0047] In some embodiments, TT-FinFET gated SCR 500 comprises gated diode 1 501, gated diode 2 502, and STI regions 503a/b/c, where STI region 503b separates gated diode 501 from gated diode 502. In some embodiments, gated diode 501 (also referred to as the first gated diode) includes source region 505 (i.e., diffusion region) of the first conductivity type (i.e., N+ doped region in this example); drain region 504 (i.e., another diffusion region) of the first conductivity type (i.e., P+ doped region in this example); lightly doped region 506 of the first conductivity type (e.g., P- type APT or P-well doping); Intrinsic Fin 507 (e.g., a fully depleted region), Metal Gate 1 508 (e.g., PMOS type gate), and Gate dielectric separating Metal Gate 508 from Intrinsic Fin 507. In some embodiments, source and drain regions 505/504 of first gated diode 501 are partially separated by lightly doped region 506. In some embodiments, Intrinsic Fin 507 (also referred to as the first fully depleted region) forms a first channel region between source and drain regions 505/504 of first gated diode 501.

[0048] In some embodiments, gated diode 502 (also referred to as the second gated diode) includes drain region 509 (i.e., diffusion region) of the first conductivity type (e.g., P+ doped region in this example); source region 510 (i.e., another diffusion region) of the second conductivity type (i.e., N+ doped region in this example); lightly doped region 511 of the second
conductivity type (e.g., N\-type APT); Intrinsic Fin 512 (e.g., a fully depleted region), Metal Gate 513 (e.g., NMOS type gate), and Gate dielectric separating Metal Gate 513 from Intrinsic Fin 512. In some embodiments, source and drain regions 510/509 of second gated diode 502 are partially separated by lightly doped region 511. In some embodiments, Intrinsic Fin 512 (also referred to as the second fully depleted region) forms a second channel region between source and drain regions 510/509 of second gated diode 502.

[0049] So as not to obscure the embodiments, the materials used for these various regions are not discussed. Any suitable material used for making the gated diode and STIs may be used.

[0050] In some embodiments, source region 505 of first gated diode 501 is adjacent to drain region 509 of second gated device 502 such that source region 505 is separated by drain region 509 via STI region 503b (also referred to as first STI region 503b). In some embodiments, second STI region 503c is coupled to source region 510 of second gated diode 502. In some embodiments, second STI region 503a is coupled to drain region 504 of first gated diode 501.

[0051] In some embodiments, TT-FinFET gated SCR 500 comprises substrate 514 (e.g., P- substrate) underlying: first, second, and third STI regions (503b/c/a, respectively), lightly doped region 511, and lightly doped region 506. In some embodiments, contacts are provided to couple the source, drain, and gate regions of gated diodes 501 and 502 to different nodes. In this example, in some embodiments, source region 505 of gated diode 501 forms the Cathode terminal of the TT-FinFET SCR 500 and is coupled to the RF-IO pad. In some embodiments, drain region 509 of gated diode 502 forms the Anode terminal of the TT-FinFET SCR 500 and is coupled to power supply line (VDD). In some embodiments, source region 510 of gated diode 502 is coupled to the power supply line VDD. As such, a well contact is provided. In some embodiments, drain region 504 of gated diode 501 is the SCR trigger tap and is coupled to VSS (i.e., ground).

[0052] Fig. 6 illustrates a circuit model of ESD circuit 600 with power-supply TT-FinFET gated SCR 601 (e.g., SCR 400), ground-supply TT-FinFET gated SCR 602 (e.g., SCR 500), and power supply ESD clamp (e.g., RCMOS) 603, according to some embodiments of the disclosure. It is pointed out that those elements of Fig. 6 having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.
ESD circuit 600 illustrates the wiring of two complementary SCR ESD elements 601 (e.g., TT-FinFET SCR 400) and 602 (e.g., TT-FinFET SCR 500) to obtain full (i.e., for positive/negative stress at RF-IO vs. VDD or VSS at ground) ESD protection at the RF-IO pin. ESD circuit 600 also illustrates RC-controlled Power Clamp (e.g., RCMOS) 603 and parasitic and/or decoupling capacitance between VDD and VSS (not shown). In some embodiments, TT-FinFET gated SCR 601 (also referred as TTPSCR) and TT-FinFET gated SCR 602 (also referred as TTNSCR) are electrically coupled RF-IO pad, VDD pad, and VSS pad.

In some embodiments, Power Clamp 603 is coupled to the VDD line and VSS line. In some embodiments, TT-FinFET gated SCR 601 (e.g., SCR 400) is modeled having NPN and PNP junction devices (shown as NPN and PNP BJT) and gated diode 401 to provide a trigger current path from RF-IO pad to VDD. In some embodiments, TT-FinFET gated SCR 602 (e.g., SCR 500) is modeled having NPN and PNP junction devices (shown as NPN and PNP BJT) and gated diode 501 to provide a trigger current path from RF-IO pad to VSS.

The following section describes the electrical operation during the different kinds of ESD events. In one example, an assumed positive ESD pulse enters at the Anode (which is connected to protect the RF-IO pin or pad) of SCR 601. The current flows first through first gated diode 401 to the VDD supply. In some embodiments, Power Clamp 603, which is used for the supply line ESD protection, first closes the loop and shunts the current to ground (VSS). Second, the current in gated diode 401 forward biases the P+ to N-well junction so that the vertical PNP junction bipolar transistor in TTPSCR 601 turns on. Carriers injected this way into P+ substrate 414 turn on the NPN junction transistor in TTPSCR 601 formed by the N-well 406, P-well 411 and the grounded N+ cathode 409. The SCR structure between the Anode and Cathode conducts to the grounded VSS. As such, transient triggering is achieved, in accordance with some embodiments.

Here, the term “transient triggered” generally refers to the SCR being triggered by the fast voltage/current transients of the ESD pulse, and not triggered by any static means such as avalanche breakdown. This is possible because the chip is generally not powered when the ESD event hits the chip. For example, merely when the chip is in normal operation mode it is obviously powered up. In that case, the SCR will not be triggered by the regular (RF) signals at the IO pad.
If a positive ESD stress at the RF-IO pad is applied versus VDD at ground, merely gated diode 401 will be active, in accordance with some embodiments, conducting the ESD current to VDD. During normal operation of the circuit, VDD is provided, thus making gated diode 401 in the trigger path reverse biased, and hence in blocking state, such that the RF signal on RF-IO pin can be passed onto the RF receiver (not shown).

Assuming a positive stress at the RF-IO pin vs. VSS at ground, in some embodiments, the fast CDM ESD current may be mainly shunted via gated diode 401 to VDD and via Power Clamp 603 to VSS, whereas the longer HBM pulse is discharged via TTPSCR 601 directly to VSS. In some embodiments, as soon as the SCR turns on during CDM, the CDM pulse is discharged via SCR 601. In some embodiments, for negative stress at the RF-IO pad, the complementary SCR (TTNSCR) 602 becomes active.

Fig. 7 illustrates layout floorplan 1500 of a power-supply TT-FinFET gated SCR 400 of Fig. 4, according to some embodiments of the disclosure. It is pointed out that those elements of Fig. 7 having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

In some embodiments, tiles of gated diodes are formed and concatenated with one another to achieve a small layout floorplan with horizontal fin orientation. For example, linear checkerboard-like arrangements are made for the gated diodes. Here, gated diodes are in the X-direction (i.e., direction of the fins).

Layout floorplan 700 shows NWELL region 406 coupled in series with PWELL region 411 such that TT-FinFET SCR 400 is in linear checkerboard-like arrangement. In some embodiments, in NWELL region 406, N+ and P+ diffusion regions 404 and 405, respectively, run orthogonal to fins 407 in their respective polysilicon regions, as shown. In some embodiments, in each polysilicon region, a layer of N+ 404 and P+ diffusion 405 runs.

In some embodiments, in PWELL region 411, N+ and P+ diffusion regions 409 and 410, respectively, run orthogonal to fins 412 in their respective polysilicon regions, as shown. The dotted region “X-section” is the cross-section shown in Fig. 4, in accordance with some embodiments.

Fig. 8 illustrates a smart device or a computer system or a SoC (System-on-Chip) 2100 having one or more ESD circuits with TT-FinFETs, according to some embodiments. It is pointed out that those elements of Fig. 8 having the same reference numbers (or names) as the
elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0064] Fig. 8 illustrates a block diagram of an embodiment of a mobile device in which flat surface interface connectors could be used. In some embodiments, computing device 2100 represents a mobile computing device, such as a computing tablet, a mobile phone or smartphone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain components are shown generally, and not all components of such a device are shown in computing device 2100.

[0065] In some embodiments, where each block shown in computing device 2100 is an individual chip, ESD circuits with TT-FinFETs are provided at the pads (coupled to pins) of the individual chip. In some embodiments, where the SoC is a single large chip, ESD circuits with TT-FinFETs are provided at the pads (coupled to the pins) of the SoC.

[0066] In one embodiment, processor 2110 (and/or processor 2190) can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 2110 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The various embodiments of the present disclosure may also comprise a network interface within 2170 such as a wireless interface so that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant.

[0067] The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting the computing device 2100 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0068] In one embodiment, computing device 2100 includes audio subsystem 2120, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions can be integrated into computing device 2100, or connected to the computing device 2100. In one embodiment, a user interacts with the computing device 2100 by providing audio commands that are received and processed by processor 2110.
Display subsystem 2130 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device 2100. Display subsystem 2130 includes display interface 2132, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 2132 includes logic separate from processor 2110 to perform at least some processing related to the display. In one embodiment, display subsystem 2130 includes a touch screen (or touch pad) device that provides both output and input to a user.

I/O controller 2140 represents hardware devices and software components related to interaction with a user. I/O controller 2140 is operable to manage hardware that is part of audio subsystem 2120 and/or display subsystem 2130. Additionally, I/O controller 2140 illustrates a connection point for additional devices that connect to computing device 2100 through which a user might interact with the system. For example, devices that can be attached to the computing device 2100 might include microphone devices, speaker or stereo systems, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

As mentioned above, I/O controller 2140 can interact with audio subsystem 2120 and/or display subsystem 2130. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the computing device 2100. Additionally, audio output can be provided instead of, or in addition to display output. In another example, if display subsystem 2130 includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 2140. There can also be additional buttons or switches on the computing device 2100 to provide I/O functions managed by I/O controller 2140.

In one embodiment, I/O controller 2140 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in the computing device 2100. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

In one embodiment, computing device 2100 includes power management 2150 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 2160 includes memory devices for storing information in
computing device 2100. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory subsystem 2160 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of the computing device 2100.

[0074] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 2160) for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium (e.g., memory 2160) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[0075] Connectivity 2170 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable the computing device 2100 to communicate with external devices. The computing device 2100 could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[0076] Connectivity 2170 can include multiple different types of connectivity. To generalize, the computing device 2100 is illustrated with cellular connectivity 2172 and wireless connectivity 2174. Cellular connectivity 2172 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity (or wireless interface) 2174 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication.
Peripheral connections 2180 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that the computing device 2100 could both be a peripheral device ("to" 2182) to other computing devices, as well as have peripheral devices ("from" 2184) connected to it. The computing device 2100 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on computing device 2100. Additionally, a docking connector can allow computing device 2100 to connect to certain peripherals that allow the computing device 2100 to control content output, for example, to audiovisual or other systems.

In addition to a proprietary docking connector or other proprietary connection hardware, the computing device 2100 can make peripheral connections 1680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.
While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

For example, an apparatus comprising: a first shallow trench isolation (STI) region; a first gated FinFET device including a source region of a first conductivity type; and a second gated FinFET device including a drain region of a second conductivity type, wherein the source region of the first gated FinFET device is adjacent to the drain region of the second gated FinFET device such that the source region of the first gated FinFET device is separated by the drain region of the second gated FinFET device via the first STI region.

In some embodiments, the first gated FinFET device further includes a drain region of the second conductivity type, and wherein the source and drain regions of the first gated FinFET device are partially separated by a lightly doped region of the second conductivity type. In some embodiments, the lightly doped region of the second conductivity type is one of an anti-punch through doping (APT) or a well of the second conductivity type. In some embodiments, the second gated FinFET device further includes a source region of the first
conductivity type, and wherein the source and drain regions of the second gated FinFET device are partially separated by a lightly doped region of the first conductivity type.

[0086] In some embodiments, the lightly doped region of the first conductivity type is one of an anti-punch through doping (APT) or a well doping of the first conductivity type. In some embodiments, the apparatus comprises a second STI region coupled to the source region of the second gated FinFET device. In some embodiments, the apparatus comprises: a third STI region coupled to the drain region of the first gated FinFET device. In some embodiments, the apparatus comprises a substrate underlying: the first, second, and third STI regions, the lightly doped region of the first conductivity type, and the lightly doped region of the second conductivity type.

[0087] In some embodiments, a silicon controlled rectifier (SCR) current path is formed from the source region of the first gated FinFET device through the substrate to the drain region of the second gated FinFET device. In some embodiments, a substrate current path is formed from the source region of the first gated FinFET device through the substrate to the source region of the second gated FinFET device. In some embodiments, the apparatus comprises a first fully depleted region coupled to the lightly doped region of the second conductivity type, wherein the first fully depleted region forms a first channel region between the source and drain regions of the first gated FinFET device.

[0088] In some embodiments, a trigger current path is formed from the source region of the first gated FinFET device through the first fully depleted region to the drain region of the first gated FinFET device. In some embodiments, the apparatus comprises a second fully depleted region coupled to the lightly doped region of the first conductivity type, and wherein the second fully depleted region forms a second channel region between the source and drain regions of the second gated FinFET device. In some embodiments, the first conductivity type is a p-type and the source region of the first gated FinFET device is coupled to an anode terminal, and the second conductivity type is an n-type and the drain region of the second gated FinFET device is coupled to a cathode terminal, wherein the drain region of the first gated FinFET device is coupled to a trigger terminal.

[0089] In some embodiments, the anode terminal is coupled to an Input-Output (I/O) pad, wherein the cathode terminal is coupled to ground, and wherein the trigger terminal is coupled to a power supply. In some embodiments, the first conductivity type is an n-type and the source
region of the first gated FinFET device is coupled to a cathode terminal, and the second conductivity type is a p-type and the drain region of the second gated FinFET device is coupled to an anode terminal, wherein the drain terminal of the first gated device is coupled to a trigger terminal. In some embodiments, the anode terminal is coupled to a power supply, wherein the cathode terminal is coupled to an Input-Output (I/O) pad, and wherein the trigger terminal is coupled to ground.

[0090] In another example, a system is provided which comprises: a integrated circuit including: an radio-frequency (RF) input-output (I/O) pad; and an electrostatic discharge (ESD) device coupled to the RF I/O pad, wherein the ESD device comprises an apparatus according to the apparatus described above; and an interface allowing the integrated circuit to communicate with another device.

[0091] In another example, an apparatus is provided which comprises: a power supply node; a ground supply node; an input-output (IO) signal node; a first silicon controlled rectifier (SCR) coupled to the power supply node and the IO signal node; and a second SCR coupled in series with the first SCR, the second SCR coupled to the IO signal node and the ground supply node, the second SCR comprising: a first shallow trench isolation (STI) region; a first gated FinFET device including a source region of a first conductivity type; and a second gated FinFET device including a drain region of a second conductivity type, wherein the source region of the first gated FinFET device is adjacent to the drain region of the second gated FinFET device such that the source region of the first gated FinFET device is separated by the drain region of the second gated FinFET device via the first STI region.

[0092] In some embodiments, the first gated FinFET device further includes a drain region of the second conductivity type, and wherein the source and drain regions of the first gated FinFET device are partially separated by a lightly doped region of the second conductivity type. In some embodiments, the lightly doped region of the second conductivity type is one of an anti-punch through doping (APT) or a well of the second conductivity type. In some embodiments, the second gated FinFET device further includes a source region of the first conductivity type, and wherein the source and drain regions of the second gated FinFET device are partially separated by a lightly doped region of the first conductivity type.

[0093] In some embodiments, the first conductivity type is a p-type and the source region of the first gated FinFET device is coupled to an anode terminal, and the second conductivity
type is an n-type and the drain region of the second gated FinFET device is coupled to a cathode terminal, wherein the drain region of the first gated FinFET device is coupled to a trigger terminal. In some embodiments, the anode terminal is coupled to the IO signal node, wherein the cathode terminal is coupled to the ground supply node, and wherein the trigger terminal is coupled to the power supply node.

[0094] In some embodiments, the first conductivity type is an n-type and the source region of the first gated FinFET device is coupled to a cathode terminal, and the second conductivity type is a p-type and the drain region of the second gated FinFET device is coupled to an anode terminal, wherein the drain terminal of the first gated device is coupled to a trigger terminal. In some embodiments, the anode terminal is coupled to the power supply node, wherein the cathode terminal is coupled to IO signal node, and wherein the trigger terminal is coupled to the ground supply node.

[0095] In another example, a system is provided which comprises: a integrated circuit including: an radio-frequency (RF) input-output (I/O) pad; and an electrostatic discharge (ESD) device coupled to the RF I/O pad, wherein the ESD device comprises an apparatus according to the apparatus described above; and an interface allowing the integrated circuit to communicate with another device.

[0096] In another example, a method is provided which comprises: providing a power supply via a power supply node; providing a ground supply via a ground supply node; providing an radio-frequency (RF) signal at an input-output (IO) signal node; and providing electrostatic discharge (ESD) protection when the RF signal has an ESD, wherein the ESD protection is provided by an apparatus which includes: a first silicon controlled rectifier (SCR) coupled to the power supply node and the IO signal node; and a second SCR coupled in series with the first SCR, the second SCR coupled to the IO signal node and the ground supply node, the second SCR comprising: a first shallow trench isolation (STI) region; a first gated FinFET device including a source region of a first conductivity type; and a second gated FinFET device including a drain region of a second conductivity type, wherein the source region of the first gated FinFET device is adjacent to the drain region of the second gated FinFET device such that the source region of the first gated FinFET device is separated by the drain region of the second gated FinFET device via the first STI region.
[0097] In some embodiments, the first gated FinFET device further includes a drain region of the second conductivity type, and wherein the source and drain regions of the first gated FinFET device are partially separated by a lightly doped region of the second conductivity type.

[0098] In another example, an apparatus is provided which comprises: means for providing a power supply via a power supply node; means for providing a ground supply via a ground supply node; means for providing an radio-frequency (RF) signal at an input-output (IO) signal node; and means for providing electrostatic discharge (ESD) protection when the RF signal has an ESD, wherein the ESD protection is provided by an apparatus which includes: a first silicon controlled rectifier (SCR) coupled to the power supply node and the IO signal node; and a second SCR coupled in series with the first SCR, the second SCR coupled to the IO signal node and the ground supply node, the second SCR comprising: a first shallow trench isolation (STI) region; a first gated FinFET device including a source region of a first conductivity type; and a second gated FinFET device including a drain region of a second conductivity type, wherein the source region of the first gated FinFET device is adjacent to the drain region of the second gated FinFET device such that the source region of the first gated FinFET device is separated by the drain region of the second gated FinFET device via the first STI region.

[0099] In some embodiments, the first gated FinFET device further includes a drain region of the second conductivity type, and wherein the source and drain regions of the first gated FinFET device are partially separated by a lightly doped region of the second conductivity type.

[0100] In another example, a system is provided which comprises: a integrated circuit including: an radio-frequency (RF) input-output (I/O) pad; and an electrostatic discharge (ESD) device coupled to the RF I/O pad, wherein the ESD device comprises an apparatus according to the apparatus described above; and an interface allowing the integrated circuit to communicate with another device.

[0101] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.
CLAIMS

We claim:

1. An apparatus comprising:
   a first shallow trench isolation (STI) region;
   a first gated FinFET device including a source region of a first conductivity type; and
   a second gated FinFET device including a drain region of a second conductivity type,
   wherein the source region of the first gated FinFET device is adjacent to the drain region of
   the second gated FinFET device such that the source region of the first gated FinFET device
   is separated by the drain region of the second gated FinFET device via the first STI region.

2. The apparatus of claim 1, wherein the first gated FinFET device further includes a drain
   region of the second conductivity type, and wherein the source and drain regions of the first
   gated FinFET device are partially separated by a lightly doped region of the second
   conductivity type.

3. The apparatus of claim 2, wherein the lightly doped region of the second conductivity type is
   one of an anti-punch through doping (APT) or a well of the second conductivity type.

4. The apparatus of claim 2, wherein the second gated FinFET device further includes a source
   region of the first conductivity type, and wherein the source and drain regions of the second
   gated FinFET device are partially separated by a lightly doped region of the first conductivity
   type.

5. The apparatus of claim 4, wherein the lightly doped region of the first conductivity type is
   one of an anti-punch through doping (APT) or a well doping of the first conductivity type.

6. The apparatus of claim 4 comprises a second STI region coupled to the source region of the
   second gated FinFET device.

7. The apparatus of claim 6 comprises a third STI region coupled to the drain region of the first
   gated FinFET device.
8. The apparatus of claim 7 comprises a substrate underlying: the first, second, and third STI regions, the lightly doped region of the first conductivity type, and the lightly doped region of the second conductivity type.

9. The apparatus of claim 8, wherein a silicon controlled rectifier (SCR) current path is formed from the source region of the first gated FinFET device through the substrate to the drain region of the second gated FinFET device.

10. The apparatus of claim 8, wherein a substrate current path is formed from the source region of the first gated FinFET device through the substrate to the source region of the second gated FinFET device.

11. The apparatus of claim 2 comprises a first fully depleted region coupled to the lightly doped region of the second conductivity type, wherein the first fully depleted region forms a first channel region between the source and drain regions of the first gated FinFET device.

12. The apparatus of claim 11, wherein a trigger current path is formed from the source region of the first gated FinFET device through the first fully depleted region to the drain region of the first gated FinFET device.

13. The apparatus of claim 4 comprises a second fully depleted region coupled to the lightly doped region of the first conductivity type, and wherein the second fully depleted region forms a second channel region between the source and drain regions of the second gated FinFET device.

14. The apparatus of claim 4, wherein:
   
   the first conductivity type is a p-type and the source region of the first gated FinFET device is coupled to an anode terminal, and
   
   the second conductivity type is an n-type and the drain region of the second gated FinFET device is coupled to a cathode terminal,
wherein the drain region of the first gated FinFET device is coupled to a trigger terminal.

15. The apparatus of claim 14, wherein the anode terminal is coupled to an Input-Output (I/O) pad, wherein the cathode terminal is coupled to ground, and wherein the trigger terminal is coupled to a power supply.

16. The apparatus of claim 4, wherein:
   the first conductivity type is an n-type and the source region of the first gated FinFET device is coupled to a cathode terminal, and
   the second conductivity type is a p-type and the drain region of the second gated FinFET device is coupled to an anode terminal,
   wherein the drain terminal of the first gated device is coupled to a trigger terminal.

17. The apparatus of claim 16, wherein the anode terminal is coupled to a power supply, wherein the cathode terminal is coupled to an Input-Output (I/O) pad, and wherein the trigger terminal is coupled to ground.

18. An apparatus comprising:
   a power supply node;
   a ground supply node;
   an input-output (IO) signal node;
   a first silicon controlled rectifier (SCR) coupled to the power supply node and the IO signal node; and
   a second SCR coupled in series with the first SCR, the second SCR coupled to the IO signal node and the ground supply node, the second SCR comprising:
   a first shallow trench isolation (STI) region;
   a first gated FinFET device including a source region of a first conductivity type; and
   a second gated FinFET device including a drain region of a second conductivity type, wherein the source region of the first gated FinFET device is adjacent to the drain region of the second gated FinFET device such that the source
region of the first gated FinFET device is separated by the drain region of the second gated FinFET device via the first STI region.

19. The apparatus of claim 18, wherein the first gated FinFET device further includes a drain region of the second conductivity type, and wherein the source and drain regions of the first gated FinFET device are partially separated by a lightly doped region of the second conductivity type.

20. The apparatus of claim 19, wherein the lightly doped region of the second conductivity type is one of an anti-punch through doping (APT) or a well of the second conductivity type.

21. The apparatus of claim 19, wherein the second gated FinFET device further includes a source region of the first conductivity type, and wherein the source and drain regions of the second gated FinFET device are partially separated by a lightly doped region of the first conductivity type.

22. The apparatus of claim 21, wherein:
   the first conductivity type is a p-type and the source region of the first gated FinFET device is coupled to an anode terminal, and
   the second conductivity type is an n-type and the drain region of the second gated FinFET device is coupled to a cathode terminal,
   wherein the drain region of the first gated FinFET device is coupled to a trigger terminal.

23. The apparatus of claim 22, wherein the anode terminal is coupled to the IO signal node, wherein the cathode terminal is coupled to the ground supply node, and wherein the trigger terminal is coupled to the power supply node.

24. The apparatus of claim 21, wherein:
   the first conductivity type is an n-type and the source region of the first gated FinFET device is coupled to a cathode terminal, and
the second conductivity type is a p-type and the drain region of the second gated FinFET device is coupled to an anode terminal,
wherein the drain terminal of the first gated device is coupled to a trigger terminal.

25. The apparatus of claim 24, wherein the anode terminal is coupled to the power supply node, wherein the cathode terminal is coupled to IO signal node, and wherein the trigger terminal is coupled to the ground supply node.

26. A system comprising:
   a integrated circuit including:
      an radio-frequency (RF) input-output (I/O) pad; and
      an electrostatic discharge (ESD) device coupled to the RF I/O pad, wherein the ESD device comprises an apparatus according to any one of claims 1 to 17; and
      an interface allowing the integrated circuit to communicate with another device.
Fig. 1
(prior art)

Fig. 2
(prior art)
Fig. 4
Fig. 8
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
H01L 29/78(2006.01)i, H01L 21/762(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 27/06; H01L 23/62; H01L 21/332; H02H 9/04; H01L 29/74; H01L 27/092; H01L 21/762

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic database consulted during the international search (name of database and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: FinFET, silicon controlled rectifier, electrostatic discharge, STI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
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| X        | US 2015-0255459 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 10 September 2015  
See abstract, paragraphs [0002], [0043]-[0097] and figures 1A-17B. | 1                    |
| Y        | A                                                                               | 26                   |
|          | US 2010-0390603 A1 (YASUYUKI MORIHITA) 00 December 2010  
See abstract, paragraphs [0019]-[0023] and figure 2. | 26                   |
| A        | US 2010-0294457 A1 (BART SORGELOOS et al.) 21 October 2010  
See abstract, paragraphs [0027]-[0029] and figures 5, 5A. | 1-26                 |
See abstract, paragraphs [0025]-[0036] and figures 1A-4. | 1-26                 |
See abstract, paragraphs [0089]-[1009] and figures 1A-2. | 1-26                 |

☐ Further documents are listed in the continuation of Box C.  ☒ See patent family annex.

* Special categories of cited documents:
  "A" document defining the general state of the art which is not considered to be of particular relevance
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  "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
  "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
  "&" document member of the same patent family

Date of the actual completion of the international search  
20 July 2016 (20.07.2016)

Date of mailing of the international search report  
21 July 2016 (21.07.2016)

Name and mailing address of the ISA/KR  
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Form PCT/ISA/210 (second sheet) (January 2015)
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