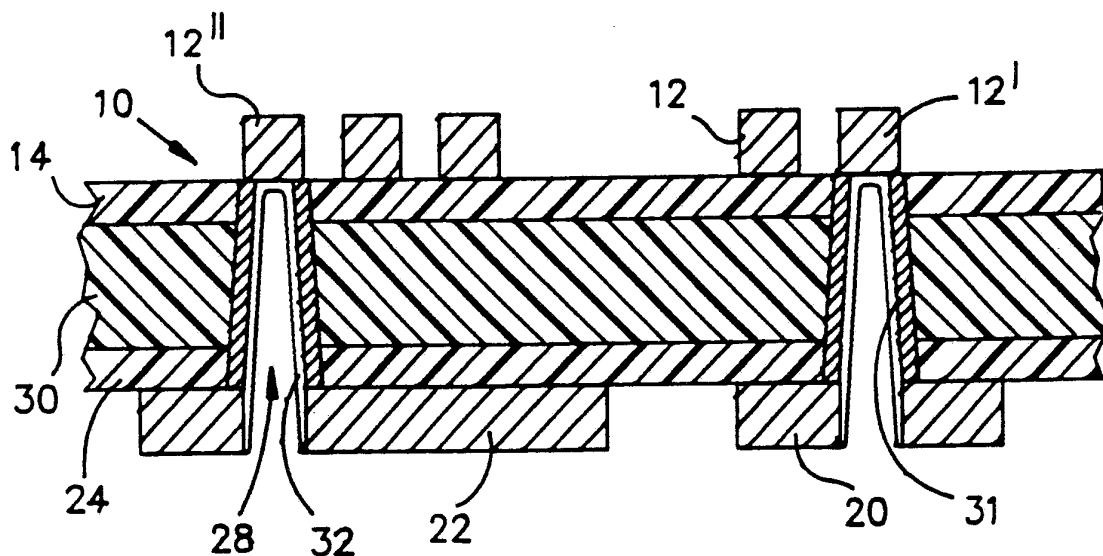




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(54) Title: GTAB MANUFACTURING PROCESS AND THE PRODUCT PRODUCED THEREBY



(57) Abstract

An electronic circuit (10) and a process of manufacture are provided. A dielectric polymer (30) supports first (12) and second (20, 22) conductive planes. The polymer (30) is selected to become electrically conductive by pyrolysis. Vias (28) are formed by a process which generates localized regions (31) of elevated temperature. The via walls (31) become electrically conductive while the remainder of the polymer (30) retains a high dielectric value. A conductive metal (32) is deposited on the conductive walls (31) and electrically interconnects conductive planes (12 and 20, 22).

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"GTAB MANUFACTURING PROCESS
AND THE PRODUCT PRODUCED THEREBY"

The invention relates to the manufacture of
5 interconnect circuits having a plurality of electrically
interconnected conductive planes. More particularly,
the invention relates to the manufacture of a tape
automated bonding leadframe assembly having a signal
plane and ground and/or power planes.

10 Packages to house microelectronic devices, such as
silicon semiconductor integrated circuits, include a
housing to encapsulate the device. A leadframe passes
through the housing and transmits electrical impulses
between external circuitry and the device.

15 The leadframe is usually an iron/nickel alloy or a
copper alloy strip about .25mm (10 mils) thick.
Individual leads are formed by etching or stamping. The
lead widths and the spacing between the leads is on the
order of the lead thickness, about .25mm (10 mils).

20 Thin, typically .025mm (1 mil) diameter, bonding wires
electrically connect the integrated circuit device to
the leadframe. The bonding wires are manufactured from
gold, aluminum or an aluminum alloy. The wires are
bonded to small bonding pads on the surface of the
25 device by a process such as ultrasonic bonding or
thermocompression bonding.

As semiconductor devices become more complex,
additional electrical connections are required. A
conventional leadframe has limited lead density. The
30 width of the leads must be about equal to the thickness
of the strip due to limitations in stamping and
etching. Also, the bonding wires require approximately
a .076mm x .076mm (3 x 3 mil) bonding pad with .15mm (6
mil) spacing between bonding pads center lines.

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Further, in high speed VLSI circuits, lead impedance is a problem at signal frequencies above about 50 MHz. The round, irregular spaced wires introduce large lead inductance and lead-to-lead capacitance which result in
5 propagation delay and signal distortion.

One solution to the limitations of conventional wire bonding is TAB leads. TAB is an acronym for tape automated bonding leadframe assemblies. TAB utilizes a metal tape which is usually wrought copper or
10 electrodeposited copper and may be plated with a second metal such as gold, nickel or tin. The tape is formed into a plurality of individual sites. Each site defines a plurality of narrow leads arranged to extend outwardly from the integrated circuit device. The inner lead
15 portions of the tape are bonded to the bonding pads of the integrated circuit and the outer lead portions are bonded to a leadframe, a circuit board or other external circuitry.

TAB is routinely capable of .051mm x .051mm (2 mil x
20 2 mil) bonding pads with .010mm (4 mil) center line. TAB leadframes are generally characterized by shorter lead lengths, larger cross sectional areas and more uniform spacing between leads than wire bonding systems. Lead density and electrical performance are
25 improved in high speed applications by using TAB leads.

There are three general forms of TAB construction. First is the single layer or all metal construction. Second is a two-layer construction comprising a metal layer with a dielectric backing. Third is a three-layer
30 construction comprising a metal layer adhesively bonded to a dielectric backing. The dielectric may be any with suitable properties for TAB processing and subsequent packaging. One exemplary dielectric is a polyimide, such as KAPTON manufactured by Dupont with a thickness
35 of from about .051mm to about .13mm (2 - 5 mils).

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The metal foil layer is typically copper or a copper alloy with a thickness from about .013mm to about .15mm (1/2 to 6 mils) thick. Leads are patterned in the foil by photolithography. The leads are generally about
5 .051mm (2 mils) wide and .051mm x .036mm (2 x 1.4 mil) lead cross sections are common.

Most leads are for transmitting electrical signals. Others supply power or provide a ground source. Better electrical performance is obtained by
10 providing a TAB leadframe having two metal layers, called a GTAB. The first metal layer is patterned into leads dedicated to transmitting electrical signals and called the signal plane. The second metal layer is patterned into circuits for ground and power and called
15 the ground or power plane.

The two-metal layer circuit may be fabricated by either two or three-layer TAB. A two metal layer circuit may have two conductive layers bonded directly to the dielectric layer or an adhesive may bond the
20 layers. United States Patent Nos. 4,634,631 and 4,647,508 disclose multiple metal layer flexible circuits with an adhesive. A two metal layer tape having crossover leads is disclosed in U.S. Patent No. 4,801,999.

25 Electrical interconnects between the conductive layers of a GTAB are much smaller, typically on the order of .051mm to .13mm (2 to 5 mils), than the typical .51mm to 1.0mm (20 to 40 mil) diameter vias found in printed circuit boards. The reduced diameter vias are a
30 direct consequence of the increased circuit densities found on electrical packages such as GTAB which are more proximate to the integrated circuit. Rather than .51mm (20 mil) wide circuit traces separated by .51mm (20 mil) spaces as in printed circuit applications, GTAB
35 leadframes are typified by .051mm (2 mil) wide circuit traces separated by .051mm (2 mils) wide spaces.

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Conventional multilayer printed circuit board manufacturing processes are not satisfactory for GTAB manufacture. Printed circuit board vias are formed by drilling or punching. The smaller vias required for GTAB
5 cannot be reliably fashioned by these methods. The space limitations inherent in a GTAB further encourage the use of blind vias rather than through holes. The blind vias are generally open to the ground plane and terminate at an interior surface of the signal plane.

10 Once a via is formed through the dielectric layer of either a printed circuit or GTAB, the via must be made electrically conductive. Through-holes for printed circuit boards are usually made electrically conductive by electroless copper deposition. A thin microlayer of
15 copper is deposited onto the walls of the holes bridging the exposed conductive layers and establishing electrical conductivity. The thin conductive layer is built up to a desired thickness by electroplating.

The electroless process has several
20 disadvantages. The process is slow. Multiple treatment baths are required. A catalyst, such as palladium/tin, may require extensive waste treatment. The baths are sensitive to contamination. The multiplicity of rinse baths require large amounts of water and the disposal of
25 the chemical waste.

Another means to form conductive vias is disclosed in United States Patent No. 4,631,117 and is known as the BLACKHOLE™ process. The BLACKHOLE™ process, developed by Olin Hunt Specialty Products, Inc., of Palisades Park,
30 New Jersey, United States of America, forms a dispersion of carbon black in a liquid medium with a surfactant. The dispersion is applied to the surfaces of the nonconducting layer. The liquid medium is removed leaving a carbon black layer which is then coated with a
35 conductive material. Coating is by either electroless or

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electrolytic means as disclosed in U.S. Patent No. 4,684,560. The application of the BLACKHOLE™ process to printed circuit boards is disclosed in U.S. Patent Nos. 4,619,741, 4,631,117 and 4,684,560. The use of the
5 BLACKHOLE™ process for the manufacture of a GTAB is disclosed in International Application Serial No. PCT/US90/01413, published October 18, 1990.

The micromachining of polymers including polyimide
10 be excimer laser is known. Excimer lasers radiating at 193, 248 and 308 nm are available. A large number of dielectric materials, including polyimides, absorb strongly at these wavelengths. At fluences above a threshold energy for ablation, the materials are essentially gassified. The organic material is reduced
15 to carbon soot, short order organic fragments and, in the presence of oxygen, to combustive by-products.

Polyimides and certain other polymers may become electrically conductive by pyrolysis. The resistivity of KAPTON is reduced from in excess of 10^{18} ohm
20 centimeters to 7.5 ohm centimeters by heating to 710°C for two hours in a vacuum. Heat treating a polyimide to above about 500°C by a means which does not lead to sample volatilization increases the carbon concentration on the surface thereby increasing electrical conductivity.

25 The ability to partially carbonize polyimide has been used to manufacture components. U.S. Patent No. 4,286,250 discloses forming a resistor by selectively applying heat to a homogeneous polyimide substrate. The resistor compares favorably with conventional carbon
30 resistors. U.S. Patent No. 4,855,985 discloses using selective pyrolysis of a polyimide disk for digital storage of information. The information written into the disk may be read using a conventional transmission approach by a laser or electrically by a capacitance
35 detecting stylus.

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Nothing in the prior art known to the inventors suggests that by selectively carbonizing the dielectric in situ during the via forming process, vias amenable to electrolytic deposition may be formed without additional surface preparation. Surprisingly, it has been found that carbonized vias may be electroplated without additional pre-treatment. Further, the adhesive which may be used to bond the dielectric to conductive layers also becomes electrically conductive by the process of the invention.

Accordingly, it is an object of the invention to provide a multilayer circuit having a plurality of conductive planes. The conductive planes are interconnected by conductive vias formed in a dielectric. It is a feature of the invention that selective regions of the dielectric are made amenable to the deposition of a conductive metal by localized heating. Yet another feature of the invention is that either a laser or mechanical means may be used to provide localized heating. It is an advantage of the invention that the vias become suitable for electrolytic deposition when formed. Yet another advantage of the invention is that the number of steps required to form conductive vias is minimized. Still another advantage of the invention is that chemical wastes are minimized by eliminating the need for electroless copper deposition and the associated chemistries. Yet another advantage of the invention is that through-hole, blind and closed vias may all be formed. The process is suitable for forming conductive vias of a wide range of diameters. As such, the process may be used for both GTAB and printed circuit boards. Still a further advantage of the invention is that direct writing of circuit traces on the surface of the polyimide is possible.

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In accordance with the invention, there is provided an electronic circuit. The circuit has at least two conductive planes. A polymer layer is disposed between the conductive planes. The polymer is selected
5 to be a dielectric which may be made electrically conducted in situ. At least one via interconnecting the first and second conductive plane is formed in the polymer. The polymer is made electrically conductive along the walls of the vias.

10 The above stated objects, features and advantages will become more apparent from the specification and drawings which follow.

Figure 1 shows in planar view the signal plane of a GTAB in accordance with the invention.

15 Figure 2 shows in planar view the ground plane of a GTAB in accordance with the invention.

Figure 3 shows in cross-sectional representation a GTAB having electrically conductive blind vias formed in accordance with the invention.

20 Figures 4-5 show in cross-sectional representation an assembly process in accordance with a first embodiment of the invention.

Figures 6-8 show an assembly process in accordance with a second embodiment of the invention.

25 Figures 9-11 show an assembly process in accordance with a third embodiment of the invention.

Figures 12-13 show is cross-sectional representations an additive process for manufacturing multilayer circuits according to the process of the
30 invention.

Figure 14 shows a photomicrograph of a conductive via formed according to the processes of the invention.

Figures 1 through 3 illustrate in planar and cross-sectional representations the construction of a
35 GTAB in accordance with the invention. While the

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Figures illustrate a GTAB and the process will be described in terms of that circuit, the structure and processes are applicable to any multilayer circuit including but not limited to printed circuit boards.

5 Figure 1 illustrates in planar view the signal plane of a five layer GTAB 10. The signal plane is patterned into a plurality of circuit traces 12 bonded by an adhesive 14 to a dielectric carrier. The circuit traces 12 are as narrow as possible to maximize lead
10 density. .051mm (2 mil) wide circuit traces separated by .051mm (2 mil) wide spaces are available by current manufacturing techniques. In the future, closer spaced leads will become more common. The process of the invention is also applicable to finer line geometries.

15 The circuit traces 12 of the GTAB 10 contain inner leads 16 which extend in cantilever fashion into a previously formed personality window 17. An integrated circuit device (not shown) is positioned within the personality window 17 and contains input/output pads.
20 The input/output pads are bonded to the inner leads 16. The opposite ends of the circuit traces 12 form outer leads 18 for bonding to a leadframe or external circuitry.

Figure 2 illustrates in planar view, the power and ground plane (conventionally referred as to "ground
25 plane") of the five layer GTAB 10 illustrated in Figure 1. The ground plane is patterned into ground circuits 20 and power circuits 22 bonded to the flexible die electric carrier by a second adhesive layer 24. The ground circuits 20 and power circuits 22 are wider than the
30 circuit traces 12 of Figure 1. Typically, the widths of the ground and power circuits are over .25mm (10 mils) and may occupy the entire ground plane. Usually, all outer leads 18 originate with the signal plane and portions of leads 12. However, it is within the scope of
35 the invention for outer leads to originate from the ground plane as well.

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Conductive apertures 28 originate at the ground circuit 20 or the power circuit 22 and extend through the nonconductive layers of. The conductive apertures interconnect the circuits of the ground plane to the
5 circuits of the signal plane.

Figure 3 illustrates in cross-sectional representation the five layer GTAB of Figures 1 and 2 as viewed along cross section line 3--3. The GTAB 10 is supported by a dielectric carrier layer 30. The carrier
10 layer is any electrically nonconductive material suitable for use in circuits TAB circuits are frequently provided in a reel-to-reel fashion and the dielectric is preferably flexible. Signal and power plane circuitry are generally formed by photolithography. The dielectric
15 30 should be inert to the chemicals used for photolithography. Lamination of the signal plane and ground plane conductive layers may require a temperature of about 180°C. The carrier should not degrade or decrease in resistivity at these temperatures.
20 Additionally, the dielectric should be hydrophobic so that it will not absorb water and develop variable electrical characteristics.

In accordance with the invention, the dielectric carrier layer is preferably selected to be a polymer.
25 The polymer should have a low dielectric constant to allow high electric transmission speeds. The polymer is further selected to be one which may be made amenable to the deposition of a conductive coating by electrolytic means in situ. "In situ" in the context of this
30 application means within its original position. The polymer becomes amenable to deposition without the addition of a second material or additional processing steps.

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Preferred dielectrics are polymers having backbones of recurring aromatic units that formed non-volatile carbonaceous residues upon pyrolysis. More preferably, aromatic polyimides, aromatic polyamides, 5 polybenzimidazoles, polybenzoxazoles, polybenzothiazoles, polyoxadiazoles, polytriazoles, polyimidazopyrrolones, aromatic polysulfones, and polyphenylene sulfide are selected. The most preferred material is polyimide.

The first 14 and second 24 adhesive layers are 10 disposed on opposing sides of the dielectric carrier layer 30 as shown in Fig. 3. The adhesive layers are optional and the use is dependent on the method of circuit manufacture. When a metal foil is laminated to a dielectric carrier, the adhesive layers are used. When 15 copper is deposited on the carrier layer by a chemical deposition process or when the dielectric is applied to the copper foil as a dispersion in a solvent which subsequently evaporates, the adhesive layers may be omitted. The processes and products of the invention are 20 equally applicable to circuits with and without the adhesive layers.

Any adhesive which is sufficiently flexible and has suitable chemical and thermal properties as detailed above for the carrier layer may be utilized. Preferably, 25 the adhesive also forms a carbonaceous surface when exposed to heat. However, since the adhesive layers 14, 24 are thin a conductive metal deposited on the conductive surfaces of the dielectric 30 and conductive metal layers 12,20,22 will bridge the adhesive layer.

30 The adhesive layers are typically less than about .025mm (1.0 mil) thick and preferably from about .013mm to about .020mm (.5 to .8 mils). One suitable adhesive is phenolic butyral.

35 Circuitry 12, 20, 22 is formed from a conductive metal foil. Copper and copper alloys with a thickness of from about .013mm to about .15mm (.5 to 6 mils) are

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suitable. Preferably, the copper thickness is from about .018mm to about .036mm (.7 to 1.4 mils). Copper is preferred because it has high electrical conductivity, good ductility and is easy to etch. Among the most
5 preferred copper alloys are C110 (electrolytic tough pitch copper having a nominal composition of 99.90% by weight copper minimum, 0.05% by weight oxygen) and C1094 (99.9% by weight copper minimum, 0.07% by weight silver minimum). The alloys have an electrical conductivity
10 about equal to copper and a high yield strength to resist lead deformation during handling.

The conductive metal planes are bonded to the dielectric 30 prior to the formation of circuitry 12, 20, 22 by lamination. One suitable lamination requires a
15 pressure of from about 14 to 35 kg/cm² (200 to 550 psi) at a temperature of about 175°C for about 90 minutes.

Vias 28 interconnect the conductive planes. The vias have a region 31 capable of receiving an electrolytic deposition of a conductive metal without
20 further processing. The region 31 is formed along the walls of the apertures and a conductive metal 32 deposited on the conductive walls. The vias 28 preferably extend from the ground plane to the signal plane. They are preferably blind vias due to the narrow
25 width of signal plane circuit traces 12, 12', 12". The conductive vias 28 are from about .051mm (2 mils) to about .25mm (10 mils) in diameter and preferably from about .076mm (3 mils) to about .13mm (5 mils) in diameter. If the via 28 pierces the signal plane, an
30 electrical short between closely spaced circuit traces is possible.

The conductive vias 28 electrically interconnect the ground plane to the signal plane. Select signal plane leads 12' are grounded and other signal plane leads
35 12'' are supplied with power. Additional conductive planes may also be added. Each conductive plane is

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separated from adjacent conductive planes by a dielectric. If electrical connection between adjacent conductive layers is required, then the second dielectric is selected to be capable of pyrolysis to carbonaceous materials. The walls of the vias are made amenable to the deposition of an electrolytic deposit either by in place deposition of the carbonaceous material or by transfer deposition.

Blind vias are one embodiment of the invention. Through-holes may also be employed. The through-hole diameter is equal to or less than the width of the signal plane circuit traces. For a GTAB, the diameter of the through-holes is from about .025mm to .051mm (1 to 2 mils). For a printed circuit board, the through-holes have a diameter of from about .25mm to 1.0mm (10 to 40 mils). Closed vias, embedded within the dielectric layer as described hereinbelow form yet another embodiment.

Figures 4 and 5 illustrate a first method to manufacture the circuit of Figure 3. A flexible circuit 36 has two conductive planes. The first conductive plane forms the signal plane and is patterned into circuit traces 12. The layer forms a ground plane and is patterned into either ground 20 or power 22 circuits or both.

Patterning of the circuits is by any method known in the art, including both subtractive and additive processes. One subtractive process entails photolithographic resist patterning followed by etching. A laminate comprising the dielectric and unpatterned conductive planes is formed either with or without intermediate adhesive layers. The surfaces of the conductive layers are coated with a uniformly thick coating of a photoresist. The photoresist is then exposed by a radiation appropriate to the resist type. Exposure takes place through a photomask. The resist is developed in the desired circuit designs on both the

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ground plane and the signal plane. The ground and signal planes may be exposed either simultaneously or separately. After the resist has been patterned, a suitable solvent removes the unexposed resist. A

5 suitable chemistry then etches the conductive layers from the exposed regions. After etching, the remaining resist is removed, resulting in a desired pattern of circuits on both the ground and signal plane.

Vias 38 are next formed through the dielectric support layer 30 and adhesive layers 14, 24, if present. The vias 38 extend from apertures 40 formed in the ground plane to an interior surface 42 of the signal plane circuits 12. Blind vias 38 are formed by any heat generating process capable of accurate placement, 15 dimensions and repeatability. Mechanical drilling, plasma etching, laser vaporization or laser ablation are suitable. The surfaces of the vias 38 must achieve a temperature sufficient to pyrolyze the walls of the vias to an essentially carbonaceous material. This material 20 may either be deposited in place or transfer deposited elsewhere. An effective temperature is that which renders the surfaces amenable for electrolytic deposition without degrading the bulk properties carrier layer 30. For polyimide, an effective temperature is at least 500°C and preferably from about 600°C to about 700°C. 25 Following the pyrolytic reaction, a thin carbon layer forms a conductive portion 31 along the walls of the vias as the aperture extends through the dielectric carrier layer. Preferably, the walls of the via within adhesive 30 layers 14, 24 is also carbonized.

The preferred method to manufacture vias 38 and selectively pyrolyze the dielectric is laser ablation with an excimer, CO₂ or YAG laser. The holes may also be drilled at a speed sufficient to generate the required

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heat. Other methods which will form vias of the desired size and generate sufficient heat are also within the scope of the invention.

An excimer laser is preferred for forming the
5 holes because alignment is simplified and the holes are of outstanding uniformity, cleanliness and resolution. The excimer laser is also capable of much higher aspect ratio features and blind feature formation terminating with exceptional cleanliness to metallic surfaces. The
10 laser wavelength is selected for the absorption characteristics of the materials to be lased. The excimer laser is adjusted by demagnification and high voltage input to excite the lased media above a threshold energy for ablation. The media is reduced to carbon soot
15 and short order organic fragments. The pyrolytic material impinges on and coats in place and along surfaces in line of sight of the ablation target.

For a polyimide, an energy density above about 1.5 J/cm² is required to ablate the polymer layers which
20 comprise the adhesives 14, 24 and the dielectric layer 30 and not penetrate the metallic layers. The ground plane circuits 20, 22 define the aperture 40 location and mask the beam. The interior surface 42 of the signal plane circuit traces 12 acts as a stop.

25 The pyrolyzed walls of the vias are amenable to electrolytic deposition of a conductive material. The resistivity of the pyrolyzed surfaces is relatively high and non-uniform. While deposition of a carbonaceous material is believed to make the walls amenable to
30 electrolytic deposition, other surface phenomena may also contribute to the effect.

A conductive coating is preferably deposited on the walls 31 of vias 38 to provide a suitable electrical interconnection. Any suitable conductive metal may be
35 used. Copper is preferred due to its high electrical

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conductivity and the ready availability of commercial electroplating solutions having high throwing power. Other conductive metals such as nickel, gold, silver or the like may be similarly deposited.

5 Both electrolytic and electroless deposition processes are suitable for the invention. In electroless deposition, the pyrolytic layer may serve as a replacement for a tin-palladium catalyst. When blind vias or small diameter through holes are to be coated,
10 solution replenishment within the via is a problem. An electrolytic deposition process is then preferred.

One suitable copper electroplating solution contains of the following components in the following proportions:

15	<u>Component</u>	<u>General Proportions</u>	<u>Preferred Proportions</u>
	Copper (as metal)	15-18.75gm/l (2-2.5oz/gal)	16.88gm/l (2.25oz/gal)
20	Copper sulfate	60-75gm/l (8-10oz/gal)	67.5gm/l (9oz/gal)
	H ₂ SO ₄ (by weight)	150-225gm/l (20-30oz/gal)	172.5gm/l (23oz/gal)
	Chloride ion	20-100mg/l	50mg/l

The electroplating bath is agitated and preferably
25 maintained at a temperature of between about 20°C and about 25°C. The bath is provided with anodes, generally copper. The flexible circuit to be plated is connected as a cathode. A current of, for example, about 108 amps per square meter (10 amps per square foot) is impressed
30 across the circuit for a period of from about 10 minutes to about 45 minutes. The preferred immersion time and current density are those sufficient to deposit an effective thickness of a layer of copper. Copper plating provides a reliable electrical interconnect

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between the ground plane and signal plane. Thickness may vary from a continuous flash up to diameter of the hole. A preferred thickness is from about .013mm to about .025mm (0.5 to 1 mil).

5 The spacing between signal plane traces 12 may be less than .051mm (2 mils). To avoid copper bridging during electroplating, both the signal plane and the ground plane may be coated with a plating resist prior to electroplating. Following deposition, the resist is
10 removed with a suitable solution.

 Figures 6-8 illustrate a second process for forming the GTAB circuit of Figure 3. First 44 and second 46 copper layers are bonded to the dielectric 30. An adhesive layer may optionally be disposed between the
15 conductive layers and the dielectric layer. Vias 38 are then formed through the second conductive layer 46 and dielectric layer 30. Sufficient heat is generated during the via opening process to develop a portion 31 along the walls of the via 38 which is amenable to
20 coating with a conductive metal.

 A conductive layer 48 is then deposited on the first 44 and second 46 metal layers as well as the portions 31 of the dielectric layer 30. Following metal deposition a photoresist coating 56 is applied to the
25 conductive layers. The layers are photopatterned into a desired pattern of signal and ground planes circuitry by photolithography.

 Figures 9-11 illustrate another process for manufacturing the circuits of the invention. The
30 dielectric 30 contains vias 38 formed by a technique capable of generating sufficient heat so the walls become suitable for electrolytic deposition. The portions 31 of the vias are coated with a conductive metal 48. Only the vias are conductive. A bussing
35 system such as a conductive silver paste must be used if electrolytic deposition is desired. An electroless

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deposition process which will deposit on the portions 31 and not the dielectric portions of the carrier 30 is also suitable.

5 Following deposition, the bussing is removed and residual plating salts are rinsed away. First 44 and second 46 conductive layers are laminated to opposing sides of the dielectric carrier 30. The conductive layers are then formed into signal and ground planes by photolithography.

10 As shown in Figure 11, through-hole vias 58 may be formed to interconnect the signal plane circuit traces 12' and ground circuits 70. Alternatively, closed vias 60 may also be formed. Closed vias are particularly favored. The sealed vias are highly resistant to
15 corrosion and associated deterioration of electrical properties.

Another process for manufacturing a GTAB or other circuit is illustrated in Figures 12 and 13. As with the preceding embodiment, the vias 38 are formed in the
20 dielectric carrier layer 30 before the first and second conductive layers are bonded. The walls of the vias are made amenable to deposition of a conductive metal by pyrolysis. Selected portions 62 of the dielectric carrier 30 are also made suitable for deposition. The
25 laser output may be controlled to an energy density below the threshold for ablation of the polymer. By appropriate control of the resolution or masking, the irradiated surfaces may be selectively pyrolyzed to carbonaceous material rich areas 62 separated by
30 dielectric regions 30. The carbonized areas form the seed layer for eventual circuit patterns. The pyrolyzed surfaces are believed to provide exceptional adhesion to the bulk dielectric since they are part of the original polymer matrix.

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The regions 64 of the carrier 30 which are not irradiated by the laser beam remain a dielectric. The irradiated polymer carrier layer 30 may then be immersed in an electrolytic or electroless deposition solution. A
5 metal, preferably copper, is deposited on the conductive regions 62, 31 to form signal plane traces 12, ground 20 and power 22 circuits, as well as conductive apertures 28. The process is especially desirable for single and multilayer circuit manufacture. It is completely
10 additive. No solvents or other chemical by-products such as are generated by a subtractive process require disposal. The high resolution of the laser permits accurate positioning of signal and ground plane circuit traces. Very fine circuit features are obtainable.

15 The processes of the invention will become more clear from the example and illustration which follow.

EXAMPLE

A five layer flexible circuit was formed by laminating two copper layers to a polyimide dielectric.
20 Each copper layer had a thickness of from about .025mm to .036mm (1.0 to 1.4 mils) and the dielectric layer was about .056mm (2.2 mils) thick. An adhesive was disposed between each copper layer and the carrier layer to facilitate bonding. Features were formed in one copper
25 layer by photolithography. Among the features formed were apertures having a diameter of from about .051mm to .15mm (2.0 to 6.0 mils). The exposed regions of foil were etched in an alkaline etchant (ac-Cu-guard™, available from Olin Hunt Specialty Products Inc., West
30 Patterson, NJ, USA). Using the apertures etched in the foil as a mask, an excimer laser was used to ablate the two adhesive layers and the polyimide underlying the hole. An excimer laser operating at 248nm by Krypton

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fluoride lasing media was operated at a frequency of 150Hz and an on-target energy density of 1.3 J/cm^2 pulse. Lasing continued for approximately 220 laser bursts until removal was completed to the terminal copper
5 of the signal plane.

Undesired carbonaceous deposits were then cleaned from copper surfaces by a lift-off microetch of the underlying copper. Carbonaceous copper is noticeable as a dark ring surrounding the hole. The microetch does not
10 affect carbonaceous surfaces bound to the dielectric materials. One suitable microetch is a sodium persulfate solution available as MICROCLEAN 1 from Olin Hunt Speciality Products, Inc. The microetch attacks the first few atomic layers of copper. The carbonaceous
15 deposits flake off as micro flakelettes which may be removed from the solution by suitable filtration. Generally, a one minute immersion in the microetch at room temperature is sufficient to remove the carbonaceous residue.

20 The circuit was rinsed and dipped in 10% sulfuric acid at 20 to 25°C for about 1 to 2 minutes. Following the acid dip, the circuit was immersed in an electroplating bath at a current density sufficient to deposit copper to a thickness of about .013mm to .025mm
25 (0.5 to about 1.0 mils) within the blind vias. The substrate was then rinsed and dried. The blind vias were then cross sectioned. As shown in Figure 14, the electroplated copper 64 was bonded to both the adhesive layers 14, 24 and the carbonized dielectric layer 30.

30 Figure 14 shows incomplete copper deposition within the via. If in place pyrolysis is the primary mechanism, then it is believed that increasing solution agitation and optimizing laser address will completely bridge the via. If transfer deposition of carbonaceous
35 material is the primary mechanism, then a sacrificial layer of pyrolytic dielectric may be required.

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Regardless of the mechanism, the process of the invention has been shown to produce an electroplated copper layer 64 is bonded to both the adhesive and the polyimide where both dielectrics were made amenable to coating in situ and without additional processing steps.

While the invention has been preferentially described in accordance with a GTAB type circuit, it is applicable to all multilayer circuits requiring electrical interconnection. Printed circuit boards and multilayer electronic package bases such as for surface mounting are particularly suited for the processes of the invention. The present technique is readily adaptable to increasingly narrow circuit traces separated by increasingly narrow spaces. While the dielectric carrier layer has been described in terms of polyimide, other suitable carrier layers may be used. The temperature for pyrolysis may require variation to satisfy the specific properties of the selected carrier.

While the invention has been described in terms of circuits having two metal layers, it is equally applicable to multilayer circuits having in excess of two metal layers.

While the walls of the vias have been described in terms of entire surfaces being coated, only a portion of the walls require coating to provide electrical conductivity.

It is apparent that there has been provided in accordance with this invention, a process for the manufacture of conductive vias in situ to electrically interconnect conductive planes of an electronic circuit and the product produced by that process which fully satisfy the objects, features and advantages set forth herein before. While the invention has been described in combination with the embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art in light of the

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foregoing description. Accordingly, it is intended to embrace all such alternatives, modifications and variations as fall within the spirit and broad scope of the appended claims.

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IN THE CLAIMS:

1. An electronic circuit 10, characterized by:
at least two conductive planes 12, 20;
a polymer layer 30 disposed between said conductive
planes 12, 20, said polymer 30 selected to be a
5 dielectric which may be made electrically conductive in
situ; and
at least one via 28 interconnecting said first 12
and second 20 conductive planes wherein said polymer 30
is electrically conductive along the walls 31 of said at
10 least one via 28.
2. The electronic circuit 10 of claim 1
characterized in that said polymer 30 may be made
electrically conductive by pyrolysis.
3. The electronic circuit 10 of claim 2
characterized in that a layer of carbon is formed on
said walls 31 of said at least one via 28.
4. The electronic circuit 10 of claim 3
characterized in that said polymer 30 is selected from
the group consisting of aromatic polyimides, aromatic
polyamides, polybenzimidazoles, polybenzoxazoles,
5 polybenzothiazoles, polyoxadiazoles, polytriazoles,
polyimidazopyrrolones, aromatic polysulfones and
polyphenylene sulfide.
5. The electronic circuit 10 of claim 4
characterized in that said polymer 30 is polyimide.
6. The electronic circuit 10 of claim 5
characterized in that said circuit contains first 12 and
second 20 copper or copper alloys conductive planes each
having a thickness of from about .013mm to about .15mm
5 (0.5 to 6 mils).

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7. The electronic circuit 10 of claim 6 characterized in that said first 12 and second 20 conductive planes have a thickness of from about .025mm to about .036mm (1 to 1.4 mils).

8. The electronic circuit 10 of claim 6 characterized in that the conductive walls 31 of at least one via 28 are coated with a conductive metal or metal alloy 32.

9. The electronic circuit 10 of claim 8 characterized in that said conductive metal or metal alloy coating 32 is selected from the group consisting of nickel, tin, gold and copper.

10. The electronic circuit 10 of claim 9 characterized in that said conductive coating 32 is copper having a thickness from at least a trace to the entire diameter of said via 28.

11. The electronic circuit 10 of claim 10 characterized in that the thickness of said copper coating layer 32 is from about .013mm to about .025mm (0.5 to 1 mil).

12. The electronic circuit 10 of claim 10 characterized in that at least one via 28 is a blind via extending from said second conductive plane 20 to an interior surface of said first conductive plane 12.

13. The electronic circuit 10 of claim 10 characterized in that at least one via 28 is a through hole via extending from said second conductive plane 20 to said first conductive plane 12.

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14. The electronic circuit 10 of claim 12 characterized in that said first conductive plane 12 is formed into a plurality of signal leads and said second conductive plane 20 is formed into ground and power
5 leads 20, 22.

15. A process for the manufacture of an electronic circuit 36, characterized by the steps of:
providing a polymer layer 30, said polymer being selected to be a dielectric which may be made
5 electrically conductive in situ;
forming a plurality of vias 38 in said polymer layer 30;
treating the walls 31 of said vias 38 such that said walls 31 become electrically conductive; and
10 electrically interconnecting said conductive vias 38 to first 44 and second 46 conductive planes bonded to opposing sides of said polymer layer 30.

16. The process of claim 15 characterized in that said polymer 30 is pyrolytic.

17. The process of claim 16 characterized in that said polymer 30 forms carbon as a by-product of pyrolysis.

18. The process of claim 17 characterized in that said polymer 30 is selected from the group consisting of aromatic polyimides, aromatic polyamides, polybenzimidazoles, polybenzoxazoles,
5 polybenzothiazoles, polyoxadiazoles, polytriazoles, polyimidazopyrrolones, aromatic polysulfones and polyphenylene sulfide.

19. The process of claim 18 characterized in that said polymer 30 is polyimide.

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20. The process of claim 19 characterized in that the walls 31 of vias 38 formed in said polyimide 30 become electrically conductive by heating to a temperature in excess of about 500°C.

21. The process of claim 20 characterized in that the walls 31 of said vias 38 become electrically conductive by heating to a temperature in the range of from about 600°C to about 700°C.

22. The process of claim 20 characterized in that the step of forming a plurality of vias 38 in said polymer layer 30 simultaneously treats the walls 31 of said vias 38 such that the walls 31 become electrically
5 conductive.

23. The process of claim 22 characterized in that said vias 38 are formed by laser ablation.

24. The process of claim 23 characterized in that said laser ablation employs an excimer laser.

25. The process of claim 22 characterized in that said plurality of vias 38 are formed by mechanical drilling.

26. The process of claim 22 characterized in that said first 44 and second 46 conductive planes are copper or a copper alloy having a thickness of from about .013mm to about .15mm (0.5 to 6 mils).

27. The process of claim 26 characterized in that said first 44 and second 46 conductive planes have a thickness of from about .025mm to about .036mm (1 to 1.4 mils).

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28. The process of claim 26 characterized in that said first conductive plane 44 forms a plurality of signal plane circuits 12 and said second conductive plane 46 forms ground 20 and power 22 plane circuits.

29. The process of claim 28 characterized in that said electrically conductive walls 31 of said via 38 are coated with a conductive metal or metal alloy 48.

30. The process of claim 29 characterized in that said electrically conductive walls 31 of said vias 38 coated with a metal selected from the group consisting of nickel, tin, silver and copper.

31. The process of claim 30 characterized in that said electrically conductive walls 31 of said vias 38 are coated with copper 48 by electrolytic deposition, the thickness of said electrolytically deposited copper
5 48 being from a flash to the entire diameter of said via.

32. The process of claim 31 characterized in that the thickness of said electrolytically deposited copper 48 is from about .013mm to about .025mm (0.5 to 1 mil).

33. The process of claim 31 characterized in that said first 44 and second 46 conductive planes are bonded to opposing sides of said polymer 30 and patterned into circuits 12, 20, 22 prior to forming said conductive
5 vias 38.

34. The process of claim 33 characterized in that said first 44 and second 46 conductive planes are selected to be copper or a copper alloy;

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5 disposing an adhesive 14, 24 between each said
plane 44, 46 and said polymer layer 30; and
laminating said conductive planes 44, 46 to said
polymer layer 30.

35. The process of claim 34 characterized in
that the portion of said adhesive 14, 24 forming the
via wall 31 becomes electrically conductive during
via 38 forming.

36. The process of claim 31 characterized in
that said first 44 and second 46 conductive planes
are bonded to said polymer 30;
5 conductive vias 38 are formed through said
polymer layer 30; and
said circuit patterns 12, 20, 22 are then formed
in said conductive planes 44, 46.

37. The process of claim 36 characterized in
that an adhesive 14, 24 is disposed between said
first 44 and second 46 conductive planes and said
polymer layer 30 and said conductive planes 44, 46
5 are laminated to said polymer layer 30.

38. The process of claim 37 characterized in
that the portion of said adhesive 14, 24 forming the
via wall 31 becomes electrically conductive during
via 38 forming.

39. The process of claim 31 characterized in
that said conductive vias 38 are formed in said
polymer layer 30 before said first 44 and second 46
conductive planes are bonded to said polymer layer 30.

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40. The process of claim 39 characterized in that said conductive vias 38 are selected from the group consisting of blind holes 38, through holes 58 and embedded holes 60.

41. The process of claim 40 characterized in that at least one conductive via 38 is selected to be a blind hole.

42. A process for the manufacture of an electronic circuit 36, characterized by the steps of:

providing a polymer layer 30 having first and second opposing sides, said polymer 30 being selected to
5 be a dielectric which may be made electrically conductive in situ;

forming a plurality of vias 38 in said polymer layer 30;

10 treating the walls 31 of said vias 38 and portions 62 of said first and second sides of polymer such that said walls 31 and portions 62 become electrically conductive; and

depositing a conductive metal or metal alloy 12, 20, 22 on said conductive walls 31 and portions 62.

43. The process of claim 42 characterized in that said walls 31 and portions 62 are made electrically conductive by pyrolysis.

44. The process of claim 43 characterized in that said walls 31 and portions 62 become conductive by forming carbon during pyrolysis.

45. The process of claim 44 characterized in that said polymer 30 is selected from the group consisting of aromatic polyimides, aromatic polyamides, polybenzimid-

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azoles, polybenzoxazoles, polybenzothiazoles,
5 polyoxadiazoles, polytriazoles, polyimidazopyrrolones,
aromatic polysulfones and polyphethylene sulfide

46. The process of claim 45 characterized in that said polymer 30 is selected to be polyimide.

47. The process of claim 46 characterized in that said walls 31 and portions 62 are made electrically conductive by heating to a temperature in excess of about 500°C.

48. The process of claim 47 characterized in that said walls 31 and portions 62 are made electrically conductive by heating to a temperature in the range of from about 600°C to about 700°C.

49. The process of claim 47 characterized in that said heating is by an excimer laser.

50. The process of claim 47 characterized in that the conductive portion 62 of said first side of said polymer layer 30 is formed into signal plane circuits 12 and the conductive portion on said second side of said
5 polymer layer 30 is formed into power 22 and ground 20 plane circuits.

51. The process of claim 50 characterized in that copper is deposited on said conductive walls 31 and portions 62.

52. The process of claim 51 characterized in that said copper is deposited electrolytically.

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53. An electronic circuit, characterized by;
a dielectric polymer carrier layer 30 having first
and second opposing sides and a plurality of vias 38;
said first and second opposing sides containing
5 conductive portions 62 formed in situ; and
said vias 38 having electrically conductive walls
31 formed in situ, said walls 31 interconnecting
selected conductive portions 62 of said first and second
portions.

54. The electronic circuit of claim 53
characterized in that said dielectric polymer 30 becomes
conductive by heating to a temperature in excess of
about 500°C.

55. The electronic circuit of claim 54
characterized in that said dielectric polymer 30 becomes
conductive by heating to a temperature in the range of
about 600°C to about 700°C.

56. The electronic circuit of claim 54
characterized in that said dielectric polymer carrier
layer 30 is polyimide.

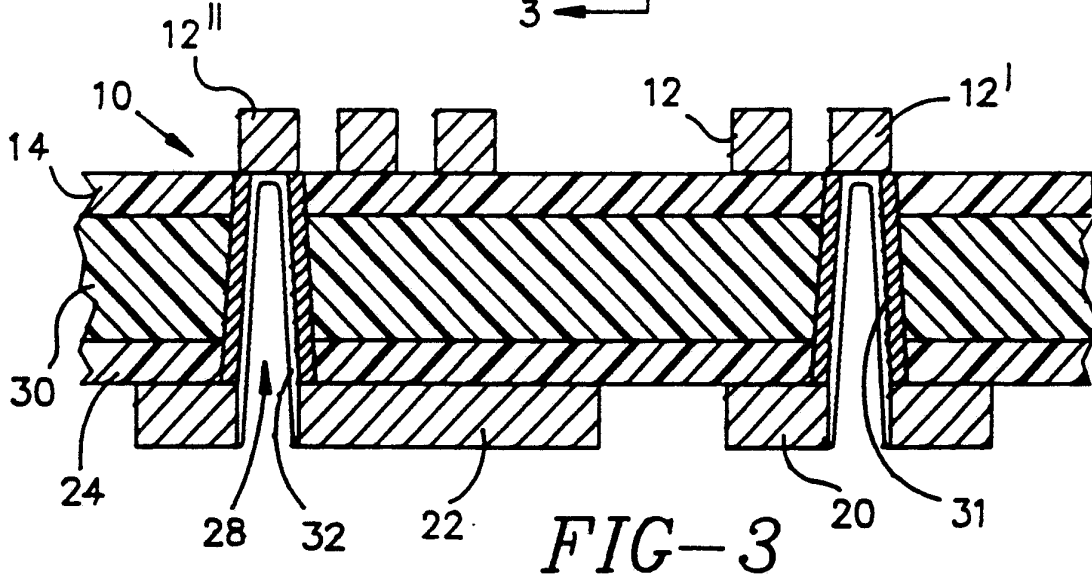
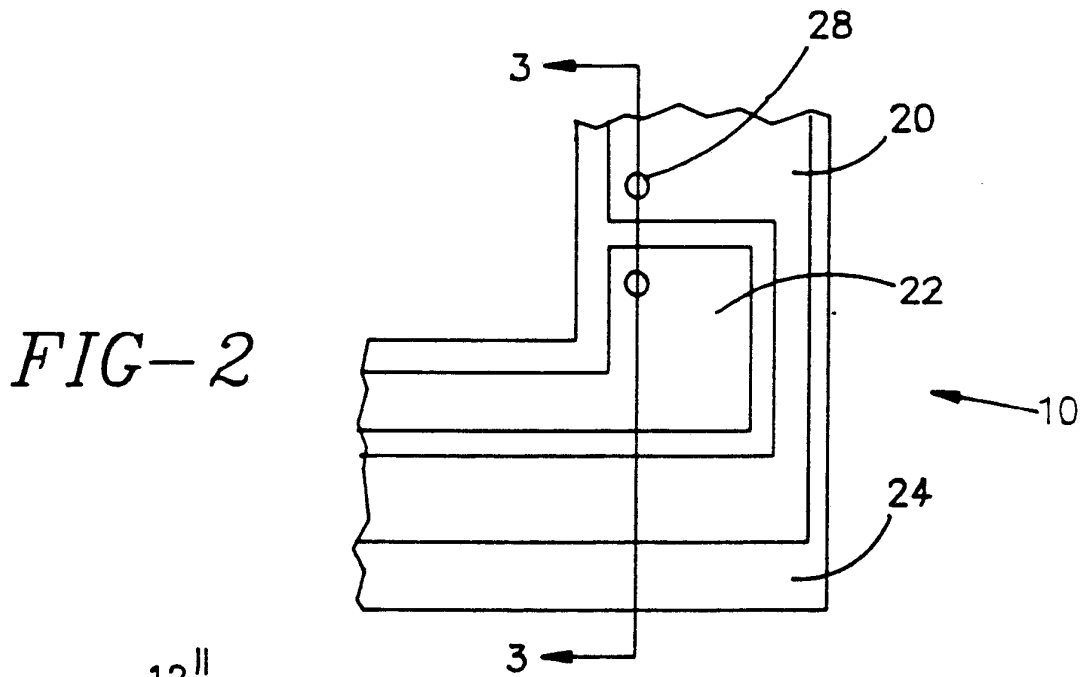
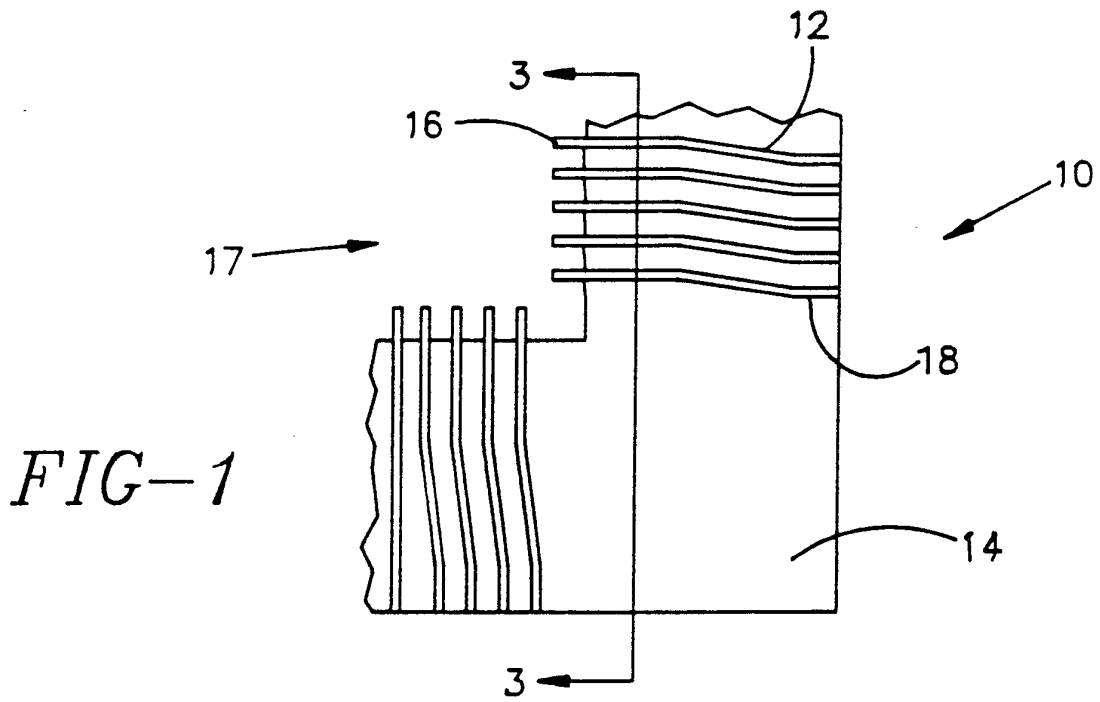
57. The electronic circuit of claim 56
characterized in that the conductive portions 62 of said
first opposing side are formed into a plurality of
signal plane circuits 12 and the conductive portions of
5 said second side are formed into ground 20 and power 22
plane circuits.

58. The electronic circuit of claim 57
characterized in that said conductive portions 62 and
walls 31 are coated with a conductive metal or metal
alloy selected from the group consisting of copper,
5 gold, silver, nickel and tin and their alloys.

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59. The electronic circuit of claim 58 characterized in that said coating is selected to be copper having a thickness of from about .013mm to about .15mm (0.5 to 6 mils).

60. The electronic circuit of claim 59 characterized in that said coating has a thickness of from about .025mm to about .036mm (1 to 1.4 mils).



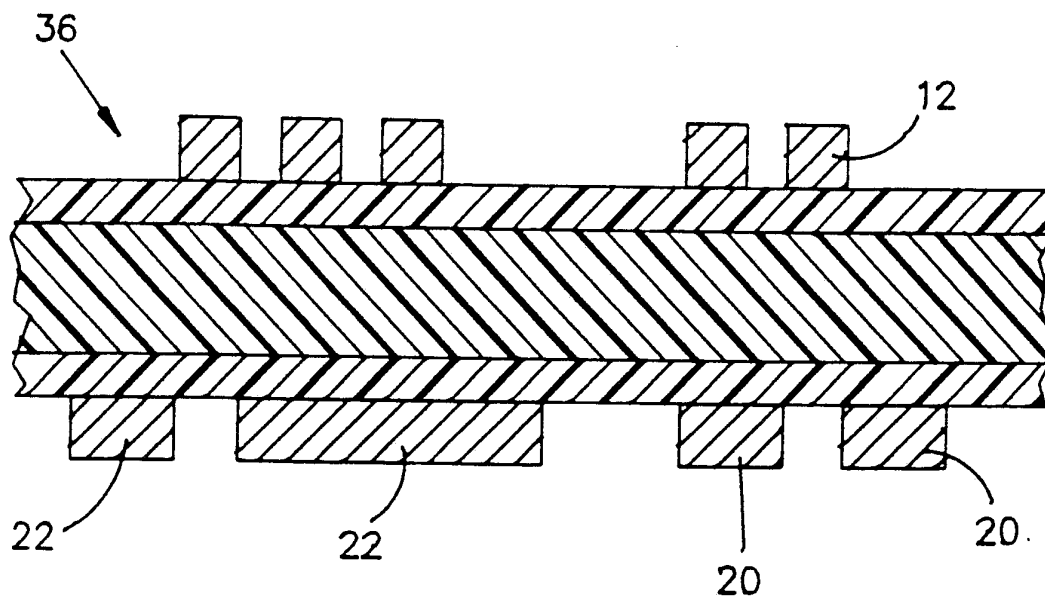


FIG-4

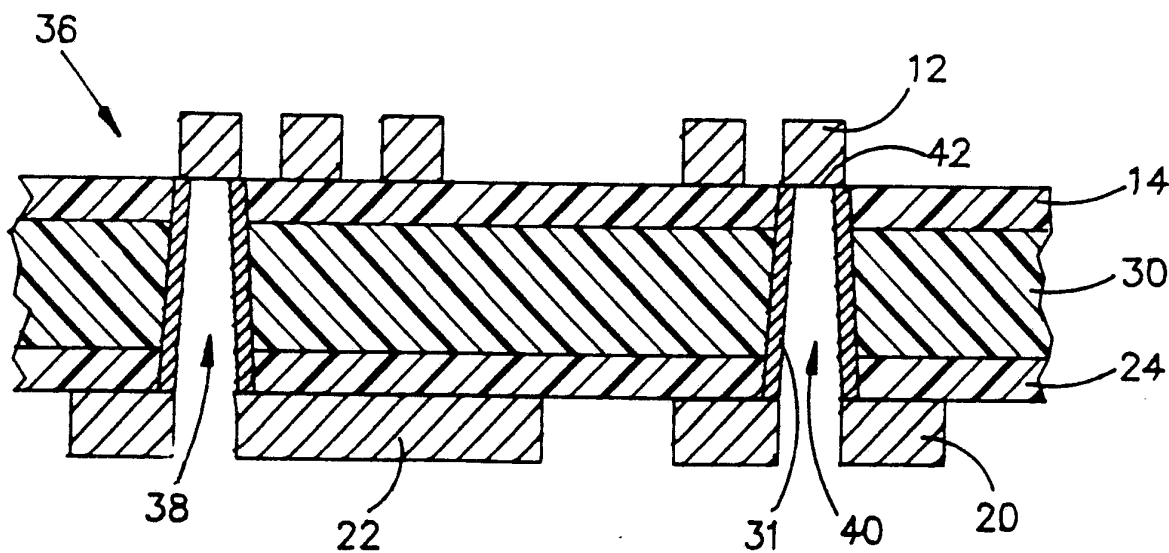


FIG-5

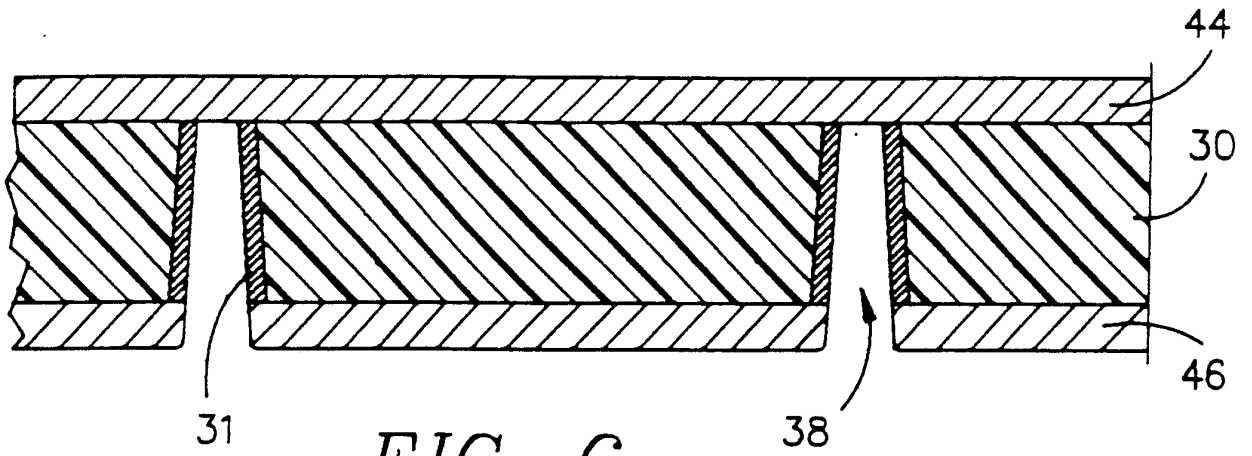


FIG-6

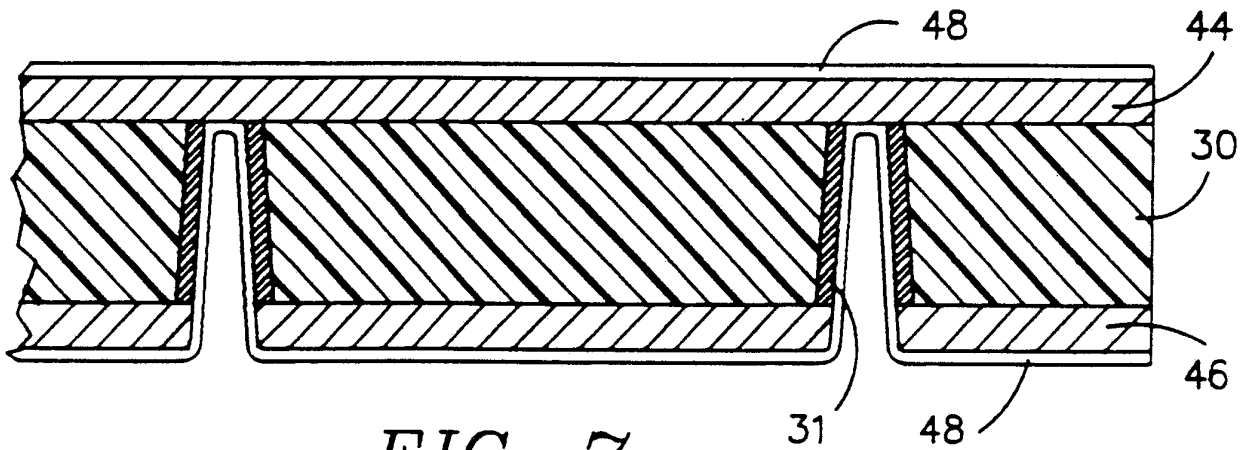


FIG-7

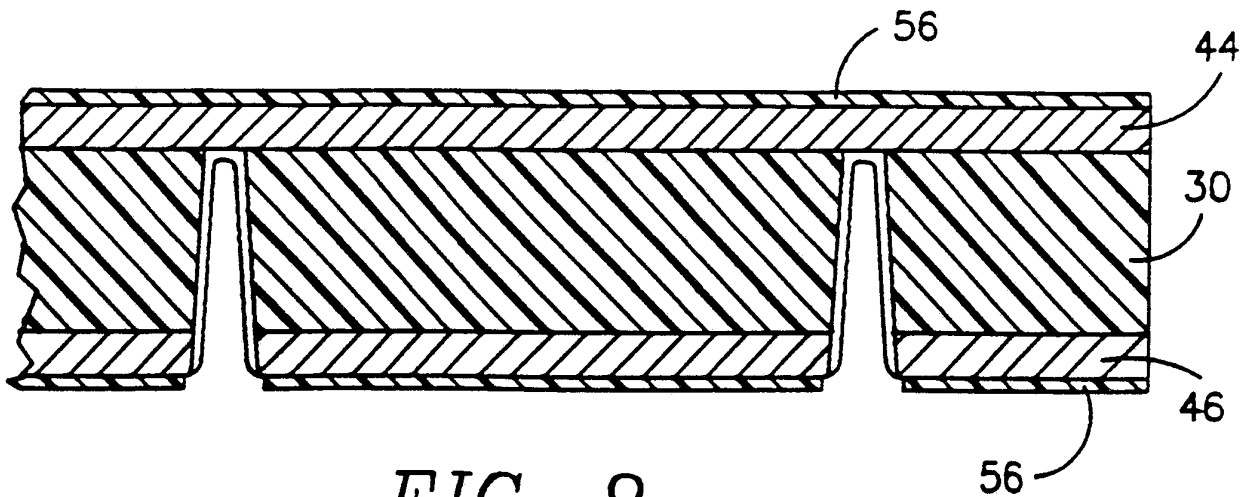


FIG-8

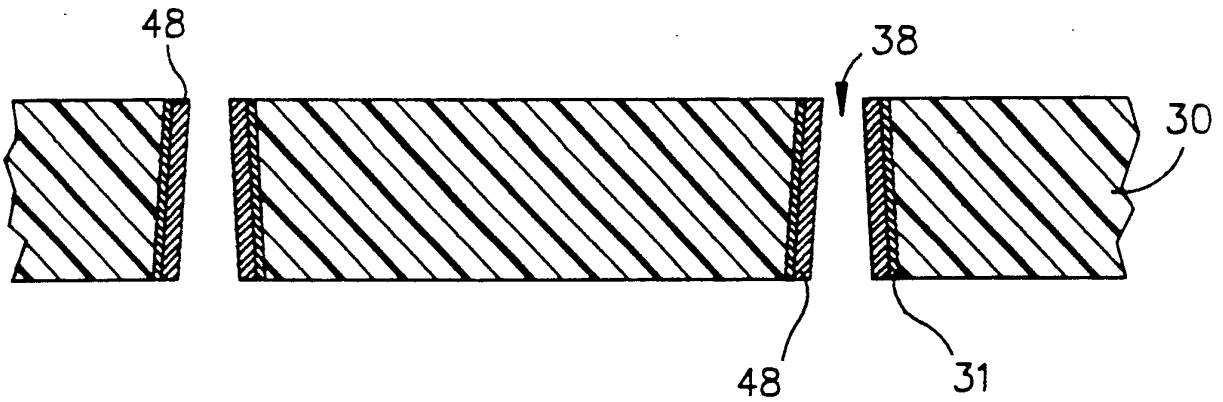


FIG-9

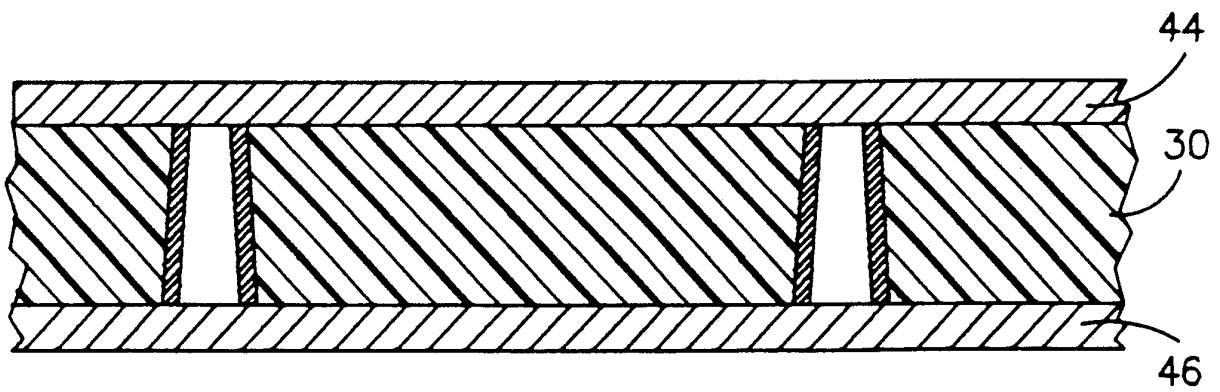


FIG-10

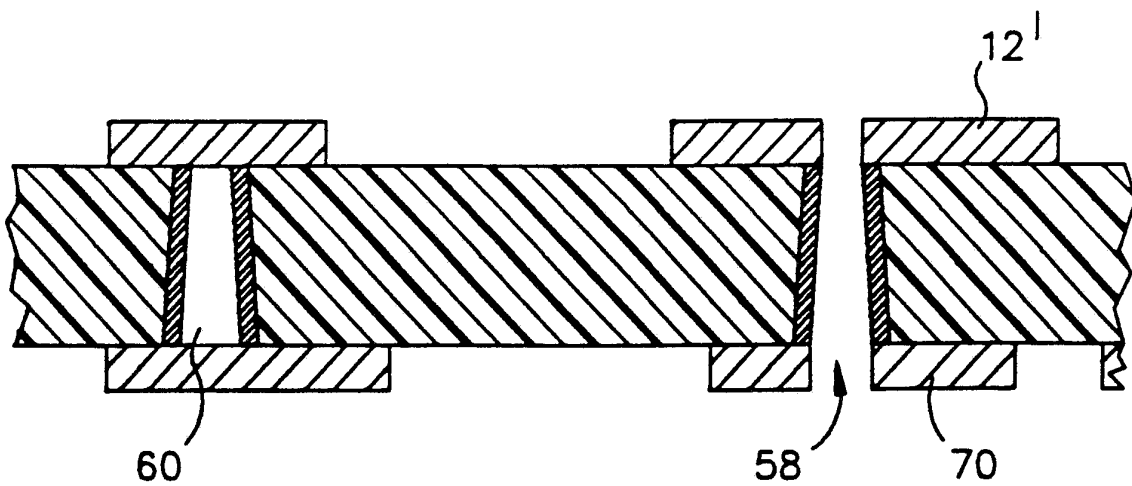


FIG-11

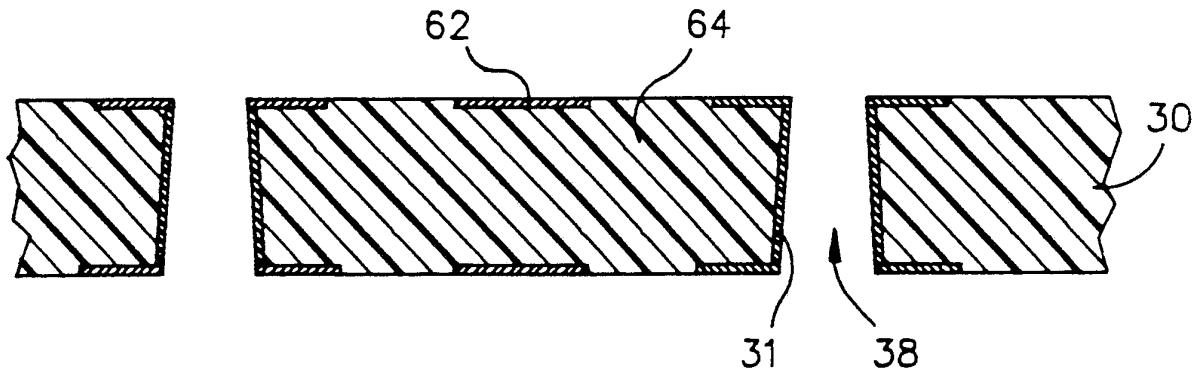


FIG-12

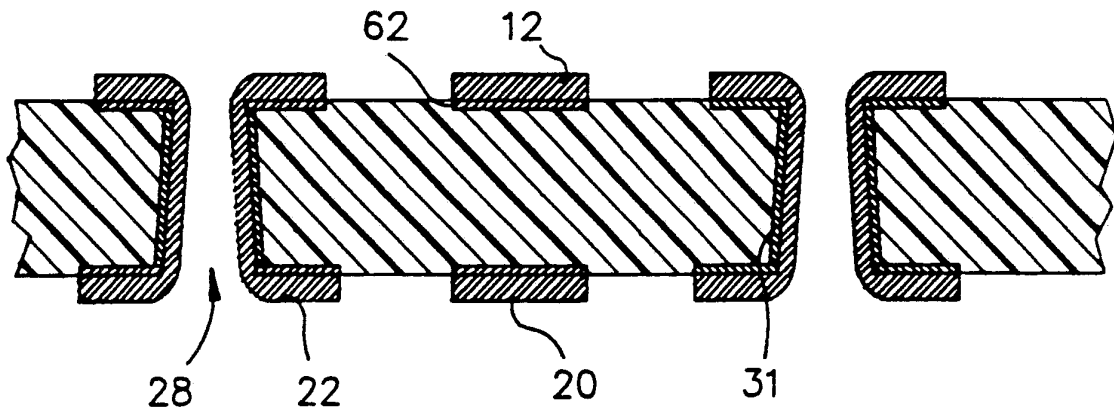


FIG-13

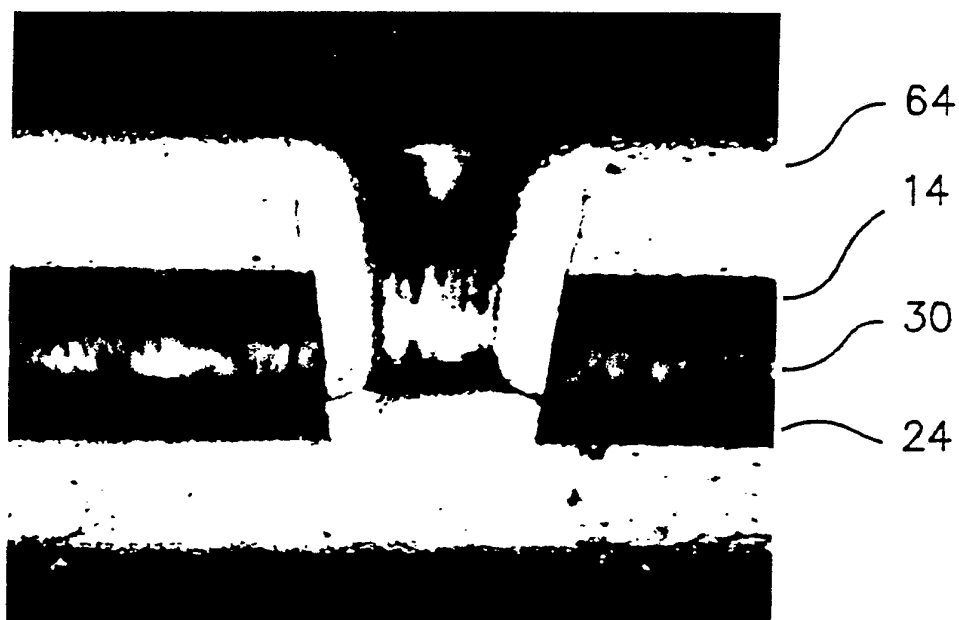


FIG-14

INTERNATIONAL SEARCH REPORT

International Application No PCT/US91/00877

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ³		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC (5): H05K 3/02		
U.S. CL.: 29/829, 852; 174/258; 357/80; 361/386, 387		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁴		
Classification System	Classification Symbols	
U.S.	29/825, 829, 846, 852; 174/258; 357/80 361/386, 387, 398, 402, 404, 421	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁵		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ¹⁴		
Category [*]	Citation of Document, ¹⁶ with indication, where appropriate, of the relevant passages ¹⁷	Relevant to Claim No. ¹⁸
Y	US, A, 4,943,346 (MATTELIN) 24 July 1990 See the entire document	1-60
Y	US, A, 4,870,751 (ANTOON) 03 October 1989	1-60
Y	US, A, 4,606,955 (EASTMAN ET AL) 19 August 1986	1-60
<p>[*] Special categories of cited documents: ¹⁵</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&" document member of the same patent family</p>		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search ²		Date of Mailing of this International Search Report ³
14 MAY 1991		05 JUL 1991
International Searching Authority ¹		Signature of Authorized Officer ²⁰
ISA/US		<i>Thi Dang</i> THI DANG