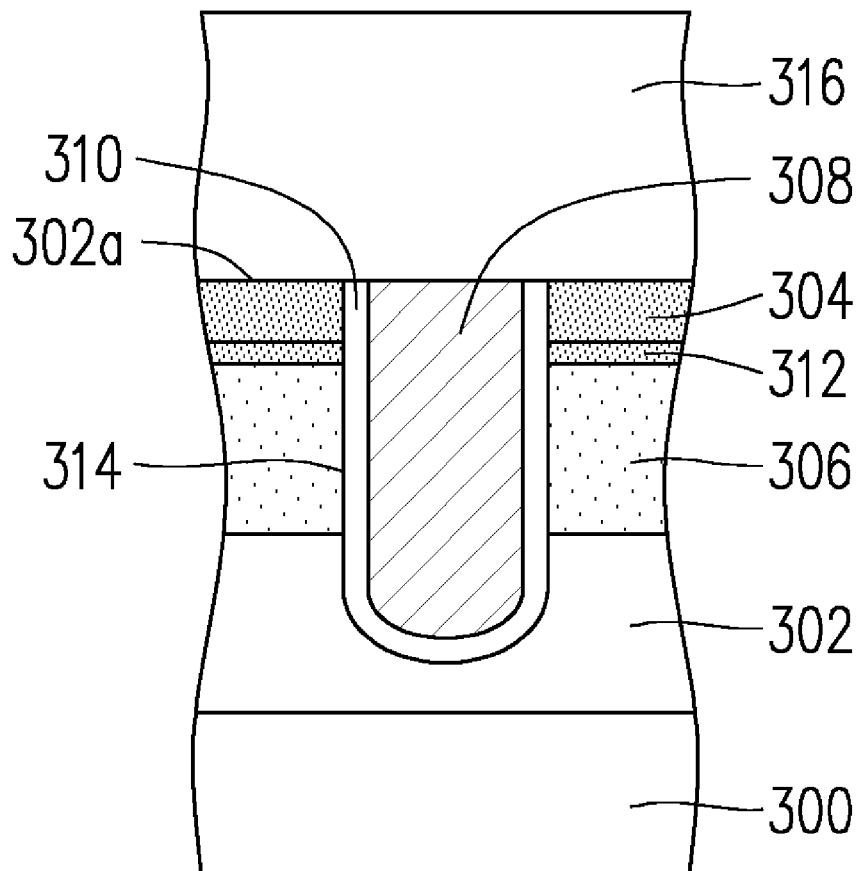


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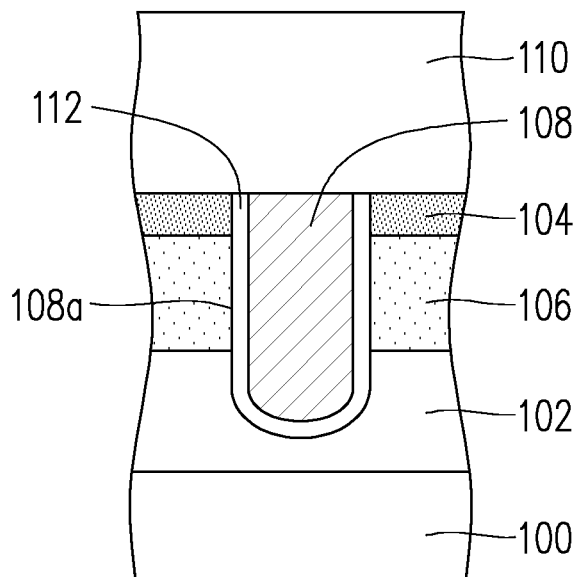


FIG. 1 (RELATED ART)

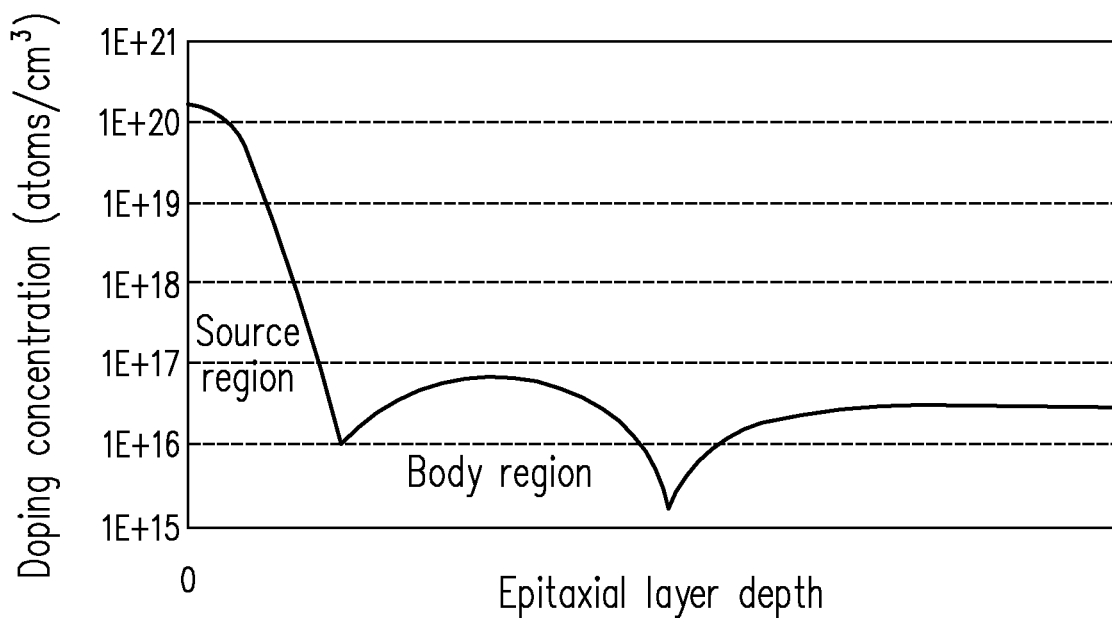


FIG. 2 (RELATED ART)

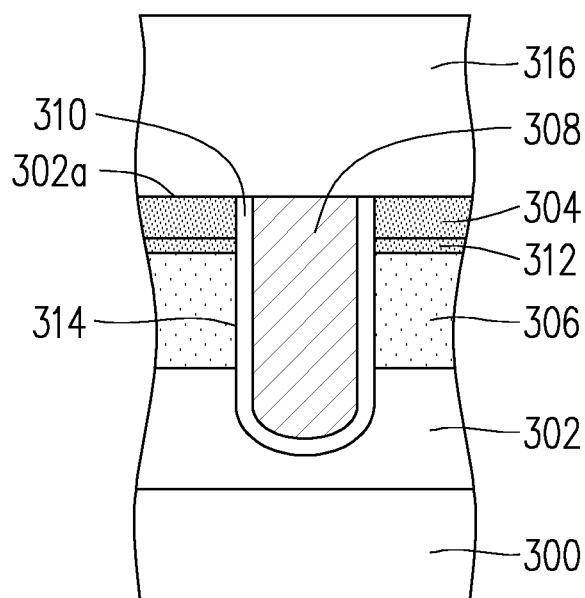


FIG. 3

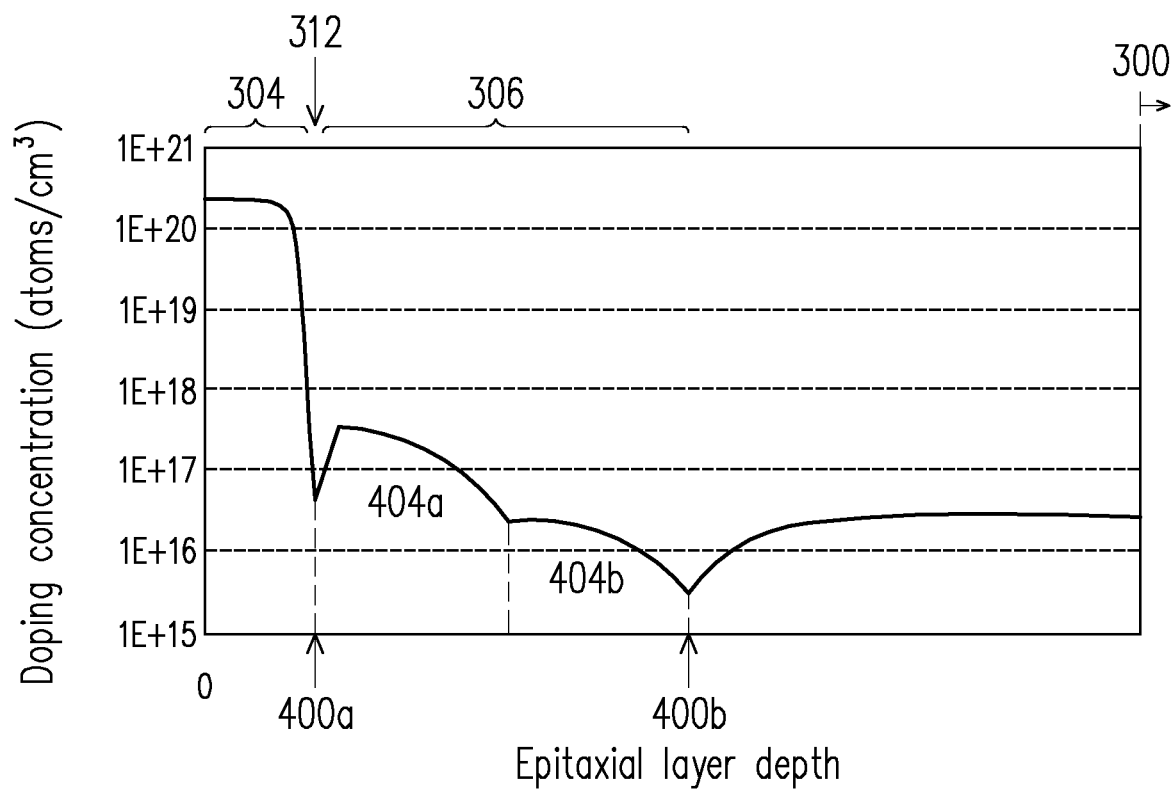


FIG. 4

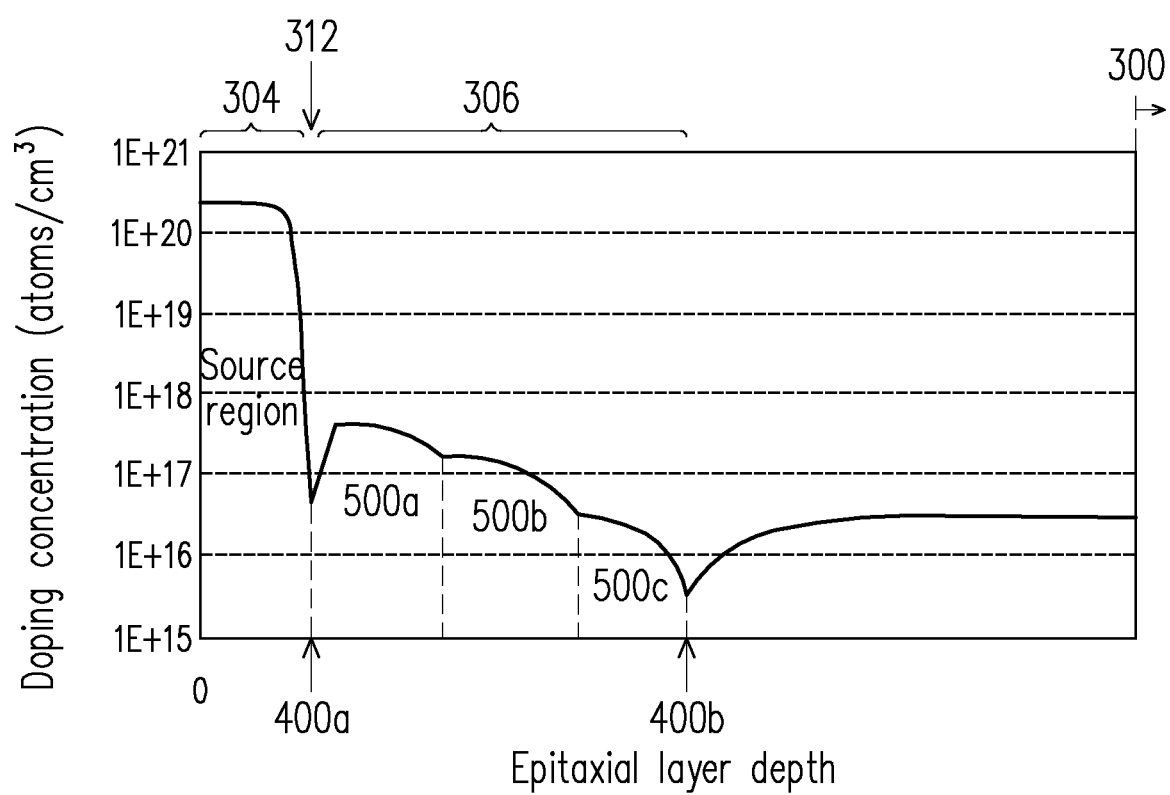


FIG. 5

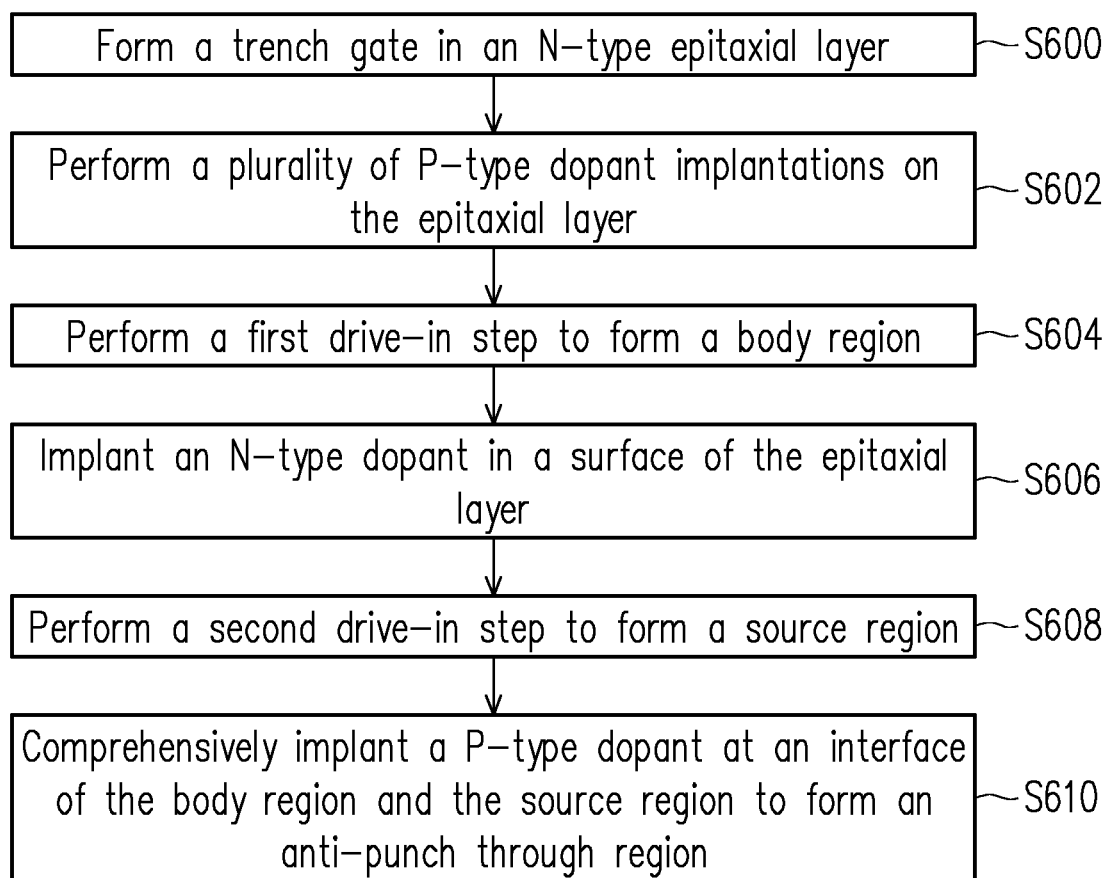


FIG. 6

MANUFACTURING METHOD OF TRENCH MOSFET

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional application of and claims the priority benefit of U.S. patent application Ser. No. 16/830,225, filed on Mar. 25, 2020, now pending. The prior application Ser. No. 16/830,225 claims the priority benefit of Taiwan application serial no. 108147542, filed on Dec. 25, 2019. The entirety of each of the above-mentioned patent applications is hereby incorporated by reference herein and made a part of this specification.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The invention relates to a power semiconductor device, and more particularly, to a trench metal-oxide semiconductor field effect transistor (MOSFET) and a manufacturing method of the same.

Description of Related Art

[0003] Among power semiconductor devices, power semiconductor devices vertically disposed in trenches have become one of the focuses of development in various industries because they may significantly increase cell density.

[0004] FIG. 1 is a diagram of a conventional trench MOSFET. In FIG. 1, a source region 104 and a body region 106 are in an epitaxial layer 102 on a substrate 100, a trench gate 108 is disposed in the epitaxial layer 102, and an inner dielectric layer (ILD) 110 covers the epitaxial layer 102 and the trench gate 108. In addition, a gate oxide layer 112 is on the surface of the trench gate 108.

[0005] FIG. 2 is a graph of doping concentration along a sidewall 108a of the trench gate structure 108 of FIG. 1, wherein it is shown that the doping concentration distribution between the source region 104 and the body region 106 is mild, so that the body resistance is higher. Once the body resistance is high, the parasitic N (source 104)-P (body 106)-N (epitaxial layer 102) bipolar transistor is easily turned on, and secondary breakdown occurs to the MOSFET so that device temperature is increased, thus causing permanent damage to the device. That is, unclamped inductive switching (UIS) performance is worsened.

SUMMARY OF THE INVENTION

[0006] The invention provides a manufacturing method of a trench MOSFET that may generate a high doping concentration region between the body and the source to reduce body resistivity (R_{s_Body}) to prevent the parasitic bipolar transistor from turning on.

[0007] The manufacturing method of a trench MOSFET of the invention includes the following steps. A trench gate is formed in an epitaxial layer having a first conductivity type on a substrate. A step of performing a plurality of implantations of a dopant having a second conductivity type is performed on the epitaxial layer in a manner that an implantation dose is gradually reduced toward a direction of the substrate. A first drive-in step is performed to diffuse the dopant having the second conductivity type in an upper half of the epitaxial layer to form a body region having the

second conductivity type. A dopant having the first conductivity type is implanted on a surface of the epitaxial layer. A second drive-in step is performed to diffuse the dopant having the first conductivity type to form a source region. After the source region is formed, the dopant having the second conductivity type is comprehensively implanted at an interface of the body region and the source region to form an anti-punch through region, wherein a doping concentration of the anti-punch through region is higher than a doping concentration of the body region.

[0008] In an embodiment of the invention, the step of performing a plurality of implantations of the dopant having the second conductivity type includes two or three implantations.

[0009] In an embodiment of the invention, an energy of implanting the dopant having the first conductivity type is, for example, between 20 KeV and 45 KeV.

[0010] In an embodiment of the invention, the second drive-in step includes rapid thermal processing (RTP).

[0011] In an embodiment of the invention, the step of forming the trench gate includes the steps of first forming a trench in the epitaxial layer, forming a gate oxide layer on a surface of the trench, and depositing a conductor in the trench as a gate.

[0012] In an embodiment of the invention, the doping concentration of the anti-punch through region is between $5E+16$ atoms/cm³ and $5E+17$ atoms/cm³.

[0013] In an embodiment of the invention, the first conductivity type is N-type, and the second conductivity type is P-type.

[0014] In an embodiment of the invention, the first conductivity type is P-type, and the second conductivity type is N-type.

[0015] Based on the above, in the invention, via the anti-punch through region formed between the body and the source, a steep concentration distribution is achieved and thereby body resistivity is reduced to prevent the parasitic bipolar transistor from turning on and improve the UIS capabilities of the trench MOSFET.

[0016] In order to make the aforementioned features and advantages of the disclosure more comprehensible, embodiments accompanied with figures are described in detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0018] FIG. 1 is a diagram of a conventional trench MOSFET.

[0019] FIG. 2 is a graph of doping concentration along a sidewall of the trench gate structure of FIG. 1.

[0020] FIG. 3 is a diagram of a trench MOSFET according to the first embodiment of the invention.

[0021] FIG. 4 is a graph of a doping concentration along a sidewall of the trench gate structure of FIG. 3.

[0022] FIG. 5 is a graph of another doping concentration along the sidewall of the trench gate structure of FIG. 3.

[0023] FIG. 6 is a manufacturing process flowchart of a trench MOSFET according to the second embodiment of the invention.

DESCRIPTION OF THE EMBODIMENTS

[0024] The disclosure below provides numerous different embodiments or examples for implementing different features of the invention. Of course, these embodiments are only examples, and are not intended to limit the scope and application of the invention. Moreover, for the sake of clarity, the relative thickness and position of each element, film layer, or region may be reduced or enlarged. In addition, similar or identical reference numerals are used in each drawing to indicate similar or identical devices or features, and if there are identical reference numerals in the drawings, descriptions thereof will be omitted.

[0025] FIG. 3 is a diagram of a trench MOSFET according to the first embodiment of the invention.

[0026] Referring to FIG. 3, the trench MOSFET of the first embodiment includes a substrate 300, an epitaxial layer 302 having a first conductivity type, a source region 304 having the first conductivity type, a body region 306, a gate 308, a gate oxide layer 310 having a second conductivity type, and an anti-punch through region 312 having the second conductivity type. In the present embodiment, the first conductivity type is N-type, and the second conductivity type is P-type. However, the invention is not limited thereto. In another embodiment, the first conductivity type may be P-type, and the second conductivity type may be N-type. The epitaxial layer 302 is formed on the substrate 300, and the epitaxial layer 302 has a trench 314. Although FIG. 3 shows only one trench 314, it should be understood that the trench MOSFET for power devices actually has a plurality of trenches 314.

[0027] Please continue to refer to FIG. 3, the gate 308 is located in the trench 314, and the gate oxide layer 310 is located between the gate 308 and the trench 314. The source region 304 is located on a surface 302a of the epitaxial layer 302 on two sides of the trench 314, and the body region 306 is located in a portion of the epitaxial layer 302 below the source region 304. Generally, if the epitaxial layer 302 is an N-type epitaxial, the source region 304 is an N+ region. The anti-punch through region 312 is located at the interface of the body region 306 and the source region 304, wherein the doping concentration of the anti-punch through region 312 needs to be higher than the doping concentration of the body region 306. That is, if the body region 306 is a P-type well region, the anti-punch through region 312 is a P+ region relatively. In an embodiment, the doping concentration of the anti-punch through region 312 is, for example, between $5E+16$ atoms/cm³ and $5E+17$ atoms/cm³. In addition, an inner dielectric layer 316 may be formed to cover the epitaxial layer 302 and the gate 308.

[0028] FIG. 4 is a graph of a doping concentration along a sidewall of the trench gate structure of FIG. 3.

[0029] In FIG. 4, the epitaxial layer has one first pn junction 400a near the source region 304 and one second pn junction 400b near the substrate 300. Two equal portions are divided between the first pn junction 400a and the second pn junction 400b. The portion near the first pn junction 400a is set as a first region 404a and the portion near the second pn junction 400b is set as the second region 404b. However, the invention is not limited thereto. N portions may be divided between the first pn junction 400a and the second pn junction 400b, and N may be other integers greater than 1 besides 2. In FIG. 4, the doping concentration in the first region 404a is greater than the doping concentration in the second region 404b, and the first region 404a has an

integrated area of first doping concentration, the second region 404b has an integrated area of second doping concentration, and the integrated area of first doping concentration is greater than the integrated area of second doping concentration. Moreover, the anti-punch through region 312 located at the interface of the body region 306 and the source region 304 has a steep concentration distribution, so that the body resistivity here is reduced, thereby improving the UIS capabilities of the trench MOSFET. That is, in the invention, the closer the region is to the first pn junction 400a, the greater the doping concentration thereof is, and the closer the region is to the first pn junction 400a, the greater the integrated area of doping concentration thereof is. The manufacturing method of such a special doping concentration distribution is described later.

[0030] FIG. 5 is another doping concentration curve of the trench sidewall of the device of FIG. 3, wherein the same reference numerals as in FIG. 4 are used to indicate the same or similar regions, and the same or similar regions are as provided above and are not repeated herein.

[0031] The difference between FIG. 5 and FIG. 4 is that three equal portions are divided between the first pn junction 400a and the second pn junction 400b, i.e., a first region 500a near the first pn junction 400a, a third region 500c near the second pn junction 400b, and a second region 500b between the first region 500a and the third region 500c. The doping concentration in the first region 500a is greater than the doping concentration in the second region 500b, the doping concentration in the second region 500b is greater than the doping concentration in the third region 500c, the integrated area of doping concentration of the first region 500a is greater than the integrated area of doping concentration of the second region 500b, and the integrated area of doping concentration of the second region 500b is greater than the integrated area of doping concentration of the third region 500c. The manufacturing method of the doping concentration distribution is also described below.

[0032] FIG. 6 is a manufacturing process flowchart of a trench MOSFET according to the second embodiment of the invention. Moreover, according to the steps of the second embodiment, a doping concentration distribution as shown in FIG. 4 or FIG. 5 may be produced.

[0033] Referring to FIG. 6, step 5600 is first performed to form a trench gate in an epitaxial layer having a first conductivity type on a substrate. In the present embodiment, the first conductivity type is N-type, and the second conductivity type is P-type; and vice versa. The steps of forming the trench gate may be exemplified but not limited to: first forming a trench in the N-type epitaxial layer, forming a gate oxide layer on the surface of the trench, and then depositing a conductor in the trench as a gate, wherein the conductor is, for example, polysilicon.

[0034] Next, in step 5602, a plurality of implantations of a dopant having the second conductivity type is performed on the epitaxial layer in a manner that the implantation dose is gradually reduced in a direction toward the substrate. In the present embodiment, the implantation step may be a step of two or three implantations of a P-type dopant.

[0035] Then, in step S604, a first drive-in step is performed to diffuse the P-type dopant in the upper half of the N-type epitaxial layer to form a P-type body region. In addition, in order to avoid the mild N-type concentration at the bottom of the source region and the mild P-type concentration of the body region, the concentrations at the first

pn junction compensate each other, resulting in an increase in the resistivity of the body region. In the invention, by reducing the thermal budget of the process, the doping concentration distribution in the body region is close to the concentration distribution after the implantation step in step S602. For example, if the conventional drive-in step is a high-temperature and long-time process (for example, higher than 1000° C. for one hour), then step S604 adopts a high-temperature and short time (for example, higher than 1000° C. for 30 minutes or less) or the temperature is reduced and the time is shortened at the same time (such as 1000° C. or less and less than one hour). That is, when there are two implantations in step S602, the impurity concentration distribution of the formed body region is shown in FIG. 4. Moreover, if there are three implantations in step S602, the doping concentration distribution of the formed body region is as shown in FIG. 5.

[0036] Subsequently, in step S606, a dopant having a first conductivity type (such as N-type) is implanted on the surface of the epitaxial layer. Moreover, in order to have a steeper doping concentration distribution in the source region formed later, the energy of the implantation step is lower than the implantation performed in the conventional forming of the source region, for example, between 20 KeV and 45 KeV. However, the invention is not limited thereto. According to the design criteria of the trench MOSFET, the energy of the implantation step may be changed.

[0037] Next, in step S608, a second drive-in step is performed to diffuse a dopant having the first conductivity type (such as N-type) to form a source region. Similarly, in order to make the source region have a steeper doping concentration distribution, the process of the invention needs to further reduce the thermal budget, so the time of the second drive-in step needs to be shorter than the conventional drive-in step, for example, 5 minutes or less. For example, the second drive-in step may adopt rapid thermal processing (RTP).

[0038] Then, step S610 is performed after step S608. Without any photoresist mask, a dopant having the second conductivity type (such as P-type) is comprehensively implanted at the interface of the body region and the source region to form an anti-punch through region, wherein the doping concentration of the anti-punch through region is higher than the doping concentration of the body region, and a high-temperature drive-in step is not performed subsequently, so that a steep concentration distribution is formed at the interface of the body region and the source region as depicted by the straight line on the left side (toward the source region 304) of the first pn junction 400a in FIG. 4 and FIG. 5. In the present embodiment, the doping concentration of the anti-punch through region is, for example, between $5E+16$ atoms/cm³ and $5E+17$ atoms/cm³. However, the invention is not limited thereto. According to the size of the doping concentration of the body region, the doping concentration of the anti-punch through region may also be changed. Subsequent processes may be performed according to existing techniques and are not repeated herein.

[0039] Based on the above, in the invention, a special doping concentration distribution is formed between the body and the source via process control, thereby reducing

the body resistivity and thereby improving the UIS capabilities of the trench MOSFET.

[0040] Although the invention has been described with reference to the above embodiments, it will be apparent to one of ordinary skill in the art that modifications to the described embodiments may be made without departing from the spirit of the invention. Accordingly, the scope of the invention is defined by the attached claims not by the above detailed descriptions.

What is claimed is:

1. A manufacturing method of a trench MOSFET, comprising:

forming a trench gate in an epitaxial layer having a first conductivity type on a substrate;

performing a plurality of implantations of a dopant having a second conductivity type on the epitaxial layer in a manner that an implantation dose is gradually reduced toward a direction of the substrate;

performing a first drive-in step to diffuse the dopant having the second conductivity type in an upper half of the epitaxial layer to form a body region having the second conductivity type;

implanting a dopant having the first conductivity type on a surface of the epitaxial layer;

performing a second drive-in step to diffuse the dopant having the first conductivity type to form a source region; and

comprehensively implanting the dopant having the second conductivity type at an interface of the body region and the source region after the source region is formed to form an anti-punch through region, wherein a doping concentration of the anti-punch through region is higher than a doping concentration of the body region.

2. The manufacturing method of the trench MOSFET of claim 1, wherein a step of performing the plurality of implantations of the dopant having the second conductivity type comprises performing two or three implantations of the dopant having the second conductivity type.

3. The manufacturing method of the trench MOSFET of claim 1, wherein the doping concentration of the anti-punch through region is between $5E+16$ atoms/cm³ and $5E+17$ atoms/cm³.

4. The manufacturing method of the trench MOSFET of claim 1, wherein the first conductivity type is N-type and the second conductivity type is P-type.

5. The manufacturing method of the trench MOSFET of claim 1, wherein the first conductivity type is P-type and the second conductivity type is N-type.

6. The manufacturing method of the trench MOSFET of claim 1, wherein an energy of implanting the dopant having the first conductivity type is between 20 KeV and 45 KeV.

7. The manufacturing method of the trench MOSFET of claim 1, wherein the second drive-in step comprises rapid thermal processing (RTP).

8. The manufacturing method of the trench MOSFET of claim 1, wherein the step of forming the trench gate comprises:

forming a trench in the epitaxial layer;

forming a gate oxide layer on a surface of the trench; and depositing a conductor in the trench as a gate.

* * * * *