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Donovan

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(54) **SYSTEM-ON-CHIP POWER REDUCTION
THROUGH DYNAMIC CLOCK FREQUENCY**

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patent is extended or adjusted under 35
U.S.C. 154(b) by 423 days.

This patent is subject to a terminal dis-
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(63) Continuation of application No. 10/845,028, filed on
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10, 2004, provisional application No. 60/506,797,
filed on Sep. 29, 2003.

(51) **Int. Cl.**
G06F 1/32 (2006.01)

(52) **U.S. Cl.** **713/322; 713/321; 713/501; 713/503;**
710/107

(58) **Field of Classification Search** **713/321,**
713/322, 501, 503; 710/107, 112, 113
See application file for complete search history.

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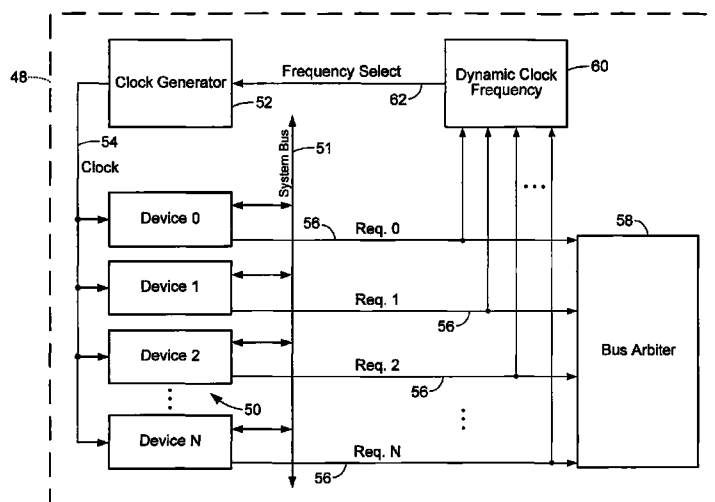
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Primary Examiner — Thuan Du

(57) **ABSTRACT**

A dynamic clock frequency module includes a request evalua-
tion module configured to generate a sum of requests to
utilize a system bus from a plurality of modules. A frequency
assignment module is configured to calculate a clock fre-
quency for the system bus in response to the requests and
adjust the clock frequency between at least two non-zero
frequency values. A pulse stretch module is configured to
increase a period of time that at least one of the requests is
asserted in response to the sum.

20 Claims, 9 Drawing Sheets



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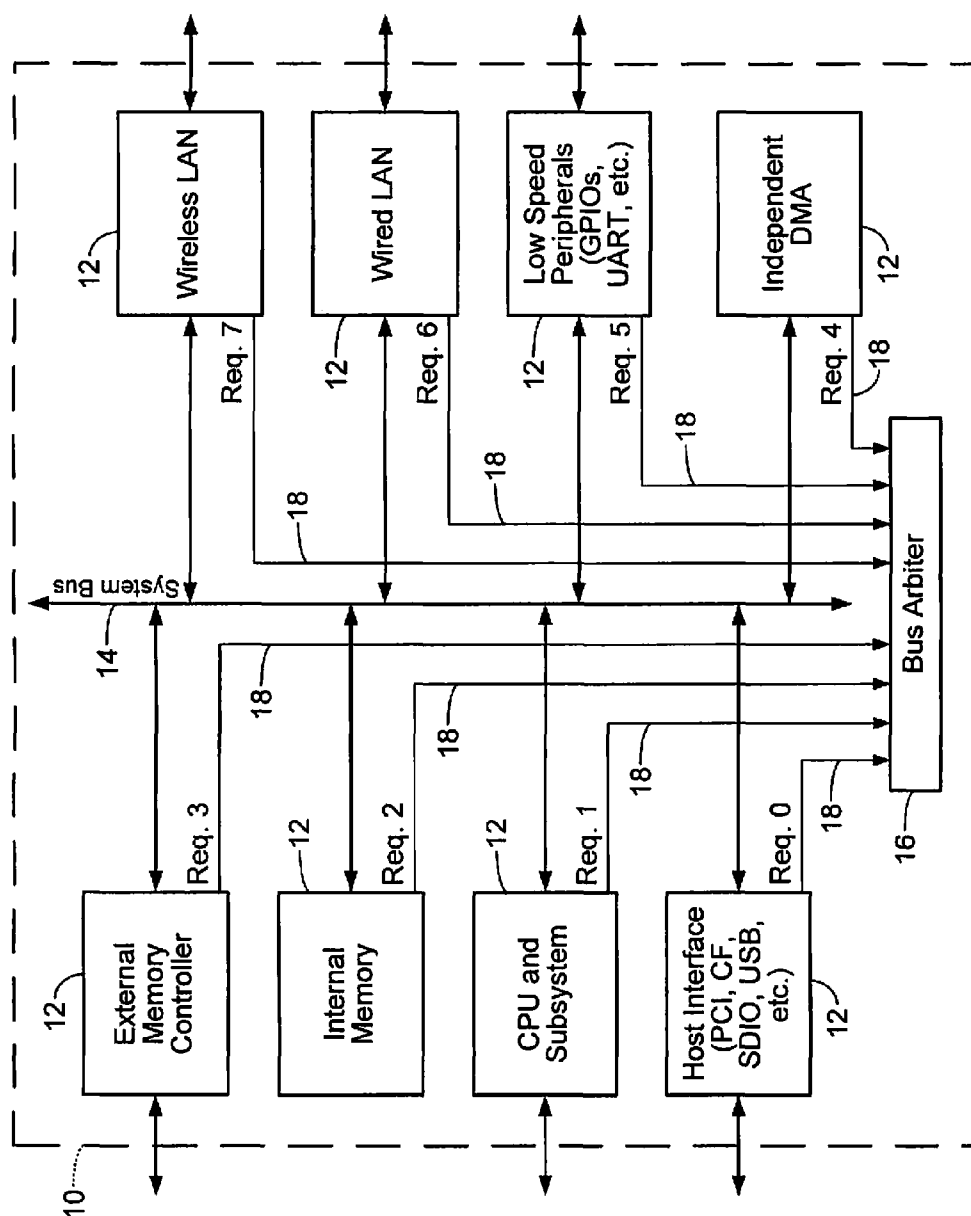


FIG. 1
Prior Art

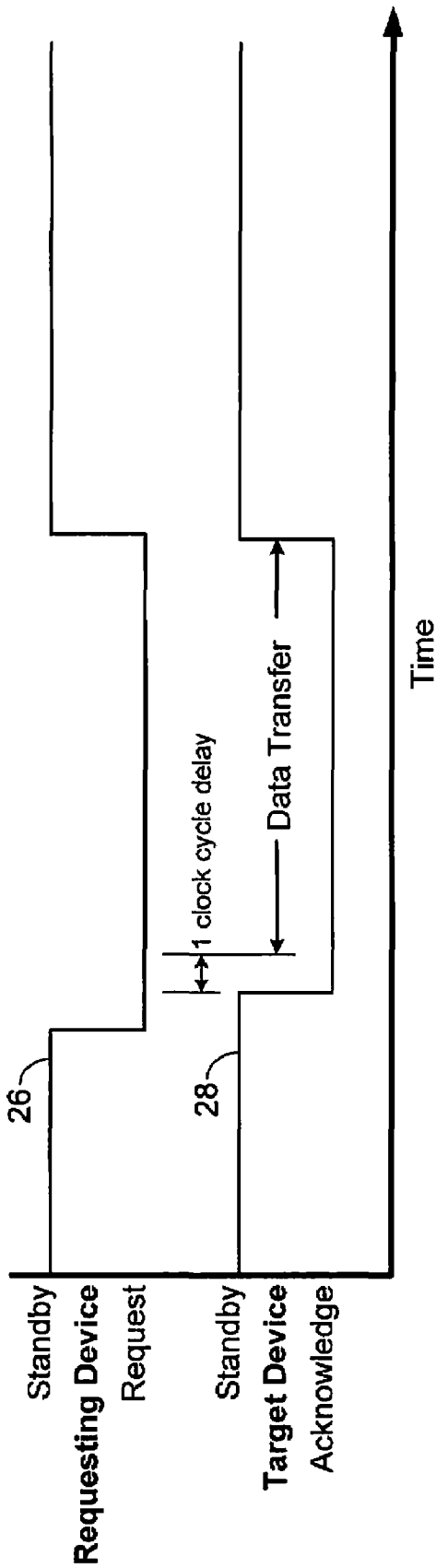


FIG. 2A
Prior Art

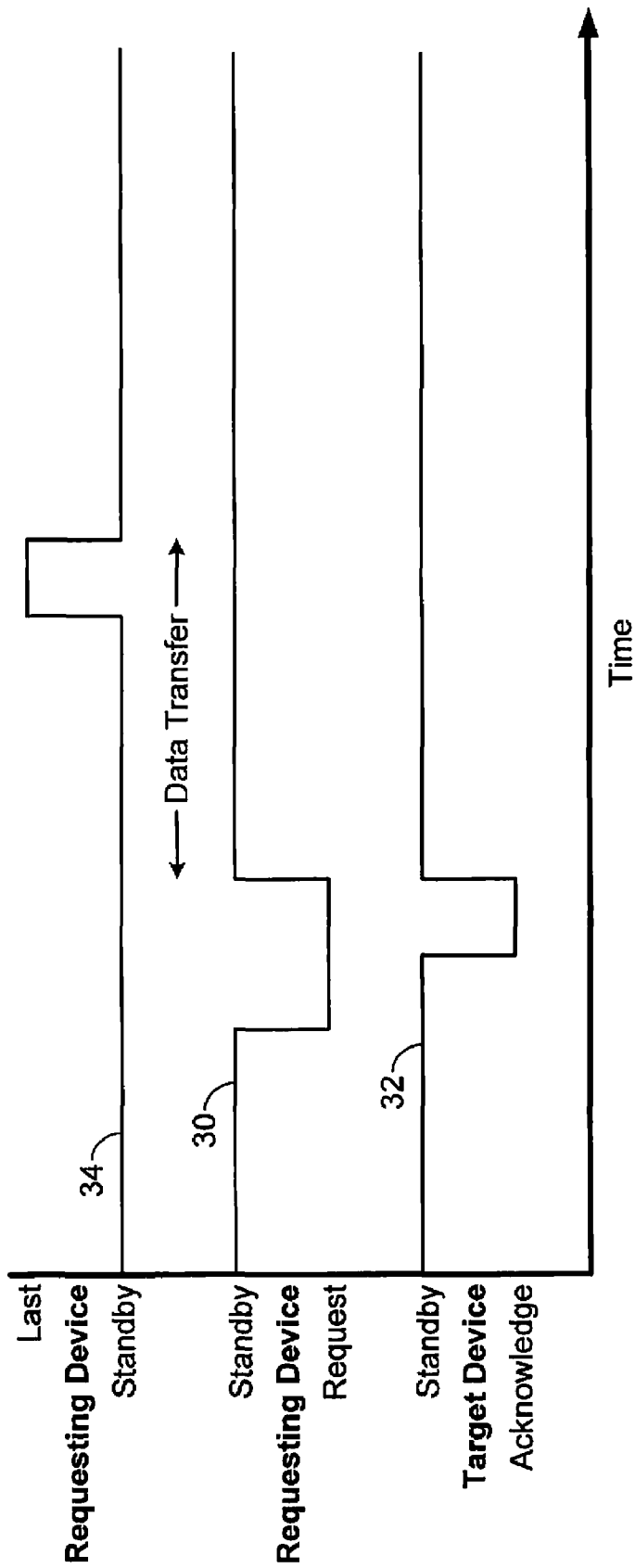


FIG. 2B
Prior Art

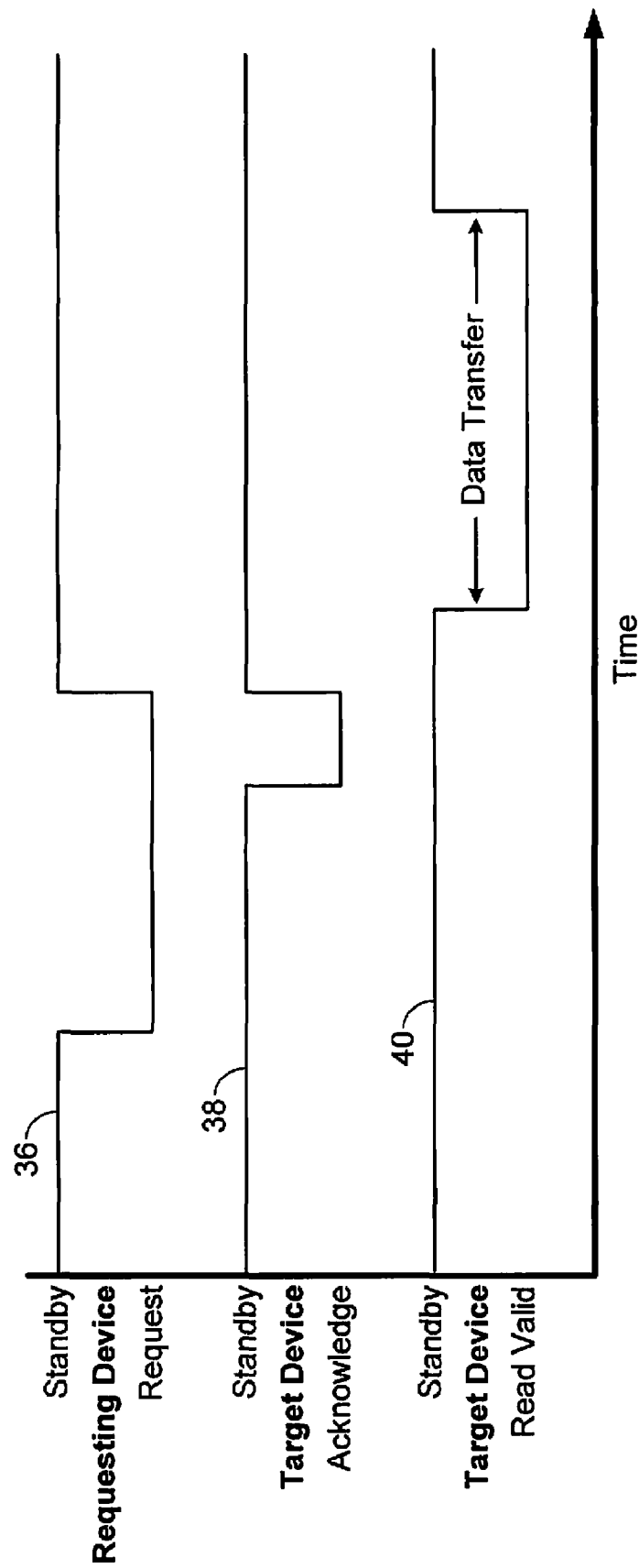


FIG. 2C
Prior Art

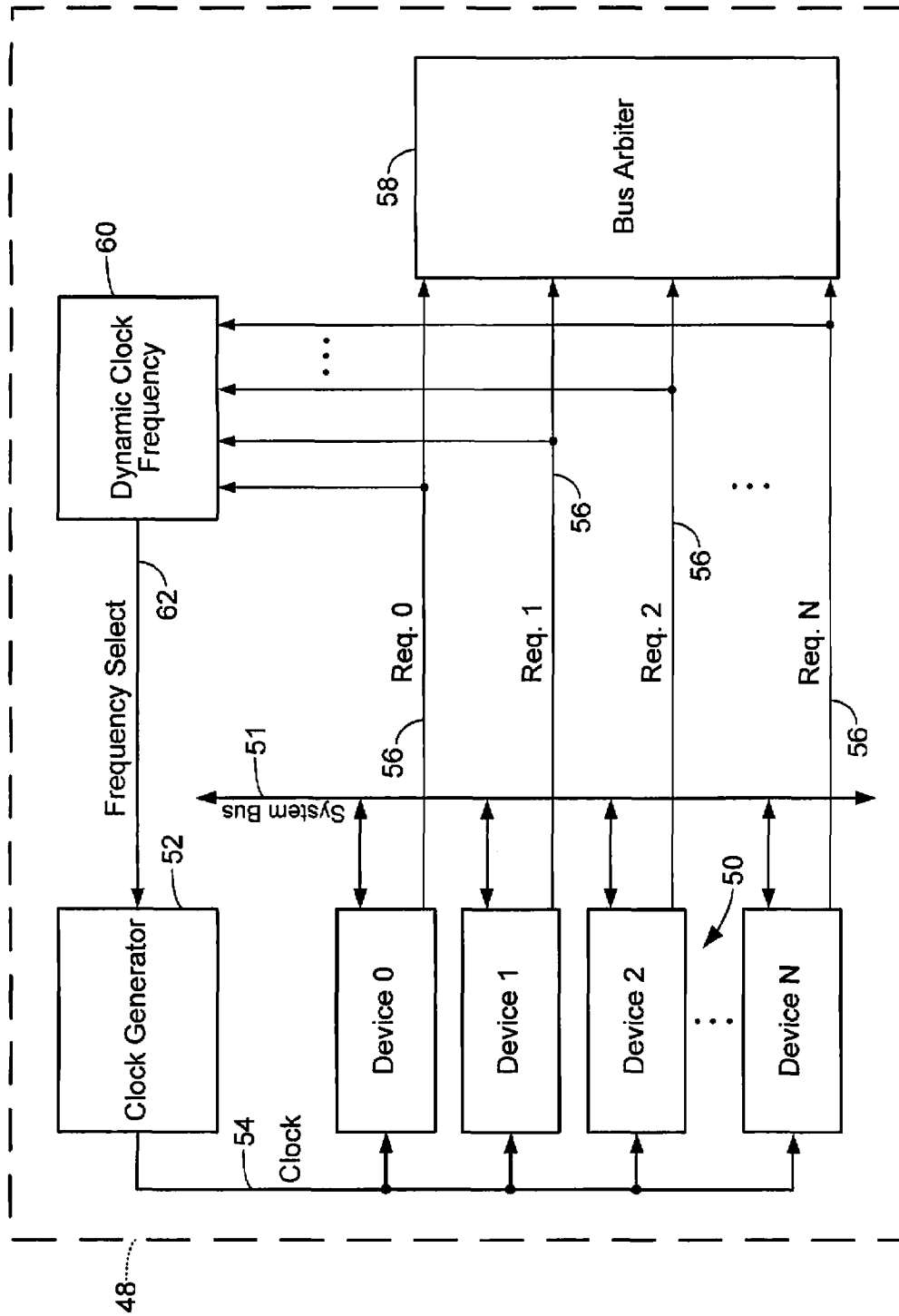


FIG. 3

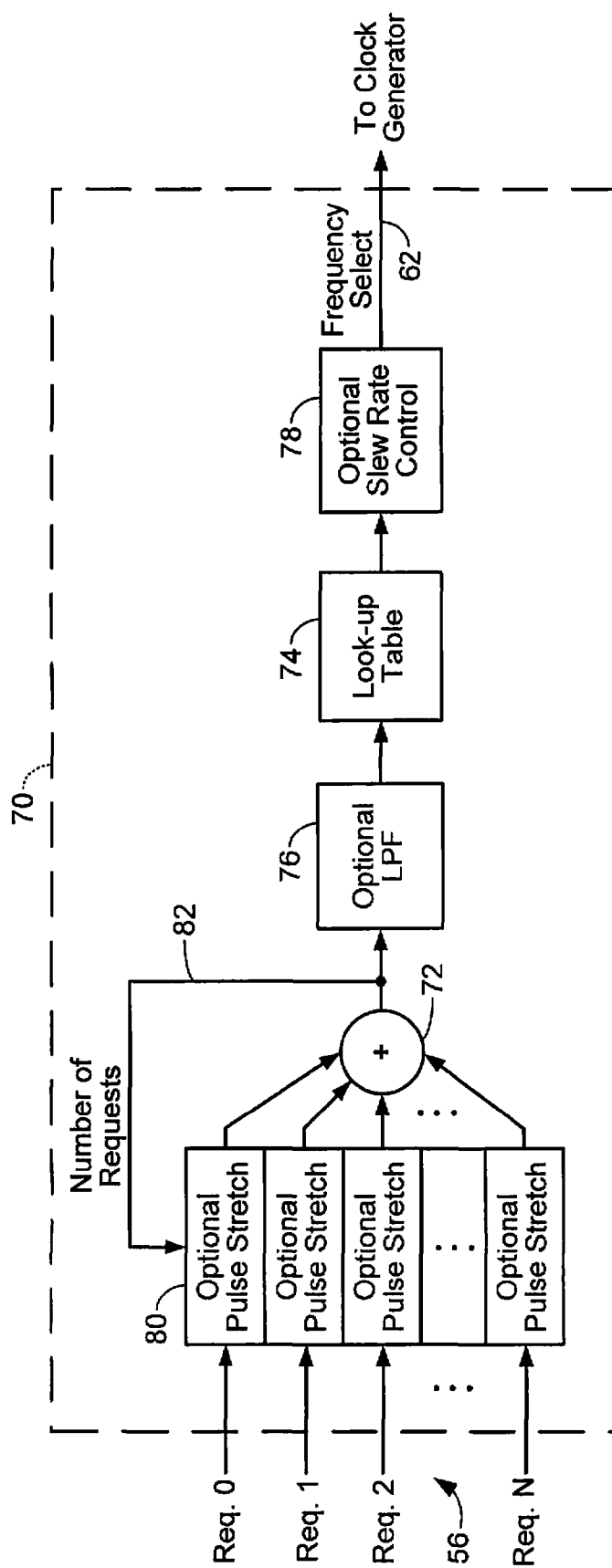


FIG. 4

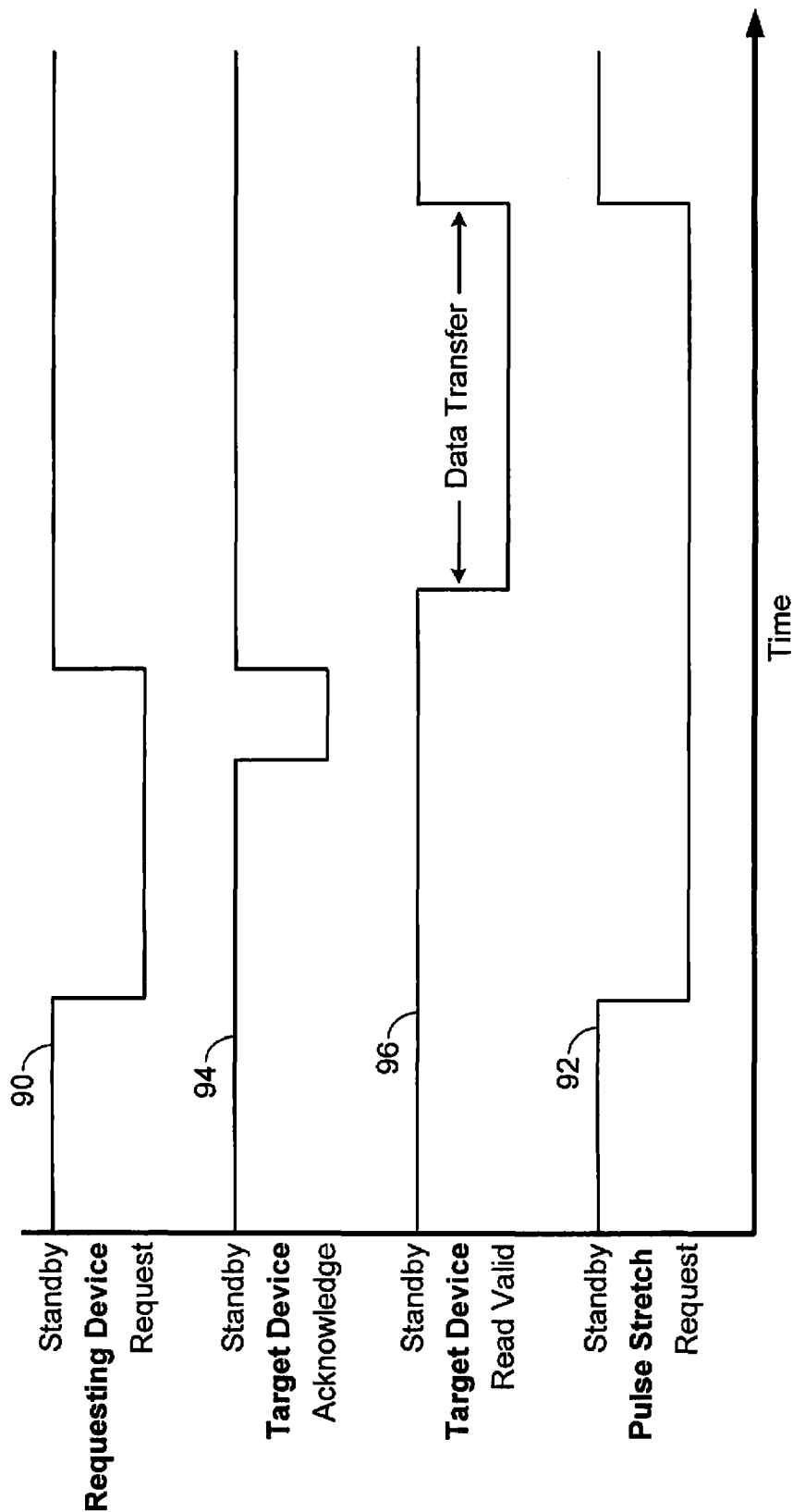


FIG. 5

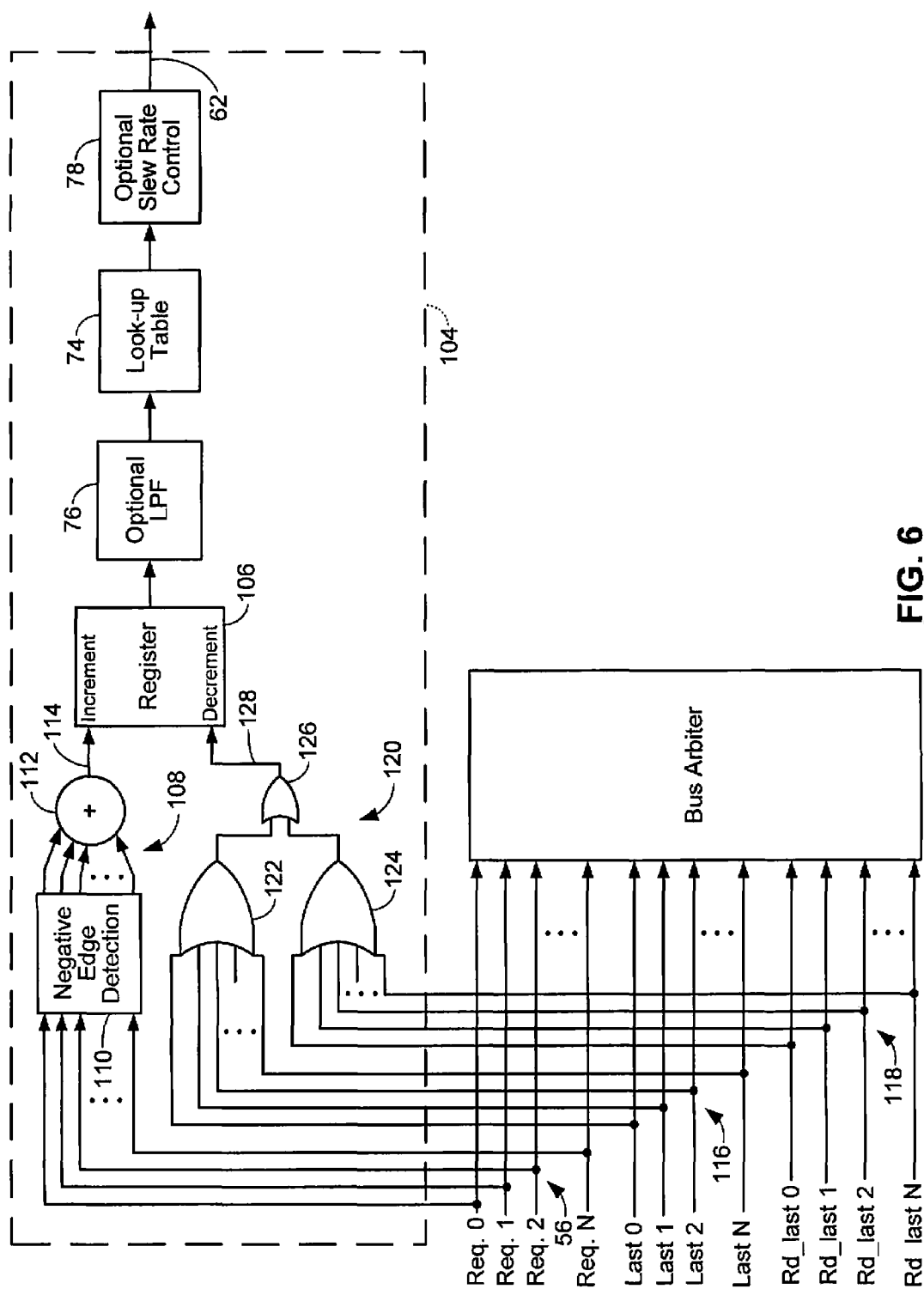


FIG. 6

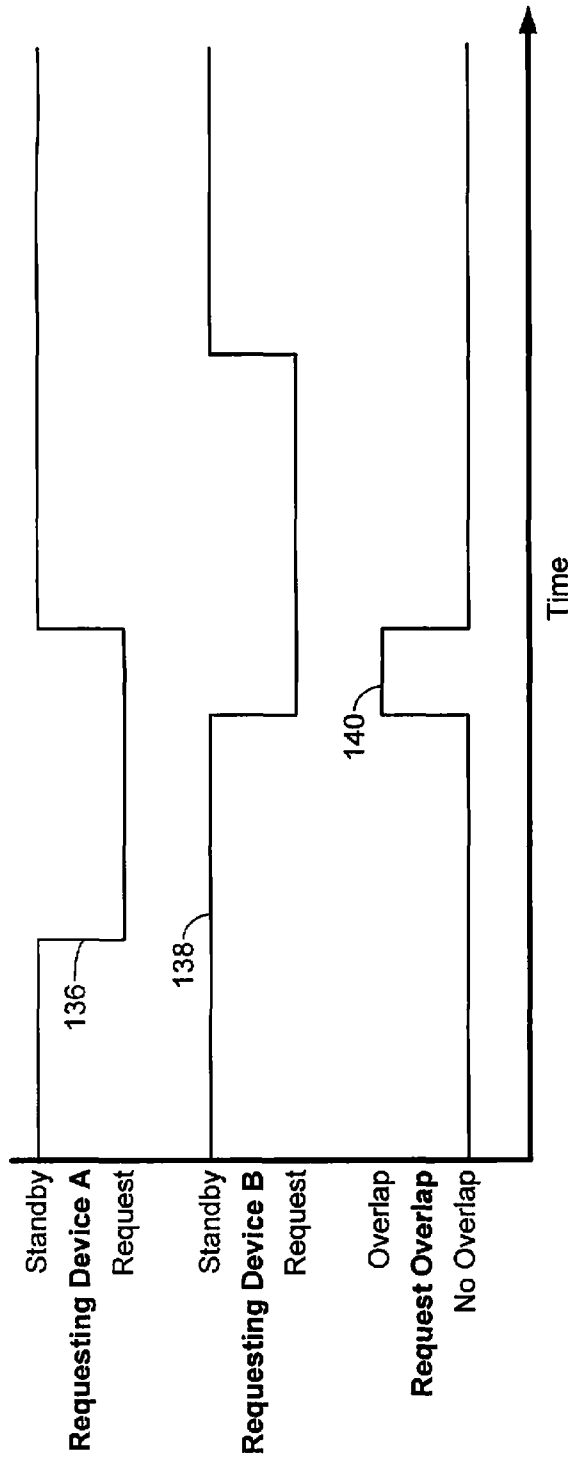


FIG. 7

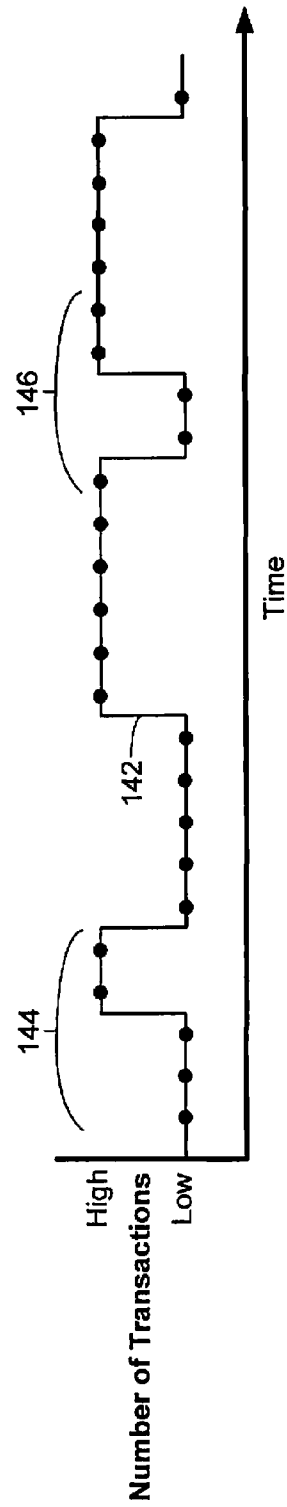


FIG. 8

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SYSTEM-ON-CHIP POWER REDUCTION THROUGH DYNAMIC CLOCK FREQUENCY

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 10/845,028, filed May 13, 2004, which claims the benefit of U.S. Provisional Application No. 60/506,797, filed Sep. 29, 2003, and U.S. Provisional Application No. 60/551,876, filed Mar. 10, 2004, which are all hereby incorporated by reference in their entirety.

FIELD OF THE INVENTION

The present invention relates to wireless network devices, and more particularly to reducing power dissipation in wireless network devices.

BACKGROUND OF THE INVENTION

Laptop computers, personal digital assistants (PDAs), and other mobile devices often incorporate wireless local area network (WLAN) technology that typically operates using battery power. Therefore, it is important to minimize power dissipation in mobile devices to preserve battery life. Sometimes WLAN circuits are implemented as a system-on-chip (SOC).

Referring now to FIG. 1, an SOC 10 for a wireless network device includes modules 12 that communicate with each other over a system bus 14. The modules 12 include memory modules, processors, host interfaces, peripheral interfaces, local area network (LAN) interfaces, and/or other modules. The wireless network device may communicate with other external devices. For example, the wireless network device may communicate with an external radio frequency (RF) transmitter. Since the modules 12 communicate through a common system bus 14, most of the modules 12 are clocked at the same rate as the system bus 14 or at rates that are derived from the system bus 14 rate.

Only one of the modules 12 is allowed to access the system bus 14 at a given time. Since more than one of the modules 12 may simultaneously attempt to use the system bus 14, a bus arbiter module 16 determines which of the modules 12 has permission to use the system bus 14 at a given time. When one of the modules 12 requires use of the system bus 14, the module 12 requests permission from the bus arbiter module 16. The modules 12 request permission by asserting request signals 18 that are transmitted to the bus arbiter module 16.

Referring now to FIG. 2A, a request signal 26 from a requesting module remains high (or low) when the requesting module does not require use of the system bus 14. When the requesting module requires use of the system bus 14, the requesting module transitions to low (or high). During a write operation, the request signal 26 typically remains asserted until the end of the transaction. The bus arbiter module 16 detects the request signal 26 and instructs a target module to assert an acknowledge signal 28 when the requesting module is free to use the system bus 14.

Once the target module asserts the acknowledge signal 28, the requesting module begins transmitting data to the target module following a single clock cycle delay. At the end of the write transaction, the request signal 26 will transition to high (or low).

Referring now to FIG. 2B, in other bus architectures, the request signal 30 will transition to high (or low) when the

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acknowledge signal 32 is received. In this case, a last signal 34 is asserted to indicate the end of the transaction.

Referring now to FIG. 2C, during a read transaction, a request signal 36 typically does not remain asserted during the entire transaction. When the requesting module requires use of the system bus 14, the module asserts the request signal 36 by transitioning to low (or high). The bus arbiter module 16 detects the request signal and instructs the target module to assert an acknowledge signal 38. During a read transaction, it typically takes the target module time to retrieve the requested data. Therefore, the acknowledge signal 38 is only asserted for a single clock cycle.

At the end of the clock cycle both the request signal 36 and the acknowledge signal 38 transition to high (or low). This allows other modules 12 in the SOC 10 to use the system bus 14 while the target module retrieves the requested data. The target module asserts a read valid signal 40 to request permission to use the system bus 14. After the bus arbiter module 16 grants permission, the target module begins transmitting data to the requesting module. This is called a split-read process. The read valid signal 40 remains low (or high) while the target module transmits data. The read valid signal 40 transitions to high (or low) when the target module is finished transmitting data to the requesting module.

Power dissipation in an SOC is proportional to the clock frequency. Therefore, power dissipation is minimized by minimizing the clock frequency of the system bus in the SOC. A minimum sufficient clock frequency for an SOC is dependant on the amount of data movement and a number of current computations. Therefore, the minimum clock frequency that sufficiently supports all data traffic will change as the amount of data traffic changes.

In one conventional approach, a clock frequency of an SOC is set to a frequency that is sufficient to handle data traffic in a worst case scenario. However, in this case, power is unnecessarily dissipated when the data traffic in the SOC is lower.

SUMMARY OF THE INVENTION

A dynamic clock frequency module for a system-on-chip (SOC) including modules that communicate over a system bus according to the present invention includes a request evaluation module that receives requests to utilize the system bus from the modules. A frequency assignment module calculates a clock frequency value for the system bus based on the requests received by the request evaluation module.

In other features, the request evaluation module includes a summing module that generates a sum of requests between the modules. A pulse stretch module communicates with the summing module and increases a period of time that at least one of the requests is asserted. The pulse stretch module increases the period of time based on the sum. The pulse stretch module increases the period of time to an estimated transaction duration.

In still other features of the invention, a low pass filter has an input that communicates with the summing module and an output that communicates with the frequency assignment module. The low pass filter prevents changes to the clock frequency value when the sum at least one of increases and decreases for less than a predetermined period. The low pass filter is one of a linear filter and a median filter. A slew rate control module communicates with the frequency assignment module and adjusts at least one of a rate of increase and a rate of decrease in the clock frequency value.

In yet other features, only one of the modules utilizes the system bus at a time. A bus arbiter module that receives the request signals selectively grants the modules access to the

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system bus. The SOC is implemented in a wireless local area network (LAN) device. The wireless LAN device is compliant with one of IEEE 802.11, 802.11a, 802.11b, 802.11g, and 802.11n. The frequency assignment module transmits the clock frequency value to a clock generator, which adjusts a clock frequency of the system bus based thereon. An SOC comprises the dynamic clock frequency module, the modules, and the system bus.

Further areas of applicability of the present invention will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples, while indicating the preferred embodiment of the invention, are intended for purposes of illustration only and are not intended to limit the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description and the accompanying drawings, wherein:

FIG. 1 is a functional block diagram of a system-on-chip (SOC) for a wireless network device according to the prior art;

FIG. 2A is a timing diagram that illustrates a write transaction between modules in the SOC according to the prior art;

FIG. 2B is a timing diagram that illustrates a write transaction between modules in the SOC when the request signal is not present during the entire transaction according to the prior art;

FIG. 2C is a timing diagram that illustrates a read transaction between modules in the SOC according to the prior art;

FIG. 3 is a functional block diagram of an SOC that includes a dynamic clock frequency module according to the present invention;

FIG. 4 is a functional block diagram of a dynamic clock frequency module that includes a pulse stretch module;

FIG. 5 is a timing diagram that illustrates a read transaction with a pulse stretch module that increases the period that the request signal is asserted;

FIG. 6 is a functional block diagram of a dynamic clock frequency module that detects a number of outstanding transactions between modules in an SOC;

FIG. 7 is a timing diagram that illustrates brief changes in a number of outstanding transactions between modules in an SOC; and

FIG. 8 is a timing diagram that illustrates operation of a median low pass filter in the dynamic clock frequency module.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following description of the preferred embodiment(s) is merely exemplary in nature and is in no way intended to limit the invention, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify similar elements. As used herein, the term module and/or device refers to an application specific integrated circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and memory that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality.

Power dissipation in a system-on-chip (SOC) is minimized by minimizing the clock frequency of the system bus of the SOC. The clock frequency is dynamically changed according to the present invention based on the data traffic to reduce

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power consumption. Modules within the SOC assert request signals to request permission to use the system bus. The request signals are used to determine the number of outstanding transactions in the SOC. The clock frequency is adjusted based on the number of outstanding transactions. However, brief changes in clock frequency are undesirable. Therefore, the clock frequency is preferably not adjusted when short fluctuations in the number of outstanding requests occur. Additionally, changes to the clock frequency are limited in magnitude to reduce the change in current to which the voltage regulator responds.

Referring now to FIG. 3, an SOC 48 includes N modules 50 that communicate with each other over a system bus 51. A clock generator 52 transmits a clock signal 54 to the modules 50. For example, the clock generator 52 may include a phase-locked loop (PLL) module, an external crystal oscillator (XOSC), and/or any other suitable clock generator. The clock signal 54 synchronizes the modules 50. The system bus 51 operates at the frequency of the clock signal 54. The modules 50 transmit request signals 56 to a bus arbiter module 58. The modules 50 assert request signals 56 to request permission from the bus arbiter module 58 to use the system bus 51.

A dynamic clock frequency module 60 according to the present invention also receives the request signals 56. The dynamic clock frequency module 60 determines the number of outstanding transactions based on the request signals 56. The dynamic clock frequency module 60 determines a clock frequency value based on the number of outstanding transactions. The clock frequency value has a minimum frequency that is sufficient to manage the current amount of data traffic in the SOC 48. The dynamic clock frequency module 60 transmits a frequency select signal 62 to the clock generator 52. The clock generator 52 adjusts the clock frequency of the system bus 51 based on the frequency select signal 62.

Referring now to FIG. 4, an exemplary dynamic clock frequency module 70 includes a summing module 72 that sums the request signals 56 from the modules 50 in the SOC 48. Therefore, an output of the summing module 72 indicates the number of outstanding requests. An input of a look-up table 74 receives the signal from the summing module 72. The look-up table 74 assigns a corresponding output value to each input value and outputs the corresponding output value on the frequency select signal 62. Therefore, each number of outstanding requests corresponds to a frequency value. However, the output values are not necessarily unique to each input value. For example, a range in the number of outstanding requests may correspond with a single output value.

When the number of outstanding requests is low, there is a small amount of data that needs to be transmitted between modules 50. Therefore, the system bus 51 can operate at a lower clock frequency without sacrificing performance. When the number of outstanding requests is high, there is a large amount of data that needs to be transmitted between modules 50. In this case, the clock frequency of the system bus 51 is increased to prevent significant delays in data transmissions. As can be appreciated, a mathematic formula or other methods may be used instead of the lookup table 74.

Brief variations in supply current from a voltage regulator that regulates voltage for the SOC 48 can cause performance degradation. Also, little power is saved from brief reductions in the clock frequency of the system bus 51. Therefore, the dynamic clock frequency module 70 optionally includes a low pass filter 76 having an input that communicates with the summing module 72 and an output that communicates with the look-up table 74. The low pass filter 76 prevents changes in the clock frequency due to brief changes in the number of outstanding requests.

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The low pass filter **76** filters out changes in the number of outstanding requests that occur for less than a predetermined time period. The low pass filter **76** may be any conventional type of low pass filter. For example, the low pass filter **76** may be a median filter that stores prior samples and outputs a median value of the prior samples. The low pass filter **76** may also be a linear filter that averages prior samples and outputs the average. A low pass filter **76** may also assign weighting factors to specific positions of samples in a list of previous samples. Still other filters can be employed.

If the number of outstanding requests increases from a very low value to a very high value, the look-up table **74** detects the increase and increases the clock frequency of the system bus **51**. However, if a sharp change in frequency occurs, current drawn from a voltage regulator that regulates power for the SOC **48** also changes sharply. Some voltage regulators are sensitive to sharp changes in load current and have trouble settling and/or maintaining a voltage when the sharp changes occur. Therefore, the dynamic clock frequency module **70** optionally includes a slew rate control module **78** that communicates with the look-up table **74**.

The slew rate control module **78** controls the rate of change in the value of frequency select signal **62**. The slew rate control module **78** adjusts the rate of increase and/or decrease in the value of the frequency select signal **62**. The slew rate control module **78** may also set a minimum time that the frequency select signal **62** remains at a given frequency before changing to a new value.

While both the low pass filter **76** and the slew rate control module **78** are optional modules, either module may be utilized individually or both modules may be utilized simultaneously. For example, a median low pass filter that is used in combination with a slew rate control module **78** provides a significant level of control over the operation of the dynamic clock frequency module **70**.

As illustrated in FIGS. 2B and 2C, request signals **56** do not always remain asserted for the entire duration of a transaction. For example, during read transactions, request signals **56** remain asserted until an acknowledge signal is asserted. The request signal is not asserted while the target module is actually transmitting data to the requesting module. Therefore, the number of outstanding transactions that the look-up table **74** detects is not accurate while at least one module is executing a read transaction. Therefore, the dynamic clock frequency module **70** optionally includes a pulse stretch module **80** that communicates with the summing module **72**.

The pulse stretch module **80** detects when one of the request signals **56** is asserted and increases the amount of time that the request signal **56** is asserted to an estimated transaction time. For example, the pulse stretch module **80** increases the amount of time to an average write and/or read transaction time. In the event that there are at least two other outstanding transactions, increasing the amount of time that the request signal **56** is asserted to a single average transaction time is insufficient. Therefore, the pulse stretch module **80** preferably receives a feedback signal **82** from the output of the summing module **72**.

The feedback signal **82** indicates the current number of outstanding transactions. This allows the pulse stretch module **80** to increase the amount of time that a request signal is asserted to a single average transaction time plus the average transaction time multiplied by the number of other outstanding transactions. For example, if there are four other outstanding transactions at a given time, the pulse stretch module **80** increases the time that a new request signal is asserted to five average transaction times. This allows the look-up table **74** to accurately detect the number of outstanding transactions

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when the request signal of at least one outstanding transaction does not remain asserted for the entire duration of the transaction. This also allows the look-up table **74** to adjust the clock frequency of the system bus **51** to appropriate levels at all times.

Referring now to FIG. 5, operation of the pulse stretch module **80** is illustrated. When a request signal **90** for a requesting module on a read transaction is asserted, an output signal **92** of the pulse stretch module **80** is also asserted. At this time, the pulse stretch module **80** determines the current number of outstanding transactions. In the scenario illustrated in FIG. 5, there are no additional outstanding transactions. Therefore, the output signal **92** of the pulse stretch module **80** is asserted for a single average transaction time.

When a target module asserts an acknowledge signal **94**, both the request signal **90** and the acknowledge signal **94** transition to high (or low). However, the output signal **92** of the pulse stretch module **80** remains asserted so that the look-up table **74** may accurately detect the number of outstanding transactions. The target module does not begin transmitting data to the requesting module until a read valid signal **96** is asserted. Without the pulse stretch module **80**, the look-up table **74** detects the end of the current transaction when the request signal **90** transitions to high (or low). This occurs before any data is actually transmitted to the requesting module.

Referring now to FIG. 6, an exemplary dynamic clock frequency module **104** includes a register **106** or other memory device before the look-up table **74**. The register **106** indicates a current number of outstanding transactions between the modules **50**. The register **106** includes two inputs. The register **106** is incremented when a signal at the first input of the register **106** is asserted. The register **106** is decremented when a signal at the second input of the register **106** is asserted. The request signals **56** are input to a request detection circuit **108**. The request detection circuit **108** includes a negative edge detection module **110** and a summing module **112**.

The negative edge detection module **110** asserts a corresponding output signal when one of the request signals **56** is asserted. For example, if the request signals **56** are active low, the negative edge detection module **110** asserts a corresponding output signal when one of the request signals **56** transitions to low (or high). The summing module **112** sums outputs of the negative edge detection module **110**. This ensures that the register **106** is incremented for each of the request signals **56** that are asserted when multiple request signals **56** are simultaneously asserted. An output signal **114** of the summing module **112** is received by the first input of the register **106**.

In addition to the request signals **56**, the bus arbiter module **58** also receives write last and read last signals **116** and **118**, respectively, from the modules **50**. Write last signals **116** are asserted at conclusions of write transactions. For example, a rising edge of an acknowledge signal in a write transaction indicates the end of the transaction. Read last signals **118** are asserted at conclusions of read transactions. The write last and read last signals **116** and **118**, respectively, are also input to a transaction detection circuit **120**. The transaction detection circuit **120** includes first, second, and third logic OR gates **122**, **124**, and **126**, respectively.

The first logic OR gate **122** receives the write last signals **116**, and the second logic OR gate **124** receives the read last signals **118**. An output of the first logic OR gate **122** is transmitted to a first input of the third logic OR gate **126**, and an output of the second logic OR gate **124** is transmitted to a second input of the third logic OR gate **126**. An output signal

128 of the third logic OR gate 126 is received by the second input of the register 106. Since only one transaction may end at a time, a summing module is not required in the transaction detection circuit 120.

When any one of the write last and read last signals 116 and 118, respectively, are asserted, the output of the third logic OR gate 126 is asserted, which decrements the register 106. While three logic OR gates are shown in the transaction detection circuit 120 of FIG. 6, a single logic OR gate with a sufficient number of inputs, additional logic OR gates, and/or other types of logic gates may be used. Therefore, the register 106 retains an accurate count of the number of outstanding transactions. Additionally, average transaction time estimations that occur with configurations including pulse stretch modules are avoided.

Referring now to FIG. 7, the low pass filter 76 preferably filters brief increases in the number of outstanding transactions. First and second request signals 136 and 138, respectively, are both asserted for only a brief period of time. An overlap signal 140 indicates when both the first and second request signals 136 and 138, respectively, are asserted. The low pass filter 76 prevents the look-up table 74 from detecting the brief overlap period and unnecessarily increasing the clock frequency of the system bus 51.

Referring now to FIG. 8, a median low pass filter examines the prior number of samples of outstanding transactions. The median low pass filter outputs the middle value when the samples are arranged in an increasing order. An exemplary signal 142 illustrated in FIG. 8 alternates between a high and a low number for varying periods of time. A median low pass filter may be programmed to remove pulses within a specific pulse width range. For example, a median low pass filter may be programmed to filter out pulses that are two samples wide or smaller. This may be accomplished by programming the median low pass filter to examine five or more prior samples at a time. For example, if the first five samples, illustrated at 144, in FIG. 8 are examined and organized in an increasing order, the median value is the low value.

The median low pass filter prevents the look-up table 74 from detecting the brief increase in the number of outstanding transactions. Similarly, if five samples that include a pair of low values, illustrated at 146, are examined and organized in an increasing order, the median value is the high value. The median low pass filter prevents the look-up table 74 from detecting the brief decrease in the number of outstanding transactions. Therefore, a median low pass filter is very effective at filtering out pulses in digital signals.

In order to implement a dynamic clock frequency system, the look-up table 74 adjusts the clock frequency of the system bus 51 while remaining synchronized with the modules 50. Therefore, clock multiplexer (MUX) circuits are preferably employed to ensure that a current clock is disabled and a new clock is enabled at the same point in the clock cycle.

The present invention reduces power dissipation in SOC's, which are typically included in battery powered wireless network devices. The dynamic clock frequency module dynamically adjusts the clock frequency of a system bus based on a number of outstanding transactions between modules in the SOC. This allows the clock frequency to remain as low as possible while retaining a minimum level of performance for modules that are currently using the system bus.

Those skilled in the art can now appreciate from the foregoing description that the broad teachings of the present invention can be implemented in a variety of forms. Therefore, while this invention has been described in connection with particular examples thereof, the true scope of the invention should not be so limited since other modifications will

become apparent to the skilled practitioner upon a study of the drawings, specification, and the following claims.

What is claimed is:

1. A dynamic clock frequency module comprising:

a request evaluation module configured to generate a sum of requests to utilize a system bus from a plurality of modules;

a frequency assignment module configured to calculate a clock frequency for the system bus in response to the requests, and adjust the clock frequency between at least two non-zero frequency values; and

a pulse stretch module configured to increase a period of time that at least one of the requests is asserted in response to the sum.

2. The dynamic clock frequency module of claim 1, wherein the pulse stretch module is configured to increase the period of time to an estimated transaction duration.

3. The dynamic clock frequency module of claim 1, further comprising a filter, wherein the filter includes:

an input in communication with the request evaluation module; and

an output in communication with the frequency assignment module.

4. The dynamic clock frequency module of claim 3, wherein the filter is configured to prevent changes to the clock frequency when the sum at least one of increases and decreases for less than a predetermined period.

5. The dynamic clock frequency module of claim 4, wherein:

the frequency assignment module transmits the clock frequency to a clock generator; and

the clock generator adjusts a bus clock frequency of the system bus in response to the clock frequency.

6. The dynamic clock frequency module of claim 3, wherein the filter is a linear filter or a median filter.

7. The dynamic clock frequency module of claim 1, further comprising a slew rate control module configured to adjust at least one of a rate of increase and a rate of decrease in the clock frequency.

8. The dynamic clock frequency module of claim 1, wherein only one of the plurality of modules utilizes the system bus at a time.

9. The dynamic clock frequency module of claim 1, further comprising a bus arbiter module configured to selectively grant the plurality of modules access to the system bus in response to the requests.

10. A system on chip (SOC) comprising:

the dynamic clock frequency module of claim 1;

the plurality of modules; and

the system bus.

11. A dynamic clock frequency module comprising:

memory configured to store a number of incomplete transactions between a plurality of modules that communicate over a system bus;

a frequency assignment module configured to calculate a clock frequency for the system bus based on the number of incomplete transactions; and

a request detection module configured to detect requests to use the system bus, increment the number of incomplete transactions following detection of one of the requests, detect when the requests are asserted, and generate a sum of request signal assertions.

12. The dynamic clock frequency module of claim 11, wherein the request detection module is configured to detect the requests to utilize the system bus from the modules.

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13. The dynamic clock frequency module of claim 11, further comprising a transaction detection module configured to:

detect conclusions to transactions between the plurality of modules; and
decrement the number of incomplete transactions when the transaction detection module detects one of the conclusions.

14. The dynamic clock frequency module of claim 11, wherein the request detection module includes:

an edge detection module configured to detect when the requests are asserted; and
a summing module configured to generate a sum of simultaneous request signal assertions.

15. The dynamic clock frequency module of claim 11, further comprising a filter, wherein the filter includes:

an input in communication with the memory; and
an output in communication with the frequency assignment module.

16. The dynamic clock frequency module of claim 15, wherein the filter is configured to prevent changes to the clock

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frequency when the sum at least one of increases and decreases for less than a predetermined period.

17. The dynamic clock frequency module of claim 16, wherein:

the frequency assignment module transmits the clock frequency to a clock generator; and
the clock generator adjusts a bus clock frequency of the system bus based on the clock frequency.

18. The dynamic clock frequency module of claim 15, wherein the filter is a linear filter or a median filter.

19. The dynamic clock frequency module of claim 11, further comprising a slew rate control module configured to adjust at least one of a rate of increase and a rate of decrease of the clock frequency.

20. The dynamic clock frequency module of claim 11, further comprising a bus arbiter module configured to selectively grant the modules access to the system bus.

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