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(71) Applicant (for all designated States except US): **ANALOG DEVICES, INC.** [US/US]; 1 Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **NGUYEN, Khiem** [CA/US]; 406 North Billerica Road, Tewksbury, MA 01876 (US).

(74) Agents: **CONNORS, Matthew, E.** et al.; Gauthier & Connors LLP, 225 Franklin Street, Suite 2300, Boston, MA 02110 (US).

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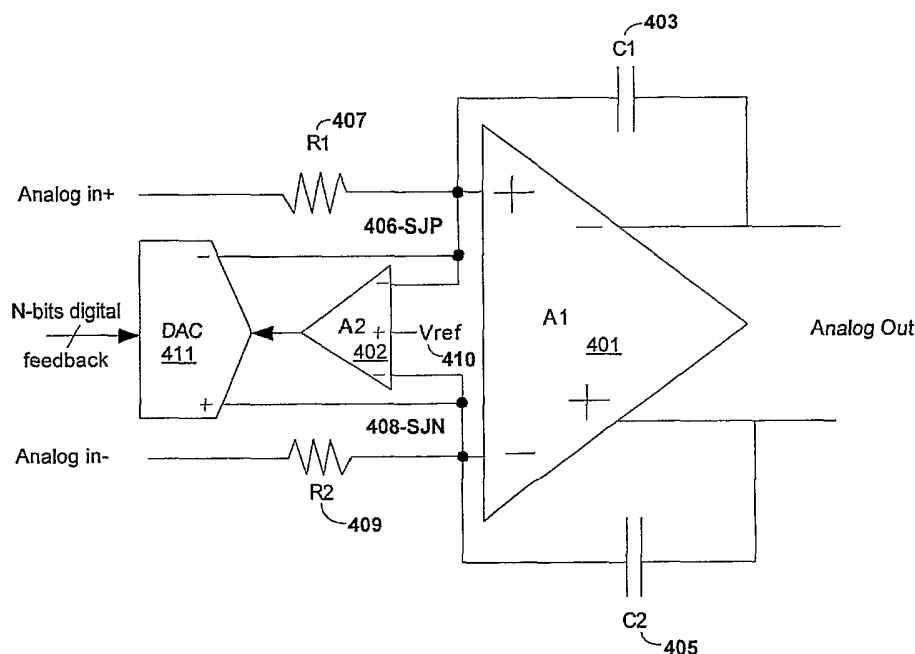
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(54) Title: AN INPUT COMMON-MODE VOLTAGE FEEDBACK CIRCUIT FOR CONTINUOUS-TIME SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER



(57) Abstract: A novel circuit is used to monitor the common-mode voltage at the summing junctions of the first integrator in a continuous-time $\Sigma\Delta$ ADC, wherein the circuit produces a control voltage which adjusts the quiescent current of the feedback DAC to compensate for any common-mode offset current. Since the adjustment takes place within the feedback DAC, there is no extra noise added to the differential signal path. The implementation provides for no degradation to the SNR of the converter.

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An Input Common-Mode Voltage Feedback Circuit for Continuous-Time Sigma-**Delta Analog-to-Digital Converter****BACKGROUND OF THE INVENTION**

This invention relates to mixed-signal converters of the sigma-delta noise shaping type, and more particularly, to mixed-signal analog-to-digital converter that employs a common-mode voltage feedback circuit.

Sigma-delta analog-to-digital converters (ADCs) provide for a means to achieve high resolution and low distortion at a relatively low cost compared to traditional Nyquist converters. The high resolution is achieved by oversampling the input signal and shaping the quantization noise in the band of interest into higher frequency region. The higher frequency noise can then be digitally filtered out by the subsequent digital filter stages. The resulting data is then down sampled to the desired sample rate at the output of the converter.

Typically, an audio sigma-delta ADC is implemented using discrete-time circuits such as switched capacitors for the following reasons. Switched capacitor circuits offer low sensitivity to clock jitter and are readily scalable with sampling rate. Moreover, tracking of coefficients of the loop is inherently good due to good matching of capacitors. However, due to the discrete-time nature, the converter suffers from harmonic distortion primarily caused by signal-dependent glitches captured by the sampling capacitors of the first integrator. In highly-integrated circuits such as a digital signal processor (DSP) with on-chip converters, it is very difficult to contain these undesirable glitches since the DSP is running at a much higher clock rate than the converter. Furthermore, for high performance converters, over 100dB of signal-to-noise ratio (SNR), the sampling capacitors have to be large to reduce the thermal noise. Such a large sampling network emits current glitches back into the signal source which leads to electromagnetic interference (EMI).

Sigma-delta analog-to-digital converters are commonly designed using fully differential circuits to achieve good power supply rejection ratio, immunity to on-chip couplings, clock feed-through, charge injections, even-order harmonic distortions and other second-order non-ideal effects. Such fully differential circuits require a defined common-mode voltage to establish the proper operating point.

In a traditional fully-differential continuous-time sigma-delta converter with current-steering feedback DAC, the internal common-mode voltage of the integrator in the first stage of the converter is undefined when the input signal is AC coupled. When the input is DC coupled, the common voltage is defined by the external circuit. This voltage may not be the same as the desirable internal common-mode and may significantly degrade the performance of the converter.

Another problem with fully differential continuous-time ADC is the common-mode offset current from the feedback DAC. Since there is no mechanism for correcting this offset, both the positive and negative outputs of the differential integrator can peg to either positive or negative supply.

Yet another problem is that the input resistors of the integrator are built on chip, they may have mismatch as much as 1 percent. When a differential input signal, even from a balanced source, is applied to the ADC, the resistor mismatch will create a common-mode voltage swing at the summing junctions of the amplifier in the integrator. This voltage swing is a significant source of harmonic distortion in the converter.

Figure 1 illustrates a simplified model of a 4-bit, 2nd-order sigma delta analog-to-digital converter with a continuous-time first-stage used in this invention. The setup primarily comprises a first summer circuit 101, continuous-time integrator 102, a second summer circuit 103, switched capacitor DAC 106, switched capacitor integrator 104, and current steering DAC 108. The continuous-time implementation of the first stage in the converter is much less susceptible to on-chip couplings than a switched capacitor implementation. Hence, the converter can be integrated into larger scale circuits in deep sub-micron processes without significant degradation in performance.

More over, since the input impedance is pure resistive, the circuit does not emit high frequency current glitches back to the external source. This yields a much lower electromagnetic interference (EMI) compared to a switched capacitor implementation. Hence, the converter is easier to use in EMI sensitive applications such as automotive systems.

Figures 2a-b illustrate two different approaches to implement the first stage of the converter. Figure 2a shows the first approach which includes a fully-differential amplifier 202 with built-in output common-mode voltage control circuit, a pair of integrating capacitors 204 and 206, and a pair of input resistor 208 and 210. The current steering feedback DAC in Figure 1 is also included as a part of the first stage.

Figure 2b illustrates the second approach which comprises two single-ended amplifiers 212 and 214, a pair of capacitors 216 and 218, and a pair of resistors 220 and 222, and the feedback DAC. The positive input terminals of the amplifiers are connected to a reference voltage V_{ref} 224.

Figure 3 illustrates the implementation of a typical thermometer-code DAC used as the feedback DAC in the design. It consists of 2 PMOS devices MP1 302 and MP2 304, and 16 NMOS devices MN0 306 through MN15 308 (which form a bank of switching current cells, such as a 16 cell thermometer style DAC implementation). The PMOS devices 302 and 304 are biased by a voltage V_{bias1} 305, and the NMOS devices 306 and 308 are biased up by a voltage V_{bias2} 310. PMOS devices MP1 302 and MP2 304 are connected to the positive 312 and negative 314 DAC output terminals respectively. Each of these PMOS devices 302 and 304 conducts a current of magnitude $I/2$. Each of the NMOS devices MN0 306 to MN15 308 is connected to the positive 312 or negative 314 DAC output via a switch controlled by the data bit 316 or the complimentary data bit 318 respectively. Each NMOS device 306 or 308 conducts a current of magnitude $1/16$.

In normal operation, when the DAC thermometer-code data input is at the logical value zero, eight bits are set to "1" and eight bits are set to "0". Therefore, the net output current delivered by the DAC is theoretically zero. In practice, however, there is a net CM offset current at the DAC output 318. This is due to mismatch between the push and pull current sources.

There are at least two problems with the approach of Figure 2a. First, while the output of the integrator has a common mode (CM) voltage defined by a feedback circuit, the input CM voltage depends on the input source. When a DC coupled source is connected to the input of the converter, the CM of the source will define the operating point at input of the converter. However, the DAC has a net CM offset current due to

circuit imperfection, wherein this current creates a voltage across the resistors R1 208 and R2 210. In this case, the voltage at the summing junctions of the amplifier may be different than the intended value and may bring the amplifier out of the linear range. Moreover, the DAC is designed to give the optimal thermal noise performance since it is one of the dominant noise sources in the converter. This implies that saturation voltage of the NMOS devices is almost near the internal CM value. Any significant decrease of the CM voltage at the summing junctions of the amplifier will bring the DAC of out the saturation region and will significantly degrade the converter distortion measurements.

Second, due to process imperfections and layout mismatch, R1 208 may differ from R2 210 by an error as much as 1%. When a differential signal is applied to the ADC input, the summing junctions of the amplifier will see a CM swing. This CM swing will cause second-order harmonic distortion in the ADC output.

Figure 2b illustrates an instrumentation style implementation. The approach in figure 2b does not suffer from the above-mentioned resistor mismatch problem associated with the circuit of figure 1, but it does require an output and an input CM feedback circuit. Moreover, it consumes more power and silicon area, and has 3dB more noise than the first approach (of figure 1). Therefore, it is more advantageous to implement the first approach in the ADC design.

A technique to shift the common-mode voltage in a low-voltage system is presented in the paper to Duque-Carillo et al. entitled, "Input common-mode feedback technique for very low voltage CMOS amplifiers." The circuit described by Duque-Carillo et al. has the ability to source and sink current and acts as a CM current attenuator so that the summing junctions can operate at a different CM voltage than that of the external signal source. However, implementation of such a circuit in a continuous-time integrator significantly degrades the signal-to-noise ratio (SNR) of the converter. This penalty comes directly as a result of the addition of the push-pull current sources in the mentioned technique. Since the noise gain of these devices is unity, the full noise strength of the CM attenuator circuit will appear at the output.

In the design of the ADC, the main noise sources are the feedback DAC and the input resistors. These components are optimized to yield the target SNR. If the mentioned

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technique is implemented, then the DAC has to be re-optimized to meet the target noise performance. This will lead to bigger chip area and higher power consumption. The impact becomes even more significant in smaller geometry processes such as 0.18u and below.

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Whatever the precise merits, features, and advantages of the above cited references, none of them achieves or fulfills the purposes of the present invention. The present invention solves the above-mentioned problems via a small feedback circuit to stabilize the common-mode voltage of the first integrator and set it to a proper level.

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SUMMARY OF THE INVENTION

The present invention provides for a control circuit and method to monitor the common mode voltage at the summing junctions of the first-stage integrator associated with a continuous-time sigma-delta analog-to-digital converter. The circuit produces a control voltage which adjusts the quiescent current of the feedback DAC to compensate for any common-mode offset current. As the adjustment takes place within the feedback DAC, no extra noise is added to the differential signal path. Furthermore, the circuit of the present invention causes no degradation to the signal-to-noise (SNR).

20 The present invention also provides for a method of partitioning a feedback DAC (such as a thermometer-coded DAC or a binary weighted DAC) in a continuous-time sigma-delta analog-to-digital converter, wherein the method comprises the steps of including at least a portion of said feedback DAC in a negative feedback loop and stabilizing a common mode (CM) voltage at the summing junctions of a continuous-time integrator via the negative feedback loop. The step of stabilizing CM voltage further comprises the steps of monitoring a common mode (CM) voltage (i.e., monitored via a triple-input amplifier, with three inputs of SJP, SJN, and V_{ref} , and a single output that adjusts the quiescent current.) at the summing junctions of the continuous-time integrator and generating a control voltage that adjusts the quiescent current of the feedback DAC based on the monitored CM voltage, with the control voltage compensating for the CM offset current. The present invention also provides for the stabilization of the negative feedback loop via a compensation network implemented via a pair of capacitors and a pair of resistors.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a simplified model of a 4-bit, 2nd-order sigma delta analog-to-digital converter with a continuous-time first-stage $\sigma\delta$ used in this invention.

Figures 2a-b illustrate two different prior art approaches to implement the first stage of the converter.

Figure 3 illustrates the implementation of a typical thermometer-code DAC used as the feedback DAC in the design.

Figures 4a-b illustrate the present invention's differential and instrumentation implementation circuits.

Figure 5 illustrates an implementation of amplifier A2 shown in figures 4a-b.

Figure 6 illustrates the use of a compensation network in conjunction with the present invention.

Figure 7 illustrates a CM servo loop providing the quiescent or offset current.

Figure 8 illustrates a variation of the present invention's technique wherein the pair of PMOS devices MP1 and MP2 (of fig 6) is split into two parallel pairs of PMOSs.

DETAILED DESCRIPTION OF THE INVENTION

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

In figure 3, varying Vbias1 305 can adjust the net common mode (CM) current of the DAC. The design of the present invention comprises a circuit that monitors the voltage at the summing junctions of the amplifier. The present invention's circuit rejects any differential voltage and compares the CM voltage to a reference Vref. The circuit of the present invention adjusts the Vbias1 in a negative feedback manner to stabilize the CM voltage at the summing junctions of the amplifier.

Figures 4a-b illustrates a pair of implementations of the present invention. Figure 4a illustrates the present invention's differential style implementation circuit. Figure 4b illustrates the present invention's differential and instrumentation implementation circuit.

It should be noted that although the DAC shown in the figures is a thermometer-code DAC, the type of DAC should not limit the scope of the present invention. For example, a binary weighted DAC could also be used to implement the present invention. However, it should be noted that such an implementation can be subjected to element-mismatch problem and hence, not the best choice.

The implementation of amplifier A2 **402** and **404** in figures 4a-b is shown in figure 5. MP3 **502** has a size of 2x, MP4 **504** and MP5 **506** have a size of 1x, MN1 **508** and MN2 **510** have a size of 1x. By sizing them in such a manner, it is seen that the circuit forms a balance triple-input and single-output amplifier. SJP and SJN are connected to the positive and negative summing junctions of amplifier as shown in figure 4. The current source **512** provides the bias current for the triple-input amplifier of figure 4a and 4b.

Figure 4a shows the first approach which includes a fully-differential amplifier **401** with built-in output common-mode voltage control circuit, a triple-input amplifier **402**, a pair of integrating capacitors **403** and **405**, a pair of input resistor **407** and **409**, and a feedback DAC **411**. In figure 4a, SJP **406** and SJN **408** are connected to the positive and negative summing junctions of the amplifier A1 **401** respectively. The triple-input terminal amplifier **402** compares SJP **406**, SJN **408**, and Vref **410**. The circuit does not respond to any differential signal applied to SJP **406** and SJN **408**. If the CM at SJP **406** and SJN **408** varies, then Vbias 1 changes. Since the circuit is connected to the DAC **411** to form a negative feedback loop, Vbias changes in such a way that stabilizes the CM at SJP **406** and SJN **408**.

Figure 4b illustrates the present invention's instrumentation style implementation. The circuit of figure 4b comprises two single-ended amplifiers **412** and **414**, a triple-input amplifier **404**, a pair of capacitors **416** and **418**, and a pair of resistors **420** and **422**, and the feedback DAC **424**. The positive input terminals of the amplifiers are connected to a reference voltage Vref **224**. The triple-input terminal amplifier **404** compares SJP **424**, SJN **426**, and Vref **428**. As in figure 4a, the circuit does not respond to any differential signal applied to SJP **424** and SJN **428**. If the CM at SJP **424** and SJN **428** varies, then Vbias 1 changes. Since the circuit is connected to the DAC **424** to form a negative feedback loop, Vbias changes in such a way that stabilizes the CM at SJP **424** and SJN **428**.

Figure 6 illustrates the use of a compensation network in conjunction with the present invention, wherein the compensation network is used to enhance the stability of the negative feedback loop. Without this compensation network, the loop may become unstable. The compensation network comprises resistors R3 606 and R4 608 and C3 610 and C4 612, wherein the compensation network is coupled to a pair of PMOS devices MP1 602 and MP2 604 .

An advantage of the present invention's technique of CM stabilization is that the circuits of figures 4a-b do not add any extra noise into the main ADC.

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Another advantage of the present invention's technique is low power consumption. Since the loop only has to work with the input signal bandwidth, the gain bandwidth requirement for the three-input amplifier is at most the same as the input. Therefore, the power consumption is insignificant.

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Yet another advantage of the present invention's technique is that the loop gain does not have to be large since it only has to suppress an already small variation of CM at the summing junctions of the amplifier.

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Additionally, the circuits of figures 4a-b do not require a clean Vref since any variation of Vref within the loop bandwidth will inject a CM signal into the ADC and will be rejected by the differential circuits.

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Also, the power-up time of the continuous time integrator is shorter due to the assistance of the CM feed-back loop to the main loop.

It should be noted that instead of adjusting Vbias1 305 of figure 3, Vbias2 310 of figure 2 can be adjusted for similar results and the choice between Vbias1 305 or Vbias2 310 should not be used to limit the scope of the present invention. However, it should also be noted that it is advantageous to adjust Vbias1 since this does not result in any amplitude modulation effect.

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Furthermore, the present invention is also not limited to adjusting the bias voltage(s) of the feedback DAC in order to stabilize the CM voltage at the summing junctions of the

amplifier. For example, the DAC can be partitioned so that it consists of only signal dependent switching current source. The quiescent or offset current can then be provided by a CM servo loop such as on in Figure 7. The circuit in Figure 7 assumes that the feedback DAC consists of only the 16 NMOS devices MN0 to MN15 as in Figure 3. As seen, the triple-input amplifier compares the CM at SJP and SJN to Vref and creates a voltage at its output. This output is buffered up to drive a pair of resistor R3 and R4. The currents through these resistors compensate for the quiescent current required by switching NMOS DAC.

Yet another variation of the present invention's technique is shown in Figure 8. In this example, the pair of PMOS devices MP1 802 and MP2 804 in fig 6 are split into two parallel pairs of PMOS devices. The first pair, MP6-MP7, has the gates connected to a fixed bias voltage. This pair provides one-half of the required quiescent current of the DAC. The second pair, MP1-MP2, has the gates connected to the output of amplifier (Vbias1) in Figure 5. The operation of the triple-input amplifier and the pair MP1-MP2 is as described above. This variation yields a lower loop gain in the negative feedback loop and therefore, easier to compensate. However, this result comes at a cost of smaller CM stabilization range.

CLAIMS

1 1. A method of partitioning a feedback DAC in a continuous-time sigma-delta analog-to-
2 digital converter, said method comprising the steps of:

3 including at least a portion of said feedback DAC in a negative feedback loop; and
4 stabilizing the common mode (CM) voltage at the summing junctions of a
5 continuous-time integrator via said negative feedback loop, wherein said continuous-time
6 integrator is part of said continuous-time sigma-delta analog-to-digital converter.

1 2. A method as per claim 1, wherein said step of stabilizing CM voltage further comprises
2 the steps of:

3 monitoring a common mode (CM) voltage at the summing junctions of said
4 continuous-time integrator; and

5 generating a control voltage that adjusts the quiescent current of said feedback
6 DAC based on said monitored CM voltage, said control voltage compensating for CM
7 offset current.

1 3. A method as per claim 2, wherein said adjustment of quiescent current is within said
2 feedback DAC.

1 4. A method as per claim 2, wherein said CM voltage is monitored via a triple-input
2 amplifier with inputs SJP, SJN, and V_{ref} , said amplifier generating a bias voltage for said
3 feedback DAC.

1 5. A method as per claim 1, wherein said DAC is a thermometer-code DAC.

1 6. A method as per claim 1, wherein said DAC is a binary weighted DAC.

1 7. A method as per claim 1, wherein said method further comprises the step of enhancing the
2 stability of said negative feedback loop via a compensation network.

1 8. A method as per claim 7, wherein said compensation network is implemented via a pair
2 of capacitors and a pair of resistors.

1 9. A method as per claim 7, wherein said feedback DAC and said negative feedback loop
2 suppress the variation of the CM voltage at the summing junctions of an integrator due to
3 resistor mismatch.

- 1 10. A method of partitioning a feedback DAC in a continuous-time sigma-delta analog-to-
2 digital converter comprising, in a first stage, a continuous-time integrator and said feedback
3 DAC, said method comprising the steps of:
- 4 including at least a portion of said feedback DAC in a negative feedback loop; and
- 5 monitoring a common mode (CM) voltage at the summing junctions of said
6 continuous-time integrator; and
- 7 generating a control voltage that adjusts the circuit generating the quiescent current
8 of said feedback DAC based on said monitored CM voltage.
- 1 11. A method as per claim 10, wherein said adjustment of quiescent current is partially
2 within said feedback DAC.
- 1 12. A method as per claim 10, wherein said CM voltage is monitored via a triple-input
2 amplifier, with inputs of SJP, SJN, and Vref, said triple-input amplifier outputs a bias voltage
3 for said feedback DAC.
- 1 13. A method as per claim 10, wherein said DAC is a thermometer-code DAC.
- 1 14. A method as per claim 10, wherein said DAC is a binary weighted DAC.
- 1 15. A method as per claim 10, wherein said method further comprises the step of enhancing
2 the stability of said negative feedback loop via a compensation network.
- 1 16. A method as per claim 15, wherein said compensation network is implemented via a pair
2 of capacitors and a pair of resistors.
- 1 17. A method of partitioning the feedback DAC in a continuous-time sigma-delta analog-to-
2 digital converter, said method comprising the steps of
- 3 including a non-signal dependent portion of said feedback DAC in a negative
4 feedback loop; and
- 5 correcting a quiescent current of the DAC or the CM offset current of an integrator,
6 or both, via said negative feedback loop wherein the offset is adjusted via said loop,
7 wherein said integrator is part of said continuous-time sigma-delta analog-to-digital
8 converter.
- 1 18. A method as per claim 17, wherein said DAC is a thermometer-code DAC.

- 1 19. A method as per claim 17, wherein said DAC is a binary weighted DAC.
- 1 20. A method as per claim 17, wherein said method further comprises the step of stabilizing
2 said negative feedback loop via a compensation network.
- 1 21. A method as per claim 20, wherein said compensation network is implemented via a pair
2 of capacitors and a pair of resistors.
- 1 22. A method to adjust the bias voltages of a feedback DAC in a continuous-time sigma-
2 delta analog-to-digital converter, said method comprising:
- 3 including at least a portion of said feedback DAC in a negative feedback loop; and
4 stabilizing an input common mode (CM) voltage of a continuous-time integrator that
5 is part of said continuous-time sigma-delta analog-to-digital converter via said negative
6 feedback loop, wherein the bias voltages of said feedback DAC is changed to stabilize said
7 CM voltage.
- 1 23. An amplifier embedded in a negative feedback loop in a continuous-time sigma-delta
2 analog-to-digital converter, said continuous-time sigma-delta analog-to-digital converter
3 comprising, in a first state, a continuous-time integrator and a feedback DAC, said amplifier
4 comprising:
- 5 an input means SJP receiving positive summing junction voltage;
6 an input means SJN receiving negative summing junction voltage;
7 an input means VREF receiving a reference voltage;
8 an output means adjusting a quiescent current of said feedback DAC, wherein said
9 amplifier monitors a common mode (CM) voltage at the summing junctions of said
10 continuous-time integrator and generates a control voltage that adjusts a quiescent current of
11 said feedback DAC based on said monitored CM voltage.
- 1 24. An amplifier as in claim 23, wherein stability of said amplifier is enhanced via a
2 compensation network.
- 1 25. An amplifier as in claim 24, wherein said compensation network comprises a pair of
2 resistors and a pair of capacitors.
- 1 26. An amplifier as in claim 23, wherein said amplifier is implemented via three PMOS
2 each receiving as input SJP, SJN, and Vref respectively, two NMOS devices working in

- 3 conjunction with said PMOS devices to output a voltage V_{bias} , and a current source I
- 4 providing a bias current for said amplifier.

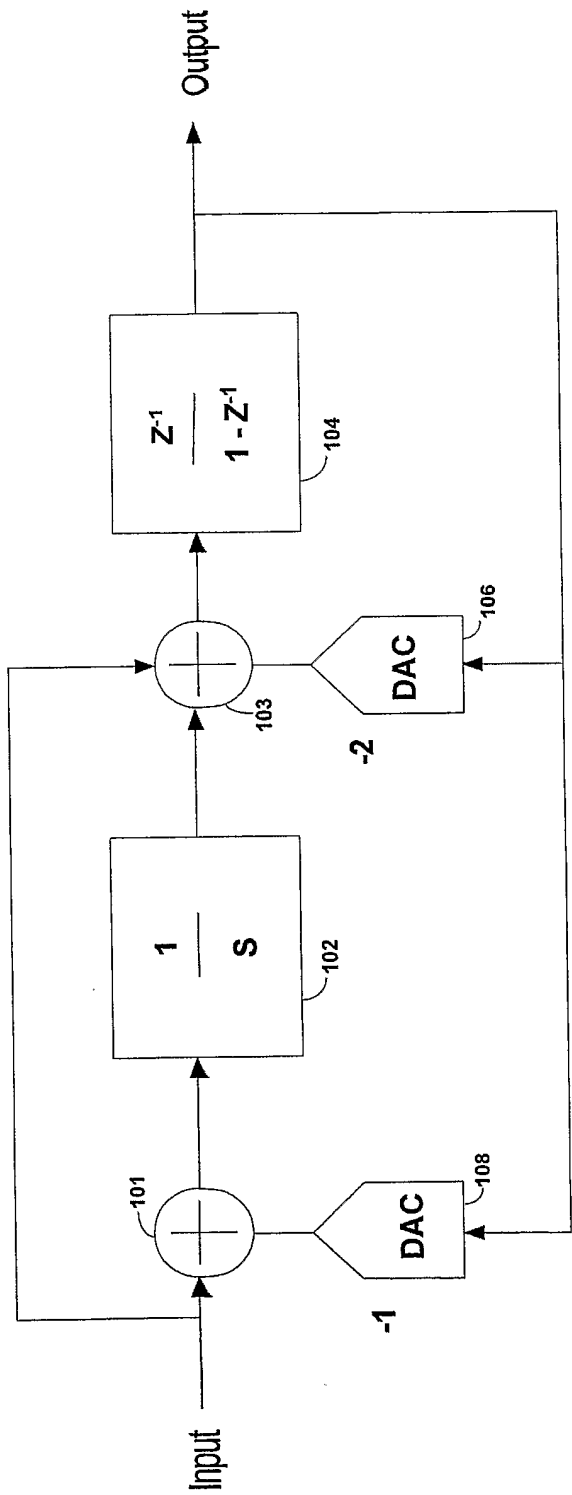


Figure 1
(PRIOR ART)

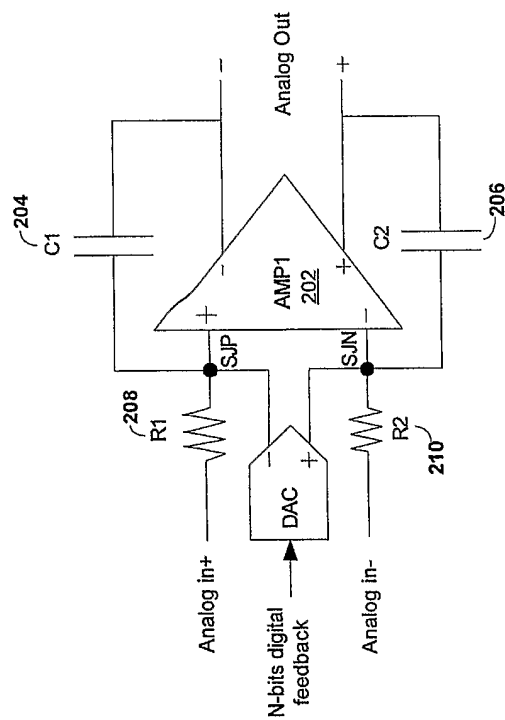


Figure 2a
(PRIOR ART)

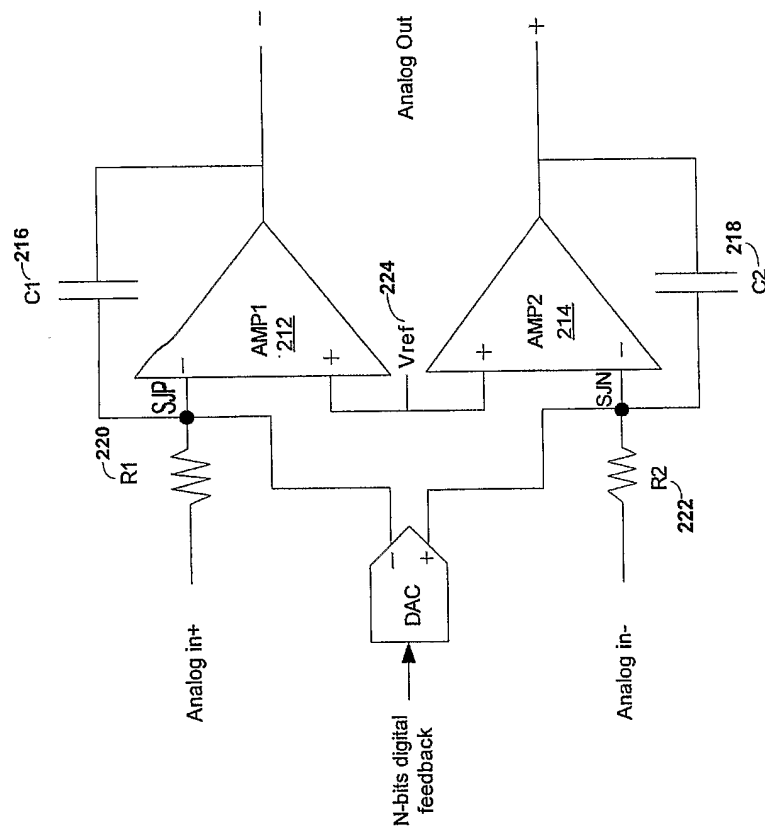


Figure 2b
(PRIOR ART)

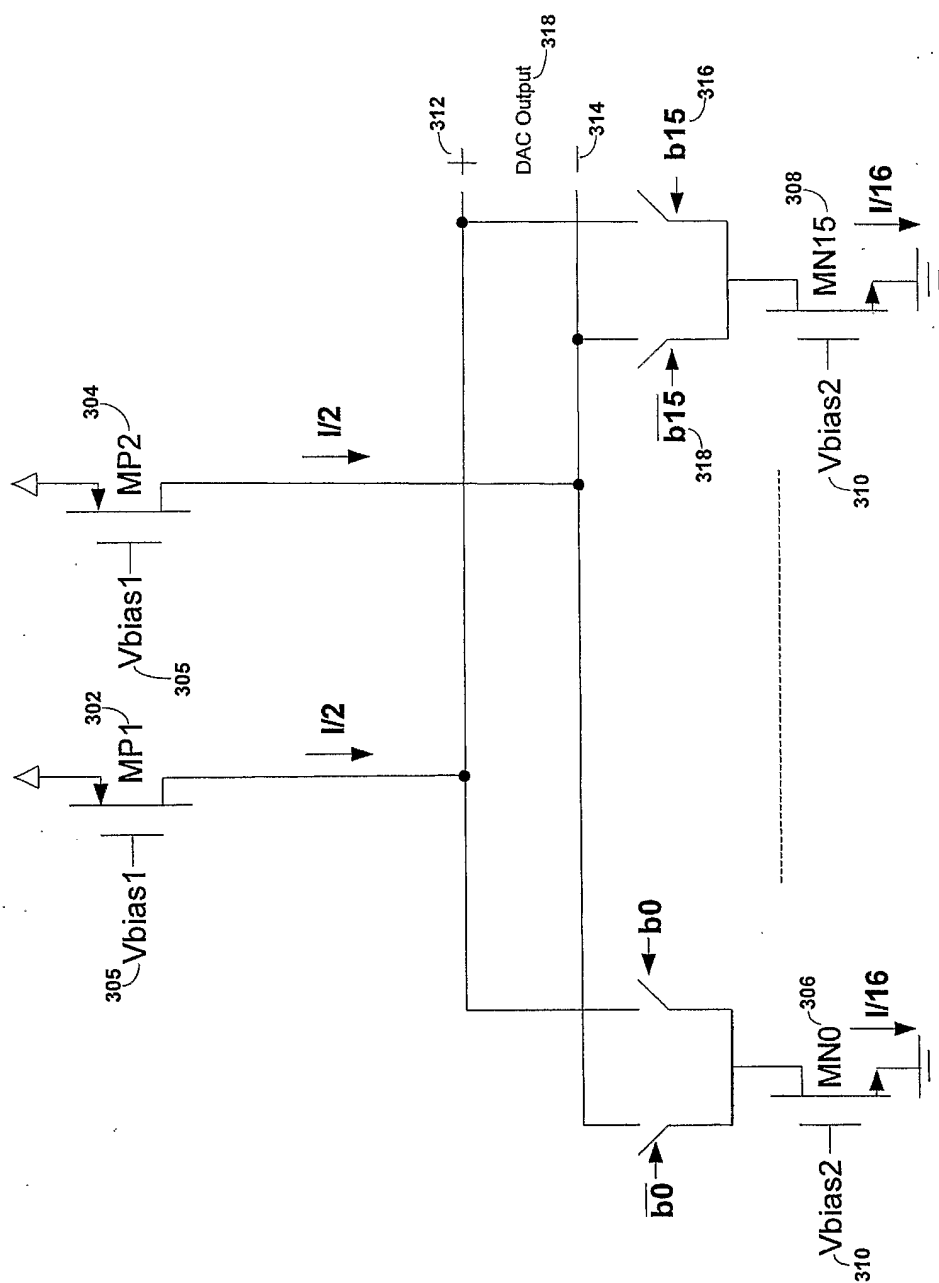


Figure 3
(PRIOR ART)

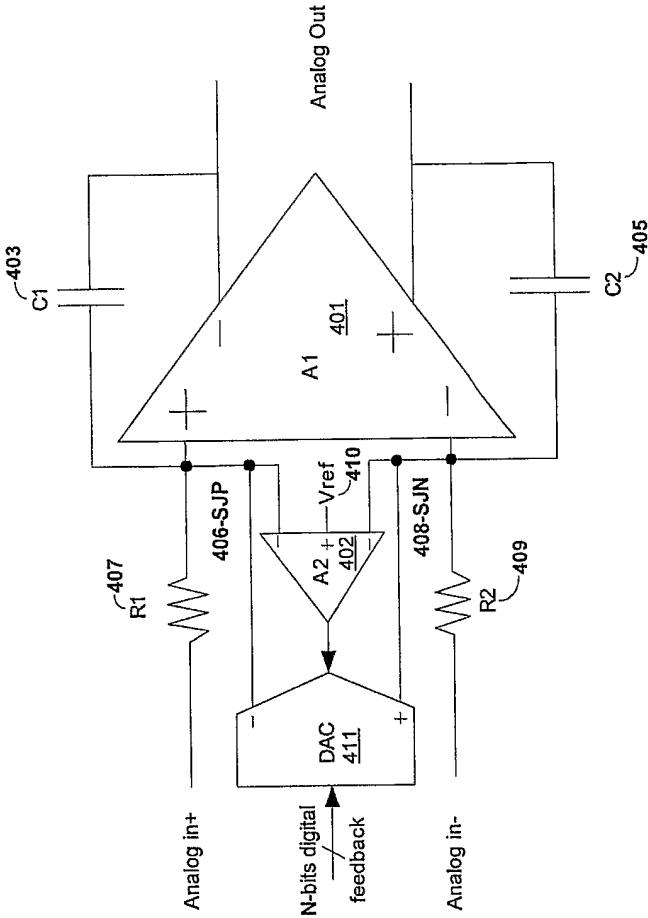


Figure 4a

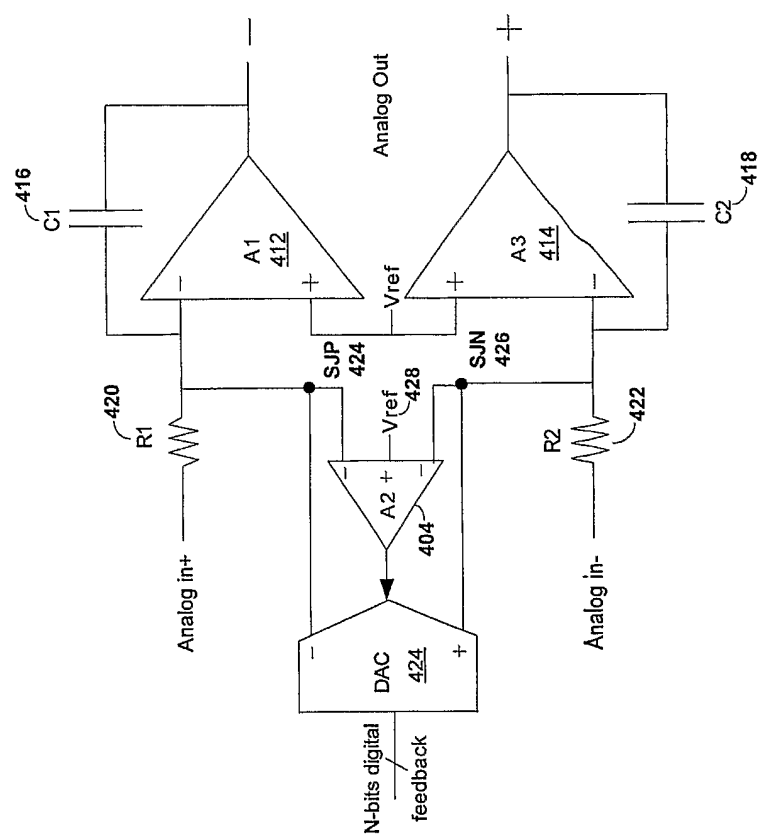


Figure 4b

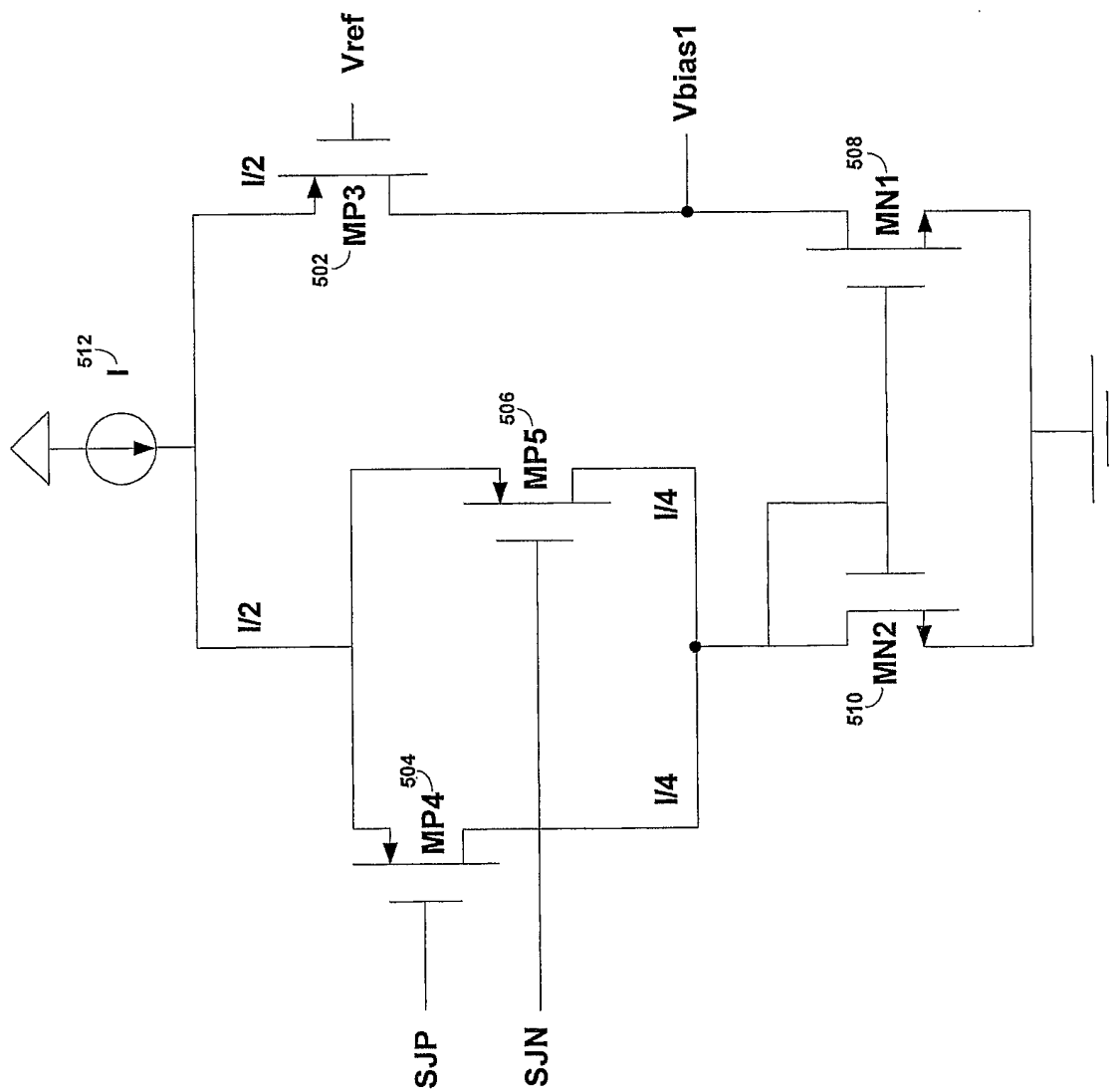


Figure 5

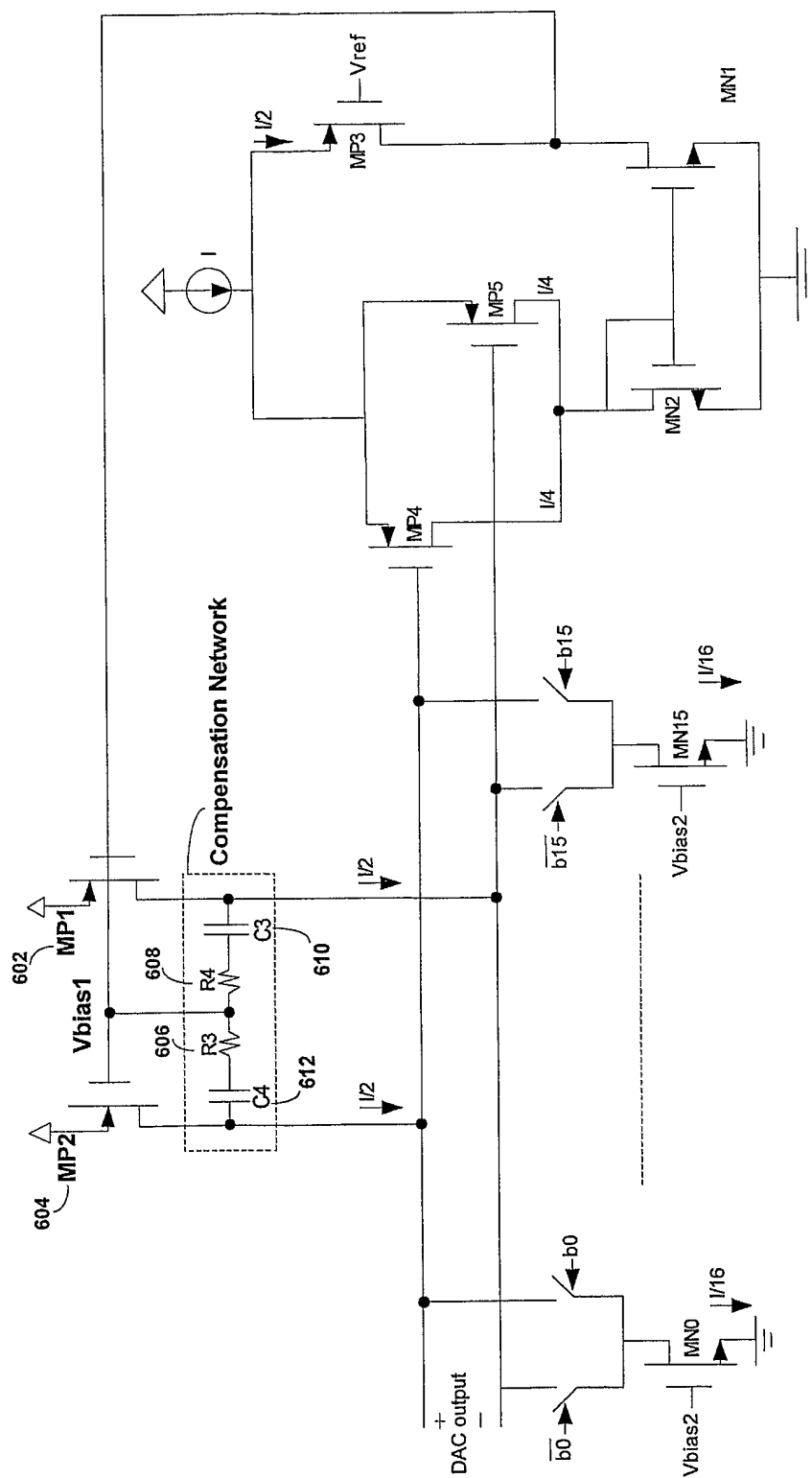


Figure 6

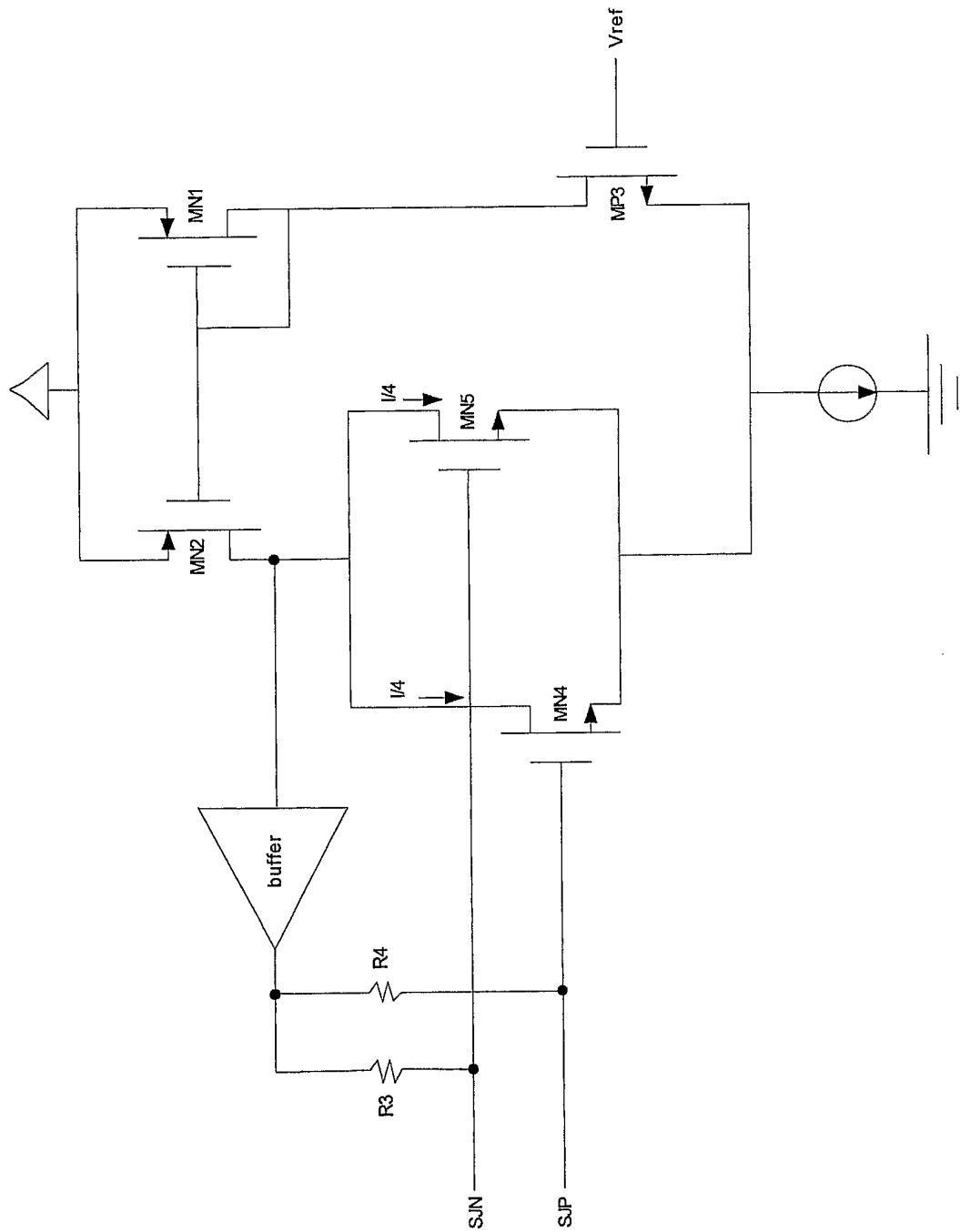


Figure 7

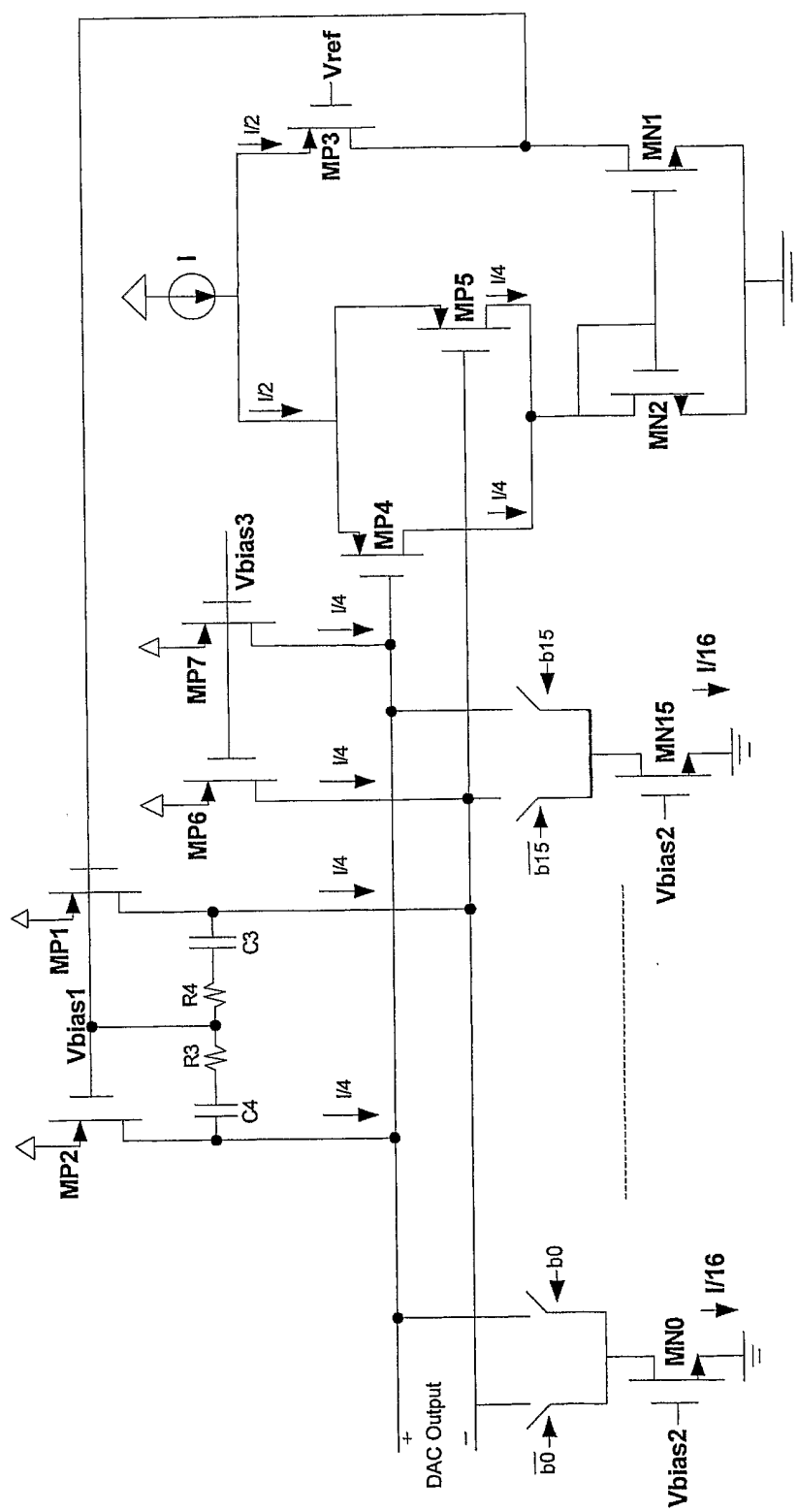


Figure 8

INTERNATIONAL SEARCH REPORT

International application No

PT/US2005/037495

A. CLASSIFICATION OF SUBJECT MATTER

H03M3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 02/03747 A (KONINKLIJKE PHILIPS ELECTRONICS N.V) 10 January 2002 (2002-01-10)	1-6, 10-14, 17-19, 22, 23
Y	figures 3-5 page 2, lines 1-6 page 3, line 10 - line 13 page 4, line 27 - line 31 page 5, line 6 - line 10 page 5, line 33 - page 6, line 14 ----- -/--	7-9, 15, 16, 20, 21, 24-26

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Date of the actual completion of the international search

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Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Oliveira, J.

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2005/037495

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