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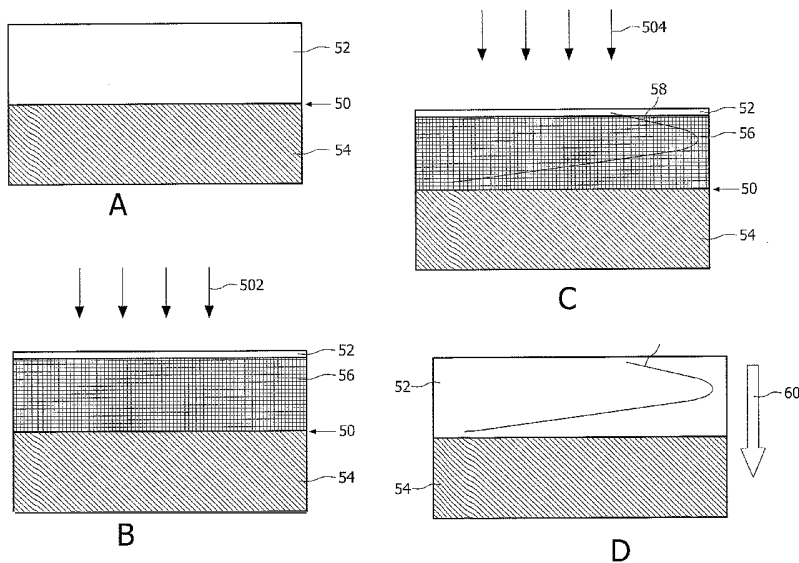
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(54) Title: INTEGRATED CIRCUIT FABRICATION USING SOLID PHASE EPITAXY AND SILICON ON INSULATOR TECHNOLOGY



(57) Abstract: A method of forming a junction extension in respect of a CMOS device based on a composite semiconductor-on-insulator substrate (50). The method comprises performing an implementation step to form a buried amorphous layer (56) in the semiconductor layer (52) of the substrate, such that a portion of the crystalline semiconductor layer (52) is left covering the buried layer (56). A doping step is performed to create a doped region (58) in the semiconductor layer (52). The structure is then annealed at a relatively low temperature so as to cause re-crystallization of the semiconductor layer (52) and activation of the dopants forming the doped region (58).

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INTEGRATED CIRCUIT FABRICATION USING SOLID PHASE EPITAXY AND SILICON ON INSULATOR TECHNOLOGY

FIELD OF THE INVENTION

This invention relates generally to integrated circuit fabrication and, more particularly, to a method of fabricating an integrated circuit using Silicon on insulator (SOI) technology.

BACKGROUND OF THE INVENTION

The basic building block of typical integrated circuits is the transistor, and particularly the Metal-Oxide-Silicon (MOS) transistor, which has a relatively rapid switching speed. MOS devices are formed on a substrate with doped regions forming source and drain regions. In conventional implant techniques, dopants are implanted into the substrate and, subsequent to the implantation step, an annealing step (i.e. a thermal treatment) is generally performed. The annealing step tends to be a mandatory step in the field of semiconductor processing, as annealing will repair any damage to the substrate caused by the implant, and activate the doped regions.

Solid Phase Epitaxy (SPE) is well known as a good technique for providing shallow and well-activated junctions compatible with metal gate, high dielectric constant, so-called high-k, and strain layers. The principle of this technique is based on the fact that amorphous Silicon is preferred by dopants over crystalline Silicon. As is generally known in the semiconductor field, ion implantation will typically damage the crystalline structure of the substrate, i.e. the bombardment of ions on the substrate surface causes the substrate's crystalline lattice structure to break down. When the dose of the implant is high enough and at certain energy levels, it will result in amorphization of an upper portion of the substrate, said substrate being typically formed of Silicon. While crystalline Silicon has a regular lattice structure, amorphous Silicon lacks such a lattice structure.

Referring to Figure 1a of the drawings, a schematic cross-sectional view of a Silicon substrate having a crystalline Silicon (c-Si) region 100 and an amorphous Silicon (a-Si) region 102, as a result of ion implantation represented by arrows 112, is shown. Next, and referring to Figure 1b of the drawings, dopant implantation, represented by arrows 113, is effected. An annealing step is then performed under conditions to ensure the repair of the damage to the substrate, including the re-crystallization of the amorphized Silicon 102, and to

activate the doped region 114. Referring additionally to Figure 1c of the drawings, such re-crystallization is achieved by means of solid phase epitaxy (SPE) which can be realized in any number of processing environments, including rapid thermal anneal (RTA) and furnace annealing, although in this case annealing is preferably performed at a relatively low
5 temperature so as to ensure that diffusion of dopants is negligible.

Re-crystallization generally starts at the amorphous-Silicon/crystalline-Silicon (a-Si/c-Si) boundary 102a, gradually moving up (as indicated by arrow 108) toward the substrate surface 106, at which point the amorphous-Silicon region 102 will have been entirely re-crystallized and encompassed within the crystalline-Silicon region 100. Nevertheless, a line
10 103 of defects tends to remain along the previous a-Si/c-Si interface 102a, which line 103 of defects tends to induce junction leakages in the eventual device.

Silicon On Insulator (SOI) technology, in which a composite substrate is utilized which comprises a mono-crystalline semiconductor layer, such as a Silicon, epitaxially deposited on a supporting insulating layer (such as Silicon oxide), is well known and includes
15 in its advantageous properties the effective elimination of leakage currents flowing between adjacent active devices as well as a substantial reduction in parasitic capacitance between charged active regions of a device.

However, it has not previously been possible to implement solid phase epitaxy in respect of SOI technologies because this process requires a crystalline interface for the re-
20 growth. In such a process, and referring to Figure 2a of the drawings, an amorphous Silicon (a-Si) layer 200 may be provided by implantation on an SOI substrate 202, and the a-Si layer 200 can be subjected to dopant implantation as illustrated by the arrows 204 to create a doped region 206 in the a-Si layer 200. However, referring to Figure 2b of the drawings, when the resulting structure is subjected to a low temperature annealing step, the amorphous Silicon of
25 layer 200 changes to polycrystalline Silicon which, in turn, leads to bad junction characteristics.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an improved integrated circuit
30 fabrication process wherein solid phase epitaxy is used in respect of semiconductor on insulator substrate to create a doped region defining a pn or np junction between first and second semiconductor regions.

Thus, in accordance with the present invention, there is provided a method of forming
in a composite substrate, a doped region defining a junction between semiconductor materials

of a first and second type, said composite substrate comprising a semiconductor layer over a layer of insulating material, the method comprising performing an ion implantation step in such a way that an amorphous sub-layer is formed in said semiconductor layer and a sub-layer of said semiconductor layer remains unamorphous, performing a dopant implantation
5 step to introduce dopants into said semiconductor layer, and annealing said composite substrate so as to activate said dopants and cause the amorphous sub-layer to re-crystallize starting from an interface between said amorphous sub-layer and the unamorphous sub-layer of said semiconductor layer.

Also in accordance with the present invention, there is provided a MOS device
10 comprising a source region, a drain region and a gate electrode on a composite semiconductor-on-insulator substrate, said source and/or said drain region comprising a doped region formed according to the above-defined method.

The present invention extends further to an integrated circuit die comprising at least one MOS device as defined above.

15 The integrated circuit die preferably includes at least one CMOS device comprising an NMOS device and a PMOS device as defined above.

The present invention provides a relatively very easy way to integrate solid phase epitaxy techniques on a Silicon-on-insulator substrate in order to provide ultra-shallow and well-activated junctions.

20 Beneficially, the amorphous sub-layer is adjacent the layer of insulating material. In one exemplary embodiment of the invention, the ion species implanted during said ion implantation step comprises Germanium, and said semiconductor layer preferably comprises Silicon. Preferably, the ion implantation step is performed at a dose below a predetermined threshold value, said threshold value defining a dosage level below which ion implantation
25 will result in the formation of a buried amorphous layer.

These and other aspects of the present invention will be apparent from, and elucidated with reference to, the embodiment described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

30 An embodiment of the present invention will now be described by way of example only and with reference to the accompanying drawings, in which:

- Figures 1a, 1b and 1c illustrate the principal steps of a solid phase epitaxy method, according to the prior art, for forming a doped region in a semiconductor substrate;

- Figures 2a and 2b illustrate the effect of performing a solid phase epitaxy method, according to the prior art, in respect of an SOI substrate;
- Figure 3 is a schematic cross-sectional illustration of a typical CMOS structure;
- Figure 4 is a schematic cross-sectional illustration of a portion of the structure of
5 Figure 3, illustrating a source junction;
- Figures 5a to 5d illustrate the principal steps of a solid phase epitaxy process according to the present invention, for forming a junction extension in a SOI substrate; and
- Figure 6 illustrates an ion implant density distribution (typically generally Gaussian) for Germanium Ge ion species implantation in a semiconductor layer.

10

DETAILED DESCRIPTION OF THE INVENTION

Referring to Figure 3 of the drawings, a typical complementary metal oxide semiconductor (CMOS) structure comprises a p-channel MOS device 300 and an n-channel MOS device 302 diffused into an n-type substrate 304. As shown, in this case, the n-channel
15 source 306 and drain 308 have been diffused into a well 320 of p-type material which is isolated from the substrate 304 only by a reverse-biased pn junction.

Referring in addition to Figure 4 of the drawings, each of the source and drain regions 306, 308 defines a junction also called "extension", i.e. a transition region between
20 semiconductor regions of differing electrical properties. Thus, the portion of the MOS illustrated in Figure 3 of the drawings comprises an n-type source 306 diffused within the p-type well 320 forming a junction 310. The structure further comprises a gate including a gate electrode layer 312 over a gate oxide 318 and having a sidewall 314, and a silicide contact region 316, as shown.

25 As CMOS devices are scaled down below 100 nm, a highly doped ultra-shallow junction is mandatory for high-current drive capability and Solid Phase Epitaxy (SPE) is well known as a good technique for providing shallow and well-activated junctions compatible with metal gate, high-k and strain layers, but a problem with this technique in respect of Silicon substrates, as set out above, is the remaining defects along the former a-Si/c-Si
30 interface, which defects can cause junction leakages. This problem can be alleviated by the use of an SOI substrate, and the present invention proposes a method by which solid phase epitaxy can be effectively used with an SOI substrate to produce shallow and well-activated junctions.

Referring to Figure 5a of the drawings, in a method according to an exemplary embodiment of the present invention, a substrate 50 comprises a mono-crystalline semiconductor layer 52, such as a Silicon, epitaxially deposited on a supporting insulating layer 54 (such as Silicon oxide). Such composite SOI substrates are well known in the art, and many different suitable types thereof will be apparent to a person skilled in the art. For example, Silicon on Silicon oxide, Silicon on alpha-aluminium oxide, Silicon on spinel insulators, Silicon on chrysoberel, Silicon or other semiconductor material (e.g. Gallium Arsenide GaAs) on sapphire (Al_2O_3), etc. The present invention is not intended to be limited in this regard.

As shown in Figure 5b, a buried amorphous region 56 is formed within the semiconductor layer 52 by judicious ion implantation 502. The ion implantation step necessary to create the buried amorphous sub-layer, will depend on the semiconductor and insulator used to form the composite substrate 50, and of course the substance used to form the non-crystalline, buried amorphous region 56, as will be apparent to a person skilled in the art. Several different semiconductor/insulator combinations are envisaged for the substrate, and several different materials may be used to form the buried amorphous region 56 accordingly, such that the present invention is not necessarily intended to be strictly limited in this regard. Examples of suitable amorphizing dopants include Silicon and Germanium. In the case where the semiconductor material of the SOI substrate is Silicon Si, Silicon might be a suitable amorphizing dopant because of its relatively low cost.

However, consider as one preferred exemplary embodiment, the use of Germanium to form the buried amorphous layer 54. Referring to Figure 6 of the drawings, there is illustrated graphically, the amorphous depth that can be achieved at various respective energies of Germanium implant as a function of the implant dose. As shown, if the implant dose is below a predetermined value, represented by the line 62, a buried amorphous Ge layer is obtained. It will be appreciated that the use of a buried amorphous layer in a Silicon substrate would not be appropriate, since there would be two fronts of re-crystallization (at the top and bottom respectively of the buried layer), leading to the potential creation of severe defects at two locations of the resultant structure, following re-crystallization. However, in the case of the SOI substrate, there is only one front of re-crystallization between the amorphous layer and the semiconductor.

The ion implantation step may be performed before or after a non-amorphizing dopant implantation step 504, as shown in Figure 5c, but in a preferred embodiment, the ion implantation step is performed first. In one exemplary embodiment, the Ge ion species may

be implanted in respect of the entire structure, following which the p-channel devices may be covered with a resist material, for example photo-resist material, and the n-channel devices implanted with p-type dopants and then the p-channel devices may be uncovered, the n-channel devices covered with resist material and the p-channel devices implanted with n-type dopants. However, in an alternative embodiment, the ion implantation step may also be performed separately in respect of each device type (i.e. the n-channel devices are covered with resist material, the ion species is implanted in respect of the p-channel devices, the n-type dopants are implanted in respect of the p-channel devices, or vice versa, the n-channel devices are uncovered, the p-channel devices are covered with resist material, the ion species is implanted in respect of the n-channel devices and the p-type dopants are implanted in respect of the n-channel devices, or vice versa).

Referring to Figure 5d of the drawings, a low-temperature annealing step is performed under conventional conditions to ensure the repair of the damage to the substrate, including the re-crystallization of the amorphized semiconductor region 56, and to activate the doped region 58 to create the desired junction in the semiconductor layer 52. The portion of the semiconductor layer left above the buried amorphous layer 56, prior to the annealing step, forms the seed for re-crystallization of the mono-crystalline amorphous layer during the annealing process in the direction illustrated by the arrow 60. The implanted dopants are activated during crystallization to form the junction and the line of defects which might otherwise be left at the interface between the amorphous region 56 and the semiconductor layer 52 is consumed during the silicidation.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be capable of designing many alternative embodiments without departing from the scope of the invention as defined by the appended claims. In the claims, any reference signs placed in parentheses shall not be construed as limiting the claims. The word "comprising" and "comprises", and the like, does not exclude the presence of elements or steps other than those listed in any claim or the specification as a whole. The singular reference of an element does not exclude the plural reference of such elements and vice-versa. The invention may be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In a device claim enumerating several means, several of these means may be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually

different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS

1. A method of forming in a composite substrate (50), a doped region (58) defining a junction between semiconductor materials of a first and second type, said composite substrate (50) comprising a semiconductor layer (52) over a layer of insulating material (54), the method comprising:
- 5
- performing an ion implantation step in such a way that an amorphous sub-layer (56) is formed in said semiconductor layer (52) and a sub-layer of said semiconductor layer (52) remains unamorphous,
 - performing a dopant implantation step to introduce dopants into said semiconductor

10 layer (52), and

 - annealing said composite substrate (50) so as to activate said dopants and cause the amorphous sub-layer (56) to re-crystallize starting from an interface between said amorphous sub-layer (56) and the unamorphous sub-layer of said semiconductor layer (52).
- 15 2. A method according to claim 1, wherein the amorphous sub-layer (56) is adjacent the layer of insulating material (54).
3. A method according to claim 2, wherein the ion implantation step is performed at a dose below a predetermined threshold value, said threshold value defining a dosage level
- 20 below which ion implantation will result in the formation of a buried amorphous sub-layer (56).
4. A method according to claim 1, wherein the ion species implanted during said ion implantation step comprises Germanium and said semiconductor layer (52) comprises
- 25 Silicon.
5. A MOS device comprising a source region (306), a drain region (308) and a gate electrode (312) on a composite semiconductor-on-insulator substrate, said source and/or said drain region (306, 308) comprising a doped region formed according to the method of
- 30 claim 1.
6. An integrated circuit die comprising at least one MOS device according to claim 5.

7. An integrated circuit die comprising at least one CMOS device comprising an NMOS device and a PMOS device according to claim 5.

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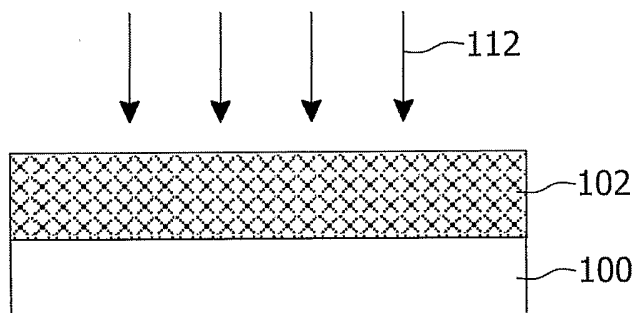


FIG. 1A

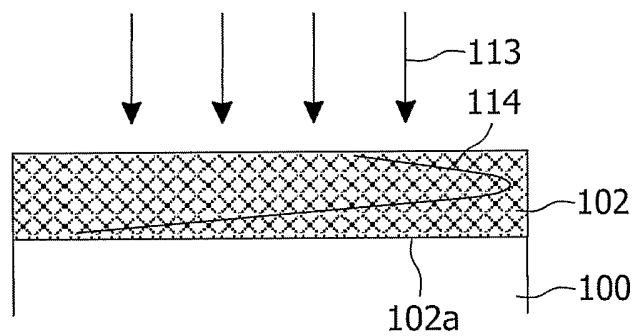


FIG. 1B

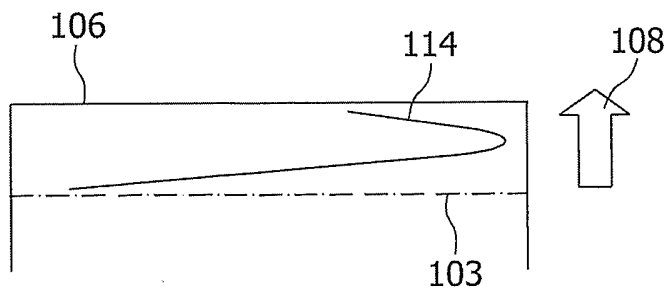


FIG. 1C

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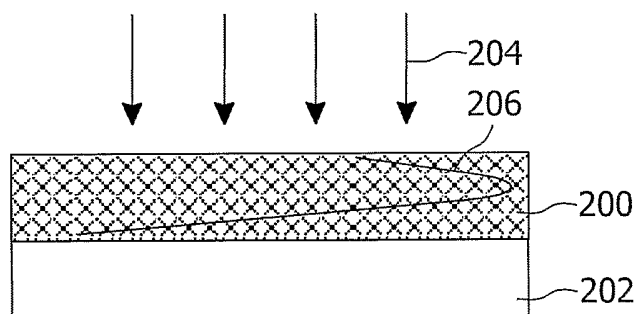


FIG. 2A

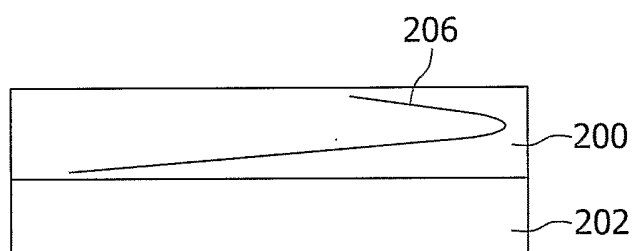


FIG. 2B

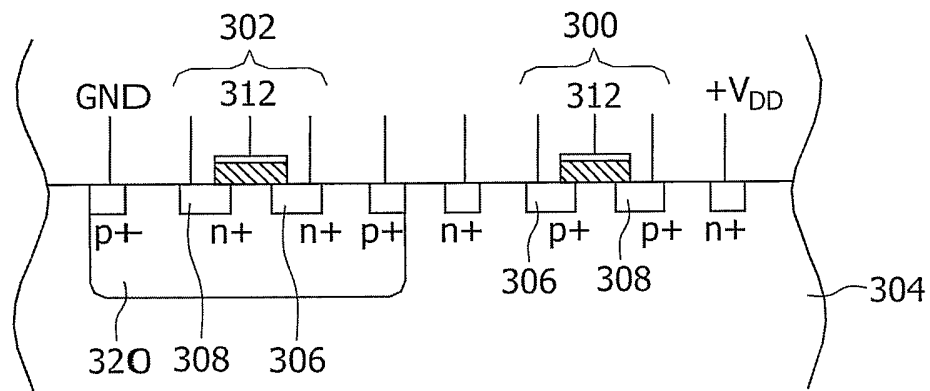


FIG. 3

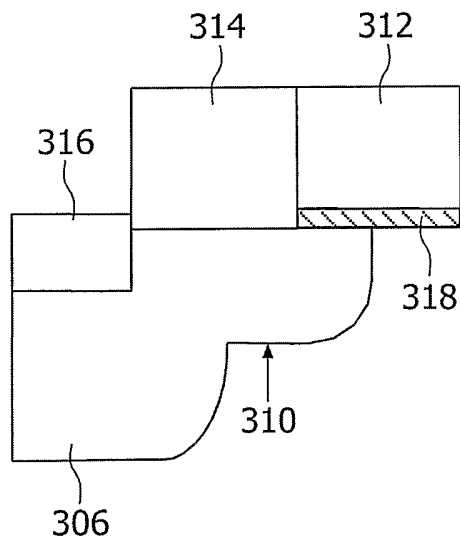


FIG. 4

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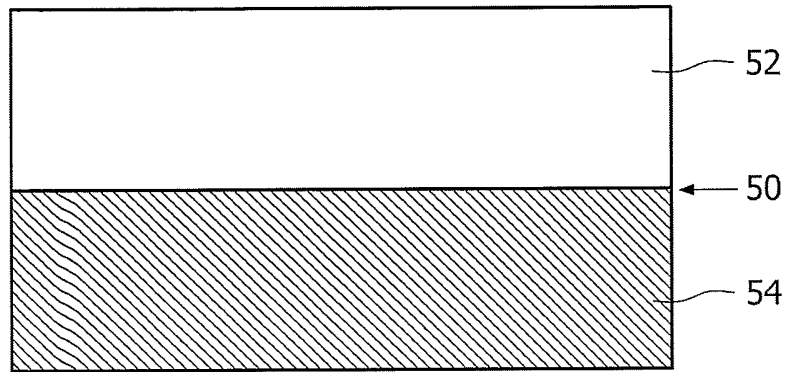


FIG. 5A

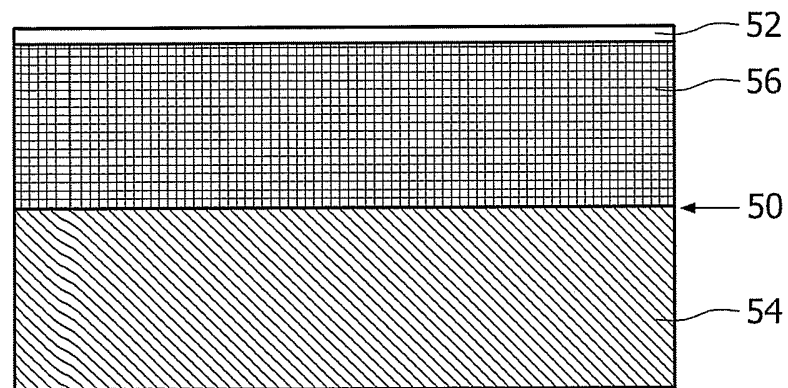
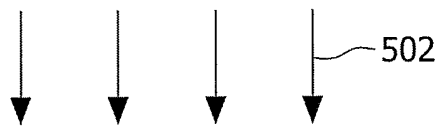


FIG. 5B

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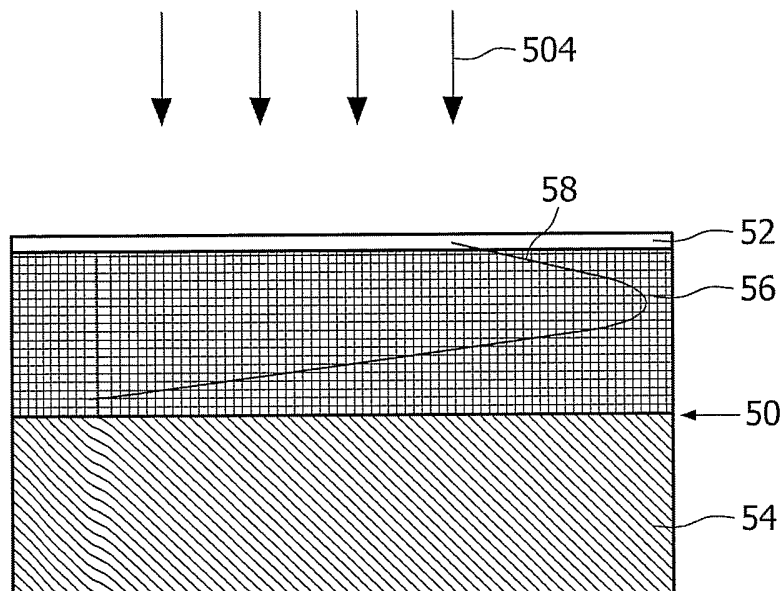


FIG. 5C

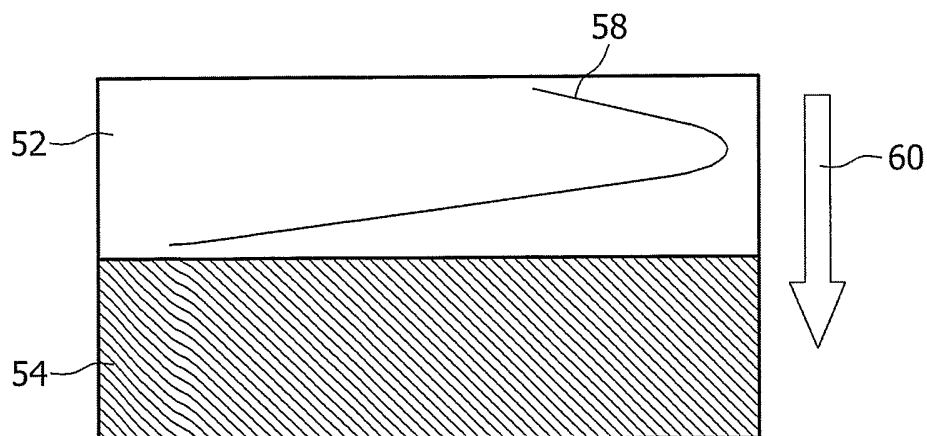


FIG. 5D

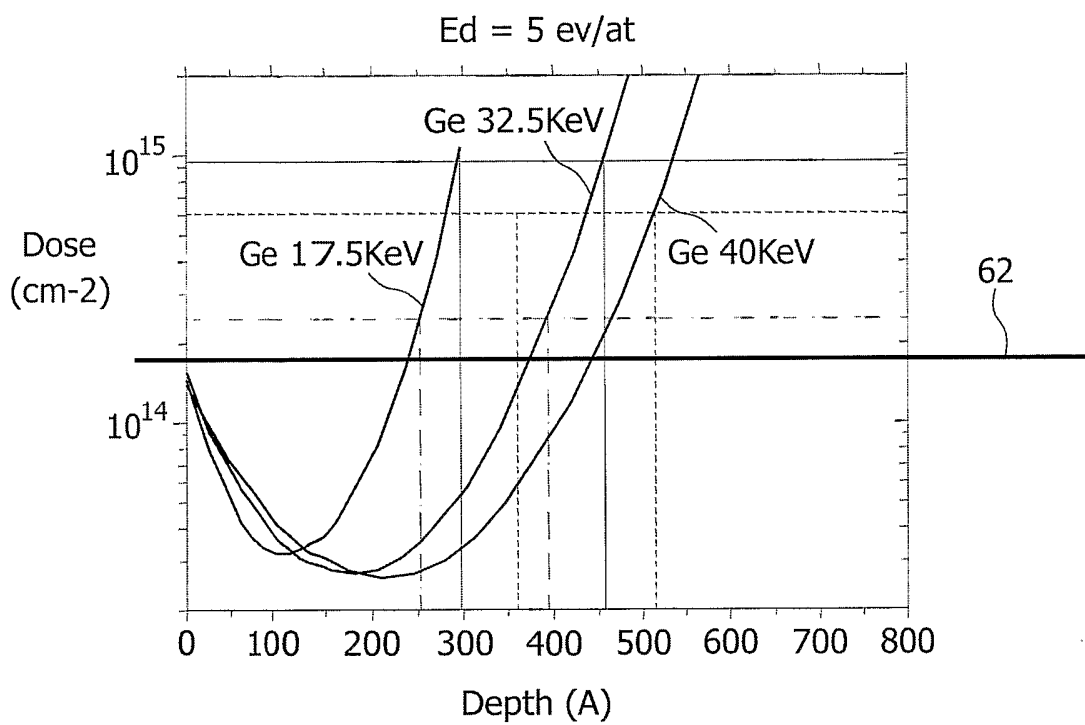


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2005/052977

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/84 H01L21/336 H01L21/265

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 463 492 A (MAEGUCHI ET AL) 7 August 1984 (1984-08-07) abstract; claims; figures 5-10 column 4, line 24 - line 27 column 4, line 60 - column 5, line 28	1-3,5
X	US 4 816 893 A (MAYER ET AL) 28 March 1989 (1989-03-28) abstract; claims; figures 1,2,6 column 3, line 21 - line 43	1-3,5-7
X	US 6 514 829 B1 (YU BIN) 4 February 2003 (2003-02-04) abstract; claims; figures 3-5 column 5, line 53 - column 6, line 42	1-5
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INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 03/075357 A (ADVANCED MICRO DEVICES, INC) 12 September 2003 (2003-09-12) abstract; claims; figures 3-11 page 4, line 20 - line 27 page 5, line 15 - line 36 page 6, line 9 - line 26 -----	1-6
X	WO 03/012844 A (ADVANCED MICRO DEVICES, INC) 13 February 2003 (2003-02-13) abstract; claims; figures 1,2 page 4, line 2 - line 13 -----	1
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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