We Claim:

1. A method for ordering memory requests requiring ordered memory accesses, the method comprising: splitting a stream of memory requests from a single source according to an address attribute into two or more streams of memory requests; identifying a memory request that requires ordered memory accesses in one of the two or more streams of memory requests, the memory request having a first address attribute; and stalling the memory request that requires ordered memory accesses upon determining a previous memory request from a different one of the two or more streams of memory requests is pending and has a second address attribute.

2. The method of claim 1, wherein the address attribute is an address boundary value.

3. The method of claim 2, wherein the address boundary value is an address bit which determines whether a memory region is an odd address memory region or an even address memory region.

4. The method of claim 2, wherein the address boundary value is determined from a plurality of bits in a memory request address that identifies one of N memory regions.

5. The method of claim 1, wherein the stream of memory requests is split according to an availability to transfer data on each stream of memory requests of the two or more streams of memory requests.

6. The method of claim 1, wherein a memory request in the stream of memory requests is directed to one of N memory regions according to the address boundary value.

7. The method of claim 1, wherein the memory request requiring ordered memory accesses is a strongly ordered memory request or a device memory request (SO/DV).

8. The method of claim 1, wherein the memory request requiring ordered memory accesses is a sequence of memory access exclusive instructions that provide atomic memory accesses.

9. The method of claim 1, wherein the stalled memory request is processed after receiving an indication that the pending previous memory request is guaranteed to complete in order.

10. The method of claim 1 further comprising: incrementing a memory access counter for each memory request; and decrementing the memory access counter for each memory request indicated to be guaranteed to complete in the desired order, wherein a count value in the memory access counter different from an initialized state of the

memory access counter indicates one or more pending requests have not been guaranteed to complete in the desired order.

11. An apparatus for ordering memory requests requiring ordered memory accesses, the apparatus comprising: a stream splitting circuit configured to monitor a first stream of memory requests from a single source and configured to split the first stream of memory requests based on address attribute of each memory request into a second stream of memory requests and a third stream of memory requests; a tracking circuit configured to detect a memory request at a first interleaved memory address requiring ordered memory accesses from the second stream of memory requests that is a different stream of memory requests from the third stream of memory requests having a pending memory request at a second interleaved memory address; and a stall circuit configured to stall the second stream of memory requests requiring ordered memory accesses in response to the pending memory request until the pending memory request is guaranteed to complete in order.

12. The apparatus of claim 11, wherein the split is determined according to the address attribute based on a number of memory regions and a memory region size.

13. The apparatus of claim 11, wherein the first stream of memory requests is split according to an availability to transfer data on each stream of memory requests of the two or more streams of memory requests.

14. The apparatus of claim 11, wherein the tracking circuit comprises: a counter that is configured to increment upon receiving a memory request from the second stream of memory requests or from the third stream of memory requests that is the same stream of memory requests as a previous memory request and to indicate the received memory request is pending, wherein the counter is configured to decrement upon receiving an acknowledgement that the pending memory request is guaranteed to complete in order.

15. The apparatus of claim 11 further comprising: a first memory region and a second memory region, wherein the second stream of memory requests is associated with the first memory region and the third stream of memory requests associated with the second memory region; and a processor configured to generate the first stream of memory requests, wherein each memory request includes an associated address attribute that identifies the first memory region as an odd address memory region and the second memory region as an even address memory region.

16. The apparatus of claim 11, wherein the address attribute is one or more address bits that identifies two or more streams of memory requests.

17. The apparatus of claim 11, further comprising: N memory regions, wherein the first stream of memory requests is monitored and split into N streams of memory requests,

wherein each stream of memory requests is associated with a different memory region of the N memory regions; and a processor configured to generate the first stream of memory requests, wherein each memory request includes an associated address attribute that identifies one of the N memory regions.

18. The apparatus of claim 11, wherein the tracking circuit comprises: a second counter that is configured to increment upon receiving a strongly ordered or device (SO/DV) memory request from a second stream of SO/DV memory requests or from a third stream of device memory requests that is the same stream of device memory requests as a previous device memory request and to indicate the received SO/DV memory request is pending, wherein the second counter is configured to decrement upon receiving an acknowledgement that the pending device memory request is guaranteed to complete in order.

19. The apparatus of claim 11, wherein the memory request requiring ordered memory accesses is a memory access exclusive instruction that provides atomic memory access.

20. The apparatus of claim 11, wherein the pending memory request is in response to a memory access exclusive instruction, wherein processing of the stalled second stream of memory requests is enabled after receiving indication that the pending memory request is guaranteed to complete in order.

21. An apparatus for ordering memory accesses, the apparatus comprising: a switch and control circuit configured to interleave a stream of memory requests into two or more streams of memory requests directed to two or more corresponding bus ports according to an attribute associated with the corresponding bus ports; a tracking circuit configured to detect a memory request at a first interleaved memory address requiring ordered memory access in a first stream of memory requests and to detect at least one pending memory request at a second interleaved memory address in a second stream of memory requests; and a stall circuit configured to stall the ordered memory access request until the tracking circuit indicates there are no more pending memory requests.

22. The apparatus of claim 21, wherein the attribute is based on a number of memory regions and a memory region size.

23. The apparatus of claim 21, wherein the stream of memory requests is from a single source and is interleaved into the two or more streams of memory requests based on an availability to transfer data on each stream of memory requests of the two or more streams of memory requests.

24. The apparatus of claim 21, wherein the attribute is based on a memory interleave address.

25. The apparatus of claim 21, wherein the attribute is based on a hash of a destination address of a memory request.

26. The apparatus of claim 21, wherein the switch and control circuit monitors a bit field within a destination address field of the memory request to determine the attribute.

27. The apparatus of claim 21, wherein the ordered memory access request has an asserted strongly ordered attribute.

28. The apparatus of claim 21, wherein the tracking circuit comprises: a memory access counter configured to increment for each received memory request and to decrement for each received memory request that is guaranteed to complete, wherein a count value in the memory access counter different from an initialized state of the memory access counter indicates there is one or more pending memory requests that have not been guaranteed to complete.

29. The apparatus of claim 21 further comprising: a tracking circuit configured to detect a memory request with an asserted device attribute in a first stream of memory requests and to detect one or more pending memory requests in a second stream of memory requests; and a stall circuit configured to stall the device memory request until the tracking circuit indicates there are no more pending memory requests.

30. The apparatus of claim 21, wherein the attribute is an address bit which determines whether a memory region is an odd address memory region or an even address memory region.

31. The apparatus of claim 21, wherein the stalled ordered memory access request is processed after receiving acknowledgements that the pending memory requests are guaranteed to complete in order.

32. An apparatus for ordering memory requests requiring ordered memory accesses, the apparatus comprising: means for monitoring a first stream of memory requests from a single source and for splitting the first stream of memory requests based on an address attribute of each memory request into a second stream of memory requests and a third stream of memory requests; means for detecting a memory request at a first interleaved memory address requiring ordered memory accesses from the second stream of memory requests that is a different stream of memory requests from the third stream of memory requests having a pending memory request at a second interleaved memory address; and means for stalling the second stream of memory requests requiring ordered memory accesses in response to the pending memory request until the pending memory request is guaranteed to complete in order.

33. An apparatus for ordering memory accesses, the apparatus comprising: means for interleaving a stream of memory requests into two or more streams of memory requests directed to two or more corresponding bus ports according to an attribute associated with the corresponding bus ports; means for detecting a memory request at a first interleaved memory address requiring ordered memory access in a first stream of memory requests and for detecting at least one pending memory request at a second interleaved memory address in a second stream of memory requests; and means for stalling the ordered memory access request until there is an indication that there are no more pending memory requests.

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Shanker

(Archana Shanker)
Of Anand and Anand Advocates
Agents for the Applicant