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(71) Applicants
N.V. Philips' Gloeilampenfabrieken,
Pieter Zeemanstraat 6,
NL-5621 CT,
Eindhoven,
The Netherlands.
(72) Inventors
Dominique Boccon Gibod
(74) Agents
R.J. Boxall,
Mullard House,
Torrington Place,
London WC1E 7HD.

(54) **Integrated series-connected diodes**

(57) An IC comprises a plurality of Schottky or p-n diodes connected in series by bridges (7) crossing isolation grooves, the lower region (3) of each diode being provided with an underlying more heavily doped layer (2) which is connected to one end of the appropriate bridge (7) by a conductive column (6). Preferably the conductive columns (6) are of metal and the diodes are supported by a semi-insulating substrate 1.

The circuit is produced by forming the semiconductor layers (2,3) on the substrate (1), applying Schottky contacts (5), etching a recess and filling it with metal to form the conductive column depositing the bridging strips, utilising the metal layers as a mask for etching grooves down to the more heavily doped layer while undercutting the bridges, and then extending the grooves between the diodes and under the bridges down to the substrate.

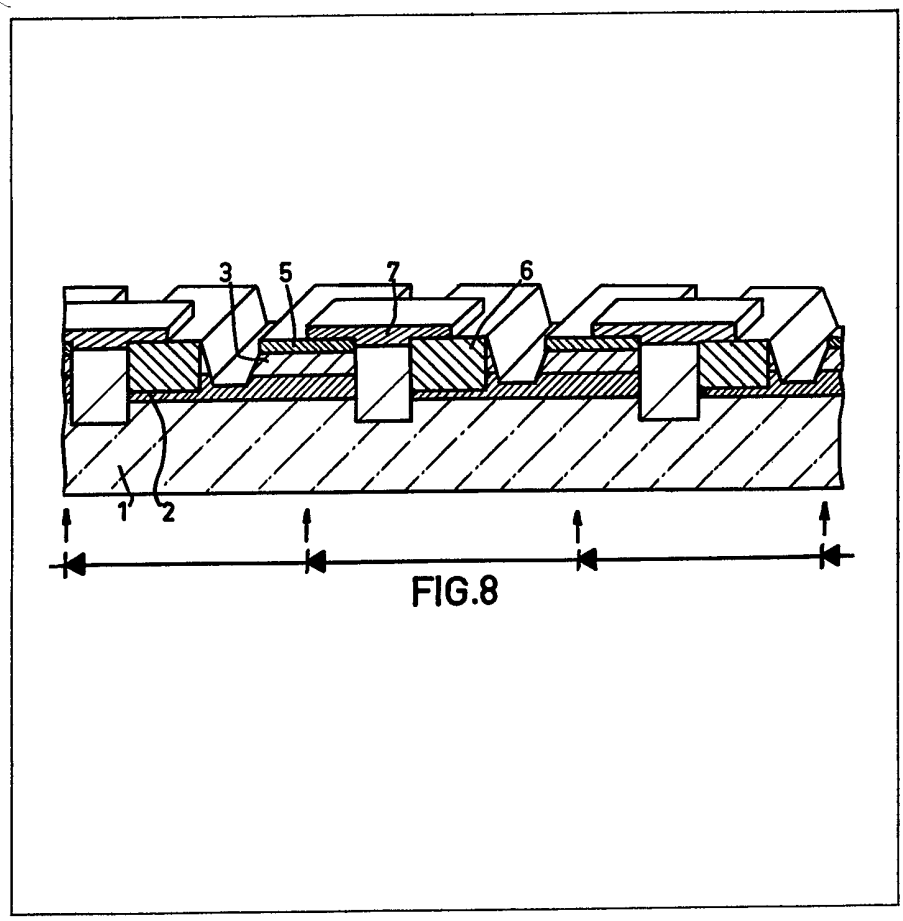

FIG.8

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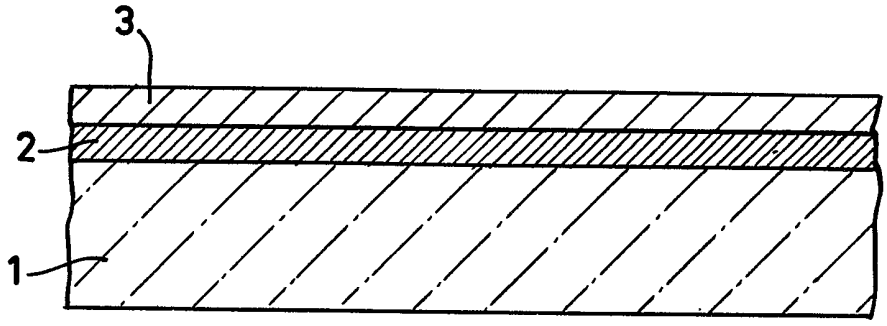

FIG.1

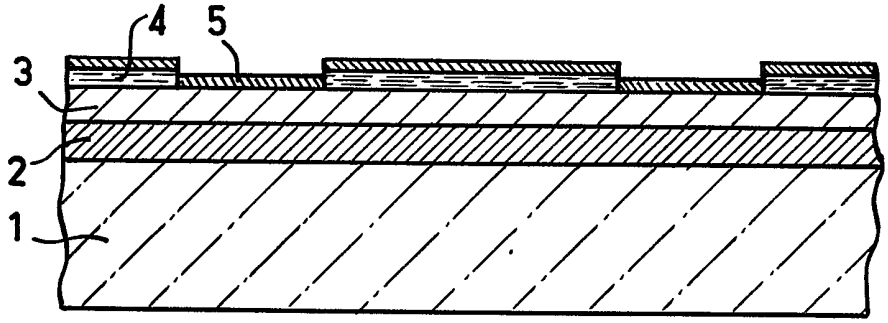

FIG.2

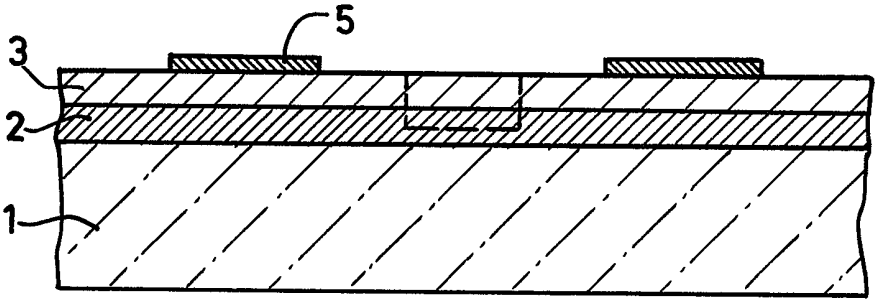

FIG.3

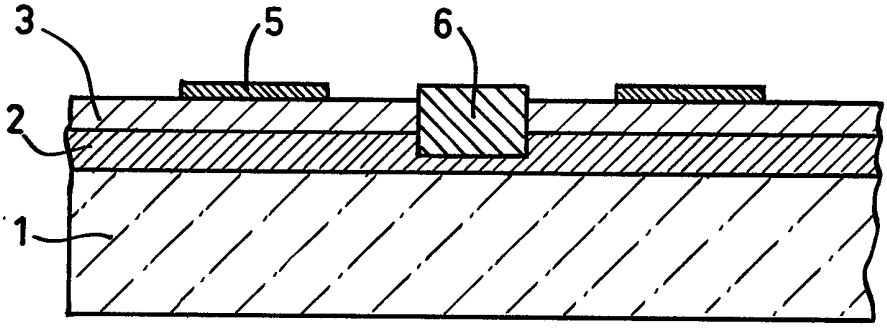

FIG.4

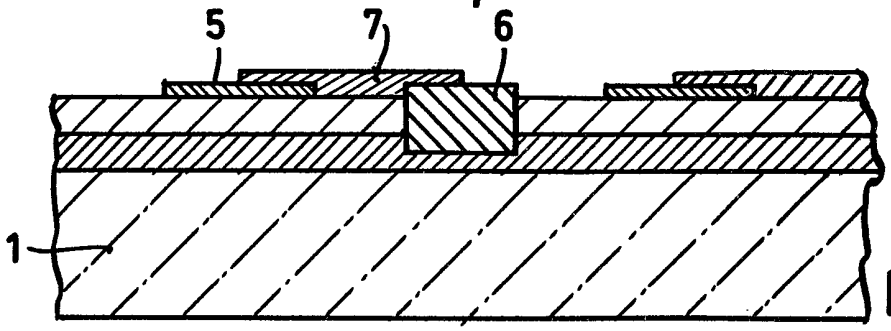

FIG.5

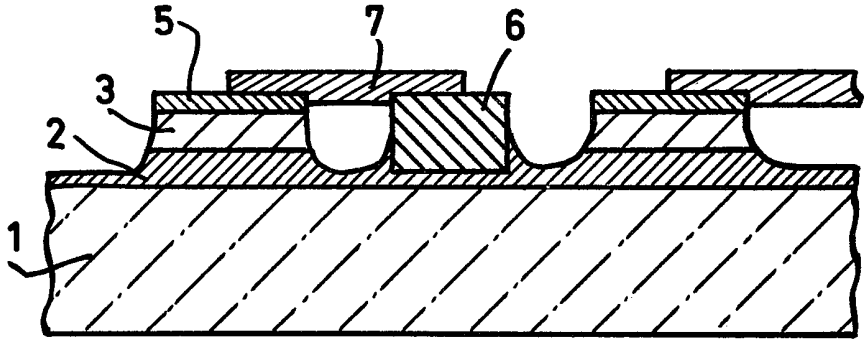

FIG.6

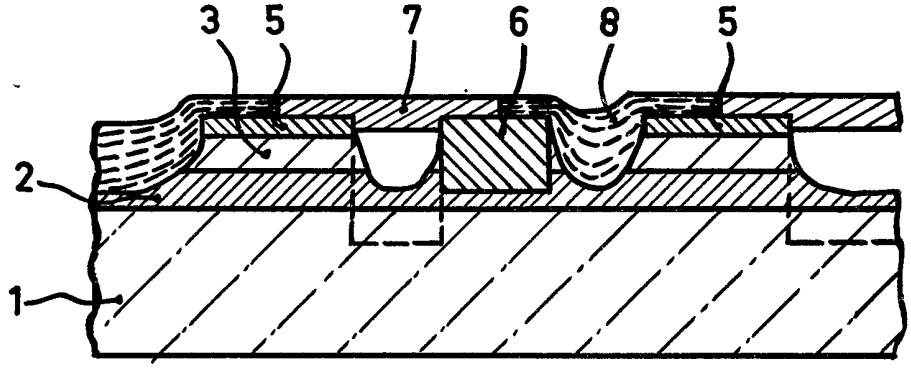

FIG.7

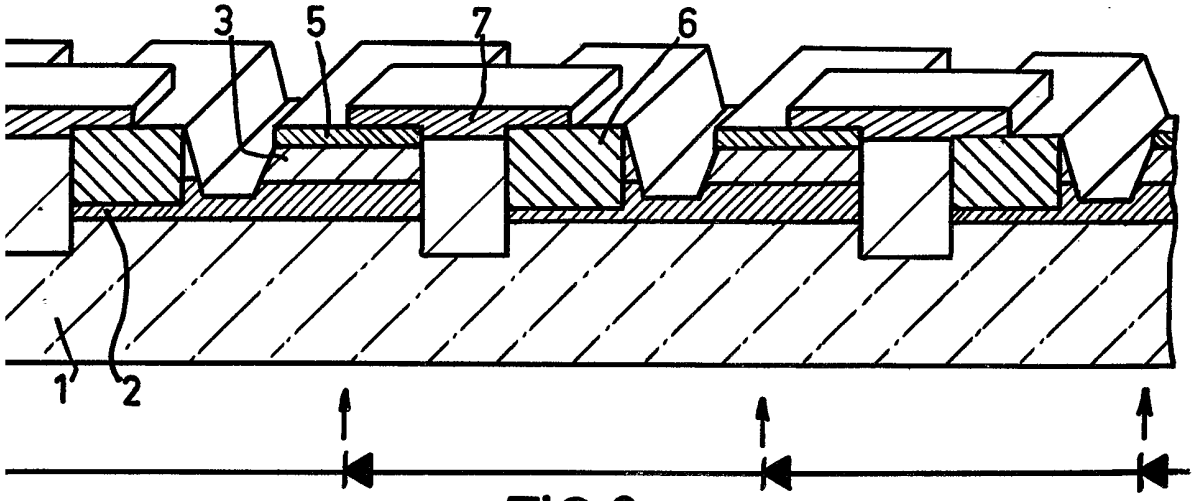

FIG.8

SPECIFICATION

Semiconductor device

The invention relates to a semiconductor device having a substrate region, a layer-shaped semiconductor region of a first conductivity type which is situated on the substrate region and which is divided into at least first and second electrically separated island-shaped parts by a groove extending into the substrate region, each part comprising an electrode region which forms a rectifying junction with the adjoining semiconductor material, the electrode region of the first part and the region of the first conductivity type of the second part being connected electrically *via* a metal strip which bridges the groove.

The invention furthermore relates to a method of manufacturing such a semiconductor device.

A semiconductor device of the kind described is disclosed in British Patent Specification GB 1,244,759.

In manufacturing semiconductor devices for high frequencies, in particular of high frequency X-band generators, it is often necessary for diodes to be connected in series so as to increase the power of said devices.

This may be done by connecting individual diodes in series. One of the disadvantages of this is that the manufacture of the diodes on the one hand and the mutual arrangement of the diodes on the other hand is carried out separately while in this manner non-flat structures are obtained.

In the semiconductor device as described in GB 1,244,759, the collector-base junctions of two *npn*-transistors separated by a V-groove are connected in series *via* a metal bridge on the same semiconductor wafer. However, the manufacture of such a device requires a large number of masking and alignment steps.

It is the object of the invention to provide a semiconductor device in which two or more diodes are connected in series on the same semiconductor wafer, which device is compact and can be manufactured in a reproducible manner by means of relatively few aligning and masking steps.

According to the invention, a semiconductor device of the kind described in the opening paragraph is characterized in that the layer-shaped semiconductor region comprises a highly doped layer adjoining the substrate region and a lower doped layer present thereon, and that the metal strip is connected to the highly doped layer by a column of electrically conductive material extending from the surface into the highly doped layer.

"Electrode region" is to be understood to mean in this Application the region across which a rectifying contact is formed with the material of the first conductivity type. In the case of a Schottky diode this is the region of the Schottky junction; in the case of a *p-n* diode this is the region of the second conductivity type which forms the *p-n* junction with the layer-shaped semiconductor region of the first conductivity type.

The conductive columns may consist of a metal or of a readily conducting semiconductor material, for example, highly doped polycrystalline silicon.

Advantageously an insulating or a so-called semi-insulating substrate region is used, although a substrate region of the second conductivity type which forms a blocking *p-n* junction with the layer-shaped region might also be used.

A preferred form of the device which can be manufactured with relatively few masking steps is characterized according to the invention in that the conductive column and the electrode region are both bounded by the said first groove and by a second groove which is present between the conductive column and the electrode region and extends from the surface to at most over a part of the thickness of the high doped layer.

The device in accordance with the invention can be manufactured in a particularly suitable manner according to a method which is characterized in that a highly doped and a lower-doped semiconductor layer of a first conductivity type are provided successively on an electrically substantially insulating substrate region, that at least two electrode regions with associated electrodes are realised on the lower doped semiconductor layer and form rectifying junctions with the said semiconductor layer, that a recess is then etched between said electrodes and extends into the highly doped layer, that said recess is filled with an electrically conductive material so as to form a conductive column, that an etchant-resistant metal strip is then provided which connects one electrode to the juxtaposed conductive column, that, while using all available electrodes and conductive columns as an etching mask, the semiconductor material is then etched away also below the metal strips in a first etching step down to at most over a part of the thickness of the highly doped layer so as to form grooves which surround the electrodes and the conductive columns, that the grooves between a conductive column and the juxtaposed electrode not connected thereto *via* a metal strip are then masked, after which the non-masked grooves are etched into the substrate region during a second etching step.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which

Figures 1 to *8* show the manufacture of a diode system according to the invention in successive stages.

According to the invention, a first highly doped semiconductor layer 2 (for example, of GaAs of the n^{++} conductivity type having a doping concentration of approximately 10^{18} atoms per cm^3 and a thickness of approximately 5μm) is provided on a substrate 1, in this example of semi-insulating gallium arsenide, see Figure 1, by means of epitaxial growth, for example, from the vapour phase, and then a second lower doped semiconductor layer 3 of the same material (for example, GaAs of the *n* conductivity type having a doping concentration of approximatey 2.10^{16} atoms/cm^3 and a thickness of approximately 4μm) is provided on top of said first layers 2.

In the manufacture of Schottky diodes, a photolacquer layer 4 is then provided which is exposed in

such manner that a number of windows situated at regular distances from each other are formed, as shown in Figure 2. A metal (5), for example aluminium, is then vapour-deposited in a vacuum and forms in an electrode region a Schottky contact with the semiconductor layer 3. After removing the photolacquer by means of a usual solvent, the metal which forms the electrodes 5 remains only in the places where previously the windows were provided in the photo-lacquer, as shown in Figure 3 (which process is known by the English name of "lift off").

In manufacturing *p-n* diodes, according to various known methods, a *p-n* junction is provided either by vapour-depositing an epitaxial layer of a conductivity type which is opposite to the conductivity type of the already existing layer 2 and 3, or by forming inside the semiconductor layer 3 electrode regions of a different coductivity type, for example, by ion implantation or by in-diffusion of dopants *via* windows. This is of no further significance for the invention.

Starting from the stage shown in Figure 3, the semiconductor material is locally etched between the various electrodes 5 by means of a suitable etchant in such manner that a cavity is formed which extends down to preferably approximately the centre of the semiconductor layer 2. A suitable etchant for a semiconductor material, for example GaAs, is, for example, a mixture of sulphuric acid and hydrogen peroxide (H_2SO_4 = 5 parts by volume; H_2O_2 = 1 part by volume, H_2O = 1 part by volume). This cavity is then filled with a readily conductive material, in this example by electrolytically growing a gold column 6 as shown in Figure 4.

The upper side of the device is then covered with a photolacquer which is exposed *via* a mask in such manner that windows can be etched in parts of the surface which are present above a metal electrode 5 and also above an immediately adjacent conductive column 6. By vapour-depositing a thin metal layer consisting, for example, of a molybdenum-gold compound in a thickness of approximately 0.5 μm and after removal (by lift-off) of the remaining lacquer, only the metal strips 7 as shown in Figure 5 are left.

The semiconductor body is then etched again, preferably down to approximately the centre of the semiconductor layer 2, so that the various elementary diodes and gold columns protected by the metal electrodes 5 are separated from each other and the strips 7 are undercut so that they are formed into bridges as shown in Figure 6.

The upper side of the device is then covered again with a photolacquer layer 8 which is maintained only in the spaces between the columns 6 and the electrodes 5 not connected by a bridge so as to mask said spaces, while the etching treatment with the same solution is continued in the non-masked places, as is shown in Figure 7.

After etching down to the semi-insulating substrate 1 and after removing the remaining lacquer by means of a usual solvent, the structure shown in Figure 8 is obtained. (Figure 8 is, in part, a perspective view).

As already stated, an etching liquid of sulphuric acid and hydrogen peroxide may be used for etching gallium arsenide; for this purpose may also be used a dilute solution of citric acid on another etchant.

The direction of the diodes is also shown diagrammatically in the conventional manner in Figure 8. The device obtained forms a series arrangement of diodes. While a metal (Al)/semiconductor (GaAsn) junction forms a diode, said diodes are interconnected by the metal bridge 7, the metal column 6 and a part of the n^{++} semiconductor layer, with which in this manner the upper side of one diode is connected to the lower side of the other diode and hence a series arrangement is obtained.

Since this circuit arrangement is provided on a semi-insulating substrate, said substrate at the same time serves as a mechanical support - all diodes are supported in the same manner and compactly - and as an electric insulation - the electrons do not penetrate into the substrate but flow through the highly doped n^{++} semiconductor layer. Since the substrate is comparatively thick, it also serves at least partly as a heat sink. However, it is not necessary for the circuit to be assembled in an envelope which comprises a cooling plate, for example of copper. Such cooling plates are sufficiently known is those skilled in the art and will not be further described here. Since the device comprises a number of diodes which during their operation give off a comparatively large amount of thermal energy, and the lower side of the substrate which is to be connected to the upper side of the cooling plate is comparatively large, it is to be preferred to use special envelopes in which the upper side of the cooling plate is optically polished. It is to be noted that the cooling plate may also be provided differently; for example, it may be advantageous, since the heat dissipation takes place substantially in the upper part of the device, to provide the cooling plate on the upper side. According to this modified embodiment the cooling plate may not be of copper or of another electrically conductive material but, for example, may consist of an electrically non-conductive readily heat conductive material, for example, beryllium oxide. The metal strips 7 may be provided directly on the surface of the cooling plate.

It will be obvious that many variations are possible to those skilled in the art without departing from the scope of the invention. For example, other semiconductor materials, other metals and other etchants may be used. The various cavities in the upper side of the semiconductor body also be filled with any dielectric material.

CLAIMS

1. A semiconductor device having a substrate region, a layer-shaped semiconductor region of a first conductivity type which is situated on the substrate region and which is divided into at least first and second electrically separated island-shaped parts by a groove extending into the substrate region, each part comprising an electrode region which forms a rectifying junction with the adjoining semiconductor material, the electrode region of the first part and the region of the first conductivity type

of the second part being connected electrically *via* a metal strip which bridges the groove, characterized in that the layer-shaped semiconductor region comprises a highly doped layer adjoining the substrate region and a lower doped layer present thereon, and that the metal strip is connected to the highly doped layer by a column of an electrically conductive material extending from the surface into the highly doped layer.

2. A semiconductor device as claimed in Claim 1, characterized in that the substrate region consists of an electrically substantially insulating material.

3. A semiconductor device as claimed in Claim 1 or 2, characterized in that the conductive column and the electrode region are both bounded by the said first groove and by a second groove which is present between the conductive column and the electrode region and extends from the surface to at most over a part of the thickness of the highly doped layer.

4. A method of manufacturing a semiconductor device as claimed in any of the preceding Claims, characterized in that a highly doped and a lower doped semiconductor layer of a first conductivity type are provided successively on an electrically substantially insulating substrate region, that at least two electrode regions with associated electrodes are realized on the lower doped semiconductor layer and form rectifying junctions with said semiconductor layer, that a recess is then etched between said electrodes and extends into the highly doped layer, that said recess is filled with an electrically conductive material so as to form a conductive column, that an etchant-resistant metal strip is then provided which connects one electrode to the juxtaposed conductive column, that, while using all electrodes and conductive columns present as an etching mask, the semiconductor material is then etched away also below the metal strips in a first etching step down to at most over a part of the thickness of the highly doped layer so as to form grooves which surround the electrodes and the conductive columns, that the grooves between a conductive column and the juxtaposed electrode not connected thereto *via* a metal strip are then masked after which the non-masked grooves are etched into the substrate region during a second etching step.

5. A method as claimed in Claim 4, characterized in that the conductive columns are manufactured by electrolytically depositing metal in the recesses.

6. A method as claimed in Claim 4 or 5, characterized in that during the first etching step the grooves are etched into the highly doped layer.

7. A semiconductor device substantially as herein described with reference to Figure 8 of the accompanying drawings.

8. A method substantially as herein described with reference to Figures 1 to 8 of the accompanying drawings.

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