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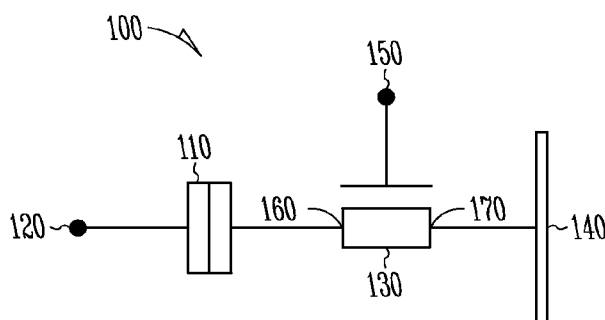


Fig. 1

(57) **Abstract:** Apparatus and methods are disclosed, including a method that performs a first operation on a first resistance variable element using a common source voltage, a first data line voltage and a first control gate voltage, and then performs a second operation on a second resistance variable element using the common source voltage, a second data line voltage and a second control gate voltage. Additional apparatus and methods are described.

RESISTANCE VARIABLE ELEMENT METHODS AND APPARATUSES

5 PRIORITY APPLICATION

[0001] This application claims the benefit of priority to US Application Serial No. 13/947,807, filed July 22, 2013, which is incorporated herein by reference in its entirety.

BACKGROUND

10 [0002] Semiconductor memory devices are used in many electronic devices such as personal digital assistants (PDAs), laptop computers, mobile phones and digital cameras. Some of these semiconductor memory devices have arrays of resistance variable memory cells.

15 BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Some embodiments are illustrated by way of example and not limitation in the figures of the accompanying drawings in which:

[0004] FIG. 1 is an electrical schematic diagram of an apparatus in the form of a resistance variable memory cell according to various embodiments of the invention;

[0005] FIG. 2 is an electrical schematic diagram of an apparatus in the form of a portion of an array of resistance variable memory cells according to various embodiments of the invention;

[0006] FIG. 3 is a timing diagram for the array of FIG. 2 according to various embodiments of the invention where each of the resistance variable memory cells may be similar or identical to the resistance variable memory cell shown in FIG. 1;

[0007] FIG. 4 is a timing diagram for the array of FIG. 2 according to various embodiments of the invention where each of the resistance variable memory cells may be similar or identical to the resistance variable memory cell shown in FIG. 1;

5 [0008] FIG. 5 is an electrical schematic diagram of an apparatus in the form of a resistance variable memory cell according to various embodiments of the invention;

[0009] FIG. 6 is an electrical schematic diagram of an apparatus in the form of a resistance variable memory cell according to various embodiments of
10 the invention;

[00010] FIG. 7 is a timing diagram for the array 200 of FIG. 2 according to various embodiments of the invention where each of the resistance variable memory cells may be similar or identical to the resistance variable memory cell shown in FIG. 6;

15 [00011] FIG. 8 is a timing diagram for the array of FIG. 2 according to various embodiments of the invention where each of the resistance variable memory cells may be similar or identical to the resistance variable memory cell shown in FIG. 6;

[00012] FIG. 9 is an electrical schematic diagram of an apparatus in the
20 form of a resistance variable memory cell according to various embodiments of the invention;

[00013] FIG. 10 is a flow diagram of a method according to various embodiments of the invention; and

[00014] FIG. 11 is a block diagram of an apparatus in the form of a memory
25 device according to various embodiments of the invention.

DETAILED DESCRIPTION

[00015] For the purposes of this document, an “apparatus” can refer to any of a number of structures, such as circuitry, a device or a system. In this description, a transistor is described as being switched on to assume an activated state when it is rendered conductive by a control gate voltage. The transistor is described as being switched off to assume an inactive state when it is rendered non-conductive by a control gate voltage. Potentials refer to electrical potentials.

[00016] A resistance variable memory cell has an architecture in which resistance states of a resistance variable element correspond to stored data. The resistance states can include a low resistance state (LRS) and a high resistance state (HRS). A resistance variable element with multiple material regions can have more than two resistance states. First data may be written by applying a predetermined drive current to a resistance variable memory cell in a first direction. Writing the first data may also be called programming the resistance variable memory cell or setting the resistance variable memory cell, both of which being referred to hereinafter as programming the resistance variable memory cells. Second data may be written by applying a predetermined drive current to the resistance variable memory cell in a second direction opposite to the first direction. Writing the second data may also be called erasing the resistance variable memory cell or resetting the resistance variable memory cell, both of which being referred to hereinafter as erasing the resistance variable memory cell. Resistance variable memory cells can be arranged in a resistive random access memory (RRAM) device.

[00017] Resistance variable memory cells can be programmed or erased with a substantial drive current through an access device. The access device may be a field-effect transistor (FET), for example. Many RRAM memory array architectures have a common source design in which a potential of a common source may be substantially constant during both program and erase operations to reduce power dissipation and write delay. A potential may be substantially constant if it does not change more than 0.2 volts in either a positive or a negative direction. The potential of the common source can have a minimum limit based on characteristics of the access device and a voltage used to program

or erase the resistance variable element. A non-zero potential on the common source can reduce current in the access device in an RRAM memory cell. The potential on the common source can reduce an effective gate-source voltage of the access device and increase the threshold voltage of the access device due to a reverse bias between source and body terminals of the access device. The substantially constant potential of the common source during program and erase operations can limit the drive current in at least one of the operations. The challenge noted above, as well as others, can be addressed by programming or erasing the resistance variable memory cells in two acts. A control gate voltage of the access device is raised for an erase operation when a data line (e.g., a bit line) is at a higher potential with respect to the common source. The control gate voltage is lowered for a program operation when the data line is at a lower potential with respect to the common source.

[00018] FIG. 1 is an electrical schematic diagram of an apparatus in the form of a resistance variable memory cell 100 according to various embodiments of the invention. The resistance variable memory cell 100 includes a resistance variable element 110 coupled between a data (e.g., bit) line 120 and an access device 130. A data line voltage may be provided on the data line 120 when an operation is performed on the resistance variable element 110. The access device 130 is coupled between the resistance variable element 110 and a common source 140 (e.g., a common source plate, a common source line, a common source slot or other common source structure). The access device 130 is a FET and in particular an n-channel FET. The access device 130 includes a gate terminal 150 coupled to an access (e.g., word) line (not shown), a first terminal 160 coupled to the resistance variable element 110 and a second terminal 170 coupled to the source 140. The access device 130 can be controlled by a control gate voltage on the gate terminal 150 and provided on the access line. The source 140 may be coupled to thousands or millions of other resistance variable memory cells and can have a common source voltage that is substantially constant. The access device 130 may allow current to flow between the data line 120 and the source 140 when it is switched on by the potential on its gate terminal 150. The first terminal 160 can be a drain or a source and the second terminal 170 can be a drain or a source depending on the

direction of current in the access device 130. The data line 120 may be used to sense (e.g., read) a data state of the resistance variable element 110. The data state of the resistance variable element 110 can be read by measuring a resistance value of the resistance variable element 110 which can include sensing
5 a value of a current flowing through the resistance variable element 110.

[00019] FIG. 2 is an electrical schematic diagram of an apparatus in the form of a portion of an array 200 of resistance variable memory cells according to various embodiments of the invention. The array 200 can be formed on a semiconductor substrate (not shown). The array 200 includes resistance variable
10 memory cells 201, 202, 203, 211, 212, 213, 221, 222 and 223. Each of the resistance variable memory cells 201-223 may be similar or identical to the resistance variable memory cell 100 shown in FIG. 1 and includes the access device 130 coupled to the resistance variable element 110.

[00020] The resistance variable memory cells 201, 211 and 221 are in a first row 250 and the access devices 130 of the resistance variable memory cells 201, 211 and 221 are coupled to a first access line 252. The resistance variable memory cells 202, 212 and 222 are in a second row 254 and the access devices 130 of the resistance variable memory cells 202, 212 and 222 are coupled to a second access line 256. The resistance variable memory cells 203, 213 and 223
20 are in a third row 258 and the access devices 130 of the resistance variable memory cells 203, 213 and 223 are coupled to a third access line 259.

[00021] The resistance variable memory cells 201, 202 and 203 are in a first column 260 and the resistance variable elements 110 of the resistance variable memory cells 201, 202 and 203 are coupled to a first data line 262. The
25 resistance variable memory cells 211, 212 and 213 are in a second column 264 and the resistance variable elements 110 of the resistance variable memory cells 211, 212 and 213 are coupled to a second data line 266. The resistance variable memory cells 221, 222 and 223 are in a third column 268 and the resistance variable elements 110 of the resistance variable memory cells 221, 222 and 223
30 are coupled to a third data line 269. The array 200 may have more or less than the nine resistance variable memory cells 201-223 shown in Figure 2.

[00022] With reference to FIG. 1 and FIG. 2, the resistance variable memory cell 100 can be programmed to store a first value (e.g., a logic “1”) by driving a first current through the resistance variable element 110 in a first direction. The resistance variable memory cell 100 can be erased to store a second value (e.g., a logic “0”) by driving a second current through the resistance variable element 110 in a second direction opposite to the first direction. The second current may be substantially equal to the first current. The access device 130 is biased to conduct the first current in the first direction and the second current in the second direction. The gate terminal 150 can be biased by a first control gate voltage during programming of the first value and by a different second control gate voltage during erasing to the second value to provide sufficient drive current through the resistance variable element 110. Two or more of the resistance variable memory cells 201-223 may be programmed or erased at the same time with the same voltage on one or more of the access lines 252, 256 and 259. The first value is programmed into one or more of the resistance variable memory cells 100 at a first time, and one or more of the resistance variable memory cells 100 is erased to store the second value at a second time.

[00023] FIG. 3 is a timing diagram 300 for the array 200 of FIG. 2 according to various embodiments of the invention where each of the resistance variable memory cells 201-223 may be similar or identical to the resistance variable memory cell 100 shown in FIG. 1. The timing diagram 300 illustrates voltages in the array 200 during a programming operation and/or an erasing operation for the resistance variable memory cells 201, 211 and 221 in the first row 250. The voltages are represented on a vertical axis 302 and time t is represented on a horizontal axis 304. Data line voltages on the data lines 120, 262, 266 and 269 are illustrated at the bottom of the timing diagram 300. A control gate voltage on the access line 252 and the gate terminals 150 of the access devices 130 is illustrated above the data line voltages. Control gate voltages on the access lines 256 and 259 may be the same as the control gate voltage on the access line 252.

[00024] The control gate voltage on the access line 252 is at V_{WL_low} which can be a reference voltage (e.g., ground) before programming begins. Programming begins at a time t_1 when the control gate voltage on the access line 252 rises to a first pulse at a voltage V_{WL_highA} which is sufficient to switch on the access device 130 to program the first value into one or more of the resistance variable memory cells 201-223. Each pulse comprises a raised (or lowered) electrical potential of a limited duration. One or more of the data lines 262, 266 and 269 are held at a standby data line voltage. The standby data line voltage can be substantially equal to a source voltage V_{PL} which is the potential of the source 140 such that none of the resistance variable memory cells 201-223 coupled to a data line 262, 266 and 269 at the source voltage V_{PL} is programmed or erased. One or more of the data lines 262, 266 and 269 are brought to a lower voltage V_{BL_low} at the time t_1 to program the resistance variable memory cells 201, 211 and 221 coupled to the data lines 262, 266 and 269 at V_{BL_low} to the first value. The voltage V_{BL_low} is lower than the source voltage V_{PL} . The pulse on the access line 252 ends at a time t_2 when the potential of the access line 252 falls to V_{WL_low} . The potential of the data lines 262, 266 and 269 (at V_{BL_low}) is raised to the source voltage V_{PL} at the time t_2 to end the programming. One or more of the resistance variable memory cells 201, 211 and 221 is programmed to the first value during the pulse on the access line 252 between the times t_1 and t_2 .

[00025] Erasing begins at a time t_3 when the control gate voltage on the access line 252 rises from V_{WL_low} to begin a second pulse at a voltage V_{WL_highB} which is sufficient to switch on the access device 130 to erase the second value into one or more of the resistance variable memory cells 201-223. The voltage V_{WL_highB} is higher than the voltage V_{WL_highA} . A difference between the voltage V_{WL_highA} and the voltage V_{WL_highB} is less than or equal to the source voltage V_{PL} . The voltage V_{WL_highB} may be substantially equal to the voltage V_{WL_highA} plus the source voltage V_{PL} . A first voltage may be substantially equal to a second voltage if it does not differ from the second voltage by more than 0.2 volts. One or more of the data lines 262, 266 and 269 are held at the source voltage V_{PL} such that none of the resistance variable memory cells 201-223 coupled to a data line 262, 266 and 269 at the source voltage V_{PL} is erased. One

or more of the data lines 262, 266 and 269 are raised to a higher voltage V_{BL_high} at the time t3 to erase one or more of the resistance variable memory cells 201, 211 and 221 coupled to the data lines 262, 266 and 269 at V_{BL_high} to the second value. The voltage V_{BL_high} is higher than the source voltage V_{PL} . The pulse on the access line 252 ends and the potential of the data lines 262, 266 and 269 at V_{BL_high} is lowered to the source voltage V_{PL} at a time t4 to end the erase. One or more of the resistance variable memory cells 201, 211 and 221 is erased to the second value during the pulse on the access line 252 between the times t3 and t4. The resistance variable memory cells 201, 211 and 221 that were erased to the second value between the times t3 and t4 may be the same or different than the resistance variable memory cells 201, 211 and 221 programmed to the first value between the times t1 and t2.

[00026] Specific values of the voltages shown in the timing diagram 300 resistance variable memory cell 100 are listed in TABLE I according to various embodiments of the invention:

SIGNAL	VOLTS
V_{PL}	1.5
V_{BL_low}	0
V_{BL_high}	3
V_{WL_low}	0
V_{WL_highA}	4.5
V_{WL_highB}	6

TABLE I

The voltages listed in TABLE I show that the source 140 is at approximately 1.5 volts through the acts of programming and erasing. With respect to FIG. 1, the

gate terminal 150 is at approximately 4.5 volts and the data line 120 is at approximately 0 volts when the resistance variable element 110 is being programmed between the times t1 and t2 to store the first value. Current flows from the source 140 to the data line 120, and the terminal 160 is the source such that a gate-source voltage difference V_{GS} is approximately 4.5 volts for the access device 130. The gate terminal 150 is at approximately 6 volts and the data line 120 is at approximately 3 volts when the resistance variable element 110 is being erased between the times t3 and t4 to store the second value. Current flows from the data line 120 to the source 140, and the terminal 170 is the source such that the gate-source voltage difference V_{GS} is approximately 4.5 volts for the access device 130. Through the acts of programming and erasing the gate-source voltage difference V_{GS} is not substantially higher than approximately 4.5 volts so that the access device 130 is not compromised.

[00027] FIG. 4 is a timing diagram 400 for the array 200 of FIG. 2 according to various embodiments of the invention where each of the resistance variable memory cells 201-223 may be similar or identical to the resistance variable memory cell 100 shown in FIG. 1. The timing diagram 400 illustrates voltages in the array 200 during programming and erasing for the resistance variable memory cells 201, 211 and 221 in the first row 250. The voltages are represented on a vertical axis 402 and time t is represented on a horizontal axis 404. Data line voltages on the data lines 262, 266 and 269 are illustrated at the bottom of the timing diagram 400. A control gate voltage on the access line 252 and the gate terminals 150 of the access devices 130 are illustrated above the data line voltages. Control gate voltages on the access lines 256 and 259 may be the same as the control gate voltage on the access line 252.

[00028] The resistance variable memory cells 201, 211 and 221 are programmed and/or erased according to the timing diagram 400 to store the same values that were programmed and/or erased according to the timing diagram shown in FIG. 3. The voltages on the data lines 262, 266 and 269 in timing diagram 400 are similar to the voltages on the data lines 262, 266 and 269 in timing diagram 300 and will not be further described for purposes of brevity and clarity. The difference is that the pulses on the access line 252 are merged

into a single signal from the time t_1 to the time t_4 . In other words, instead of returning the control gate voltage to V_{WL_low} between times t_2 and t_3 , the control gate voltage is simply raised from V_{WL_highA} to V_{WL_highB} .

[00029] All of the resistance variable memory cells that are being
5 programmed may be programmed at the same time with a first control gate voltage. All of the resistance variable memory cells that are being erased may be erased at the same time with a second control gate voltage according to various embodiments of the invention.

[00030] FIG. 5 is an electrical schematic diagram of an apparatus in the
10 form of a resistance variable memory cell 500 according to various embodiments of the invention. The resistance variable memory cell 500 includes a resistance variable element 510. A data line 520 is coupled to an access device 530, and the access device 530 is coupled to the resistance variable element 510. A data line voltage may be provided on the data line 520 when an operation is
15 performed on the resistance variable element 510. In contrast to the embodiment of FIG. 1, the resistance variable element 510 is coupled between the access device 530 and a common source 540. The access device 530 is a FET and in particular an n-channel FET. The access device 530 includes a gate terminal 550 coupled to an access line (not shown), a first terminal 560 coupled to the data
20 line 520 and a second terminal 570 coupled to the resistance variable element 510. The access device 530 can be controlled by a control gate voltage on the gate terminal 550 and provided on the access line. The source 540 may be coupled to thousands or millions of other resistance variable memory cells and can have a common source voltage that is substantially constant. The access
25 device 530 may allow current to flow between the data line 520 and the source 540 when it is switched on by the potential on its gate terminal 550. The first terminal 560 can be a drain or a source and the second terminal 570 can be a drain or a source depending on the direction of current in the access device 530. The data line 520 may be used to sense a data state of the resistance variable
30 element 510. The data state of the resistance variable element 510 can be read by measuring a resistance value of the resistance variable element 510 which can include sensing a value of a current flowing through the resistance variable

element 510. Each of the resistance variable memory cells 201-223 in the array 200 shown in FIG. 2 may be similar or identical to the resistance variable memory cell 500 shown in FIG. 5 and includes the access device 530 coupled to the resistance variable element 510.

- 5 [00031] The resistance variable memory cell 500 can be programmed or erased according to the timing diagrams 300 and 400 shown in FIGs. 3 and 4 although the voltages are different than the voltages shown in Table I. Specific values of the voltages shown in the timing diagrams 300 and 400 for the resistance variable memory cell 500 are listed in TABLE II according to various
- 10 embodiments of the invention:

SIGNAL	VOLTS
V_{PL}	1.5
V_{BL_low}	0
V_{BL_high}	3
V_{WL_low}	0
V_{WL_highA}	4.5
V_{WL_highB}	6.4

TABLE II

- The voltages listed in TABLE II show that the source 540 is at approximately 1.5 volts through the acts of programming and erasing. With respect to FIG. 5, the gate terminal 550 is at approximately 4.5 volts and the data line 520 is at
- 15 approximately 0 volts when the resistance variable element 510 is being programmed between the times t_1 and t_2 to store the first value. Current flows from the source 540 to the data line 520, and the terminal 560 is the source such that a gate-source voltage difference V_{GS} is approximately 4.5 volts for the

access device 530. The gate terminal 550 is at approximately 6.4 volts and the data line 520 is at approximately 3 volts when the resistance variable element 510 is being erased between the times t3 and t4 to store the second value. Assuming a voltage drop of about 0.4V on the resistance variable element 510, the gate to source voltage in this case is approximately 4.5V. Current flows from the data line 520 to the source 540, and the terminal 570 is the source such that the gate-source voltage difference V_{GS} is approximately 4.5 volts for the access device 530. Through the acts of programming and erasing the gate-source voltage difference V_{GS} is not substantially higher than approximately 4.5 volts so that the access device 530 is not compromised.

[00032] A resistance variable memory cell may have an access device that is a p-channel FET. FIG. 6 is an electrical schematic diagram of an apparatus in the form of a resistance variable memory cell 600 according to various embodiments of the invention. The resistance variable memory cell 600 includes a resistance variable element 610 coupled between a data line 620 and an access device 630. A data line voltage may be provided on the data line 620 when an operation is performed on the resistance variable element 610. The access device 630 is coupled between the resistance variable element 610 and a common source 640. The access device 630 is a FET and in particular a p-channel FET. The access device 630 includes a gate terminal 650 coupled to an access line (not shown), a first terminal 660 coupled to the resistance variable element 610 and a second terminal 670 coupled to the source 640. The access device 630 can be controlled by a control gate voltage on the gate terminal 650 and provided on the access line. The source 640 may be coupled to hundreds or thousands of other resistance variable memory cells and can have a common source voltage that is substantially constant. The access device 630 may allow current to flow between the data line 620 and the source 640 when it is switched on by the potential on its gate terminal 650. The first terminal 660 can be a drain or a source and the second terminal 670 can be a drain or a source depending on the direction of current in the access device 630. The data line 620 may be used to sense a data state of the resistance variable element 610. The data state of the resistance variable element 610 can be read by measuring a resistance value of the resistance variable element 610 which can include sensing

a value of a current flowing through the resistance variable element 610. Each of the resistance variable memory cells 201-223 in the array 200 shown in FIG. 2 may be similar or identical to the resistance variable memory cell 600 shown in FIG. 6 and includes the access device 630 coupled to the resistance variable
 5 element 610.

[00033] FIG. 7 is a timing diagram 700 for the array 200 of FIG. 2 according to various embodiments of the invention where each of the resistance variable memory cells 201-223 may be similar or identical to the resistance variable memory cell 600 shown in FIG. 6. The timing diagram 700 illustrates
 10 voltages in the array 200 during a programming operation and/or an erasing operation for the resistance variable memory cells 201, 211 and 221 in the first row 250. The voltages are represented on a vertical axis 702 and time t is represented on a horizontal axis 704. Data line voltages on the data lines 620, 262, 266 and 269 are illustrated at the bottom of the timing diagram 700. A
 15 control gate voltage on the access line 252 and the gate terminals 650 of the access devices 630 are illustrated above the data line voltages. Control gate voltages on the access lines 256 and 259 may be the same as the control gate voltage on the access line 252.

[00034] The control gate voltage on the access line 252 is at V_{WL_high} which
 20 can be V_{BL_high} or a supply voltage V_{cc} before programming begins. Programming begins at a time t_1 when the control gate voltage on the access line 252 falls to a first pulse at a voltage V_{WL_lowA} which is sufficient to switch on the access devices 630 to program the first value into one or more of the resistance variable memory cells 201-223. One or more of the data lines 262, 266 and 269
 25 are held at a standby data line voltage. The standby data line voltage can be substantially equal to a source voltage V_{PL} (the potential of the source 640) such that none of the resistance variable memory cells 201-223 coupled to a data line 262, 266 and 269 at the source voltage V_{PL} is programmed. One or more of the data lines 262, 266 and 269 are brought to a lower voltage V_{BL_low} at the time t_1
 30 to program the resistance variable memory cells 201, 211 and 221 coupled to the data lines 262, 266 and 269 at V_{BL_low} to the first value. The voltage V_{BL_low} is lower than the source voltage V_{PL} . The pulse on the access line 252 ends at a

time t_2 when the potential of the access line 252 rises to V_{WL_low} . The potential of the data lines 262, 266 and 269 at V_{BL_low} is raised to the source voltage V_{PL} at the time t_2 to end the programming. One or more of the resistance variable memory cells 201, 211 and 221 is programmed to the first value during the pulse
 5 on the access line 252 between the times t_1 and t_2 .

[00035] Erasing begins at a time t_3 when the control gate voltage on the access line 252 falls from V_{WL_high} to begin a second pulse at a voltage V_{WL_lowB} which is sufficient to switch on the access devices 630 to erase the second value into one or more of the resistance variable memory cells 201-223. The voltage
 10 V_{WL_lowB} is higher than the voltage V_{WL_lowA} . A difference between the voltage V_{WL_lowA} and the voltage V_{WL_lowB} is less than or equal to the source voltage V_{PL} . The voltage V_{WL_lowB} may be substantially equal to the voltage V_{WL_lowA} plus the source voltage V_{PL} . One or more of the data lines 262, 266 and 269 are held at the source voltage V_{PL} such that none of the resistance variable memory cells
 15 201-223 coupled to a data line 262, 266 and 269 at the source voltage V_{PL} is erased. One or more of the data lines 262, 266 and 269 are raised to a higher voltage V_{BL_high} at the time t_3 to erase one or more of the resistance variable memory cells 201, 211 and 221 coupled to the data lines 262, 266 and 269 at V_{BL_high} to the second value. The voltage V_{BL_high} is higher than the source
 20 voltage V_{PL} . The pulse on the access line 252 ends and the potential of the data lines 262, 266 and 269 at V_{BL_high} is lowered to the source voltage V_{PL} at a time t_4 to end the erase. One or more of the resistance variable memory cells 201, 211 and 221 is erased to the second value during the pulse on the access line 252 between the times t_3 and t_4 . The resistance variable memory cells 201, 211 and
 25 221 that were erased to the second value between the times t_3 and t_4 may be the same or different than the resistance variable memory cells 201, 211 and 221 programmed to the first value between the times t_1 and t_2 .

[00036] Specific values of the voltages shown in the timing diagram 700 resistance variable memory cell 600 are listed in TABLE III according to various
 30 embodiments of the invention:

SIGNAL	VOLTS
V_{PL}	1.5
V_{BL_low}	0
V_{BL_high}	3
V_{WL_high}	3
V_{WL_lowA}	-3
V_{WL_lowB}	-1.5

TABLE III

The voltages listed in TABLE III show that the source 640 is at approximately 1.5 volts through the acts of programming and erasing. With respect to FIG. 6, the gate terminal 650 is at approximately -3 volts and the data line 620 is at approximately 0 volts when the resistance variable element 610 is being programmed between the times t1 and t2 to store the first value. Current flows from the source 640 to the data line 620, and the terminal 670 is the source such that a gate-source voltage difference V_{GS} is approximately -4.5 volts for the access device 630. The gate terminal 650 is at approximately -1.5 volts and the data line 120 is at approximately 3 volts when the resistance variable element 610 is being erased between the times t3 and t4 to store the second value. Current flows from the data line 620 to the source 640, and the terminal 660 is the source such that the gate-source voltage difference V_{GS} is approximately -4.5 volts for the access device 630. Through the acts of programming and erasing the gate-source voltage difference V_{GS} is not substantially lower than approximately -4.5 volts so that the access device 630 is not compromised.

[00037] FIG. 8 is a timing diagram 800 for the array 200 of FIG. 2 according to various embodiments of the invention where each of the resistance variable memory cells 201-223 may be similar or identical to the resistance

variable memory cell 600 shown in FIG. 6. The timing diagram 800 illustrates voltages in the array 200 during programming and erasing for the resistance variable memory cells 201, 211 and 221 in the first row 250. The voltages are represented on a vertical axis 802 and time t is represented on a horizontal axis 804. Data line voltages on the data lines 262, 266 and 269 are illustrated at the bottom of the timing diagram 800. A control gate voltage on the access line 252 and the gate terminals 650 of the access devices 630 are illustrated above the data line voltages. Control gate voltages on the access lines 256 and 259 may be the same as the control gate voltage on the access line 252.

[00038] The resistance variable memory cells 201, 211 and 221 are programmed and/or erased according to the timing diagram 800 to store the same values that were programmed and/or erased according to the timing diagram shown in FIG. 7. The voltages on the data lines 262, 266 and 269 in timing diagram 800 are similar to the voltages on the data lines 262, 266 and 269 in timing diagram 700 and will not be further described for purposes of brevity and clarity. The difference is that the pulses on the access line 252 are merged into a single signal from the time t_1 to the time t_4 . In other words, instead of returning the control gate voltage to V_{WL_low} between times t_2 and t_3 , the control gate voltage is simply raised from V_{WL_lowA} to V_{WL_lowB} .

[00039] FIG. 9 is an electrical schematic diagram of an apparatus in the form of a resistance variable memory cell 900 according to various embodiments of the invention. The resistance variable memory cell 900 includes a resistance variable element 910. A data line 920 is coupled to an access device 930, and the access device 930 is coupled to the resistance variable element 910. A data line voltage may be provided on the data line 920 when an operation is performed on the resistance variable element 910. In contrast to the embodiment of FIG. 1, the resistance variable element 910 is coupled between the access device 930 and a common source 940. The access device 930 is a FET and in particular a p-channel FET. The access device 930 includes a gate terminal 950 coupled to an access line (not shown), a first terminal 960 coupled to the data line 920 and a second terminal 970 coupled to the resistance variable element 910. The access device 930 can be controlled by a control gate voltage on the

gate terminal 950 and provided on the access line. The source 940 may be coupled to thousands or millions of other resistance variable memory cells and can have a common source voltage that is substantially constant. The access device 930 may allow current to flow between the data line 920 and the source 940 when it is switched on by the potential on its gate terminal 950. The first terminal 960 can be a drain or a source and the second terminal 970 can be a drain or a source depending on the direction of current in the access device 930. The data line 920 may be used to sense a data state of the resistance variable element 910. The data state of the resistance variable element 910 can be read by measuring a resistance value of the resistance variable element 910 which can include sensing a value of a current flowing through the resistance variable element 910. Each of the resistance variable memory cells 201-223 in the array 200 shown in FIG. 2 may be similar or identical to the resistance variable memory cell 900 shown in FIG. 9 and includes the access device 930 coupled to the resistance variable element 910.

[00040] The resistance variable memory cell 900 can be programmed or erased according to the timing diagrams 700 and 800 shown in FIGs. 7 and 8 although the voltages are different than the voltages shown in Table III. Specific values of the voltages shown in the timing diagrams 700 and 800 for the resistance variable memory cell 900 are listed in TABLE IV according to various embodiments of the invention:

SIGNAL	VOLTS
V_{PL}	1.5
V_{BL_low}	0
V_{BL_high}	3

V_{WL_high}	3
V_{WL_lowA}	-3.4
V_{WL_lowB}	-1.5

TABLE IV

The voltages listed in TABLE IV show that the source 940 is at approximately 1.5 volts through the acts of programming and erasing. With respect to FIG. 9, the gate terminal 950 is at approximately -3.4 volts and the data line 920 is at approximately 0 volts when the resistance variable element 910 is being programmed between the times t1 and t2 to store the first value. Current flows from the source 940 to the data line 920, and the terminal 970 is the source such that a gate-source voltage difference V_{GS} is approximately -4.5 volts for the access device 930. The gate terminal 950 is at approximately -1.5 volts and the data line 920 is at approximately 3 volts when the resistance variable element 910 is being erased between the times t3 and t4 to store the second value. Current flows from the data line 920 to the source 940, and the terminal 960 is the source such that the gate-source voltage difference V_{GS} is approximately -4.5 volts for the access device 930. Through the acts of programming and erasing the gate-source voltage difference V_{GS} is not substantially lower than approximately -4.5 volts so that the access device 930 is not compromised.

[00041] FIG. 10 is a flow diagram of a method 1000 according to various embodiments of the invention. In block 1010, the method 1000 starts. In block 1020, a first access device is switched on with a first control gate voltage and a first data line voltage is provided to a first data line. A first resistance variable element coupled to the first access device is then programmed in a first operation. In block 1030, a second data line voltage is provided to a second data line that is different than the first data line voltage. A second access device is switched on with a second control gate voltage that is different than the first control gate voltage. A second resistance variable element coupled to the second access device is then erased in a second operation. In block 1040, the method

1000 ends. Various embodiments may have more or fewer activities than those shown in FIG. 10. In some embodiments, the activities may be repeated, and/or performed in serial or parallel fashion. Some embodiments may comprise the same activities in a different order.

5 [00042] FIG. 11 is a block diagram of an apparatus in the form of a memory device 1100 according to various embodiments of the invention. The memory device 1100 can include a plurality of memory cells 1101 in a memory array 1102. The memory cells 1101 can be arranged in rows and columns along with access lines 1104 and first data lines 1106. The memory device 1100 can use the
10 access lines 1104 and the first data lines 1106 to transfer data to and from the memory cells 1101. A row decoder 1107 and a column decoder 1108 can decode address signals A0 through AX on address lines 1109 to determine which ones of the memory cells 1101 are to be accessed.

[00043] A sense amplifier circuit 1110 can operate to determine the value of
15 data read from memory cells 1101 and the data read is communicated in the form of signals to the first data lines 1106. The sense amplifier circuit 1110 can also use the signals on the first data lines 1106 to determine values of data to be written to the memory cells 1101.

[00044] The memory device 1100 can include circuitry 1111 to transfer data
20 between the memory array 1102 and input/output (I/O) lines 1112. Signals DQ0 through DQN on the I/O lines 1112 can represent data read from or written into the memory cells 1101. The I/O lines 1112 can include nodes within the memory device 1100 (or alternatively, pins, solder balls, or other interconnect technologies such as controlled collapse chip connection (C4), or flip chip attach
25 (FCA)) on a package where the memory device 1100 can reside. Other devices external to memory device 1100 can communicate with the memory device 1100 through the I/O lines 1112, the address lines 1109, or control lines 1120. For example, such external devices can include a memory controller or a processor.

[00045] The memory device 1100 can perform memory operations, such as
30 a read operation, to read data from selected ones of the memory cells 1101, and a write operation to store data into selected ones of the memory cells 1101. A

memory control unit 1122 controls memory operations based on signals on the control lines 1120. Examples of the signals on the control lines 1120 can include one or more clock signals and other signals to indicate which operation (e.g., a write or a read operation) the memory device 1100 can or should perform. Other devices external to the memory device 1100 can control the values of the control signals on the control lines 1120. The external devices can include, for example, a processor or a memory controller. Specific values of a combination of the control signals on the control lines 1120 can produce a command, such as a write or read command for example, that can cause the memory device 1100 to perform a corresponding memory operation. The corresponding memory operation can include, for example, a write or a read operation.

[00046] Each of the memory cells 1101 can be programmed or erased to store data representing a value of a single bit or a value of multiple bits such as two, three, four, or a higher number of bits. For example, each of the memory cells 1101 can be programmed or erased to store data representing a binary value “0” or “1” of a single bit. The single bit per cell is sometimes called a single level cell. In another example, each of the memory cells 1101 can be programmed or erased to store data representing a value representing multiple bits, such as one of four possible values “00,” “01,” “10,” and “11” of two bits, one of eight possible values “000,” “001,” “010,” “011,” “100,” “101,” “110,” and “111” of three bits, or one of another set of values of multiple bits. A cell that has an ability to store multiple bits is sometimes referred to as a multi-level cell or multi-state cell.

[00047] The memory device 1100 can receive a supply voltage, including supply voltage signals Vcc and Vss, on a first supply line 1130 and a second supply line 1132, respectively. The supply voltage signal Vss can operate at a ground potential. The ground potential can have a value of approximately zero volts. The supply voltage signal Vcc can include an external voltage supplied to the memory device 1100 from an external power source such as a battery or an alternating current to direct current (AC-DC) converter circuitry.

[00048] The circuitry 1111 of memory device 1100 can include a select circuit 1124 and an input/output (I/O) circuit 1126. Select circuit 1124 can respond to signals SEL1 through SELn to select signals on first data lines 1106 and second data lines 1113 that can represent the data read from or to be written
5 into memory cells 1101. Column decoder 1108 can selectively activate the SEL1 through SELn signals based on the A0 through AX address signals on address lines 1109. Select circuit 1124 can select the signals on first data lines 1106 and second data lines 1113 to provide communication between memory array 1102 and I/O circuit 1126 during read and write operations.

10 [00049] The memory cells 1101 can comprise one or more of the resistance variable memory cells 100, 500, 600 and 900 shown in FIGs. 1, 5, 6 and 9, respectively. The memory device 1100 can include the array 200 of resistance variable memory cells shown in FIG. 2 including one or more of the resistance variable memory cells 100, 500, 600 and 900 shown in FIGs. 1, 5, 6 and 9,
15 respectively.

[00050] The methods described herein can result in higher drive current from an access device in a resistance variable memory cell. This can lead to a significant performance improvement over conventional technology.

[00051] Example structures and methods of resistance variable elements
20 have been described. Although specific embodiments have been described, it will be evident that various modifications and changes may be made to these embodiments. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

[00052] The Abstract of the Disclosure is provided to comply with 37
C.F.R. §1.72(b), requiring an abstract that allows the reader to quickly ascertain
the nature of the technical disclosure. It is submitted with the understanding that
5 it will not be used to interpret or limit the claims. In addition, in the foregoing
Detailed Description, it may be seen that various features are grouped together in
a single embodiment for the purpose of streamlining the disclosure. This
method of disclosure is not to be interpreted as limiting the claims. Thus, the
following claims are hereby incorporated into the Detailed Description, with
10 each claim standing on its own as a separate embodiment.

CLAIMS

What is claimed is:

- 5 1. A method comprising:
performing a first operation on a first resistance variable element coupled
to a first access device, wherein performing the first operation comprises
providing the first access device with a first control gate voltage, the first
resistance variable element and the first access device being coupled between a
10 first data line at a first data line voltage and a common source at a common
source voltage; and
performing a second operation on a second resistance variable element
coupled to a second access device, wherein performing the second operation
comprises providing the second access device with a second control gate voltage
15 that is different than the first control gate voltage, the second resistance variable
element and the second access device being coupled between a second data line
at a second data line voltage that is different than the first data line voltage and
the common source at the common source voltage.
- 20 2. The method of claim 1, wherein the second control gate voltage is lower
than the first control gate voltage.
3. The method of claim 1, wherein the second control gate voltage is higher
than the first control gate voltage.
- 25 4. The method of claim 1, wherein:
providing the first access device with the first control gate voltage
comprises providing a first field-effect transistor with the first control gate
voltage; and
30 providing the second access device with the second control gate voltage
comprises providing a second field-effect transistor with the second control gate
voltage.

5. The method of claim 1, further comprising providing a common source voltage of approximately 1.5 volts to the common source.
6. The method of claim 1, wherein:
- 5 performing the first operation on the first resistance variable element comprises programming the first resistance variable element; and performing the second operation on the second resistance variable element comprises erasing the second resistance variable element.
- 10 7. The method of claim 1, wherein the second control gate voltage is substantially equal to the first control gate voltage plus the common source voltage.
8. The method of claim 1, wherein the first data line voltage is less than the
- 15 common source voltage.
9. The method of claim 8, further comprising providing the common source voltage to the first data line and the second data line after performing the first operation and before performing the second operation.
- 20 10. The method of claim 1, wherein the second data line voltage is higher than the common source voltage.
11. A method comprising:
- 25 providing a common source voltage to a common source;
providing a plurality of data lines with a standby data line voltage;
providing a plurality of access devices with a control gate voltage;
providing a first data line voltage to a first one of the data lines to program a first resistance variable element coupled to a first one of the access
- 30 devices, the first one of the access devices and the first resistance variable element being coupled between the first one of the data lines and the common source;

providing a second data line voltage to a second one of the data lines to erase a second resistance variable element coupled to a second one of the access devices, the second one of the access devices and the second resistance variable element being coupled between the second one of the data lines and the common source, the second data line voltage being different from the first data line voltage.

12. The method of claim 11, wherein the second data line voltage is higher than the first data line voltage.

10

13. The method of claim 11, wherein the standby data line voltage equal to the common source voltage.

14. A method comprising:
15 providing a common source voltage to a common source of an array of memory cells;
providing a plurality of data lines of the array with a standby data line voltage;
providing a first data line voltage to a first one of the data lines;
20 providing a first access device with a first control gate voltage to program a first resistance variable element coupled to the first access device between the common source and the first one of the data lines;
providing the standby data line voltage to the first data line;
providing a second data line voltage to the second one of the data lines;
25 and
providing a second access device with a second control gate voltage to erase a second resistance variable element coupled to the second access device between the common source and the second data line, wherein the second control gate voltage is different than the first control gate voltage.

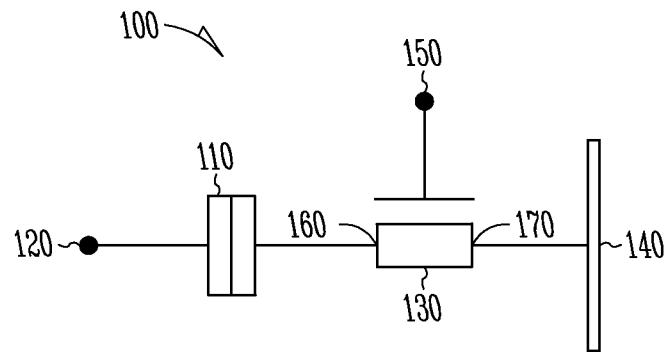
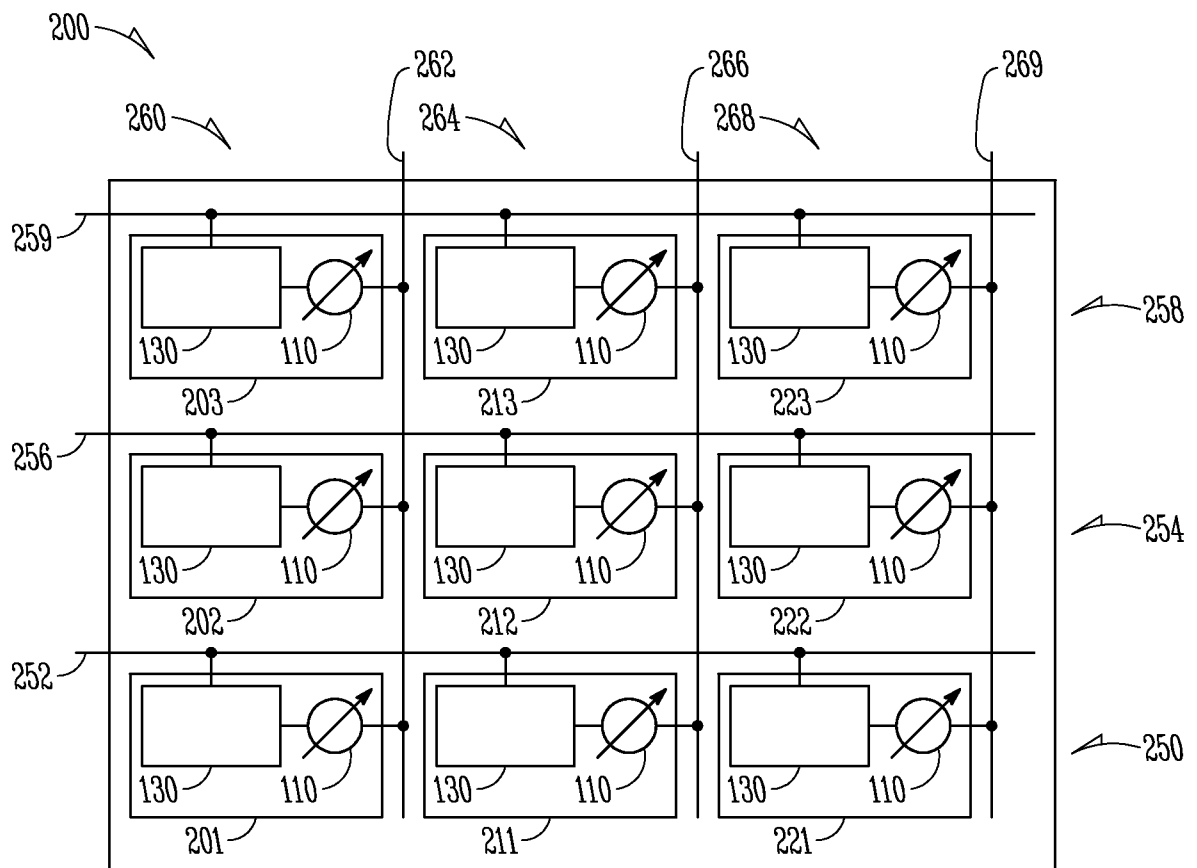
30

15. The method of claim 14, wherein:
providing the first access device with the first control gate voltage
comprises raising a gate terminal of the first access device from a reference
voltage to the first control gate voltage; and
5 providing the second access device with the second control gate voltage
comprises raising a gate terminal of the second access device from the reference
voltage to the second control gate voltage.
16. The method of claim 14, wherein:
10 providing the first access device with the first control gate voltage
comprises raising a gate terminal of the first access device from a reference
voltage to the first control gate voltage; and
providing the second access device with the second control gate voltage
comprises raising a gate terminal of the second access device from the first
15 control gate voltage to the second control gate voltage.
17. The method of claim 14, wherein:
providing the first access device with the first control gate voltage
comprises lowering a gate terminal of the first access device from a reference
20 voltage to the first control gate voltage; and
providing the second access device with the second control gate voltage
comprises lowering a gate terminal of the second access device from the
reference voltage to the second control gate voltage.
- 25 18. The method of claim 14, wherein:
providing the first access device with the first control gate voltage
comprises lowering a gate terminal of the first access device from a reference
voltage to the first control gate voltage; and
providing the second access device with the second control gate voltage
30 comprises raising a gate terminal of the second access device from the first
control gate voltage to the second control gate voltage.

19. The method of claim 14, wherein:
the second data line voltage is different than the first data line voltage;
and
providing the plurality of data lines of the array with the standby data line
5 voltage comprises providing the plurality of data lines with the common source
voltage.
20. An apparatus comprising:
a plurality of data lines;
10 a common source;
a plurality of resistance variable memory cells, each resistance variable
memory cell being coupled between one of the data lines and the common
source, wherein each resistance variable memory cell comprises a resistance
variable element coupled to an access device; and
15 a memory control unit configured to control:
provision of a standby data line voltage to the data lines;
performance of a first operation on first one of the resistance
variable elements, wherein performance of the first operation comprises
providing a first one of the access devices with a first control gate
20 voltage, wherein a first one of the data lines is at a first data line voltage
and the common source is at a common source voltage; and
performance of a second operation on a second one of the
resistance variable elements, wherein performance of the second
operation comprises providing a second one of the access devices with a
25 second control gate voltage that is different than the first control gate
voltage and providing a second data line voltage to a second one of the
data lines that is different than the first data line voltage, wherein the
common source is at the common source voltage.
- 30 21. The apparatus of claim 20, wherein the apparatus comprises a system.
22. The apparatus of claim 20, wherein the apparatus comprises a resistive
random access memory device.

23. The apparatus of claim 20, wherein:
performance of the first operation comprises programming the first one
of the resistance variable elements; and
5 performance of the second operation comprises erasing the second one of
the resistance variable elements.
24. The apparatus of claim 20, wherein provision of a standby data line
voltage to the data lines comprises provision of the common source voltage to
10 the data lines.
25. The apparatus of claim 20, wherein the second control gate voltage is
lower than the first control gate voltage.

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*Fig. 1**Fig. 2*

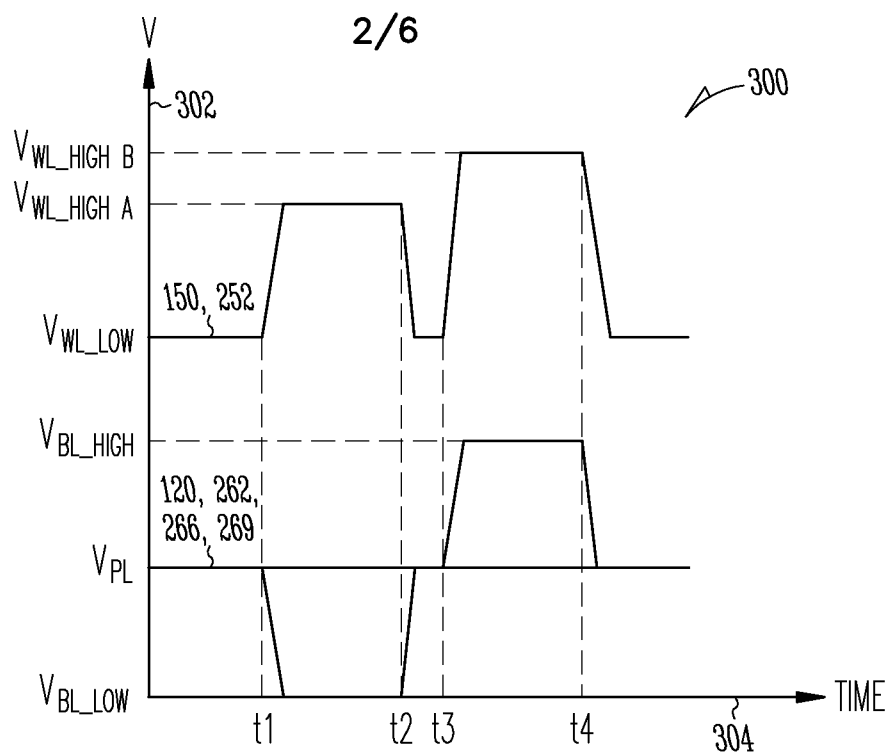


Fig. 3

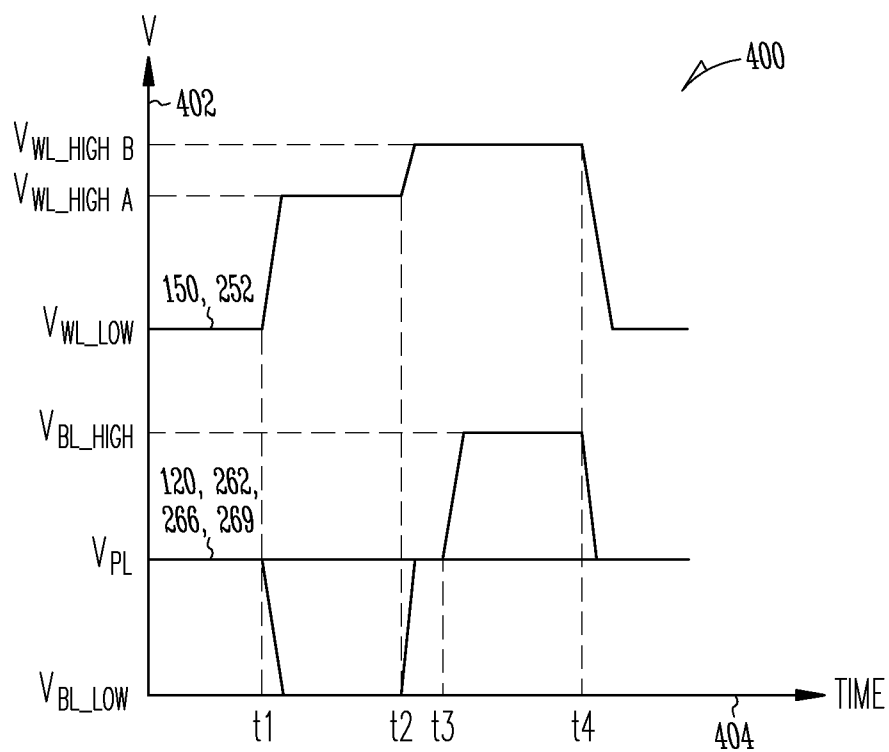


Fig. 4

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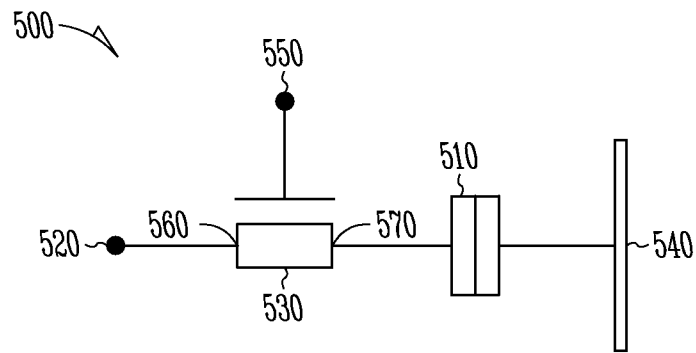


Fig. 5

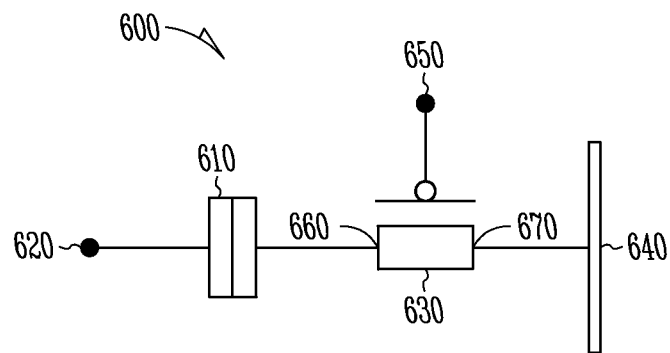


Fig. 6

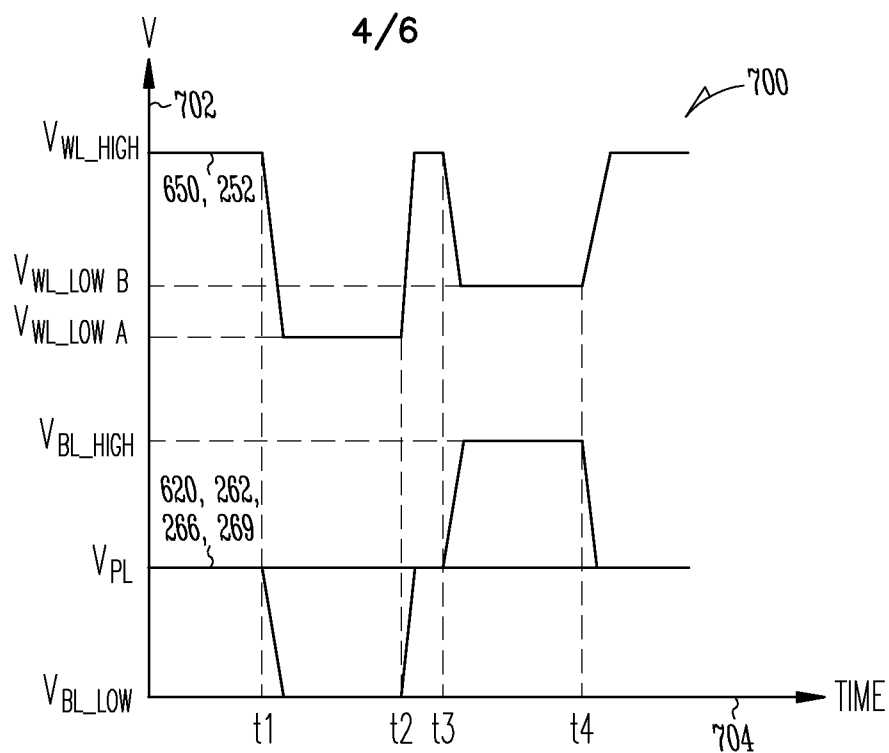


Fig. 7

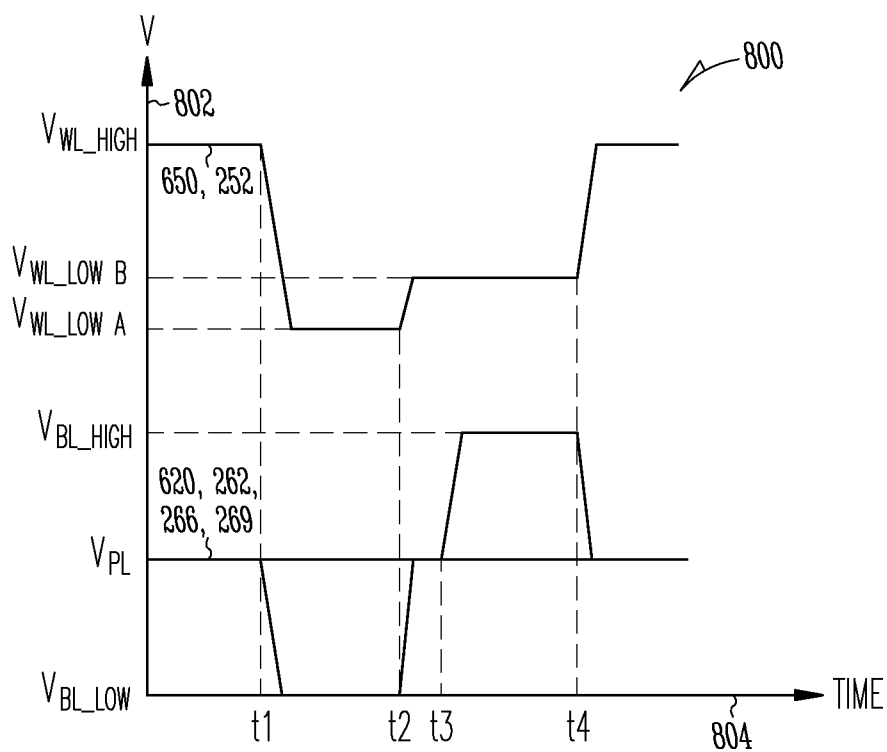
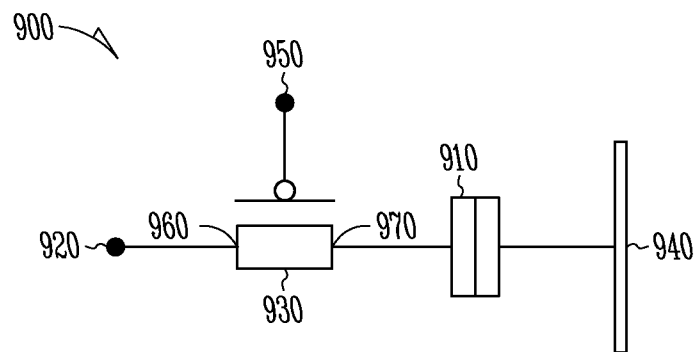
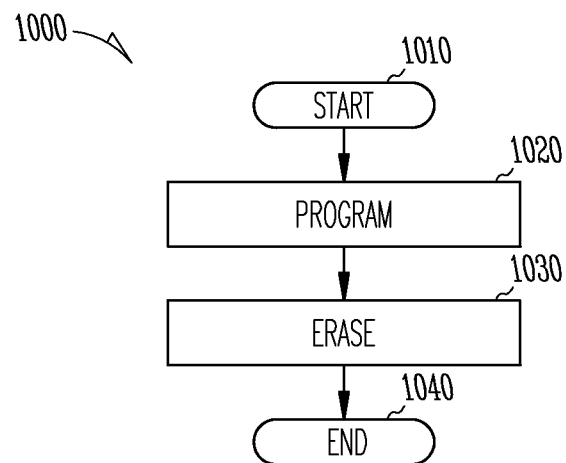


Fig. 8

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*Fig. 9**Fig. 10*

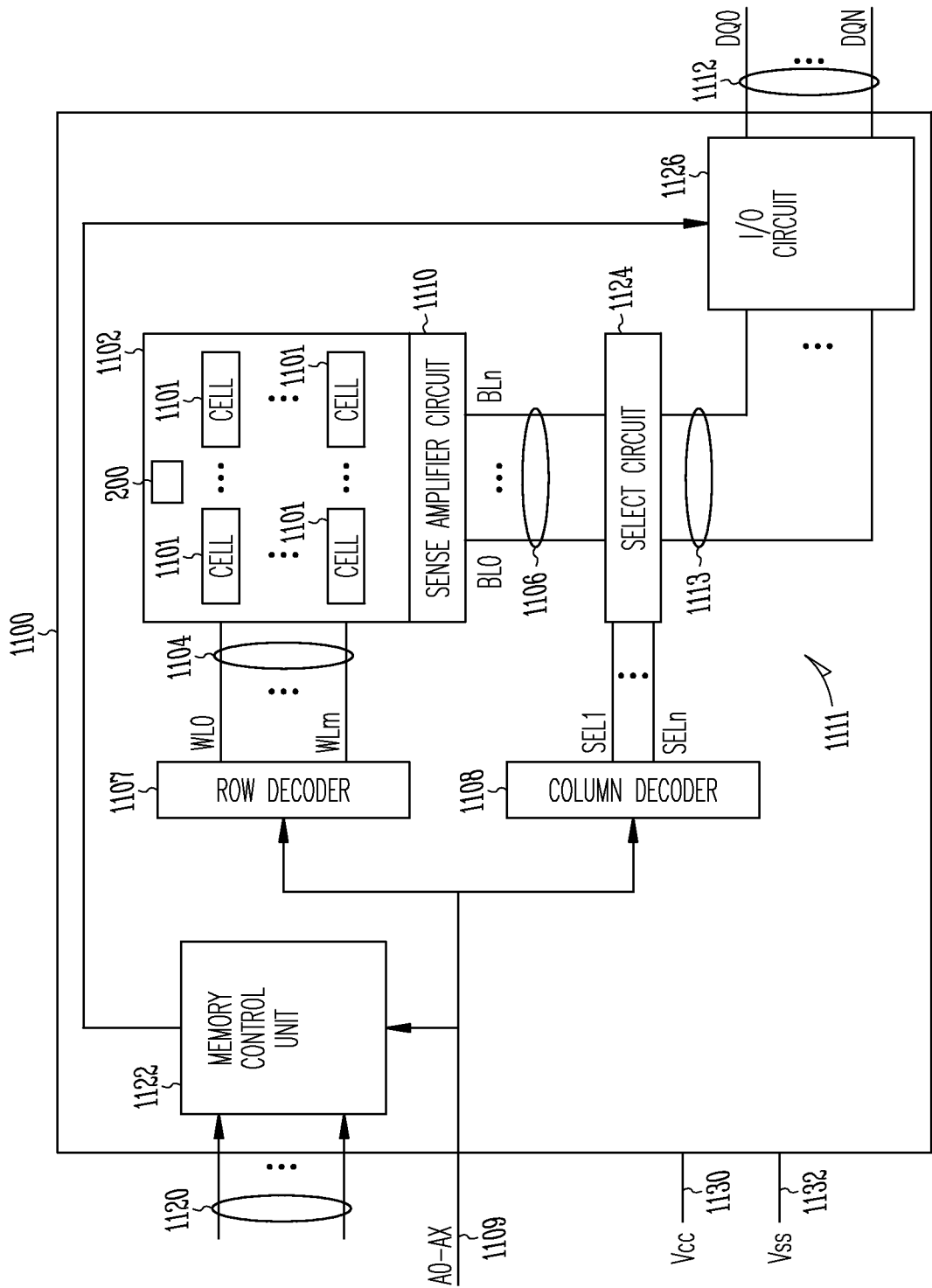


Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/047176**A. CLASSIFICATION OF SUBJECT MATTER****G11C 13/00(2006.01)i, G11C 16/06(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 13/00; H01L 45/00; G11C 11/00; H01L 21/8239; G11C 16/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: resistive, variable, element, memory, access, control, gate, data, line, common, source

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008-0106924 A1 (WOO-YEONG CHO et al.) 08 May 2008 See paragraphs [0005], [0013], [0017], [0032], [0038], [0040]-[0041]; and figures 1A, 3B-5B.	11-13, 20-23, 25
Y		1-4, 6, 8, 10
A		5, 7, 9, 14-19, 24
Y	US 2011-0149639 A1 (ANDREW JOHN CARTER et al.) 23 June 2011 See claims 11, 13-15; and figure 3.	1-4, 6, 8, 10
A	US 2013-0121056 A1 (ZENGTAO T. LIU et al.) 16 May 2013 See paragraphs [0019]-[0020]; and figure 1A.	1-25
A	US 2010-0080037 A1 (KOHJI INOUE et al.) 01 April 2010 See paragraph [0108]; and figure 2.	1-25
A	US 2012-0294064 A1 (MAKOTO KITAGAWA et al.) 22 November 2012 See paragraphs [0081]-[0084]; and figure 5.	1-25

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

24 October 2014 (24.10.2014)

Date of mailing of the international search report

27 October 2014 (27.10.2014)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/047176

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