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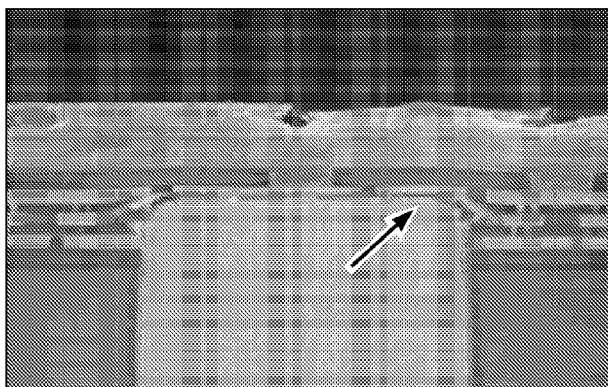


FIG. 1C

(57) Abstract: The present disclosure relates to a chip including a wafer, a back-end-of-line (BEOL) layer deposited on the wafer, a chip TSV in the wafer containing a conductive material, and a chip cap layer disposed between the chip TSV and the BEOL layer, and configured to reduce via extrusion of conductive material in the chip TSV during operation of the chip. The present disclosure further includes a 3D integrated circuit including a plurality of electrically connected chips, at least one of which is a chip as described above. The disclosure further relates to a 3D integrated circuit with an interposer, a TSV in the interposer containing a conductive material, and an interposer cap layer configured to reduce via extrusion of the conductive material located in the interposer TSV during operation of the circuit. The present disclosure further includes methods of forming such chips and 3D integrated circuits.



CAPPED THROUGH-SILICON-VIAS FOR 3D INTEGRATED CIRCUITSTECHNICAL FIELD

5 The present disclosure relates to three dimensional (3D) integrated circuits in which the through-silicon-vias (TSVs) are capped to reduce via extrusion.

BACKGROUND

3D integrated circuits contain stacked chips that are electrically connected to one another by chip TSVs that extend vertically through the silicon wafers of the chips. Common chip TSV configurations are shown in FIGURES 1A and 1B (PRIOR ART). In order to establish an electrical connection between chips, the chip TSV contains an electrically conducting material, such as a metal, particularly copper (Cu). This material sometimes extrudes from the via during manufacturing or operation of the 3D integrated circuit, causing damage to structures near the chip TSV as shown in FIGURE 1C (PRIOR ART) or cracking of an oxide film that forms on top of the chip TSV as shown in FIGURE 1D (PRIOR ART). Both of these effects are detrimental to the 3D integrated circuit and may cause the entire circuit to fail.

Prior to the present invention, causes of via extrusion were poorly understood and effective ways of reducing via extrusion have not been demonstrated.

20 SUMMARY

The present disclosure relates to a chip including a wafer, a back-end-of-line (BEOL) layer deposited on the wafer, a chip through-silicon-via (TSV) in the wafer, the chip TSV containing a conductive material, and a chip cap layer disposed over the chip TSV and between the chip TSV and the BEOL layer, wherein the chip cap layer is configured to reduce via extrusion of conductive material located in the chip TSV during fabrication or operation of the chip, or both.

The present disclosure further includes a 3D integrated circuit including a plurality of electrically connected chips, at least one of which is a chip as described above.

30 The present disclosure further includes methods of forming such chips and 3D integrated circuits.

The present disclosure further includes 3D integrated circuits with an interposer TSV and an interposer cap layer as well as 3D integrated circuits containing such an interposer and methods of forming such 3D integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present disclosure may be better understood by reference to the attached figures, in which like numerals indicate like components.

FIGURE 1A presents a PRIOR ART chip TSV in a silicon wafer in which a first BEOL metal layer is directly in contact with the top of the chip TSV;

FIGURE 1B presents a PRIOR ART chip TSV in which a silicon wafer in which a first BEOL metal layer is connected to the top of the chip TSV by intermediate vias;

FIGURE 1C is micrograph of a PRIOR ART chip TSV that has experienced via extrusion, resulting in damage of the first BEOL metal layer and other structures near the chip TSV;

FIGURE 1D is a micrograph of a PRIOR ART chip TSV that has experienced via extrusion, resulting in cracking of the oxide film formed on top of the chip TSV;

FIGURE 2A illustrates a 3D integrated circuit according to the present disclosure;

FIGURE 2B illustrates a 3D integrated circuit with an interposer (also called a 2.5 dimensional (2.5D) integrated circuit) according to the present disclosure;

FIGURE 3A illustrates a capped chip TSV according to the present disclosure;

FIGURE 3B illustrates another capped chip TSV according to the present disclosure;

FIGURES 4A-4H illustrate the steps of a method of forming a capped chip TSV according to FIGURE 3A; and

FIGURES 5A-5H illustrate the steps of a method of forming a capped chip TSV according to FIGURE 3B.

DETAILED DESCRIPTION

The present disclosure relates to 3D integrated circuits in which chip TSVs are capped to reduce via extrusion. In particular, the chip TSVs may be capped with a chip cap layer that may be deposited in a manner similar to other layers in the circuit. In addition, the disclosure relates to 3D integrated circuits containing interposer TSVs that are capped with an interposer cap layer that may be deposited in a manner similar to other layers in the circuit. Although the materials and methods herein are primarily described with respect to a chip cap layer, they may be used in connection with an interposer cap layer as well. Interposer cap layers also reduce interposer via extrusion.

FIGURE 2A illustrates a 3D integrated circuit 10 containing five chips 20. Each chip 20 contains a wafer 30 and a BEOL layer 40 (not expressly shown). Chip TSVs 50 vertically disposed in the silicon wafers 30 connect different chips 20 to create the 3D integrated circuit 10.

FIGURE 2B illustrates a 3D integrated circuit 200 containing five chips 20, three stacked chips 20a and two unstacked chips, 20b. Each chip 20a or 20b contains a silicon wafer 30a or 30b. The stacked chips 20a also contain a BEOL layer 40 (not expressly shown). As in FIGURE 2A, chip TSVs 50 vertically disposed in silicon wafers 30a connect different chips 20a to create a 3D integrated circuit among chips 20a. In addition, stacked chips 20a and unstacked chips 20b are disposed in interposer 210 to create a 3D integrated circuit with an interposer (also referred to as a 2.5D circuit) on which chips 20a and 20b are located. The 3D circuit further includes a substrate, 230.

As illustrated in FIGURE 2B, 3D integrated circuit with interposer 200 includes both stacked chips 20a and unstacked chips 20b. 3D integrated circuits with only stacked chips or only unstacked chips are also included in this disclosure. Furthermore, although chips 20a and 20b are shown on both sides of interposer 210 in FIGURE 2B, 3D integrated circuits with chips on only one side are also included in this disclosure.

Interposer 210 contains a plurality of interposer TSVs 220, which may be covered with an interposer cap layer 240. Interposer 210 may be formed from any suitable material, such as any material conventionally used to form an interposer. Suitable materials include silicon and other electrically insulating materials.

The disclosure further includes other 3D integrated circuits containing chip TSVs, interposer TSVs, or both. The capped TSVs illustrated in FIGURES 3A and 3B, as well as the methods described in FIGURES 4A-4H and FIGURES 5A-5H may be used with any 3D integrated circuit, including those of FIGURES 2A and 2B.

FIGURES 3A and 3B illustrate capped chip TSVs 50 in chips 20. In these chips 20, the chip TSVs 50 are each covered with a cap layer 60. Although it is possible to cap only selected chip TSVs 50, generally it is desirable to cap all of them on a chip 20. BEOL layer 40 includes sublayers 40a-e.

In FIGURE 3A, capped chip TSV 50 is directly in contact with the first BEOL layer 40a. This is often referred to as a one-level wiring structure.

In FIGURE 3B, capped chip TSV 50 is electrically connected to first BEOL layer 40a by intermediate vias 80 found in intermediate layer 40b. This is often referred to as a two-level wiring structure. This design is often used in chips 20 at the 20 nm technology node or smaller because of its increased compatibility with smaller-scale BEOL interconnects.

Although it is possible to form hybrid chips in which some chip TSVs 50 are in direct contact with first BEOL layer 40a and other chip TSVs 50 on the same chip are electrically connected by intermediate vias 80 in intermediate layer 40b, typically a chip or a substantial

region of a chip will use one design or the other for all chip TSVs due to manufacturing efficiencies.

Wafers 30 may be any semiconducting material, suitable for forming a 3D integrated circuit, including silicon, such as n-doped and p-doped silicon. Although the present disclosure focuses on silicon as the most common integrated circuit material, the principles may be applied to integrated circuits formed from other semiconductor wafers, such as gallium arsenide wafers or other compound III-V or II-VI material wafers as well.

Chip TSV 50 may be wholly or partially filled with an electrically conductive material sufficient to establish an electrical connection between two chips 20. Often the electrically conductive material is metallic Cu or a Cu alloy, but other materials may be used. The principles applied herein and discussed in connection with Cu may be applied to such other materials.

Cap layer 60 may be formed by any metal or metal alloy able to reduce or prevent via extrusion from the associated chip TSV 50. In order to do this, when exposed to an elevated temperature, such as during fabrication or operation of the chip or the 3D integrated circuit, the cap layer 60 may reduce or prevent material extrusion due to diffusion (also called mass transport) at a surface/interface or a grain boundary resulting from stresses generated by differences in the coefficient of thermal expansion (CTE) (*i.e.* how much the material changes in size in response to a change in temperature) of the material in chip TSV 50 as compared to silicon or other semiconducting material in wafers 30. Stresses generated by CTE differences cause interfacial or grain-boundary diffusion because both interfacial and grain-boundary diffusion are types of thermally-activated mass transport. Grain-boundary diffusion occurs along the boundaries of separate grains in a crystal and is characterized by atomic transport along these boundaries. This atomic transport occurs more readily under a stress which is generated when the grains change size in response to a temperature change. Interfacial diffusion occurs at the interface between two different materials, often to relieve stresses such as those caused by one material changing more in size due to a change in temperature than the other material. In addition, grain-boundary diffusion and interfacial diffusion may be affected by the reaction of cap layer 60 with the material in chip TSV 50.

In addition to reducing or preventing via extrusion, the material used to form cap layer 60 may also be compatible with manufacturing processes used to form chip 20 or a 3D integrated circuit, such as 3D integrated circuit 10 or 200.

When wafer 30 is formed from silicon and chip TSV 50 is filled with Cu or a Cu alloy, metallic elements which can react or alloy with Cu, such as cobalt (Co), titanium (Ti), nickel (Ni), aluminum (Al), alloys thereof, and combinations of any of the foregoing may be used to form cap layer 60.

Cap layer 60 may react with the underlying material in chip TSV 50 to form an alloying layer at the interface. Cap layer 60 may also partially dissolve at the surface/interface and/or into grain boundaries in the underlying material in chip TSV 50. These effects reduce grain boundary diffusion or surface/interfacial diffusion.

5 Cap layer 60 may have any dimensions suitable for use in chip 20 so long as cap layer 60 remains capable of reducing or preventing via extrusion. For example, cap layer 60 may be between 5 and 100 nm thick, between 10 and 75 nm thick, between 15 and 50 nm thick, at least 5 nm thick, at least 10 nm thick, or at least 15 nm thick. Cap layer 60 typically covers the entire top of chip TSV 50. It may extend beyond chip TSV 50 by at least 5 nm, or at least 10 nm at the
10 smallest extent. Suitable thickness and extensions for cap layer 60 may be affected by the material used to form wafer 30, the material contained in chip TSV 50, the material contained in interposer TSV, the material used to form layer 40a or other BEOL layers, and the material from which cap layer 60 is formed.

 Cap layer 60 may reduce via extrusion under conditions at which via extrusion by a
15 certain amount as compared to normally occurs during thermal cycling between room temperature and around 400 °C, for example, by at least 50%, by at least 75%, or by at least 80% when via extrusion is measured as the distance above the normal top of chip TSV 50 to which the material contained in chip TSV 50 has extruded.

 Inclusion of cap layer 60 may increase the yield of chip TSVs 50. Inclusion of cap layer
20 60 may increase the reliability of chip TSVs. Inclusion of an interposer cap layer may also increase the yield or reliability, or both, of interposer TSVs 220. The amount of improvement in yield and reliability may depend on the design of the chip, the BEOL layer materials, the interposer, and the manufacturing process.

 FIGURES 4A-4H and FIGURES 5A-5H illustrate methods 100 of forming capped chip
25 TSVs 50 according to FIGURES 3A and 3B, respectively. In FIGURES 4A and 5A, in a first step 110, wafer 30 after any front-end-of-line (FEOL) process is provided. Next, in FIGURES 4B and 5B, in step 120, chip TSV holes are formed by etching. In FIGURES 4C and 5C, in step 130, a liner and seed layer is deposited in the chip TSV holes. In FIGURES 4D and 5D, in step 140, the chip TSV holes are filled with electrically conductive material, such as Cu or a Cu alloy,
30 to form chip TSVs 50. Filling may include electroplating. Post-plating annealing occurs in FIGURES 4E and 5E in step 150, followed by chemical-mechanical planarization (CMP) in FIGURES 4F and 5F in step 160. A cap layer is deposited in FIGURES 4G and 5G in step 170. Cap layer may be deposited using fabrication techniques otherwise applicable to chip manufacture, such as plasma enhanced sputtering or electroplating, so long as the techniques are
35 otherwise compatible with the methods of forming chip 20 or 3D integrated circuit 10. Cap layer

60 is patterned to cover the tops of chip TSVs 50 for example using the an additive patterning or damascene process or any other compatible process prior to FIGURES 4G and 5H, step 180, in which the BEOL layer 40 is deposited. In FIGURE 5H, step 180 further includes depositing the intermediate layer 80 prior to depositing BEOL layer 40. In step 180, BEOL layer 40 may also be patterned.

Further completion processes may then be performed. Such processes may include wafer thinning to reveal the chip TSV backside and/or forming a die-stack structure.

A similar method may be used to place a cap layer on interposer TSVs, such as interposer cap layer 240 located as illustrated in FIGURE 2B. Interposer cap layer 240 may be formed by depositing a cap layer material on the interposer using fabrication techniques otherwise applicable to chip manufacture, such as plasma enhanced sputtering or electroplating, so long as the techniques are otherwise compatible with the methods of forming 3D integrated circuit 200. Interposer cap layer 140 is then patterned to cover the tops of interposer TSVs 220 for example using an additive patterning or damascene process or any other compatible process.

EXAMPLES

The following example is provided to further illustrate certain aspects of the present invention. Although it may be used in combination with any embodiments disclosed herein, it is not intended to limit those embodiments to the specific information and data of this example.

Cu-filled chip TSVs were formed in a silicon wafer and capped with different cap materials as indicated in Table 1. Average via extrusion for a group of chip TSVs was measured under conditions in which via extrusion typically occurs during thermal cycling between room temperature and around 400 °C and is also reported in Table 1.

Table 1: Average Via Extrusion for Chip TSVs with Various Cap Layer Compositions

Cap material (thickness)	Average via extrusion
No cap	163.6 nm
Co (16 nm)	54.2 nm
Ti (50 nm)	64.5 nm
Ni (50 nm)	46.9 nm
Al (50 nm)	83.6 nm

Although only exemplary embodiments of the invention are specifically described above, it will be appreciated that modifications and variations of these examples are possible without departing from the spirit and intended scope of the invention. For instance, the principles of the

present disclosure may be adapted for use in other fabrication processes, such as via-last processes, via-middle processes, direct chip attachment, or for other integrated packages, such as a fan-out wafer level package. In addition, numerical values referenced herein include the referenced number and may also include “about” the referenced number, unless it is clear from context that only the referenced number was intended.

5

CLAIMS

1. A chip comprising:

a wafer;

a back-end-of-line (BEOL) layer deposited on the wafer;

5 a chip through-silicon-via (TSV) in the wafer, the chip TSV containing a conductive material; and

a chip cap layer disposed over the chip TSV and between the chip TSV and the BEOL layer, wherein the chip cap layer is configured to reduce via extrusion of conductive material located in the chip TSV during fabrication or operation of the chip, or both.

10 2. The chip of Claim 1, wherein the wafer is formed from silicon.

3. The chip of Claim 1, wherein the BEOL layer is formed from metal.

15 4. The chip of Claim 1, wherein the BEOL layer comprises a plurality of sublayers.

5. The chip of Claim 1, wherein the conductive material is a metal or metal alloy.

6. The chip of Claim 5, wherein the metal comprises copper (Cu) or a Cu alloy.

20 7. The chip of Claim 1, wherein the chip cap layer comprises a metal or metal alloy.

8. The chip of Claim 7, wherein the chip cap layer comprises metallic elements which react with copper (Cu), alloy with Cu, or both.

25 9. The chip of Claim 8, wherein the metallic element comprises cobalt (Co), titanium (Ti), nickel (Ni), aluminum (Al), alloys thereof, or combinations of any of the foregoing.

30 10. The chip of Claim 1, wherein the chip cap layer reduces via extrusion by an amount that improves chip yield and reliability.

11. The chip of Claim 10, wherein the chip cap layer reduces via extrusion by 50% when measured as distance extruded above the chip TSV during normal operation of the chip.

12. The chip of Claim 1, wherein the chip cap layer comprises a metallic element that reduces grain boundary diffusion, surface/interface diffusion, or both of a material located in the chip TSV.

5 13. A three dimensional (3D) integrated circuit comprising a plurality of electrically connected chips, at least one chip comprising

a wafer;

a back-end-of-line (BEOL) layer deposited on the wafer;

10 a chip through-silicon-via (TSV) in the wafer, the chip TSV containing a conductive material; and

a chip cap layer disposed over the chip TSV and between the chip TSV and the BEOL layer, wherein the chip cap layer is configured to reduce via extrusion of conductive material located in the chip TSV during operation of the chip.

15 14. The 3D integrated circuit of Claim 13, wherein the wafer is formed from silicon.

15. The 3D integrated circuit of Claim 13, wherein the BEOL layer is formed from metal.

20 16. The 3D integrated circuit of Claim 13, wherein the BEOL layer comprises a plurality of sublayers.

17. The 3D integrated circuit of Claim 13, wherein the conductive material located in the chip TSV is a metal or metal alloy.

25 18. The 3D integrated circuit of Claim 17, wherein the metal comprises copper (Cu) or a Cu alloy.

30 19. The 3D integrated circuit of Claim 13, wherein the chip cap layer comprises a metal or metal alloy.

20. The 3D integrated circuit of Claim 19, wherein the chip cap layer comprises metallic elements which react with copper (Cu), alloy with Cu, or both.

21. The chip of Claim 20, wherein the metallic element comprises cobalt (Co), titanium (Ti), nickel (Ni), aluminum (Al), alloys thereof, or combinations of any of the foregoing.

22. The 3D integrated circuit of Claim 13, wherein the chip cap layer reduces via extrusion by an amount that improves chip yield and reliability.

23. The 3D integrated circuit of Claim 22, wherein the chip cap layer reduces via extrusion by 50% when measured as distance extruded above the chip TSV during normal operation of the chip.

24. The 3D integrated circuit of Claim 13, wherein the chip cap layer includes metallic elements that reduce grain boundary diffusion, surface/interface diffusion, or both of a material located in the chip TSV.

25. The 3D integrated circuit of Claim 13, comprising at least two chips of the plurality of electrically connected chips are stacked.

26. The 3D integrated circuit of Claim 13, further comprising an interposer on which the plurality of electrically connected chips are located, wherein the interposer comprises a plurality of interposer TSVs and a interposer cap layer configured to reduce via extrusion of conductive material located in the interposer TSV during fabrication or operation of the circuit, or both.

27. The 3D integrated circuit of Claim 26, wherein the conductive material located in the interposer TSV is a metal or metal alloy.

28. The 3D integrated circuit of Claim 27, wherein the metal comprises copper (Cu) or a Cu alloy.

29. The 3D integrated circuit of Claim 26, wherein the interposer cap layer comprises a metal or metal alloy.

30. The 3D integrated circuit of Claim 29, wherein the interposer cap layer comprises metallic elements which react with copper (Cu), alloy with Cu, or both.

31. The chip of Claim 30, wherein the metallic element comprises cobalt (Co), titanium (Ti), nickel (Ni), aluminum (Al), alloys thereof, or combinations of any of the foregoing.

5

32. The 3D integrated circuit of Claim 26, wherein the interposer cap layer reduces via extrusion by an amount that improves interposer yield and reliability.

33. The 3D integrated circuit of Claim 32, wherein the interposer cap layer reduces
10 via extrusion by 50% when measured as distance extruded above the interposer TSV during normal operation of the interposer.

34. The 3D integrated circuit of Claim 26, wherein the interposer cap layer includes
15 metallic elements that reduce grain boundary diffusion, surface/interface diffusion, or both of a material located in the interposer TSV.

35. The 3D integrated circuit of Claim 13, wherein at least two chips of the plurality of electrically connected chips are stacked.

20 36. The 3D integrated circuit of Claim 13, wherein at least two chips of the plurality of electrically connected chips are not stacked.

37. The 3D integrated circuit of Claim 13, wherein at least two chips of the plurality of electrically connected chips are located on opposite sides of the interposer.

25

38. A method of forming a chip, the method comprising:
forming at least one chip through-silicon-via (TSV) hole in a wafer by etching;
filling the chip TSV hole with a conductive material to form a chip TSV;
depositing a chip cap layer over the chip TSV;
30 patterning the chip cap layer; and
depositing a back-end-of-line (BEOL) layer on the cap layer.

39. The method of claim 38, further comprising performing a completion process.

35

40. The method of claim 38, wherein the completion process comprises wafer thinning to reveal the chip TSV.

41. The method of claim 38, wherein the completion process comprises forming a
5 die-stack structure.

1/9

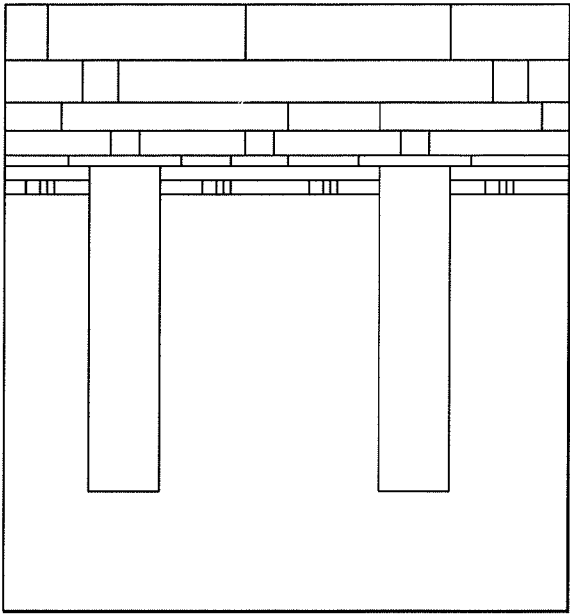


FIG. 1A
(PRIOR ART)

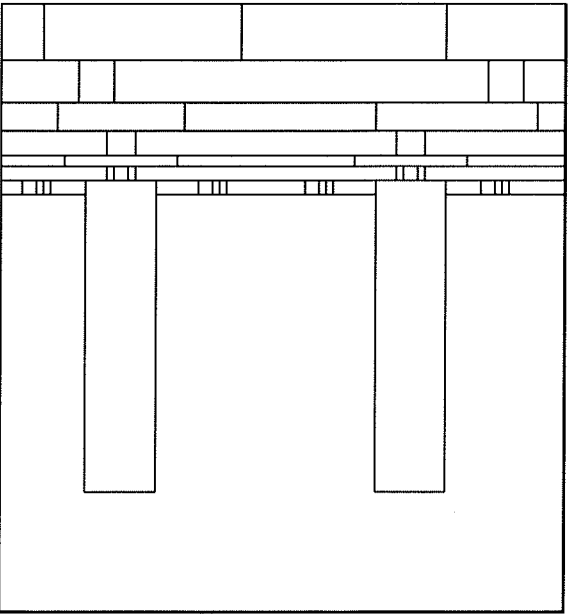


FIG. 1B
(PRIOR ART)

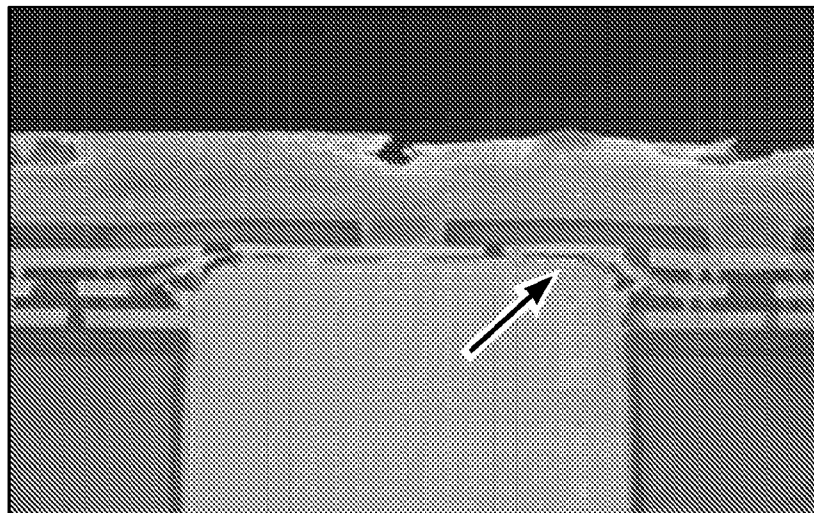


FIG. 1C

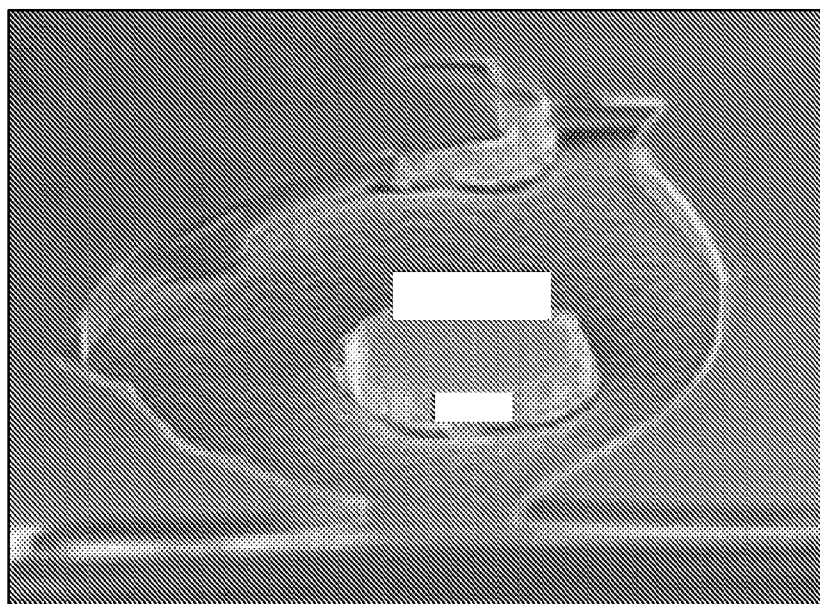


FIG. 1D

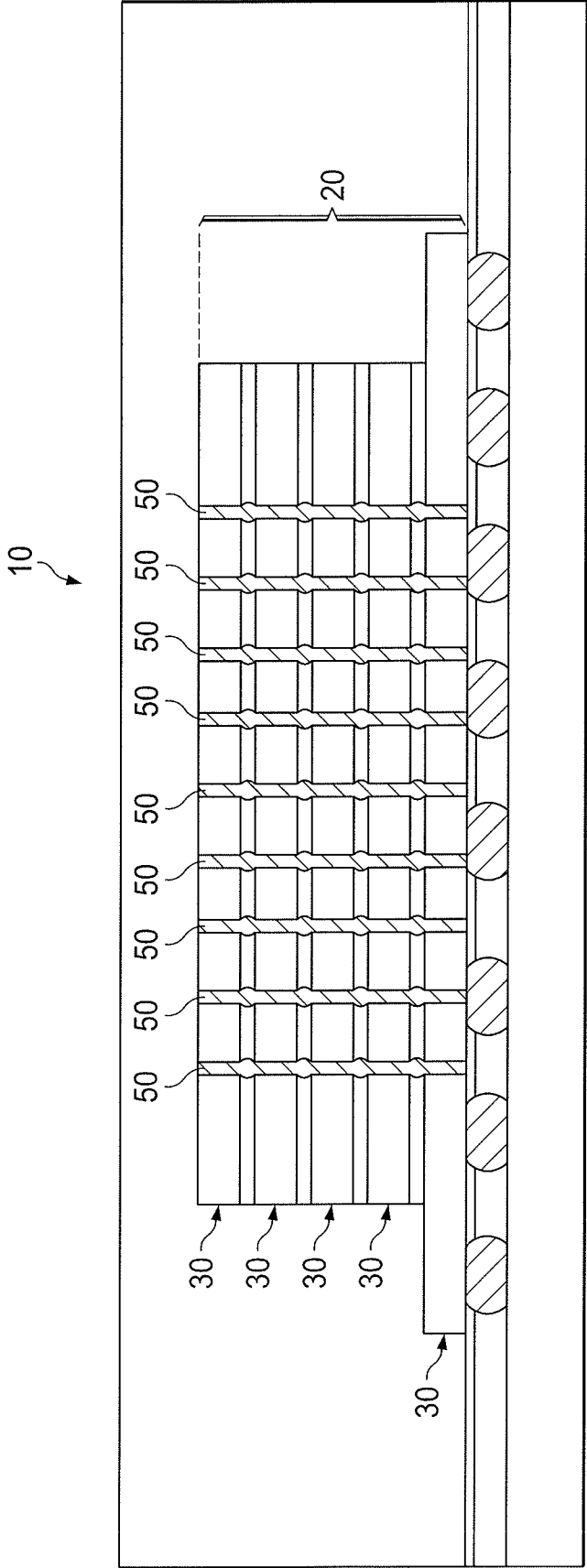


FIG. 2A

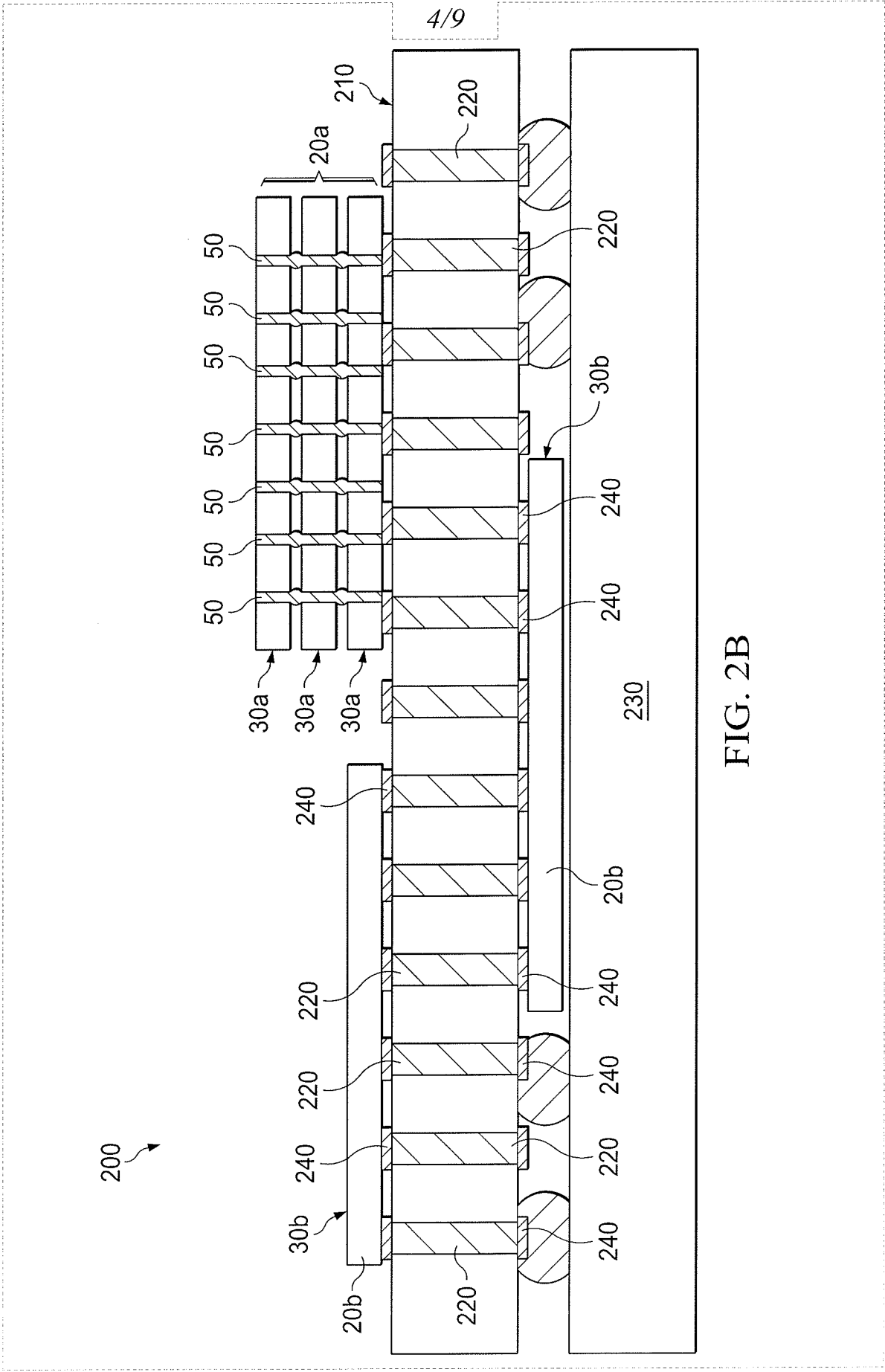


FIG. 2B

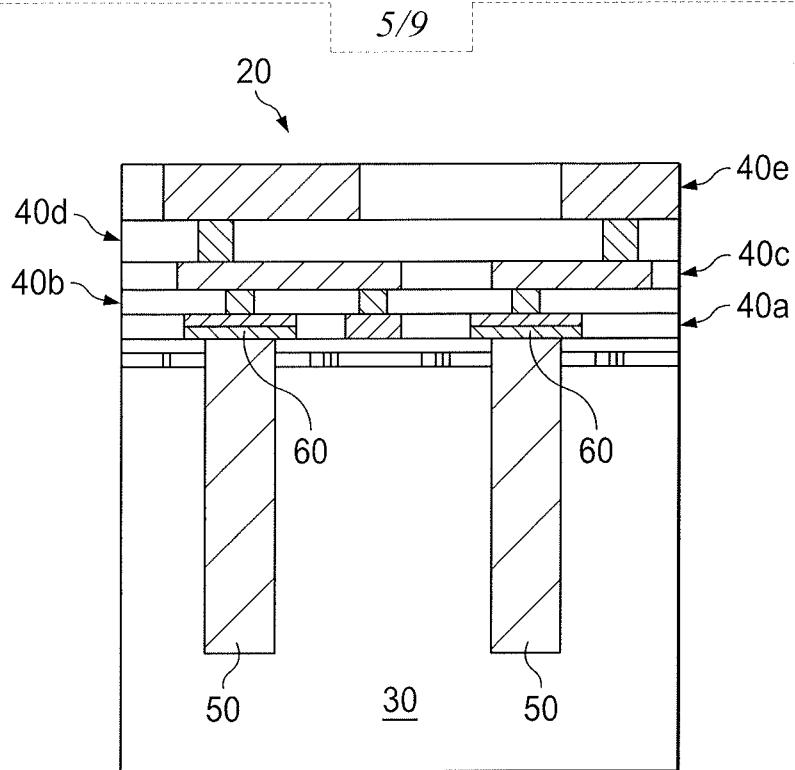


FIG. 3A

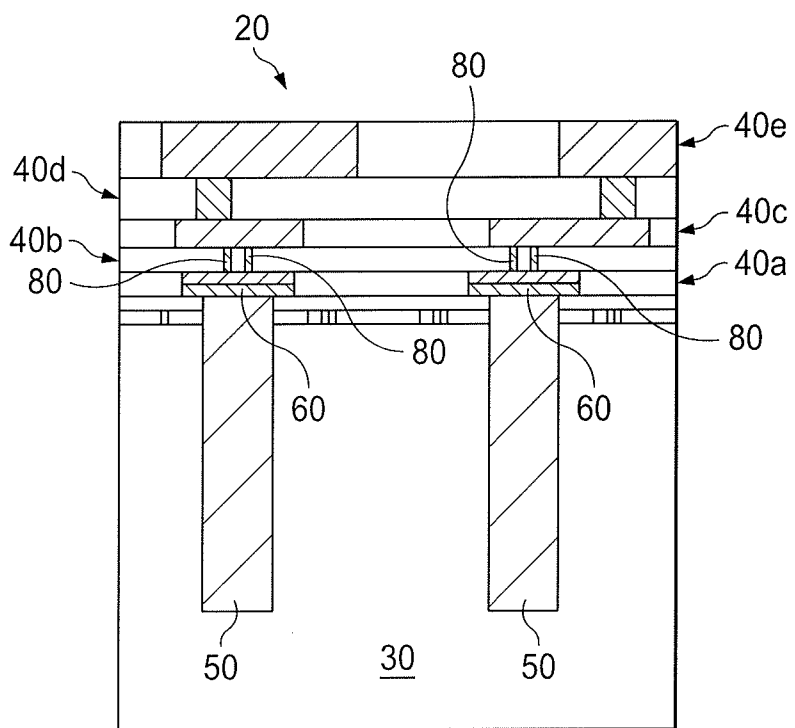


FIG. 3B

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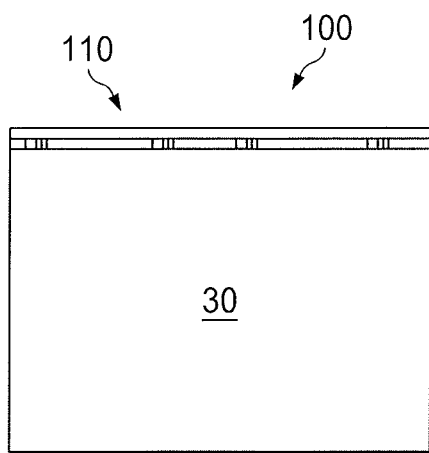


FIG. 4A

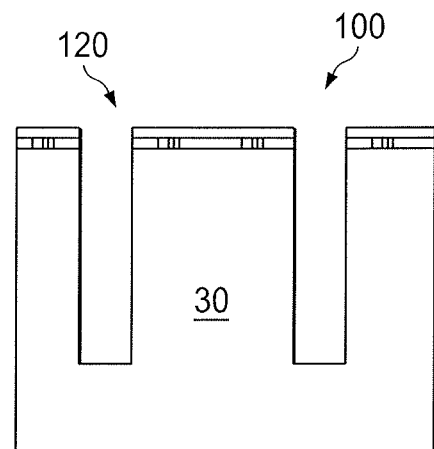


FIG. 4B

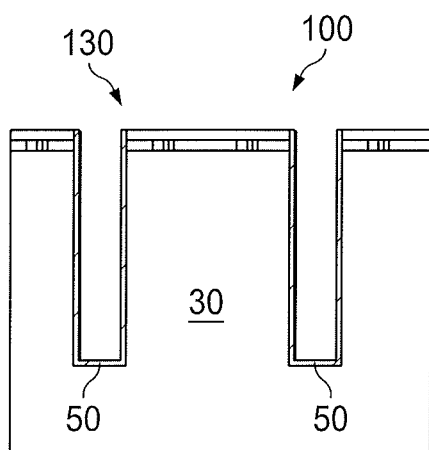


FIG. 4C

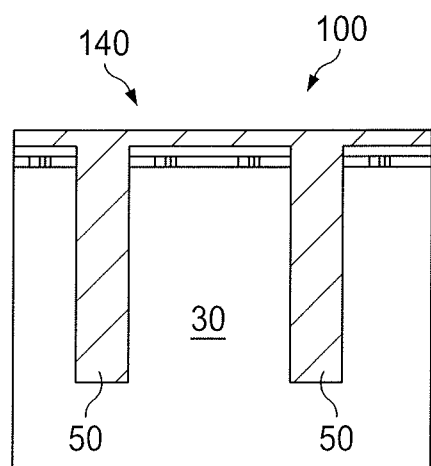


FIG. 4D

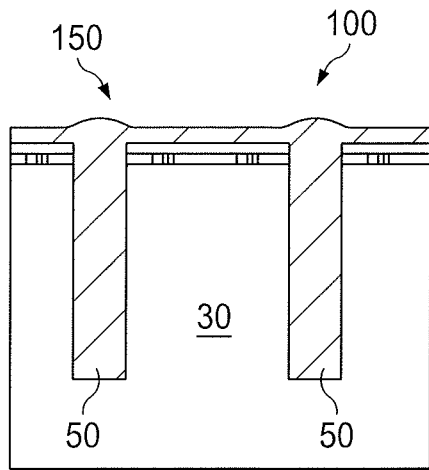


FIG. 4E

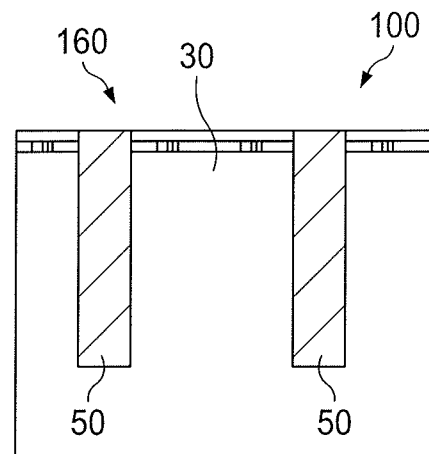


FIG. 4F

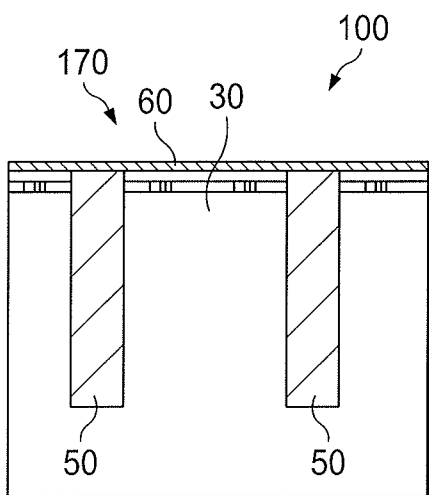


FIG. 4G

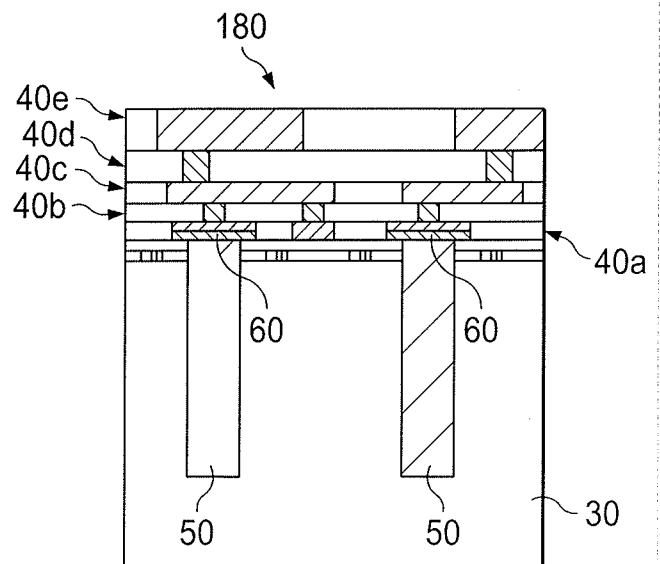


FIG. 4H

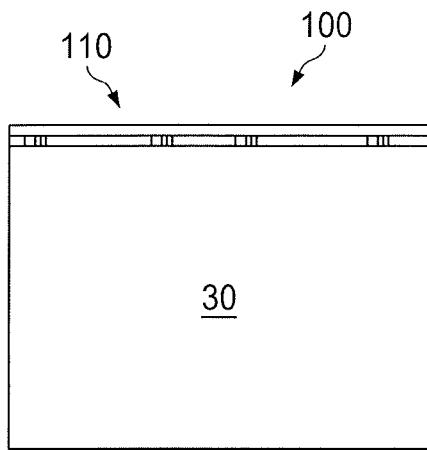


FIG. 5A

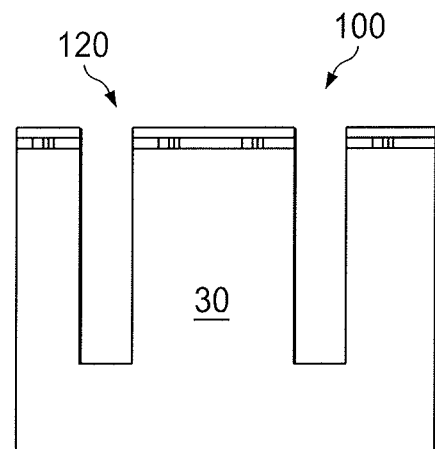


FIG. 5B

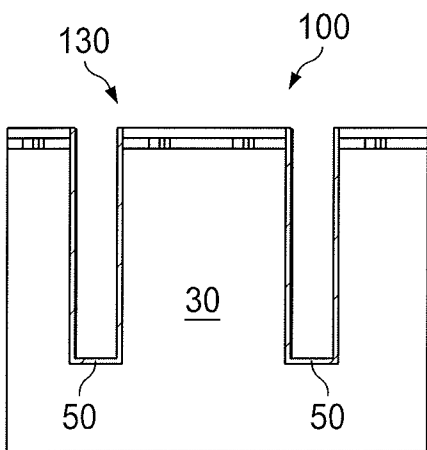


FIG. 5C

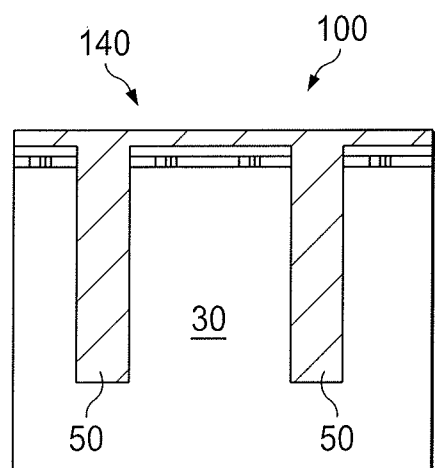


FIG. 5D

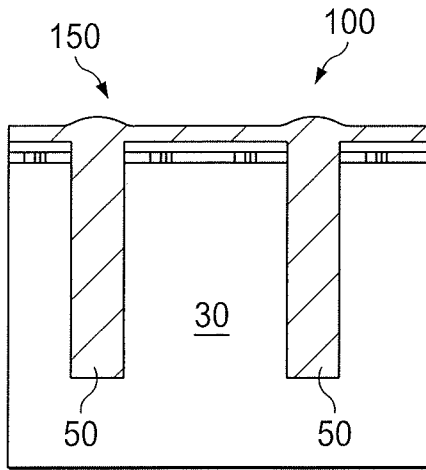


FIG. 5E

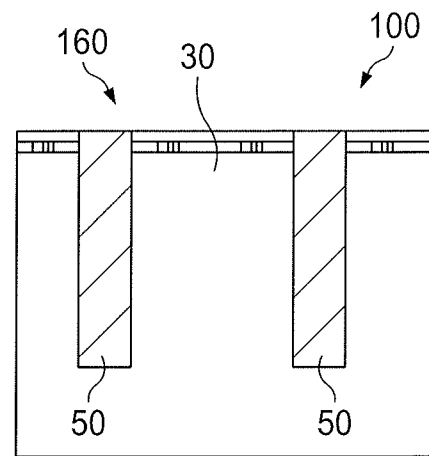


FIG. 5F

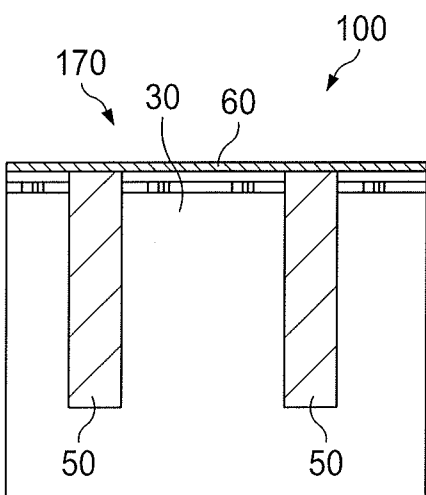


FIG. 5G

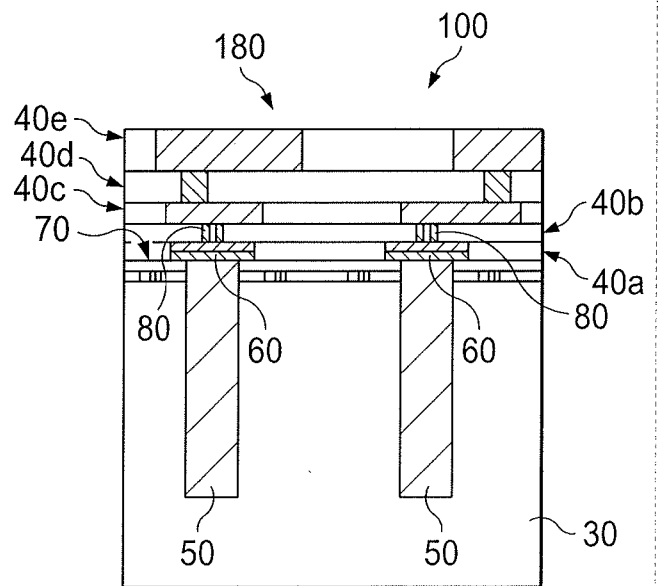


FIG. 5H

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US16/24186

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 21/768, 23/532, 25/065 (2016.01)

CPC - H01L 21/76898, 23/5328, 25/0657

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8): H01L 21/768, 21/683, 23/532, 23/538, 25/065 (2016.01)

CPC: H01L 21/76898, 21/6836, 23/53238, 23/5389, 25/0657

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSeer (US, EP, WO, JP, DE, GB, CN, FR, KR, ES, AU, IN, CA, INPADOC Data); Google; Google Scholar; EBSCO; KEYWORDS: chip wafer back-end-of-line BEOL deposited chip through-silicon-via TSV conductive material chip cap layer reduce via extrusion fabrication operation silicon copper Cu yield reliability

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y --- A	JIANG, T. et al. Through-silicon via stress characteristics and reliability impact on 3D integrated circuits. MRS Bulletin, Vol 40, No. 3, 10 March 2015, pp. 248-256 [online], retrieved on 2016-05-24 from the Internet <URL: https://armadillo.ae.utexas.edu/~ruihuang/papers/MRS2015.pdf >	1-6, 10-11, 13-18, 22-23, 25, 35, 38-41 --- 7-9, 12, 19-21, 24, 36-37 --- 26-34
Y	US 2008/0303154 A1 (HUANG, H. et al.) December 11, 2008; paragraphs [0010, 0021-0022, 0027]	7-9, 12, 19-21, 24
Y --- A	US 2011/0193235 A1 (HU, H. et al.) August 11, 2011; figures 7, 8A; paragraphs [0020-0021]	36-37 --- 26-34

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 May 2016 (27.05.2016)

Date of mailing of the international search report

27 JUN 2016

Name and mailing address of the ISA/

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