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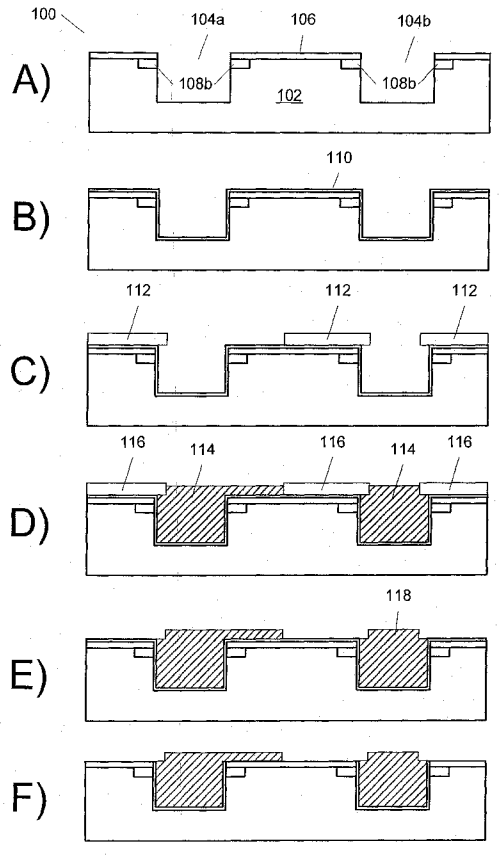
(54) Title: POST-SEED DEPOSITION PROCESS

FIG. 1



(57) Abstract: A method involves pattern etching a photoresist that is located on a wafer that contains a deposited seed layer to expose portions of the seed layer, plating the wafer so that plating metal builds up on only the exposed seed layer until the plating metal has reached an elevation above the seed layer that is at least equal to a thickness of the seed layer, removing the solid photoresist, and removing seed layer exposed by removal of the phototresist and plated metal until all of the exposed seed layer has been removed.

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— *with amended claims and statement*

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AMENDED CLAIMS
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1. A method, comprising:

depositing a seed layer onto a wafer;

forming a patterned resist on top of the seed layer, wherein the patterned resist has one or more openings exposing at least one portion of the seed layer, and wherein the patterned resist overhangs all or part of a via;

plating the exposed at least one portion of the seed layer with a layer of metal, wherein the layer of metal extends above the upper surface of the seed layer;

removing the resist; and

removing at least one portion of the seed layer that was exposed by said removing the resist.

2. The method of claim 1, wherein said removing the resist comprises exposing a side portion of the layer of metal.

3. The method of claim 1, wherein said plating the exposed areas of the seed layer comprises performing an electroless plating process on the exposed areas of the seed layer.

4. The method of claim 1, wherein said plating the exposed areas of the seed layer comprises performing an electroplating process on the exposed areas of the seed layer.

5. The method of claim 1, further comprising depositing an insulator on the wafer prior to depositing the seed layer.

6. The method of claim 1, wherein removing those portions of the seed layer that were exposed comprises concurrently etching away the exposed portions of the seed layer and the layer of metal until the height of the layer of metal has been reduced by at least the thickness of the seed layer.

7. The method of claim 1, wherein the patterned resist defines at least one opening configured to define at least a portion of an integrated circuit path along a surface of the wafer.

8. The method of claim 1, wherein the patterned resist defines at least one opening configured to define a post-like standoff.

9. The method of claim 1, wherein a via is formed in the wafer, wherein the seed layer is deposited in the via, and wherein the openings in the resist are located at least partially over the via.

10. The method of claim 9, wherein the patterned resist is a solid resist that is configured to cover at least a portion of the opening of the via.

11. The method of claim 9, wherein a portion of the layer of metal extends beyond the opening of the via and is configured to provide a routing trace.

12. A method, comprising:

patterning a resist that is located on a seed layer of a wafer to expose at least one portion of the seed layer and to overhang all or part of a via;

plating the at least one exposed portion of the seed layer with a layer of metal, wherein the layer of metal extends above the upper surface of the seed layer;

removing the solid resist; and

subsequently removing the at least one exposed portion of the seed layer and at least a portion of the metal layer.

13. The method of claim 12, wherein plating the at least one exposed area of the seed layer comprises performing an electroless plating process on the at least one exposed area of the seed layer.

14. The method of claim 12, wherein plating the at least one exposed area of the seed layer comprises performing an electroplating process on the at least one exposed area of the seed layer.

15. The method of claim 12, wherein a via is formed in the wafer, and wherein the at least one exposed portion of the seed layer is located in the via.

16. The method of claim 12, wherein removing at least a portion of the metal layer comprises reducing the thickness of the metal layer by an amount at least equal to the thickness of the seed layer.

17. The method of claim 12, wherein the resist is patterned to define at least one opening configured to define at least a portion of an integrated circuit path along a surface of the wafer.

18. The method of claim 12, wherein the resist is patterned to define at least one opening configured to define a post-like standoff.

19. The method of claim 12, wherein the resist is a solid resist.

STATEMENT UNDER ARTICLE 19 (1)

Independent claims 1 and 12 have been amended to recite, inter alia, that the patterned resist overhangs all or part of a via. Support for these amendments can be found in the originally filed specification at, for example, paragraphs 0019 and 0020. Claim 2 has been amended to recite exposing a side portion of the layer of metal. Support for this amendment can be found in the originally filed specification at, for example, paragraph 0027. Claim 3 has been amended to include elements recited in the originally filed claim 5. Claim 4 has been amended to include elements recited in the originally filed claim 6. Prior claim 11 has been rewritten as claim 5. Prior claims 7-10 have been rewritten as claims 6-9 and are amended to correct informalities. Claim 10 has been rewritten to recite that the patterned resist is a solid resist that is configured to cover at least a portion of the opening of the via.

Support for this amendment can be found in the originally filed claim 1 and in the originally filed specification at, for example, paragraphs 0019 and 0020. Claim 11 has been rewritten to recite that a portion of the layer of metal extends beyond the opening of the via and is configured to provide a routing trace. Support for this amendment can be found in the originally filed specification at, for example, paragraph 0023. Claims 13 and 14 have been amended in similar ways as claims 3 and 4, respectively. Claim 15 has been amended to recite that at least one exposed portion of the seed layer is located in the via. Support for this amendment can be found in the originally filed drawings. New claims 16-19 have been added. Support for new claims 16-19 can be found throughout the originally filed specification and the drawings.

The claim amendments are as shown in the listing of claims below, in which strike-through indicates deletion and underline indicates addition.