

- [54] **METHOD AND APPARATUS FOR GENERATING A TRAVELING DISPLAY**
- [75] Inventors: **Francis W. Albrecht, Bridgeport; William D. Baxter, Seymour; Robert J. Duggan; Stephen A. Grosky, both of Monroe, all of Conn.**
- [73] Assignee: **Bunker Ramo Corporation, Oak Brook, Ill.**
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- [52] U.S. Cl. .... **340/324 AD, 340/154, 340/172.5**
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- [58] Field of Search ..... **340/324 A, 324 AD, 340/154**

3,623,070 11/1971 Johnson et al. .... 340/154 X

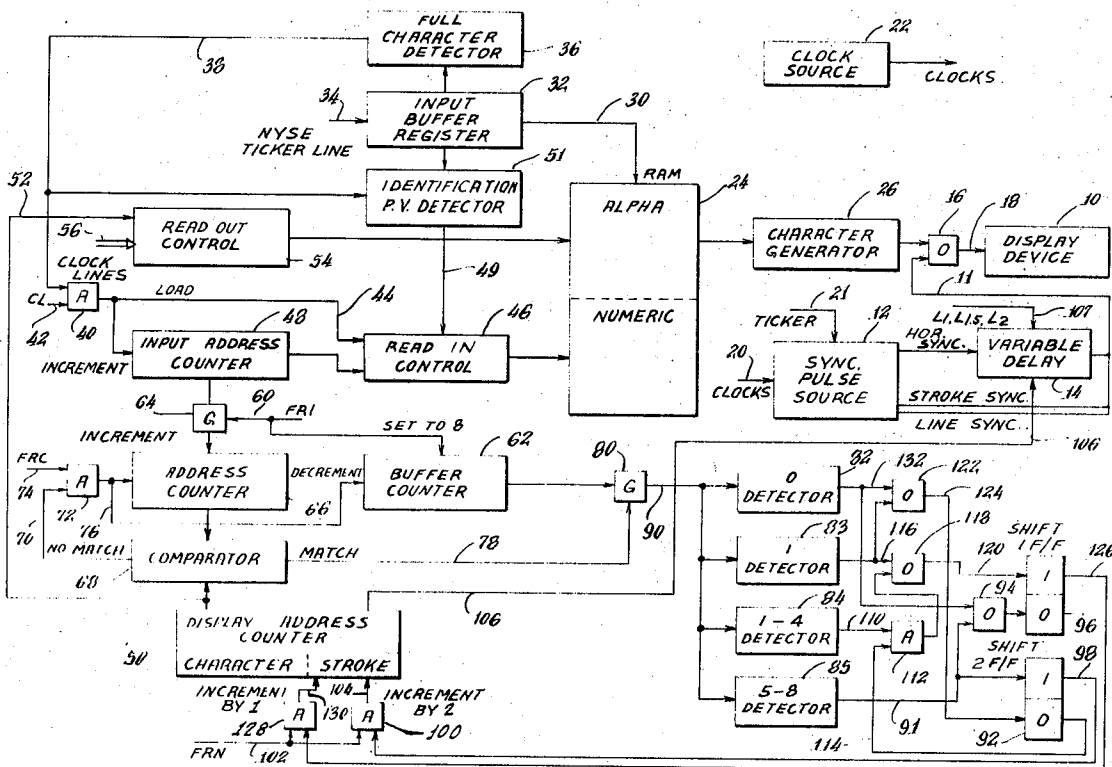
Primary Examiner—David L. Trafton  
Attorney—Frederick M. Arbuckle

[57] **ABSTRACT**

A method and apparatus for generating traveling display on a cyclically scanned electronic display device such as a cathode ray tube (CRT). The characters to be displayed are stored in a memory means with space being provided in the memory for a number of buffer characters waiting to be displayed. At a predetermined time in each cycle of the display a determination is made of the number of buffer characters then awaiting display. Each character is formed from a plurality of strokes. Depending on the number of buffer characters awaiting display, the display is shifted left by a selected number of character strokes for each display cycle. By varying the number of strokes that the display is advanced for each cycle in this way, the rate at which the display is moved may be varied as a function of the rate at which data to be displayed is received. The shifting by a small number of strokes for each cycle provides for a smooth flow of information across the display.

18 Claims, 4 Drawing Figures

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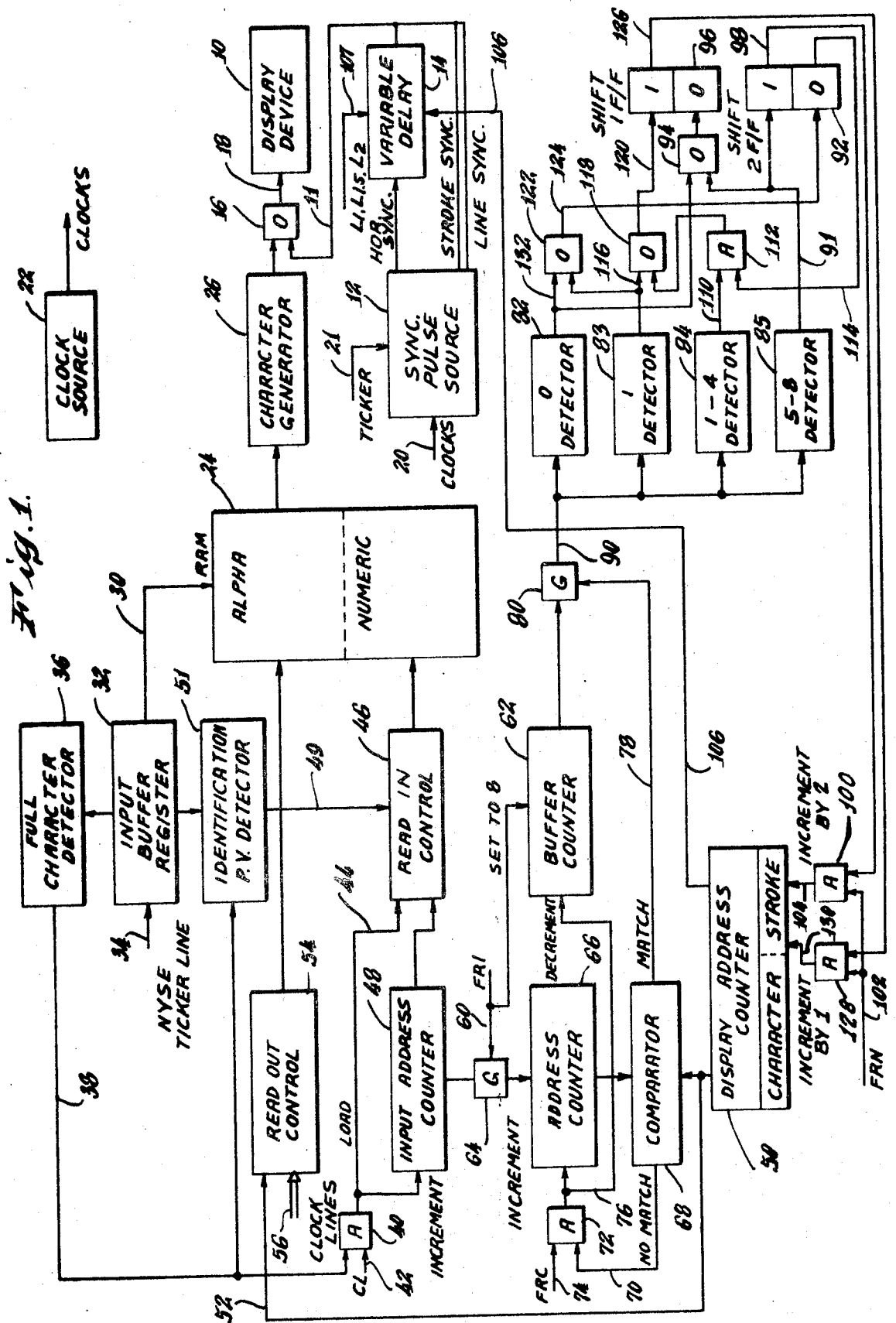
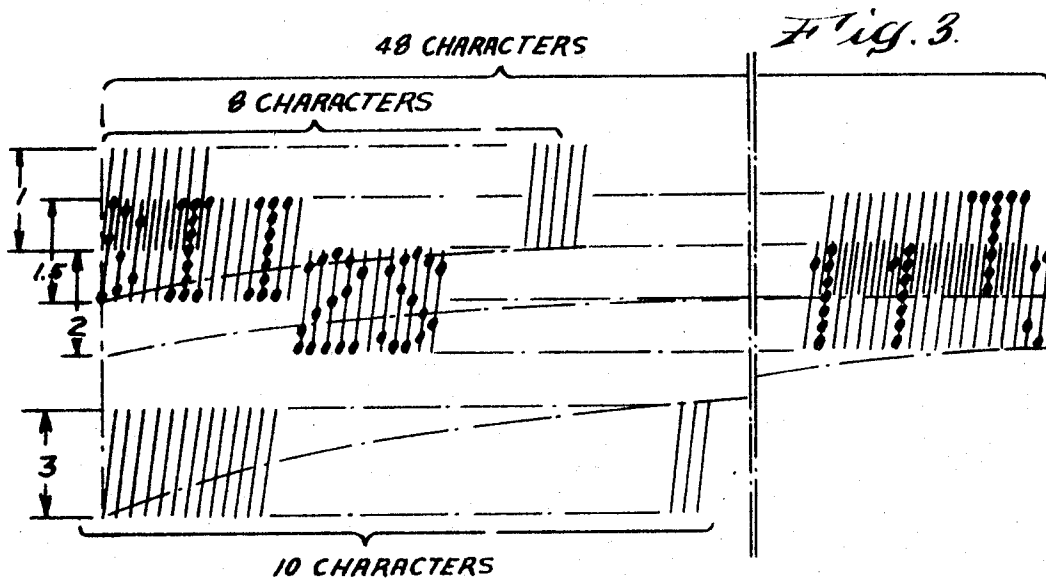
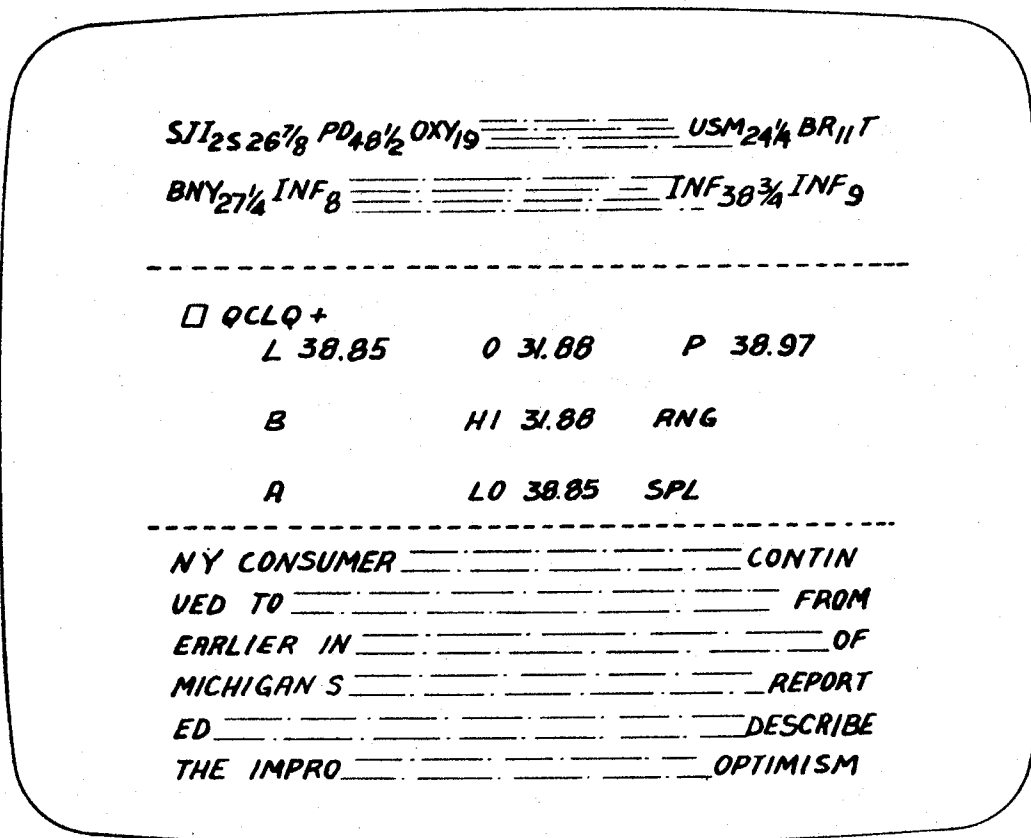


Fig. 2.



CHARACTER #

SEGMENT 1	1	-
	2	-
	3	-
	4	S
	5	I
	6	I
	7	-
	8	-
	9	-
	10	-
	11	-
	12	-
	13	P
	14	D
	15	-
<hr/>		
	47	B
	48	R
	49	-
	50	-
	51	T
	52	-
	53	-
	54	-
	55	-
	56	-
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SEGMENT 2	1	8
	2	-
	3	-
	4	-
	5	-
	6	-
	7	2
	8	S
	9	2
	10	6
	11	7
	12	8
	13	-
	14	4
	15	8
	16	/
	17	2
	18	-
	19	-
<hr/>		
	47	-
	48	-
	49	/
	50	/
	51	-
	52	2
	53	S
	54	4
	55	5
	56	3

Fig. 4.

# METHOD AND APPARATUS FOR GENERATING A TRAVELING DISPLAY

## CROSS REFERENCES TO RELATED APPLICATIONS

Related applications of particular interest include Ser. No. 178,728, filed Sept. 8, 1971 on behalf of Richard C. Casey, et al., entitled "Method and Apparatus for Controlling a Multi-Mode Segmented Display" and Ser. No. 178,691, filed Sept. 8, 1971 on behalf of Frank Albrecht, et al., entitled "Raster Control Device."

This invention relates to a method and apparatus for generating a traveling display and more particularly to the generating of a traveling display on a cyclically scanned electronic display device such as a cathode ray tube (CRT).

## BACKGROUND

Traveling displays are normally utilized to display various types of information such as advertising material, newswines or stock market prices. The later application is commonly referred to as a stock market ticker display.

Existing traveling signs are of two general types. In the first type of traveling display, characters are either mechanically or electrically formed in a character generator and are then physically moved by a belt or similar device past a viewing area. This type of display includes the projection ticker where a moving tape having printing thereon is projected on a screen. With the second type of moving display, a matrix of lamps is provided with characters being stepped from column to column on the lamps in response to timed strobe pulses. Between strobe pulses, the information is either stored within the lamps themselves, where gas discharge or other lamps having storage capability are utilized, or a separate storage device may be provided with each lamp.

Displays of the type indicated above are relatively large and expensive and generally require frequent maintenance. They are also relatively inflexible being adapted only for traveling display applications. There are applications where it is desired to display traveling information such as, for example, stock market ticker or newswine, on a general purpose display device such as a CRT. The ability to do this permits this information to be provided as part of a total information system rather than as a separate item and generally provides a lower cost, more reliable, and more flexible display.

However, to display traveling information on a device of this type, a control system must be provided to store the information to be displayed and to provide the simulated movement. In order to achieve an esthetically pleasing display, the display should appear to be moving at a fairly uniform rate. However, devices of this type are normally adapted to receive character information from a memory and to feed this information through a character generator to obtain a full character on the display. Shifting the information in full character steps would, however, give the display an unpleasant jerking appearance. A requirement therefore exists for providing a means to shift the information in partial character segments across the CRT screen so as to provide a smooth data flow.

Further, the rate in which information is received, particularly for ticker information, may not necessarily

be uniform. In order that a full screen of information can be continuously displayed without the loss of any information, the rates at which information moves across the display must vary as the input data rate varies. A control must thus be provided for varying the rate at which information is shifted.

It is therefore a primary object of this invention to provide a method and apparatus for generating a traveling display on a general purpose display device such as a CRT.

A more specific object of this invention is to provide a method and apparatus for permitting characters to be advanced across a display of the type indicated above in small steps of less than a full character each.

Another object of this invention is to provide a method and apparatus for advancing information across a display of the type indicated above at a rate which varies as a function of the rate at which input data is received.

## GENERAL DESCRIPTION

In accordance with these objects of this invention provides a method and apparatus for generating a traveling display. The apparatus includes a general purpose display device having a cyclical raster. An addressable memory means is also provided. The memory means has addressable positions for storing a first predetermined number of characters which characters are being displayed and memory positions adapted to store up to a second predetermined number buffered characters waiting to be displayed. A first means is provided for indicating the starting address of the first predetermined number of characters (i.e. the characters being displayed) and a second means is provided for indicating the address at which a new buffered character is to be stored. A means which is operative at a predetermined time in each cycle of the display device, such as for example during frame retrace, utilizes at least one of the indicating means to determine the number of buffered characters waiting to be displayed and increments the address indicated in the first indicating means by an amount which is dependent on the determined number. The first predetermined number of characters is read out from the memory means by a suitable means, starting at the address indicated in the first indicating means to control the display on the display device. If the address incremented in the first indicating means is a column or stroke address, and means are provided responsive to the column address in the first indicating means for controlling the number of columns of the character indicated by the first indicating means which are displayed, then the desired shifting in small incremental steps is achieved. By varying the number of columns or strokes which are added to the first indicating means during each display device cycle dependent upon the number of characters waiting in the memory means buffer position, the desired rate control of the traveling sign dependent upon the input data rate is achieved.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention.

## BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a schematic block diagram of a preferred embodiment of the invention.

FIG. 2 illustrates a display which might be obtained utilizing the invention.

FIG. 3 illustrates a portion of the display shown in FIG. 2 one display cycle time later.

FIG. 4 is a memory map illustrating the positions in which the characters shown in FIGS. 2 and 3 are stored for display.

#### DETAILED DESCRIPTION

FIG. 2 shows the face of a cathode ray tube (CRT) on which is displayed, at the top of the screen, the New York Stock Exchange ticker and the American Stock Exchange ticker. In the middle portion of the screen additional stock market related data is displayed and in the lower portion of the screen a newswire appears. Copending application Ser. No. 178,728 filed Sept. 8, 1971 on behalf of Richard C. Casey, et al. and entitled Method and Apparatus for Controlling a Multi-Mode Segmented Display and assigned to the assignee of the instant patent application describes a system for generating a segmented display of the type shown in FIG. 2 while copending application Ser. No. 178,691 filed Sept. 8, 1971 on behalf of Frank Albrecht, et al., entitled Raster Control Device and also assigned to the assignee of the instant patent application describes additional features of the ticker display generation. This application is concerned primarily with the method and apparatus for moving the characters of the two tickers from right to left across the screen of the CRT smoothly and in a way which varies as a function of the input data rate. It should be noted that the newswire information at the bottom of the screen may also be moved from right to left across the face of the screen. However, with six lines of newswire display as shown in FIG. 2, it is preferable that this information be displayed in the manner shown in U.S. Pat. No. 3,559,208 issued Jan. 26, 1971, to A. DiGiugno, et al., entitled "DATA DISPLAY MEANS" and assigned to the assignee of the instant application. With this mode of operation, the lines are written in succession with the first line being the one following the last line. It is also possible to display this information a line at a time with each new line being entered at the bottom of the display and the remaining lines each being moved up one line.

Since the manner in which movement is provided for the two tickers shown in FIG. 2 is the same, the following discussion will be with respect to the NYSE ticker on the first segment of the display, it being understood that what is said for this ticker will apply equally with respect to the ASE ticket on the second segment. Referring now to FIG. 1, it is seen that a display device 10 is provided which for purposes of the following discussion will be assumed to be a CRT adapted to display information such as that shown in FIG. 2. The CRT is cyclically refreshed with a raster pattern which is made up of, for example, 24 full lines each of which is made up of a plurality of strokes. Characters are formed by selectively intensifying some combination of seven index points on each of five strokes. In other words, characters are formed in a  $5 \times 7$  character matrix. Circuitry for generating the raster pattern described above are shown in U.S. Pat. No. 3,428,851 entitled "DATA DISPLAY SYSTEM" issued Feb. 18, 1969 to C Greenblum, and in U.S. Pat. No. 3,500,327, entitled "DATA HANDLING APPARATUS," issued Mar. 10, 1970 to R.D. Belcher, et al. Both of the above patents are as-

signed to the assignee of the instant application. From these patents it is seen that three-ramp signal generators are provided in the display to control the raster generation. A first ramp generator controls the stroke generation, a second ramp generator the line generation (horizontal retrace), and a third ramp generator the line spacing and frame retrace. Synchronizing pulses are applied through a line 11, OR gate 16 and line 18 to display 10 to control the various ramp generators. Stroke and line sync pulses generated by a sync pulse source 12 are applied directly to line 11 while the horizontal sync pulses from source 12 are applied to line 11 through variable delay 14. The function of delay 14 will be described later. The sync pulses are generated under the control of clocks on line 20, and a signal on line 21 indicating that it is the sync pulses for a ticker display which are required. The clock signals on lines 20 and at other points in the circuit are derived from a clock source 22. This circuit generates outputs to indicate the bit, stroke, character and line count for the raster on display 10 at each instant of time as well as providing various clocks to control the reading and writing of information from random access memory 24. In order to simplify FIG. 1, no attempt has been made to connect the outputs from clock source 22 to the various points in the circuit at which they are utilized.

The video code for the characters to be displayed on device 10 is obtained from character generator 26 through OR gate 16 and line 18. The input to character generator 26 is output line 28 from memory 24. As can be seen from the before mentioned R.C. Casey, et al. application Ser. No. 178,728, memory 24 is a large random access memory which may, for example, be a magnetic core matrix array. Various segments of this memory store information of various types for display on one or more display devices 10. For purposes of the present discussion only the portion of memory 24 which contains NYSE ticker information will be considered. New information is stored in memory 24 over line 30 from input buffer register 32. The input to this register is NYSE ticker line 34. When a full character is detected in this register by full character detector 36, a signal is applied through line 38 to one input of AND gate 40. The other input to AND gate 40 is a clock line 42. As will be seen shortly, information is read out of memory 24 in synchronism with the tracing of the characters on display device 10. Since the memory access speed is many times greater than the rate at which characters are refreshed by the CRT raster, one or more memory cycles are available for writing information into the memory between each read-out cycle. Signals appear on clock line 42 during times when the memory is available to be written into. When AND gate 40 is fully conditioned, a signal appears on load line 44 which signal is applied as one of the inputs to read-in control circuit 46. A second input to circuit 46 is derived from input address counter 48. This counter contains the address in memory 24 at which the next ticker character is to be stored. However, referring now to FIG. 4, it is seen that the stock ID portion of the ticker input is stored in a different segment of memory from the price and volume indications. The reason for this is that these items are displayed a half-line apart on the display and are therefore formed on different horizontal lines of the display. More will be said on this point later in conjunction with the description of memory read-out. However, at this point it can be seen that in

addition to the input address within a segment contained in counter 48, an indication must also be applied to circuit 46 of the segment. This information is obtained over line 49 from indent-price volume detector 51. Detector 51 may, for example, be a flip flop which is set by a signal on line 38 when the character in register 32 is indicated by a bit therein as being an indent character and is reset by a signal on line 38 if the bit is not present. Circuit 46 thus controls the character address in memory 24 at which the character on line 30 is stored. The signal on load line 44 is also applied to increment the address in counter 48 so that the next character received will be stored in a proper character position in the appropriate segment.

For the illustrative embodiment of the invention shown in FIGS. 1-4, 48 characters of ticker information may be displayed at any given time. In addition, 8 buffer character positions are provided. Thus, each segment of the memory 24 shown in FIG. 4 contains 56 character address positions. However, because of the way in which characters are displayed (see FIG. 2) a character may appear in the character position having a given number in only one of the segments. Thus, characters appear in character positions 4, 5 and 6 of segment 1 and in 7-12 of segment 2. Thus, a single register or counter may be utilized to indicate the character position at which the display starts. This information is contained in display address counter 50 (FIG. 1). This register contains both a character address and a stroke address. The character portion of the address is applied through line 52 as the starting address input to read-out control circuit 54. For example, with the information stored as shown in FIG. 4, the character position indicated in counter 50 would be character position 4. Thus, at the first character clock time when the raster is tracing the first line of the ticker display the S in character position 4 of segment 1 would be read-out. During the second character time the I in character position 5 would be read-out and so on. During character times 4-9 when character positions 7-12 are being accessed, no character or blank characters would be read-out and, as may be seen in FIG. 2, blank spaces would appear on the display during these character times. The read-out from memory segment 1 would continue under control of the clock signals on line 56 until character position 51 is reached at which time all 48 characters to be displayed will have been read-out.

A line return clock sync pulse would then be generated by source 12 and characters would be read-out for the second line of the NYSE ticker display again starting at character position 4. This time blank characters would be outputted during the first three clock times with the character 2 followed by the character S being outputted during the fourth and fifth clock times respectively. Again, appropriate characters would be outputted from the memory under control of the clock signals on line 56 until 48 character positions had been accessed (i.e. character position 51 is reached with the memory arranged as in FIG. 4).

If there were no characters waiting to be displayed in the buffer portion of memory 24 which, for the example shown in FIG. 4, is contained in memory positions 52-56 and 1-3, then the above described sequence of operations would be repeated each time the raster reached the portion of the display where ticker was appearing and a stationary display would thus be gener-

ated. However, with the example shown in FIG. 4, 6 characters are waiting to be displayed in the buffer portion of memory. Thus, at a clock time during frame retrace (frame retrace will normally occupy 6 character times) a signal appears on FR 1 clock line 60. The signal on this line is operative to set buffer counter 62 to a count of 8 and to condition gate 64 to pass the input address in counter 44 into address counter 66. The contents of counter 66 are then compared with the character count in counter 50. Since, for the example shown in FIG. 4, the initial count in counter 66 is 2 while the initial character count in counter 50 is 4, comparison circuit 68 will at this time generate at output on no-match line 70 which is applied as a conditioning input to AND gate 72. The other input to AND gate 72 is clock line 74 which has a signal applied to it for each frame retrace clock except the first. Thus, during FR 2 time, AND gate 72 is fully conditioned to generate an output on line 76 which increments the count in counter 66 to 3 and decrements the count in buffer counter 62 to 7.

Since a mis-match condition still exists in comparison circuit 68, AND gate 72 is still conditioned when the FR 3 clock pulse is applied to AND gate 72. The resulting output on line 76 is operative to increment counter 66 to a count of 4 and to decrement the count in counter 62 to 6. The character counts in counters 50 and 56 now match removing the mis-match signal from line 70 to prevent further changes in the counts in counters 66 and 62 and causing a signal to appear on match line 78 from compare circuit 68. The signal on line 78 conditions gate 80 to pass the count in counter 62 to a bank of detectors 82-85. Since the count in buffer counter 62 is 6, detector 85 is energized by the output on line 90 from gate 80 to generate an output on line 91 which is applied to set shift 2 flip flop 92 to its one state and through OR gate 94 to reset shift 1 flip flop 96 to its zero state.

One-side output line 98 from flip flop 92 is connected as one of the inputs to AND gate 100. At character clock time N of frame retrace, which for the embodiment of the invention indicated above could be clock time FR 10 or some clock time thereafter, a signal appears on line 102 fully conditioning AND gate 100 to generate an output on line 104 which is applied to increment the stroke portion of the address in display address counter 50 by two. Output line 106 from the stroke portion of counter 50 is connected as a control input to variable delay 14. Delay 14 also has an input on line 107 which permits the variable delay function to be performed only when a line 1, 1.5 or 2 of a ticker segment is being terminated.

To understand the function of variable delay 14, refer now to FIG. 3. From this figure it is seen that line 1 of the display is only 8 characters long. At the end of this line a horizontal sync or horizontal retrace pulse is generated by source 12. This pulse is delayed by delay 14 by a number of strokes equal to the stroke count in counter 50. Thus, with the example chosen, this sync pulse is delayed by two strokes. The circuit then effects a line retrace and a half line advance and the raster starts scanning at character 1 line 1.5. The reason for, and circuitry for controlling, the half-line advance are described in detail in the beforementioned Albrecht, et al. application Ser. No. 178,691. However, while the retrace pulse was being delayed by 2 strokes, clock 22 continues to run at its normal pace controlling the

read-out from memory 24. Thus, the read-out memory 24 is two strokes out of phase with the display, or in other words, the display is two stroke positions to the left of where the circuit clock indicates it is. Thus, an effective two stroke shift operation is performed. The effect of this two stroke shift left operation is shown in FIG. 3. Similarly, the horizontal retrace sync pulse at the end of line 1.5 is also delayed by two strokes in circuit 14. However, since this character position, character position 52, is blank for line 1.5, nothing is displayed during these strokes.

Since the line retrace was delayed by two strokes, line 2 starts two strokes behind where the circuit clocks indicate it should start and it is thus also effectively shifted left two stroke positions. This line thus also runs two stroke positions beyond the normal end of the line permitting two strokes of the character in character position 52, the numeral 2, to be displayed before a retrace occurs. The next retrace is a full line retrace to line 3. Since this line is blank, a delayed start of this line causes no problem. However, since the line 3 clock is not an input to variable delay 14, the horizontal retrace clock at the end of this line is not delayed and normal synchronization between the circuit clock and the display raster is reestablished. While it does not form part of the present invention, it would be noted that, for some applications, resynchronization of the display may require that less than the full number of characters be scanned on line 3 (see beforementioned pending application Ser. No. 178,691).

At the next frame retrace time, it is found that there are still 6 characters waiting in the buffer to be displayed and flip flop 92 thus remains set to its 1 state causing the stroke count in counter 50 to again be incremented by 2. Thus, during the next frame of the display, the line retrace pulses for lines 1.5 and 2 are delayed by four strokes causing an effective four stroke shift to the left on the display. The display is, however, only two strokes further to the left than it was on the preceding frame.

During the next frame retrace time the stroke count is again incremented by two causing a six stroke shift to the left to occur during the next display frame. At the end of this frame, counter 50 is again incremented by two strokes. However, since there are only seven strokes to a character, incrementing the counter by two when the stroke count is at six, causes the character count to be incremented by one and the stroke count to be reset to one. Thus, during the next display frame the character count in counter 50 will be pointing to memory position 5 (FIG. 4) and the display will start with the character in this memory position. The stroke count of one will result in a one-stroke delay so that one stroke of this character will be missing. It should be noted that at the end of this frame, when the comparisons are performed in circuit 68, it will be found that only five characters are now waiting in the buffer. However, since detector 85 is responsive to fine characters through eight characters, an output again appears on line 91 and flip flop 92 remains set.

The shifting by two strokes for each frame continues until the character in memory position 5 has been shifted out and the character count in counter 50 is pointing to character 6. At this time, assuming that no new characters have in the interim been applied to the buffer, the character count for the buffer is found to be four during the next frame retrace time. However, out-

put line 110 from detector 84 is applied as one input to AND gate 112, the other input to which is zero-side output line 114 from 2 flip flop 92. Thus, since flip flop 92 is in its one state at this time, the output on line 110 is ineffective to change the condition of the flip flops and the shifting by two strokes per frame continues.

Again, assuming that no new characters have been applied to memory 24 in the interim, the operation continues as indicated above until the character count in counter 50 has been incremented to nine. When this occurs, buffer counter 62 will be stepped down to a count of one before a match is detected in comparator 68 and detector 83 will thus be energized to generate an output on line 116. The signal on line 116 is applied through OR gate 118 and line 120 to set shift 1 flip flop 96 to its one state, and through OR gate 122 and line 124 to reset flip flop 92 to its zero state. With a signal now appearing one-side output line 126 from flip flop 96 and no signal on output line 98 from flip flop 92, AND gate 128 rather than AND gate 100 is fully conditioned at frame retrace clock time N. The resulting output signal on line 130 is applied to increment the stroke count in counter 50 by one. During the next frame the line retrace delay introduced will thus be only one stroke greater rather than two strokes greater than the preceding frame. The rate at which characters are moving across the screen will thus appear to be effectively decreased.

If no new characters are received in memory 24 during the six or seven display cycles between the time that flip flop 96 is set and the time that the character count in counter 50 is again incremented, then, during the frame retrace time following that at which the character count is incremented, the count in buffer counter 62 will be decremented to zero before a match is detected in comparator 68 and detector 82 will thus be energized to generate an output on line 132. The signal on line 132 is applied through OR gate 94 to reset flip flop 96 to its zero state. The signal on line 132 is also applied through OR gate 122 to reset flip flop 92 to its zero state. This latter operation should not normally be necessary but is included as a precaution. With both flip flops 92 and 96 in their zero state, neither AND gate 100 nor 128 is conditioned when a clock pulse appears on line 192 and the count in counter 50 is thus not changed during the frame retrace time. Thus causes the display to stop shifting or, in other words, to remain stationary until new input data is received.

When new data is received, either when the buffer is empty or when one or more characters are still in the buffer, the count in input address counter 48 is suitably incremented. It should be noted that since the characters stored in character positions 4-9 of the memory are no longer being utilized for display, these characters may now be written over. Assume that four or less characters are in the buffer after the input data is received. Under these conditions, at the end of the frame during which the new data was received, the buffer counter is decremented to a count between one and four before a match is detected. Detector 84 is thus energized to generate an output on line 110. Since flip flop 92 is now reset generating an output on line 114, AND gate 112 is fully conditioned to generate an output which is applied through OR gate 118 to set flip flop 96 to its 1 state. The circuit thus starts shifting by one or continues shifting by one in a manner previously indicated. If more characters are received while the

shift-1 flip flop is set, so that the total number of characters in the buffer portion of memory is 5 or greater, then shift-2 flip flop 92 is set and the rate at which characters are shifted across the screen increased.

A system has thus been provided which permits characters to be shifted across the face of a cathode ray tube or similar display device in relatively small steps so as to give the appearance of a smooth flow of data across the screen. The system is also capable of varying the rate of which characters are shifted across the screen depending on the rate at which input characters are received.

While for the preferred embodiment of the invention, a cathode ray tube display device has been specified, it is apparent that the teachings of this invention could be utilized with any display device which is cyclically energized. Further, the particular type of memory utilized is not critical, provided it is capable of performing the required functions. The manner in which information is stored and read out from memory 24 may also vary. For example, information on ticker line 34 may be applied first to a processing unit which performs various operations on the information before storing it in memory 24. With this mode of operation, detectors 36 and 51 would be dispensed with and the information provided by these detectors would be derived directly from the processing unit.

It should also be noted that, while for a preferred embodiment of the invention, the stroke shifting is accomplished by delaying the display, what is required is that a change be effected in the synchronization between the display raster and the clock controlling memory read-out. Thus, the shift could also be effected by delaying or otherwise altering the clock signals utilized for memory read-out. Similarly, the particular method utilized for determining the number of buffer characters awaiting display and the buffer character counts at which changes in the shift rate occur may also be altered while still remaining within the scope of the invention. The number of strokes by which shifting occurs during each retrace cycle may also be increased to three or more for applications where information is being more rapidly received. Finally, while line 18 has been shown as being connected to a single display device 10, it is apparent that this line could be connected to cause the same display to simultaneously appear on a number of display devices. By suitably controlling the reading out of memory and by multiplexing its output, the information in portion 24 may be displayed in different ones of the display segments. Shown in FIG. 2 on different ones of the devices (see beforementioned co-pending application Ser. No. 178,728).

Thus, while the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be apparent to those skilled in the art that the foregoing and other changes in form and detail may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A circuit for generating a traveling display comprising:

a display device which is cyclically scanned; an addressable memory means, said memory means having addressable positions for storing a first predetermined number of characters being displayed and addressable positions adapted to store up to a

second predetermined number of buffered characters waiting to be displayed; means for indicating the starting address of said first predetermined number of characters;

means operative at a predetermined time in each cycle of said display device for determining the number of said buffered characters waiting to be displayed and for incrementing the address indicated by said indicating means by an amount which is dependent on said determined number; and means for reading out the first predetermined number of characters from said memory means in a predetermined sequence, starting at the address indicated by said indicating means, to control the display on said display device.

2. A circuit of the type described in claim 1 including means for indicating the address at which a new buffered character is to be stored; and wherein

said number of buffered characters determining means includes means for utilizing at least one of said indicating means to make the determination.

3. A circuit of the type described in claim 2 wherein said number of buffered characters determining means includes means for comparing the addresses in said indicating means, and means responsive to the difference between said addresses for generating an indication of said number of buffered characters waiting to be displayed.

4. A circuit of the type described in claim 3 wherein said number of buffered character indication generating means includes means responsive to a mismatch in said comparing means for incrementing the count in said new buffered character address indicating means, and means for determining the number of times said address must be incremented before a match is detected in said comparing means, said number serving as an indication of said number of buffered characters.

5. A circuit of the type described in claim 1 wherein the incrementing of the address indicated by said indicating means may be by two or more discrete different amounts;

and wherein the discrete amount by which an address is incremented may vary for a given number of buffered characters depending on the previous history of the number of buffered character determination.

6. A circuit of the type described in claim 1 wherein said display device is a cathode ray tube which is cyclically refreshed;

and wherein each character to be refreshed on a display device is stored in said memory means as one of said first predetermined number of characters and is read out in synchronism with the refresh of the character to control the refresh thereof.

7. A circuit of the type described in claim 1 wherein there are two lines of characters in said traveling display;

wherein each of said lines has said first predetermined number of characters positions, but wherein characters may appear in the corresponding character position on only one of said lines;

wherein said memory includes separately identifiable areas for storing characters to be displayed on each of said lines; and

wherein the address indicated in said starting address indicating means may be in the area of memory for

either of said lines depending on which area is storing a character at the indicated address.

8. A circuit of the type described in claim 1 wherein said display consists of characters each formed by changing the visible state of selected points on a plurality of columns of a character matrix;

wherein the address incremented in said indicating means is a column address; and including means responsive to the column in said indicating means for controlling the number of columns of the character at the address indicated by said indicating means which are displayed. eadoot means and the display

9. A circuit of the type described in claim 8 wherein said characters reading out means reads characters out in synchronism with the display of said characters on said display device;

and wherein said number of columns controlling means includes means for altering the synchronism between said read out means and the display by the time required to form a number of columns equal to the amount by which said column address is incremented.

10. A circuit of the type described in claim 8 wherein said number of columns controlling means includes means for eliminating a number of columns equal to the number by which said column address is incremented from the beginning of the display, adding said number of columns to characters at the end of the display, and shifting the remaining characters of the display in the direction of the beginning of the display by said number of columns.

11. A circuit of the type described in claim 8 wherein said display device is a cathode ray tube, the beam of which cyclically traces a predetermined raster pattern; wherein said memory reading out means reads characters out of said memory in synchronism with the raster pattern reaching the points on the CRT where the characters are to be displayed; and wherein said columns controlling means includes means for altering the timing of the raster to delay line retrace by a time equal to the trace time of the columns indicated by said column address, whereby the synchronism between said memory and raster is altered.

12. A method for generating a traveling display on a cyclically scanned display device, comprising the steps of:

storing in an addressable memory means a first predetermined number of characters being displayed and a second predetermined number of characters waiting to be displayed;

indicating the starting address in said addressable memory means of said first predetermined number of characters;

determining, at a predetermined time in each cycle of said display, the number of buffered characters waiting to be displayed;

incrementing the starting address indicated for said first predetermined number of characters by an amount which is dependent on said determined number;

and reading out the first predetermined number of characters from said memory means in a predetermined sequence, starting at said indicated starting address, to control the display of said display device.

13. A method of the type described in claim 12 including the steps of indicating the address at which a new buffered character is to be stored;

and wherein said number of buffered characters determining steps includes the steps of comparing the addresses indicated for storing a new buffered character with the address for the beginning of said first predetermined number of characters, and generating an indication of said number of buffered characters waiting to be displayed in response to the difference between said addresses.

14. A circuit for generating a traveling ticker display on a cathode ray tube (CRT) having a display screen which is cyclically refreshed, characters being formed on said screen by selectively intensifying spots on a selected number of vertical strokes comprising:

a memory having an area for storing stock I.D. information and an area for storing price-volume information, each of said areas having space to store at least one buffered character in addition to the characters being displayed;

means for reading out information from the stock I.D. area of memory in synchronism to the refresh of stock I.D. characters during a first horizontal scan of said screen and for reading out information from the price-volume area of memory in synchronism with the refresh of price-volume characters during a second horizontal scan of said screen; and means operative during each succeeding refresh cycle of said CRT for selectively eliminating a number of strokes which is less than said selected number of strokes from the left-most character or characters on said horizontal scans, for adding said number of strokes to the right-most character on a scan, strokes for a new character from the appropriate one of said buffered character position being added to the right end of the display if necessary, and shifting the remaining characters of the ticker display to the left by said number of stroke positions.

15. A circuit of the type described in claim 14 wherein said means operative during each succeeding refresh cycle includes means for altering the synchronism between the reading out of information from said memory and the refresh of characters on said CRT by the time required for said CRT to form said number of strokes.

16. A circuit of the type described in claim 15 where the ray of said CRT traces a predetermined raster pattern; and

wherein said synchronism altering means includes means for altering the timing of the CRT raster to delay line retrace by said time required to form said number of strokes.

17. A circuit of the type described in claim 16 including means for generating an extra horizontal scan of said screen before said first horizontal scan and an extra horizontal scan of said screen after said second horizontal scan, the first extra scan having said number of strokes added after the last characters of its raster, and the second extra scan having said number of strokes subtracted from its first character raster, whereby raster synchronism is reestablished.

18. A circuit of the type described in claim 14 wherein there are a plurality of buffer character storing positions in each of said areas of memory;

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and including means for determining the number of characters stored in said buffered character storing positions;  
and means responsive to the number of buffered

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characters determined for controlling said number of strokes eliminated, added and shifted during each succeeding refresh cycle.

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