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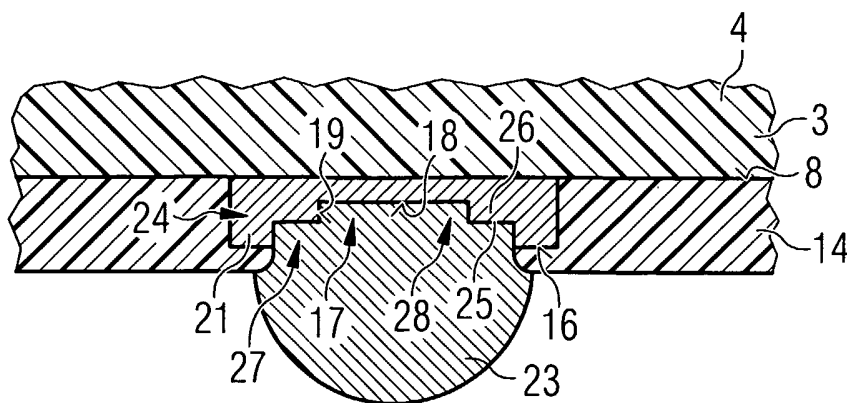
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(54) Title: SUBSTRATE, ELECTRONIC COMPONENT, ELECTRONIC CONFIGURATION AND METHODS OF PRODUCING THE SAME



(57) Abstract: A substrate (3) for an electronic component (1) comprises a dielectric body (4) having an upper surface (6) including a plurality of inner contact pads (5) and a lower surface (8) including a plurality of outer contact pads (7; 24). Each outer contact pad (7; 24) has an inner face and an outer face (16). An insulating layer (14) covers the lower surface (8) of the dielectric body (4) and the peripheral regions (16) of the plurality of outer contact pads (7; 24). A depression (17) is located in the approximate lateral centre of the outer face (16) of each of the plurality of outer contact pads (7; 24).



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Description

Substrate, Electronic component, Electronic configuration and methods of producing the same

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The present invention relates to substrates for electronic components, such as semiconductor packages, to electronic components and electronic configurations as well as to methods for fabricating substrates and assembling electronic components and electronic configurations.

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Semiconductor packages including a semiconductor chip are typically mounted on a substrate such as a printed circuit board (PCB) by the external contacts of the package. These external contacts may be pins, leads or solder balls depending on the type of package. Typically, the printed circuit board also includes other electronic components which are electrically connected by conductor tracks located on or within the PCB to form an electronic subsystem. Such subsystem boards are widely used.

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Printed circuit board including semiconductor packages suffer from the problem that the joints between the package and the board can fail. This may be caused by thermal cycling or due to the different thermal expansion coefficients.

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The problem of crack formation in the metallurgical contacts is addressed by US 6,696,757 which provide a contact which comprises a castellated contact pad. However, these contact pads are complex and expensive to produce and, therefore, the cost of the package is undesirably increased.

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In many consumer goods including printed circuit boards with electronic components and semiconductor packages, such as mobile telephones for example, the printed circuit board and the semiconductor packages mounted on the printed circuit board
5 undergo repeated mechanical stress. Mechanical stress may also lead to failure of the subsystem due to the delamination of the package from the printed circuit board.

It is, therefore, an object of the invention to provide a substrate for an electronic component, in particular a semiconductor package, an electronic component and electronic configurations which can better withstand mechanical stress and which can also be manufactured inexpensively.

15 It is a further object of the invention to provide methods for the fabrication of substrates for electronic components and methods for the assembly of electronic components and electronic configurations.

20 These objects are solved by the subject matter of the independent claims. Further advantages arise from the subject matter of the dependent claims.

The invention provides a substrate for an electronic component
25 which comprises a dielectric body having an upper surface and lower surface. Preferably, the dielectric body is provided in the form of a dielectric board. The substrate further comprises a plurality of inner contact pads disposed on the upper surface and a plurality of outer contact pads disposed on the
30 lower surface.

The substrate also includes a plurality of conductor tracks disposed on the upper and lower surfaces and vias located in the body of the substrate. The inner contact pads and electrically connected to the outer contact pads by the conductor tracks and vias and provide the electrically conductive rewiring or redistribution structure of the substrate. Each outer contact pad has an inner face and an outer face. The inner face of each of the outer contact pads is level and lies in a single plane. Essentially, the whole of the single plane, inner face is in contact with the lower surface of the dielectric body.

The substrate further comprises an insulating layer covering the lower surface of the dielectric body and the peripheral regions of the plurality of outer contact pads. The central portion of the outer contact pads remains free from the insulating layer. The insulating layer is, preferably, a solder resist layer. A solder resist layer comprises a material which is not wetted by solder. This prevents solder from flowing away from the contact areas during the solder reflow process and prevents short circuits between adjacent contact areas or conductor tracks for example.

The plurality of outer contact areas each include a depression or recess which is located in the outer face of each of the plurality of outer contact pads. Each depression has a base and at least one side wall and is located in the approximate lateral centre of the outer face of the outer contact pad.

The depression of each of the outer contact pads remains free from the insulating or solder resist layer and, therefore, provides the electrically conductive surface of the outer con-

tact pad. The depression, therefore, has a depth which is less than the thickness of the peripheral region of the outer contact area.

5 Alternatively, the outer contact pad is described as comprising a base portion comprising an annular protrusion situated at the periphery of the base portion. The outwardly facing surfaces of the annular protrusion are covered by the insulating layer.

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The provision of a depression in the outer face of each of the outer contact pads advantageously provides a more reliable interface between the solder ball, which will be attached to the outer contact pads, and the outer contact pad itself. The substrate of the invention is a laminate substrate and is advantageously used in ball grid array (BGA) type packages.

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The outer contact pads of the invention including a depression can be fabricated using existing equipment and existing materials. Therefore, the use of alternative materials, in particular alternative alloy compositions of the solder avoided. This reduces the cost of the substrate and ultimately the cost of the electronic component or semiconductor package.

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25 Also, the use of an additional underfill material between the package and the printed circuit board can be avoided. This is particularly advantageous as this additional step has to be performed by the customer. Therefore, the invention provides a more reliable substrate which can be more simply handled by the customer. This also increases the reliability of the package.

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Typically, the substrate includes a plurality of outer contact pads, each having a depression or recess located in the outer face of the outer contact pad. The outer contact pad and depression of each of the plurality of outer contact pads is essentially the same. Preferably, the depression is concentrically positioned in the outer face of each of the outer contact pads. This has the advantage that mechanical stress is more uniformly distributed as the ball thickness of the annular protrusion is essentially the same at all points around the ring.

The depression and the outer contact pad are, preferably, laterally essentially circular. This has the advantage that a reliable joint can be formed between the solder ball and the inner surfaces, that is the base and inner side walls, of the outer contact pad. Since, during the solder reflow process, the effects of surface tension result in the solder ball tending to form a sphere. Therefore, an essentially laterally circular depression provides a more uniform contact between the solder ball and the inner surfaces of the depression and, therefore, provides a more uniform distribution of stress and a more reliable joint.

In an alternative embodiment of the invention, the side wall of each depression further comprises at least one step. The provision of a step in the side wall increases the interfacial surface area between the outer contact pad and the solder ball. Therefore, a more reliable joint can be provided. Preferably, each depression is laterally smaller at the base than at the plane of the outer face of the outer contact area. This structure has the advantage that it is easily fabricated by etching techniques for example.

The step is, preferably, concentrically positioned in the side wall. The step, therefore, has approximately the same width along the whole of its length. This enables a more even distribution of mechanical stress and a more uniform interfacial surface area between the outer contact pad and the solder ball.

The outer contact pad, preferably, comprises copper or a copper alloy and the dielectric body, preferably, comprises a BT-resin or FR4. These materials are widely used and inexpensive. They are, therefore, easy to use in the existing manufacturing line so that costs are not increased.

The substrate of the invention is, preferably, provided as a panel. The panel comprises a plurality of component or package positions, each component position provides a substrate for a single component. The component positions are typically arranged in a matrix grid of rows and columns. Adjacent component positions are separated by singulation trenches or saw streets. Typically, a semiconductor package is assembled on each of the package positions of the panel and then the packages are singulated from the panel, typically, by a sawing process.

In an alternative embodiment, the substrate further comprises a plurality of solder balls. A solder ball is disposed on each of the outer contact pads. At least part of the solder ball is located within the depression of each of the outer contact pads and, preferably is in contact with and electrically connected to, the base and inner side walls of the depression.

The side wall of the depression, therefore, laterally surrounds at least part of the solder ball.

5 The solder ball, therefore, has a volume which is larger than the volume of the cavity formed by the depression. Therefore, only the portion of the solder ball facing towards the outer contact pad is located within the depression and the outer portion of the solder ball protrudes from the depression. The protruding outer portion enables the solder ball to be connected to an external substrate such as a printed circuit board.

15 The invention also provides an electronic component comprising a substrate according to one of the embodiments previously described. The electronic component also comprises a semiconductor chip having an active surface with chip contact pads and a passive surface. The semiconductor chip is mounted on the upper surface of the substrate. The electronic component further comprises a plurality of electrical connections which electrically connect the semiconductor chip to the inner contact pads positioned on the upper surface of the substrate. An electrical connection is in electrical contact with each of the chip contact pads and a corresponding inner contact on the upper surface of the substrate.

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The electronic component also includes a plurality of solder balls. As previously described, a solder ball is disposed on each of the outer contact pads and at least part of the solder ball is located within the depression of each of the outer contact pad. The side wall of the depression laterally surrounds at least part of the solder ball.

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The electrical connections may comprise solder bumps or balls so that the semiconductor chip is mounted by a flip-chip technique on the upper surface of the substrate. In this embodiment of the invention, the inner contact pads of the substrate are located towards the centre of the upper surface and have a lateral arrangement which, preferably, corresponds to the lateral arrangement of the chip contact pads.

Alternatively, the electrical connections comprise bond wires.

In this embodiment, the inner contact areas of the substrate are located towards the periphery of the upper surface and laterally surround the semiconductor chip. The passive surface of the semiconductor chip is mounted on the upper surface of the substrate. The outer contact areas of the substrate can be of any of the embodiments previously described.

The semiconductor chip and upper surface of the substrate may also be encapsulated in a plastic molding compound, typically an epoxy-based resin. This encapsulation protects the chip from mechanical damage and from the environment.

The invention also provides an electronic configuration which comprises an electronic component according to one of the embodiments already described and a circuit board. The circuit board comprises a plurality of component contact areas on its upper surface and a plurality of conductor tracks which enable the electronic component to be electrically connected to other components. The electronic component is mounted on the circuit board by the plurality of solder balls. A solder ball is disposed between each outer contact pad of the substrate of the electronic component and a component contact area of the circuit board.

The invention provides a more reliable electronic configuration due to the improved reliability of the solder joints formed between the outer contact pads of the laminate substrate and the solder balls. Therefore, the reliability of the joint formed between the electronic component and the component contact areas. The likelihood of failure of the electrical contact is reduced.

The invention also relates to methods of fabricating a substrate. A dielectric body having an upper surface and a lower surface is provided. Preferably, the dielectric body is a dielectric board. A plurality of precursor outer contact pads are provided on the lower surface of the dielectric body.

The precursor outer contact pads may be deposited using a masking and deposition technique or, alternatively, by depositing a closed layer and removing the undesired areas to leave the precursor outer contact pads. The precursor outer contact pads have a thickness which is approximately that of the desired thickness of the peripheral regions of the final outer contact pads of the package. The outer surface of the precursor contact pad is level and uniform and lies in a plane parallel to the lower surface of the substrate.

A plurality of depressions are then formed, a depression being formed in the approximate lateral centre of each of the plurality of outer contact pads to form a contact pad according to an embodiment previously described.

An insulating layer is then deposited on the lower surface of the dielectric body. The plurality of depressions remain un-

covered by the insulating layer. The insulating layer is a solder resist layer and includes apertures or through-openings positioned in alignment with the plurality of depressions. The periphery of the outer face of the depression is covered by the insulating layer. The insulating layer, therefore, has a thickness which is greater than the thickness of the periphery of the outer contact pad and greater than the thickness of the precursor outer contact pad.

10 The plurality of depressions can be formed by the following method. A first structured photoresist layer is deposited on the lower surface of the dielectric body. The central portion of the precursor outer contact pads remains free from the first photoresist layer. A depression in the uncovered portion
15 of each of the precursor outer contact pad is then formed by an etching process. The first photoresist layer is removed and a second photoresist layer is applied.

The second photoresist layer essentially covers the depressions in the outer contact pads but leaves the remaining areas of the lower surface and the outer peripheral face of the outer contact pads exposed. The insulating layer is then applied to the lower surface of the dielectric body and, afterwards, the second photoresist layer is removed to expose the
25 depressions in the outer contact pads.

In an alternative embodiment, the method may also include the further process step of forming a step in the side wall of each of the depressions. The step is, preferably, formed by
30 applying a third structured photoresist layer to the lower surface of the dielectric body. The central portion of each of the depressions already formed in the outer contact area re-

mains uncovered by the third photoresist layer. A second depression is then formed in the uncovered region of each of the outer contact pads by an etching process. The third structured photoresist layer is then removed.

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The etching process to form both the first and, in an alternative embodiment, also the second depressions in the outer contact pads is, preferably, performed by a chemical etching process or they plasma etching technique.

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The invention also relates to methods of assembling an electronic component. A method comprises the steps of providing a substrate according to one of the embodiments already described. A semiconductor chip having an active surface and a plurality of chip contact pads positioned on the active surface is also provided.

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The semiconductor chip is then mounted on the upper surface of the substrate and electrical connections are made between the chip contact pads and the inner contact pads positioned on the upper surface of the substrate. A solder ball is placed on each outer contact pad positioned on the lower surface of the substrate.

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As previously described, at least part of the solder ball is located within the depression positioned in each of the outer contact pads. The solder ball is in contact with and electrically connected to the base and side wall of the depression. The side wall of the depression, therefore, laterally surrounds at least part of the solder ball.

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The electrical connections are, in one embodiment of the invention, provided by solder balls of flip-chip contacts positioned between each of the chip contact pads and inner contact pads of the substrate. In a second embodiment, the electrical connections are provided by forming bond wires between each of
5 the chip contact pads and an inner contact pad.

The invention also relates to methods of assembling an electronic configuration. Firstly, an electronic component such as
10 a semiconductor package which includes a substrate as previously described, is provided. A circuit board, preferably a printed circuit board, is provided. A plurality of component contact areas and electrically conducting conductor tracks are disposed on the upper surface of the circuit board.

15

The electronic component is mounted on the circuit board by the plurality of solder balls. A solder ball is disposed between each outer contact pad of the substrate of the electronic component and a component contact area disposed on the
20 upper surface of the circuit board. A solder reflow process is then performed to provide the electrical connection between the component and the printed circuit board.

The invention, therefore, provides a laminate substrate for a
25 semiconductor device, and is advantageously used in a ball grid array type integrated circuit. The peripheral regions of the outer contact pad or solder pad are surrounded by, and covered with, an insulating layer which is preferably a solder resist layer. According to the invention, a depression or re-
30 cess is provided in the approximate lateral centre of the outer face of each of the contact pads.

The outer contact pad, according to the invention, is thought to move the weakest intermetallic interface away from the area of greatest stress concentration thereby reinforcing the weakest metallic interface and providing a more reliable joint. It is through that the interface between the outer contact area and the solder ball may be the weakest into metallic interface Analysis of drop tests indicates that the peeling stress (SZ) and equivalent stress according to von Mises (SEQV) at the interface between the outer contact area of the substrate, according to the invention, and the solder ball is reduced by 12 to 14% compared to a substrate including conventional contact pads. A more reliable package, which is better able to withstand mechanical stress, is, therefore, provided.

Embodiments of the invention will now be described with reference to the diagrams.

Figure 1 shows a ball grid array (BGA) semiconductor package having outer contact pads according to a first embodiment of the invention, and

Figure 2 shows a portion of a laminate substrate including an outer contact pad according to a second embodiment of the invention,

Figures 3 to 8 show steps in the fabrication of an outer contact pad according to the embodiment of the invention of Figure 1.

Figure 3 illustrates a section of a laminate substrate including a precursor outer contact pad,

Figure 4 shows the application of a first photoresist layer to the precursor outer contact pad of figure 3,

Figure 5 shows the etching of the depression in the precursor contact pad of figure 4,

Figure 6 shows the application of a second photoresist layer to the depression formed in the method step of figure 5,

Figure 7 shows the deposition of a solder resist layer on the structure of figure 6,

Figure 8 shows the removal of the second photoresist layer.

Figure 1 illustrates a ball grid array (BGA) semiconductor package 1 according to a first embodiment of the invention. The semiconductor package 1 includes a semiconductor chip 2 which is mounted on a laminate substrate 3.

The laminate substrate 3 comprises a dielectric board 4 of FR4 material. A plurality of inner contact areas 5 are positioned on the upper surface 6 of the dielectric board 4 towards the lateral centre. The plurality of inner contact areas 5 are electrically connected to outer contact areas 7 disposed on the lower surface 8 of the dielectric board 4 by conductive tracks 9, disposed on the upper surface 6 and lower surface 8, and vias 10 which stretch from the upper surface 6 to the lower surface 8 of the dielectric board 4. The conductor tracks 9 and vias 10 comprise copper and provide the electrically conducting rewiring structure of the laminate substrate 3.

The semiconductor chip 2 has an active surface which includes integrated circuit devices and a plurality of chip contact pads 11. A flip chip contact 12, in this case a solder ball, is disposed between each chip contact pad 11 and an inner contact pad 5 located on the upper surface 6 of the laminate substrate 3. Therefore, the lateral arrangement of the inner contact pads 5 is essentially the same as, and corresponds to, the lateral arrangement of the chip contact areas 11. In the cross-sectional view of Figure 1, only two of the plurality of flip-chip contacts 12 are shown for clarity.

In the semiconductor package 1, the laminate substrate 3 is laterally larger than the semiconductor chip 2. As the outer contact areas 7 are disposed across the whole of the width and breadth of the lower surface 8 of the laminate substrate 3, the wiring structure provides a so-called "fan out" redistribution structure. This describes that the distance between adjacent outer contacts areas 7, known as the pitch, is greater than the pitch between adjacent inner contact areas 5.

The upper surface 6 and lower surface 8 of the dielectric board 4 also include a respective upper 13 and lower 14 solder resist layer. The solder resist layer 13 disposed on the upper surface 6 of the dielectric board 4 covers the conductor tracks 9 but leaves the inner contact areas 5 uncovered.

In the semiconductor package 1 of figure 1, the cavity formed between the active surface of the semiconductor chip 2 and the upper surface of the solder resist layer 13 is underfilled by underfill material 15. In this embodiment of the invention,

the underfill material comprises an epoxy-based underfill material with filler particles.

5 The second solder resist layer 14 disposed on the lower surface 8 of the dielectric board 4 of the laminate substrate 3 covers the conductor tracks 9 and the peripheral regions of the outwardly facing surface 16 of the outer contact areas 7. The lower solder resist layer 14, therefore, includes openings or apertures which are positioned in approximately the lateral
10 centre of each outer contact pad 7.

In a first embodiment of the invention, each of the plurality of outer contact pads 7 includes a depression 17 which is positioned in the outer face 16 of each of the outer contact
15 pads 7. A detailed view of an outer contact pad 7 according to the first embodiment of the invention, is also shown in Figure 8. Each of the pluralities of outer contact pads 7 and depressions 17 of the laminate substrate 3 are essentially the same. Each depression 17 has a base 18 which lies in a plane essentially parallel to the lower surface 8 of the dielectric board
20 4 and side walls 19 which lie in a plane essentially perpendicular to the base 18. Essentially is used in this context to include small deviations from an exactly parallel or perpendicular plane.

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Although this cannot be seen in the cross-sectional view of figure 1, each outer contact pad 7 is laterally essentially circular and the depression 17 is also laterally essentially circular. The depression 17 is positioned concentrically in
30 the lateral centre of the outer surface 16 of the contact pad 7. Each outer contact pad 7, therefore, comprises a thin base portion 20 and an annular protrusion 21. The annular protru-

sion 21 is positioned at the periphery of the base portion 20 of the contact pad 7.

5 The outwardly facing the surfaces 22, 16 of the outer contact pads 7 and, therefore, the outer surface of the annular protrusion 21 are covered by the solder resist layer 14. The depression 17, including the base 18 and inwardly facing side wall 19, remains free from the lower solder resist layer 14. The apertures positioned in the lower solder resist layer 14
10 are of essentially the same lateral size as the depressions 17 and which are located in the solder resist layer 14 in alignment with the depressions 17.

15 An external contact 23, in this case a solder ball, is disposed on each outer contact pad 7. The inner portion of each solder ball 23, i.e. the portion of the solder ball 23 facing towards the outer contact pad 7 and lower surface 8 of the laminate substrate 3, is disposed in the depression 17 of the outer contact pad 7. The annular protrusion 21, therefore,
20 surrounds the inner portion of the solder ball 23. The solder ball 23 is in mechanical contact with, and electrically connected to, the base 18 and side walls 19 of the depression 17.

25 The semiconductor package is depicted as mounted on and electrically connected to a higher level printed circuit board 36. A plurality of component contact areas 37 are disposed on the upper surface 38 of the printed circuit board 36 along with a plurality of conductor tracks (which are not illustrated in the figure). The conductor tracks enable the semiconductor package
30 1 to be accessed and to communicate with other electronic components mounted on the board 36.

Figure 2 depicts a portion of a laminate substrate 3 including an outer contact pad 24 according to a second embodiment of the invention. The outer contact pad 24 is disposed on the lower surface 8 of the dielectric board 4. The outer contact pad 24 also includes a depression 17 located in its outer surface 16. Similarly to the embodiment of the invention shown in figure 1, the depression 17 is positioned in approximately the lateral centre of the outer contact area 24. The outer contact pad 24 and the depression 17 are essentially circular and the depression 17 is located concentrically in the outer face 16 of the outer contact pad 24.

The depression 17 has a base 18 which lies in a plane essentially parallel to the plane of the lower surface 8 of the dielectric board 4. In the embodiment of the invention shown in Figure 2, the side wall 19 of the depression 17 further includes a step 25. The step 25 is concentrically positioned with respect to the base 18 and outer side surface 22 of the outer contact area 24. The step 25 is, therefore, an annular ring.

The depression 17 includes a protrusion 26 positioned in the edge formed between the base 18 and the side wall 19. The protrusion 26 has the form of an annular ring. The outer facing surface 27 of the protrusion 26 provides the step 25 in the side wall 19. The tread of the step 25 lies in a plane essentially parallel to the plane of the base 18. The side wall 19, therefore, has two portions, a lower portion and an upper portion. Each portion lies in a plane essentially perpendicular to the base 18. The lateral distance between opposing points on the lower portion is, therefore, smaller than the distance between opposing points on the upper portion of the side wall.

The depression 17 of the second embodiment of the invention can also be described as comprising two laterally circular depressions 27, 28. A first depression 27 is positioned in the outer surface 16 of the outer contact pad 24. The second depression 28 is laterally smaller than the first depression 27 and is located concentrically in the base of the first depression 27 which is located in the outer face 16 of the outer contact area 24. The remaining peripheral region of the base of the first depression 27 adjoins the upper portion of the side wall 19 of the first depression and provides the step 25.

A solder ball 23 is located in the depression 17 of the outer contact area 24 and is in contact with the base 18, side wall 19 and step 25 of the depression 17. The peripheral annular protrusions 26 and 21, therefore, surround the inner portion of the solder ball 23. The inner surfaces of the annular protrusions 26 and 21 are, therefore, in mechanical and electrical contact with the solder ball 23. The outer surface 16 of the protrusion 21 is covered by the solder resist layer 14. The solder ball 23 is, therefore, electrically connected to the outer contact pad 24.

A method to fabricate a plurality of outer contact pads 7, as shown in Figure 1, will now be described with reference to figures 3 to 8. Only one outer contact pad 7 is depicted in the portion of the laminate substrate 3 illustrated in Figures 3 to 8 for clarity. Although the process is described in terms of one outer contact pad, the process steps are carried out in parallel, i.e. essentially simultaneously, for all of the outer contact pads 7 located on the lower surface 8 of the dielectric board 4.

Figure 3 illustrates the first stage in the method and shows a portion of a laminate substrate 3. A plurality of precursor outer contact pads 29 are deposited on the lower surface 8 of the dielectric board 4 of the laminate substrate 3. The precursor outer contact pads 29 are laterally essentially circular and have a defined thickness. The precursor pads 29 have a lateral arrangement which is essentially the same as that desired for the outer contacts 23 of the semiconductor package. The lateral arrangement of the outer contacts, in this case solder balls, of the package is typically dictated by agreed industry standards.

Figure 4 shows the deposition of a first photoresist layer 30 on the lower surface 8 of the dielectric board 4. A photoresist material is a material which can be structured by photolithographic techniques. The first photoresist layer 30 has a thickness which is greater than the thickness of the precursor contact pad 29. The first photoresist layer 30 includes a plurality of through-openings or apertures 31. One aperture 31 is arranged on the lateral centre of each outer face 16 of the precursor contact pad 29.

The lateral size of the aperture 31 is smaller than that of the precursor contact pad 29 so that the peripheral regions of the outer surface 16 are covered by the photoresist layer 31 and the central area of the outer face 16 remains exposed from the photo resist layer 30. In this embodiment, the aperture is laterally circular and arranged concentrically on the outer surface 16 of the precursor outer contact pad 29.

Figure 5 shows the next stage in the fabrication process. In this step, the exposed portion of the precursor outer contact pad 29 is subjected to a chemical etching treatment as indicated by the arrows 32. Material is removed from the exposed area and a depression 17 is formed in the centre of the outer face 16 of the precursor contact pad 29. By control of the etching parameters, a depression 17 is formed which has a base 18 which lies in a plane essentially parallel to the lower surface 8 of the dielectric board 4 and a side wall 19 which lie in a plane essentially perpendicular to the base 18. The outer contact pad 7 is, therefore, formed which comprises a base portion 20 with a protruding annular ring 21 at its lateral periphery. The outer surface 16 of the protruding ring 21 is covered by the photoresist layer 30.

Figure 6 illustrates the next stage in the method. The first photoresist layer 30 is then removed and a second structured photoresist layer 33 is applied to the lower surface 8 of the dielectric board 4.

As can be seen in Figure 6, the second structured photoresist layer 33 comprises isolated portions 34 of photoresist which fill the depression 17 but leave the outer surface 16 of the protrusion 21 and the upper surface 8 of the dielectric board 4 exposed. The isolated protrusion 34 of the second photoresist layer 33 has a thickness which is greater than the depth of the depression 17. The isolated portions 34 of the second photoresist layer 33, therefore, protrude above the outer surface 16 of the periphery of the outer contact pad 7. The outer side wall of the protrusion is essentially perpendicular to the outer face 16.

Figure 7 illustrates the next stage in the method. A solder resist layer 14 is deposited on the lower surface 8 of the dielectric board 4. The solder resist layer 14 covers the lower surface 8 of the dielectric board 4, the outer side walls 22 and the outer face 16 of the protruding peripheral region of the outer contact pad 7. The solder resist layer 14, therefore, includes apertures 35 whose size and lateral arrangement corresponds to, and is essentially the same as, the protrusions 34 of the photoresist layer 33.

In the next stage of the process, as depicted in Figure 8, the second photoresist layer 33 is removed to leave the outer contact area 7 disposed on the lower surface 8 of the dielectric board. The contact pad 7 includes a depression 17 located in its approximate lateral centre which is exposed from the solder resist 14. The outer contact pad 7 includes a peripheral protruding annular ring 21 which is covered by the solder resist layer 14.

The outer contact pad 24 according to a second embodiment of the invention shown in Figure 2 is fabricated using a similar process which is not illustrated in the figures.

Essentially, the process of Figures 3 to 5 is carried out to produce a first depression 27 in the outer face 26 of the precursor outer contact area 29. Then a third structured photoresist layer is deposited on the lower surface 8 of the dielectric board which covers the peripheral regions of the protruding portion 21 of the first depression 17 and the peripheral regions of the base of the first depression.

A second etching step is then performed to form a second depression in the exposed central portion of the base of the first depression. After the photoresist has been removed, a depression 17 is formed in which the side wall 19 has a step.
5 A solder resist layer 14 is then deposited on the lower surface in a similar way to that illustrated in Figures 6 to 8 which leaves the inner surfaces of the depression exposed.

The laminate substrate 3 including the outer contact areas 7,
10 24 fabricated as shown in Figures 3 to 8 is then used in the assembly of semiconductor packages. Typically, the laminate substrate is fabricated in the form of a large board which includes a number of component positions arranged in rows and columns. A semiconductor package is assembled on each compo-
15 nent position.

Firstly, a semiconductor chip is mounted on the upper surface of each component position and electrically connected to the substrate. The electrical connections may be provided by flip
20 chip contacts in which case the active surface of the semiconductor chip faces the upper surface of the substrate. Alternatively, the electrical connections may be provided by bond wires. In this case, the passive surface of the chip is attached to the upper surface of the substrate by die attach ma-
25 terial.

The chip and electrical connections may then be encapsulated by an epoxy-based mold material in order to provide protection from mechanical stress and environmental damage. The individ-
30 ual packages are then singulated from the panel. The packages are tested and shipped to the user who typically mounts the package on a higher level circuit board such as a printed cir-

cuit board. The mechanical and electrical connection between the package and the PCB is provided by reflowing the solder balls.

Reference numbers

1	semiconductor package	27	first depression
2	semiconductor chip	28	second depression
3	laminate substrate	29	precursor contact pad
4	dielectric board	30	first photoresist layer
5	inner contact area	31	aperture
6	upper surface	32	arrow
7	outer contact area	33	second photoresist layer
8	lower surface	34	portion of second photore-
9	conductor track	sist layer	
10	via	35	aperture
11	chip contact pad	36	circuit board
12	flip chip contact	37	component contact area
13	upper the solder resist	38	upper surface
	layer		
14	lower the solder resist		
	layer		
15	underfill material		
16	outer face		
17	depression		
18	base		
19	side wall		
20	base portion		
21	annular protrusion		
22	outer surface		
23	solder ball		
24	second contact pad		
25	step		
26	protrusion		

Patent claims

1. A substrate (3) for an electronic component (1) comprising:

- 5 - a dielectric body (4) having an upper surface (6) and a lower surface (8);
- a plurality of inner contact pads (5) disposed on the upper surface (6);
- a plurality of outer contact pads (7;24) disposed on
- 10 the lower surface (8), each outer contact pad (7; 24) having an inner face and an outer face (16), the inner face being level and being in contact with the lower surface (8) of the dielectric body (4);
- an insulating layer (14) covering the lower surface (8)
- 15 of the dielectric body (4) and the peripheral regions (16) of the plurality of outer contact pads (7; 24);

wherein

a depression (17) is located in the outer face (16) of each of the plurality of outer contact pads (7; 24), each

20 depression (17) having a base (18) and at least one side wall (19), each depression (17) being located in the approximate lateral centre of the outer face (16) of the outer contact pad (7; 24).

25 2. A substrate (3) according to claim 1 characterised in that the depression (17) is concentrically positioned in the outer face (16) of each of the outer contact pads (7; 24).

30 3. A substrate (3) according to claim 1 or claim 2 characterised in that the depression (17) is laterally essentially circular.

4. A substrate (3) according to one of claims 1 to 3
characterised in that
the side wall (19) of each depression (17) further com-
5 prises at least one step (25).

5. A substrate (3) according to claim 4
characterised in that
each depression (17) is laterally smaller at the base
10 (18).

6. A substrate (3) according to claim 4 or claim 5
characterised in that
the step (25) is concentrically positioned in the side
15 wall (19).

7. A substrate (3) according to one of the previous claims
characterised in that
the plurality of outer contact pad (7; 24) comprises cop-
20 per or a copper alloy.

8. A substrate (3) according to one of the previous claims
characterised in that
the dielectric body (4) comprises BT or FR4.
25

9. A substrate (3) according to one of the previous claims
characterised in that
the substrate (3) further comprises a plurality of solder
balls (23), a solder ball (23) being disposed on each of
30 the outer contact pads (7; 24), wherein at least part of
the solder ball (23) is located within the depression (17)
of each of the outer contact pads (7; 24) and the side

wall (19) of the depression (17) laterally surrounds at least part of the solder ball (23).

10. An electronic component (1) comprising:

- 5 - the substrate (3) of one of claims 1 to 8;
- a semiconductor chip (2) having an active surface and chip contact pads (11) positioned on the active surface, the semiconductor chip (2) being mounted on the upper surface (6) of the substrate (3); and
- 10 - a plurality of electrical connections (12) electrically connecting the semiconductor chip (2) to the inner contact pads (5) positioned on the upper surface (6) of the substrate (3);
- a plurality of solder balls (23), wherein a solder ball
- 15 (23) is disposed on each of the outer contact pads (7; 24), and wherein at least part of the solder ball (23) is located within the depression (17) of each of the outer contact pad (7; 24), and wherein the side wall (19) of the depression (17) laterally surrounds at
- 20 least part of the solder ball (23).

11. An electronic component (1) according to claim 10

characterised in that

- the electrical connections (12) comprise solder bumps or
- 25 bond wires.

12. An electronic configuration comprising:

- the electronic component (1) of claim 10 or claim 11;
 - a circuit board (36) comprising a plurality of component contact areas (37) on its upper surface (38);
- 30 wherein the electronic component (1) is mounted on the circuit board (36) by the plurality of solder balls (23),

a solder ball (23) being disposed between each outer contact pad (7; 24) of the substrate (3) of the electronic component (1) and a component contact area (37) of the circuit board (36).

5

13. A method of fabricating a substrate (3) for an electronic component (1):

- providing a dielectric body (4) having an upper surface (6) and a lower surface (8);
 - 10 - forming a plurality of precursor outer contact pads (29) on the lower surface (8) of the dielectric body (4);
 - forming a plurality of depressions (17), a depression (17) being formed in the approximate lateral centre of the outer face (16) of each of the plurality of precursor outer contact pads (29); and
 - 15 - applying an insulating layer (14) to the lower surface (8) of the dielectric body (4), the plurality of depressions (17) remaining uncovered by the insulating layer (14).
- 20

14. A method of fabricating a substrate (3) according to claim 13

characterised in that

25

the plurality of depressions (17) is formed by:

- applying a first structured photoresist layer (30) to the lower surface (8) of the dielectric body (4), wherein the central portion of the precursor outer contact pads (29) remains free from the first photoresist layer (30);
- 30

- forming a depression (17) in the uncovered portion of each of the precursor outer contact pad (29) by an etching process;
- removing the first photoresist layer (30);
- 5 - applying a second photoresist layer (33), the second photoresist layer (33) essentially covering the depressions (17) in the outer contact pads (7; 24); and
- after the insulating layer (14) is applied to the lower surface (8) of the dielectric body (4), removing the
- 10 second photoresist layer (33) to expose the depressions (17) in the outer contact pads (7; 24).

15.A method of fabricating a substrate (3) according to claim 13 or claim 14, further comprising the step of:

- 15 forming a step (25) in the side wall (19) of each of the depressions (17).

16.A method of fabricating a substrate (3) according to claim 15

20 characterised in that

the step (25) in the side wall (19) is formed by:

- applying a third structured photoresist layer to at least the depressions (17), wherein the central portion of each of the depressions (17) remains uncovered by
- 25 the third photoresist layer;
- forming a second depression (28) in the uncovered portion of each of the outer contact pads (7; 24) by an etching process; and
- removing the third structured photoresist layer.

30

17.A method of fabricating a substrate (3) according to one of claims 13 to 16

characterised in that
the etching process is performed by a chemical etching or
a plasma etching technique.

- 5 18. A method of assembling an electronic component (1) comprising the steps of:
- providing the substrate (3) of one of claims 1 to 8;
 - providing a semiconductor chip (2) having an active
10 surface and a plurality of chip contact pads (11) positioned on the active surface;
 - mounting the semiconductor chip (2) on the upper surface (6) of the substrate (3);
 - making electrical connections (12) between the chip
15 contact pads (11) and the inner contact pads (5) positioned on the upper surface (6) of the substrate (3);
and
 - placing a solder ball (23) on each outer contact pad
(7; 24), wherein at least part of the solder ball (23)
20 is located within the depression (17) of each of the
outer contact pad (7; 24) and the side wall (19) of the
depression (17) laterally surrounds at least part of
the solder ball (23).

19. A method of assembling an electronic configuration comprising the steps of:
- 25
- providing the electronic component (1) of claim 10 or claim 11;
 - providing a circuit board (36) comprising a plurality
of component contact areas (37) on its upper surface
30 (38);
 - mounting the electronic component (1) on the circuit board (36) by the plurality of solder balls (23), a

solder ball (23) being disposed between each outer contact pad (7; 24) of the substrate (3) of the electronic component (1) and a component contact area (37) of the circuit board (36); and

- 5 - performing a solder reflow process.

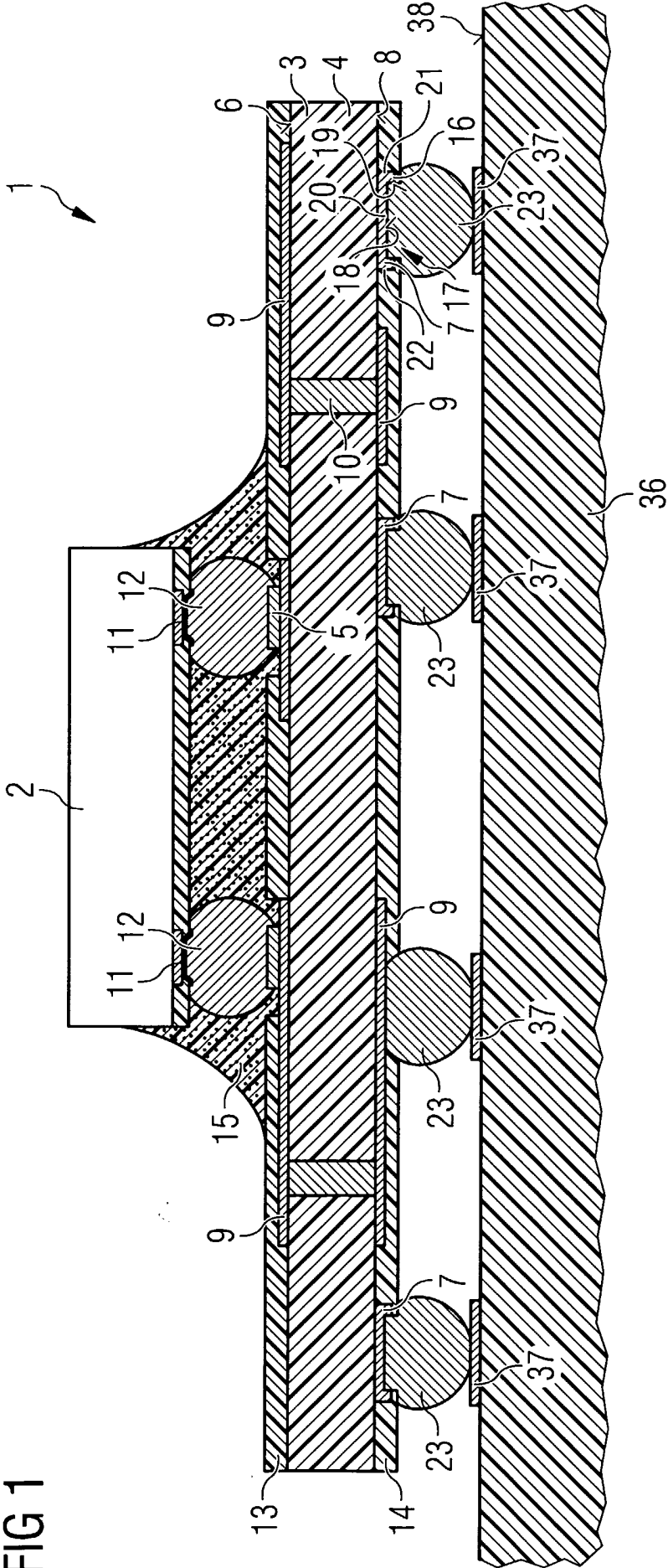


FIG 1

FIG 2

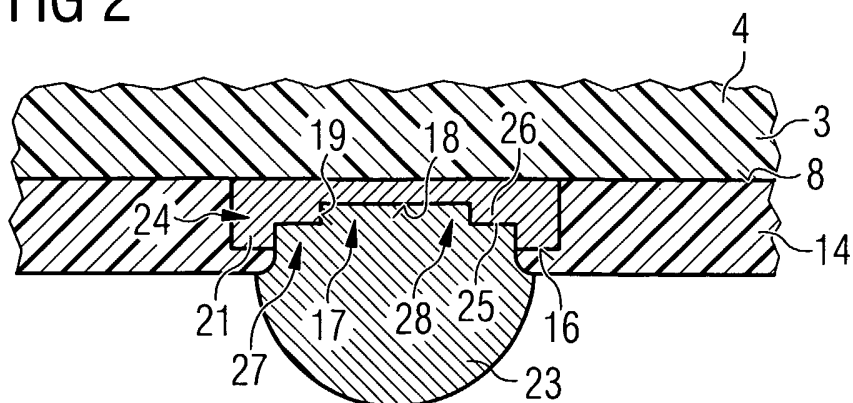


FIG 3

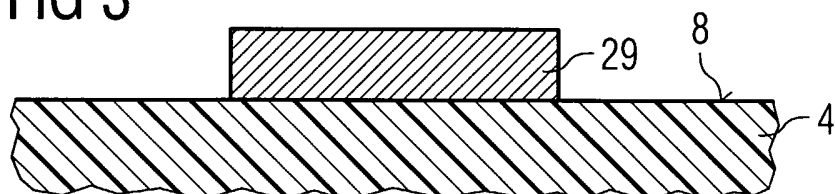


FIG 4

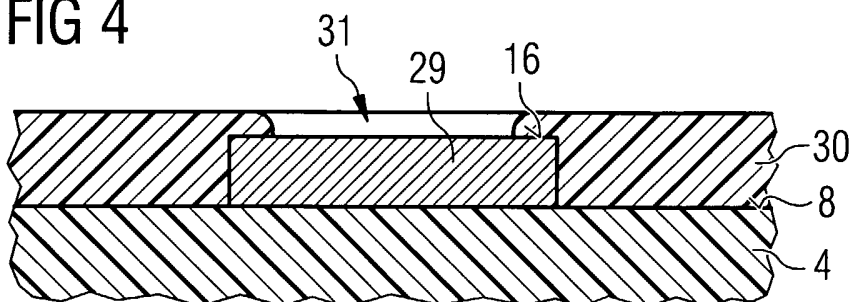


FIG 5

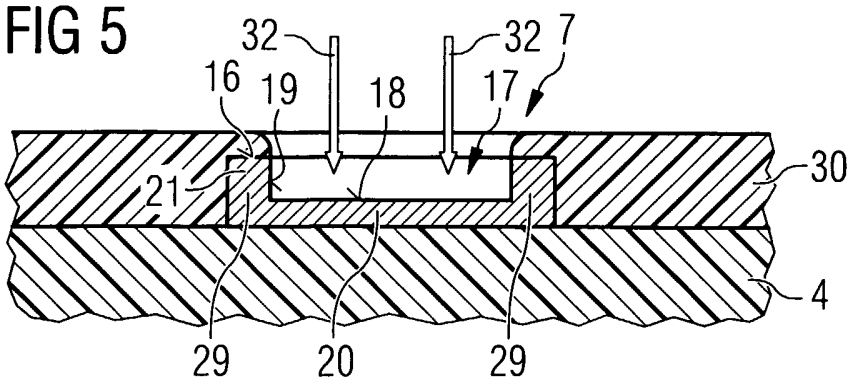


FIG 6

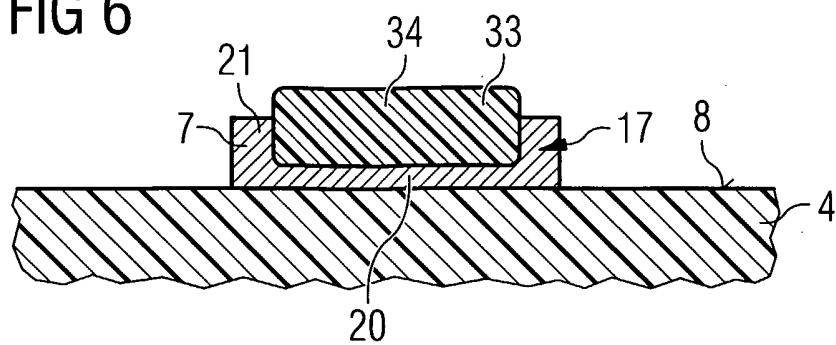


FIG 7

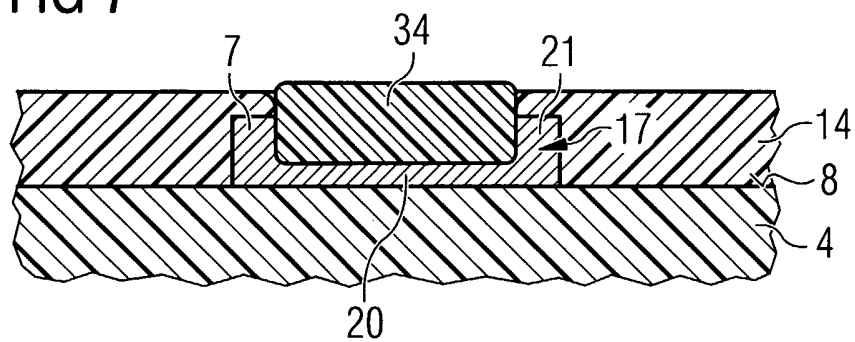
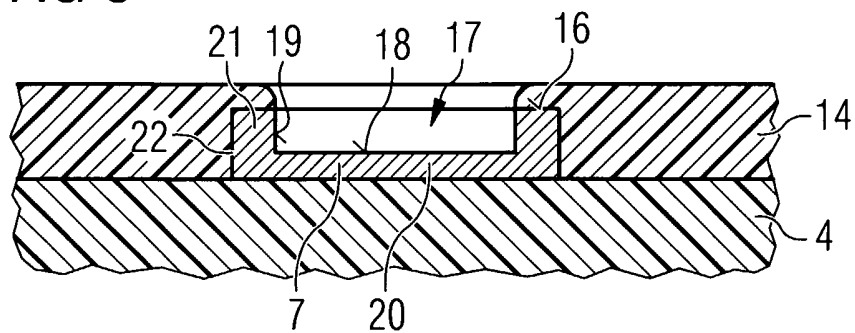


FIG 8



INTERNATIONAL SEARCH REPORT

Internat Application No
PCT/IB2005/000672

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L23/498

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/188836 A1 (KEY CHUNG C ET AL) 30 September 2004 (2004-09-30) the whole document -----	1-19
X	US 2005/017375 A1 (KO SHUN-FU ET AL) 27 January 2005 (2005-01-27) the whole document -----	1-19
A	DE 101 38 042 A1 (INFINEON TECHNOLOGIES AG) 21 November 2002 (2002-11-21) paragraph '0009! -----	4-6
A	US 5 260 518 A (TANAKA ET AL) 9 November 1993 (1993-11-09) the whole document -----	4-6



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Patent family members are listed in annex.

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Date of the actual completion of the international search

29 September 2005

Date of mailing of the international search report

07/10/2005

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Internationa I Application No
PCT/IB2005/000672

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