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[54] **LOGARITHMIC AMPLIFIER**
6 Claims, 7 Drawing Figs.

[52] **U.S. Cl.** **307/230,** 307/229, 328/145
[51] **Int. Cl.** **G06g 7/12**
[50] **Field of Search** 307/230, 229; 328/145; 235/197, 150.53

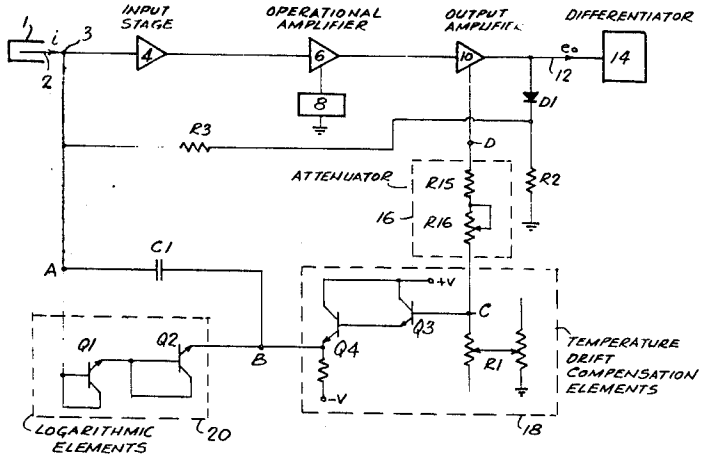
[56] **References Cited**

UNITED STATES PATENTS

3,140,408	7/1964	May	307/229
3,152,250	10/1964	Platzer	328/145
3,329,836	7/1967	Pearlman et al.	328/145
3,369,128	2/1968	Pearlman	307/229
3,393,369	7/1968	Embley	307/229

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ABSTRACT: A logarithmic amplifier capable of operating with input currents as low as 10^{111} amps having a capacitor feedback loop for smoothing out fluctuations at very low current inputs and a second feedback loop consisting of a resistor and diode to switch in the resistor at very low outputs to limit the time constant of the parallel connection of the feedback capacitor and logarithmic transistor elements to reduce output fluctuations at switch-on.



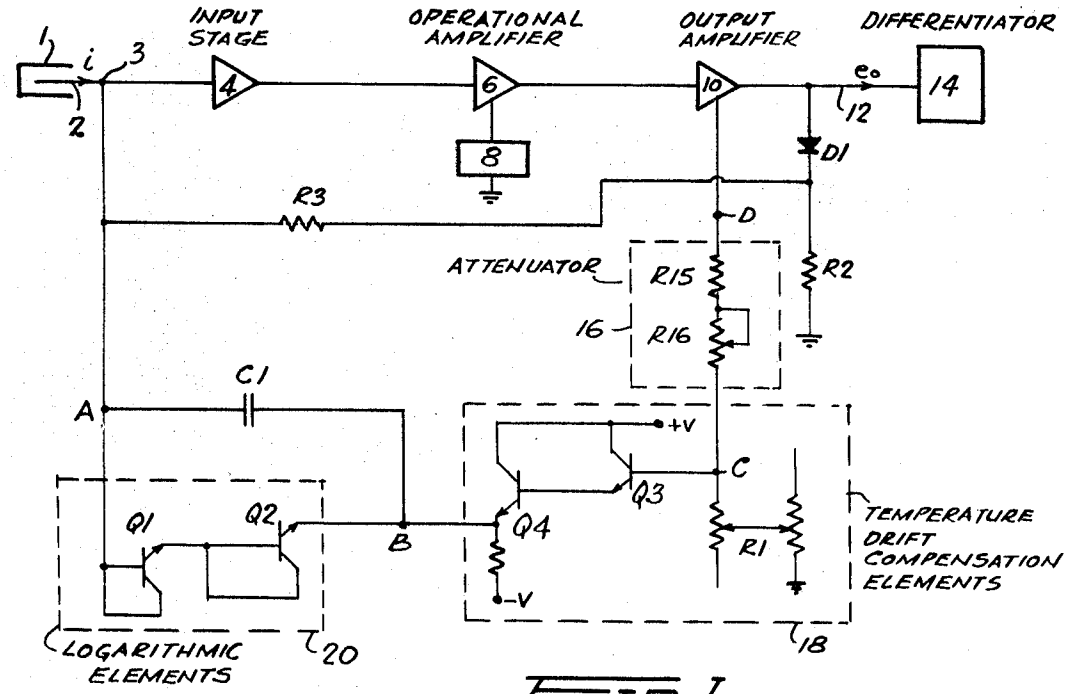


Fig. 1.

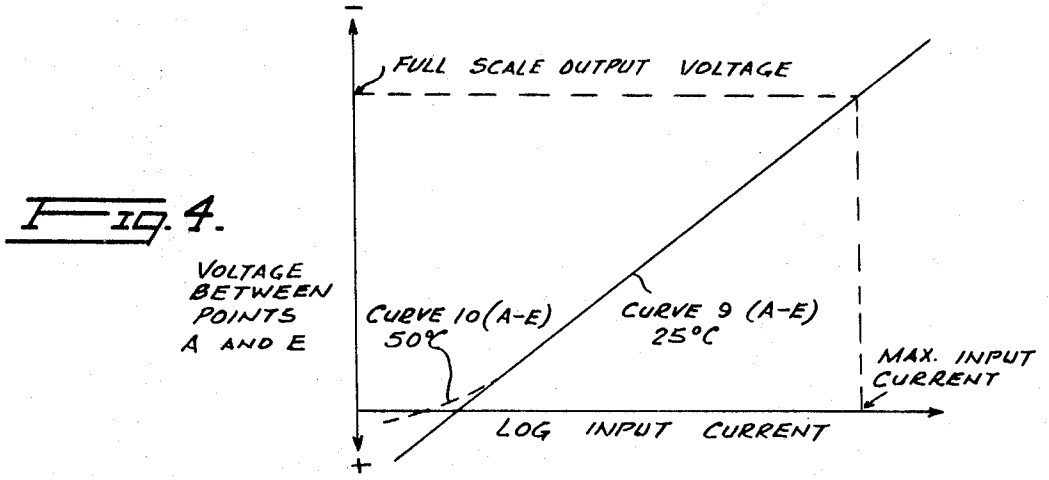


Fig. 4.

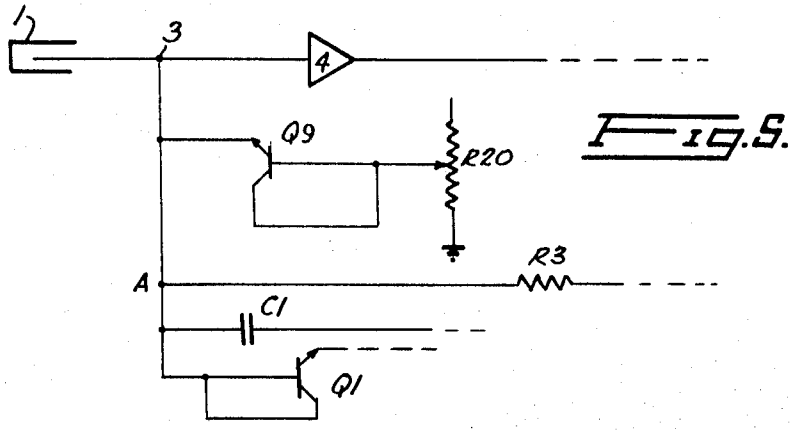


Fig. 5.

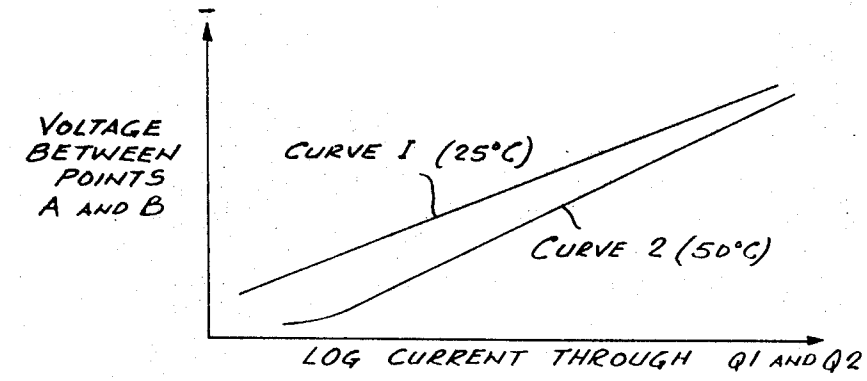


Fig. 2a.

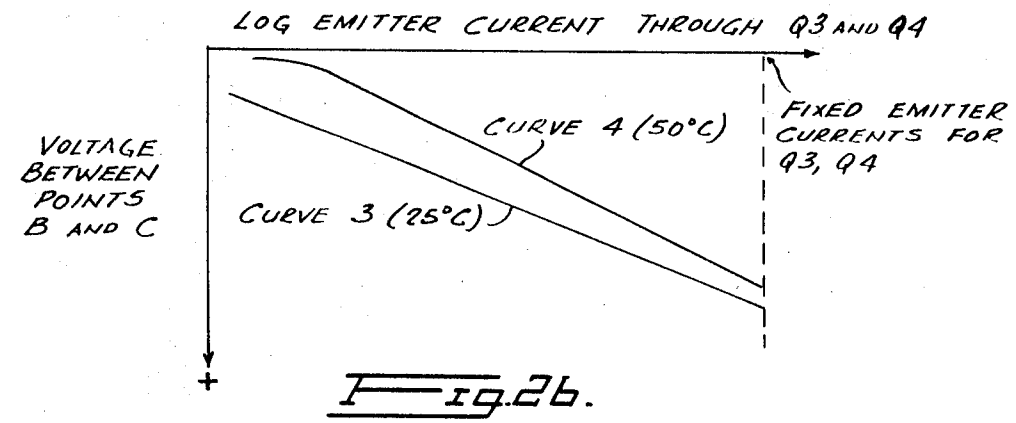


Fig. 2b.

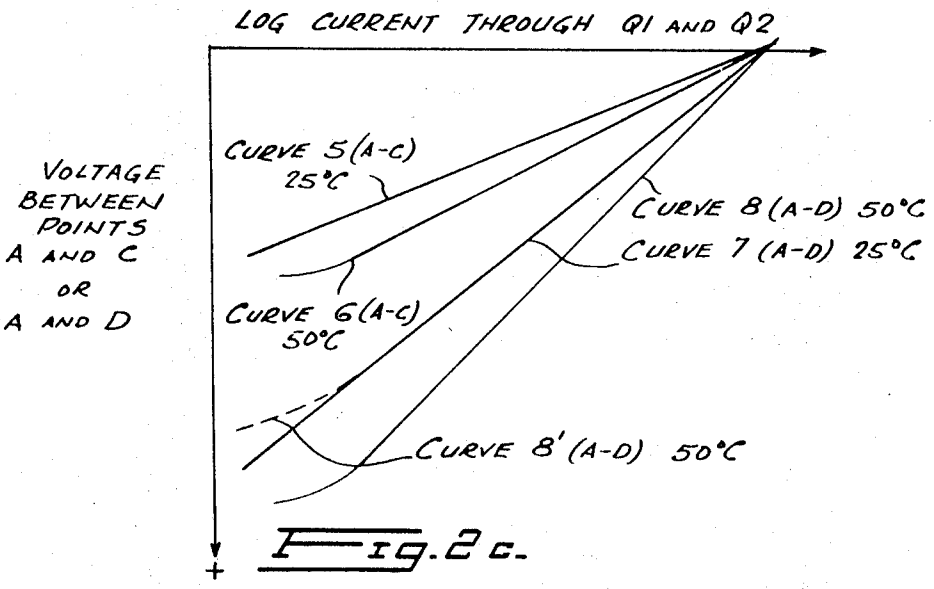


Fig. 2c.

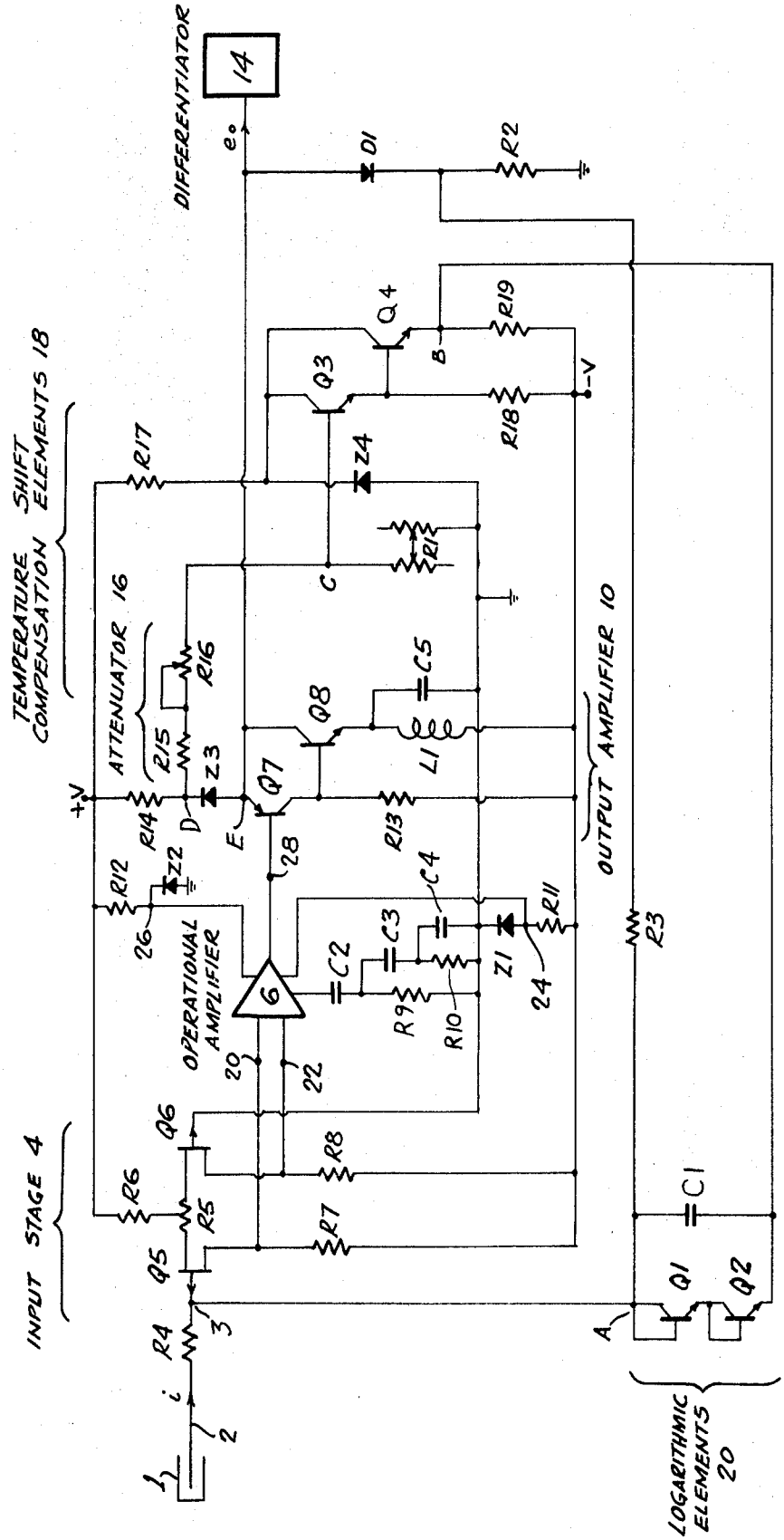

DIFFERENTIATOR
14
e₀
D1
R2
Q4
R19
B
Q3
-V
R18
Z4
R17
C
R21
TEMPERATURE COMPENSATION SHIFT ELEMENTS 18
ATTENUATOR 16
R16
R15
Z3
C5
Q8
L1
+V
R14
D
Q7
E
R13
OUTPUT AMPLIFIER 10
28
R12
Z2
C4
R11
26
C3
C2
Z1
24
R23
OPERATIONAL AMPLIFIER
6
R9
R10
20
22
Q6
R8
C1
R6
R5
R7
Q5
Q1
Q2
INPUT STAGE 4
R4
3
A
i
2
LOGARITHMIC ELEMENTS 20

FIG. 3.

LOGARITHMIC AMPLIFIER

This invention relates to a logarithmic amplifier, and more particularly, it relates to a logarithmic amplifier suitable for use with an ionization chamber such as is commonly used with nuclear reactors.

Logarithmic amplifiers have in the past been built in various forms but their design for use with low-input currents, for example from 10^{111} to 10^{14} amperes, has presented a number of problems. Prior art amplifiers have commonly needed ovens to maintain at least some of their components at constant temperature for stability, moreover, they have required large numbers of adjustments and trims in use; and they have typically given rise to noise and drift problems.

Accordingly, it is an object of the present invention to provide a logarithmic amplifier suitable for use with an input current ranging from approximately 10^{111} to 10^{14} amperes, which amplifier requires little if any adjustment in use, and in which no oven is required, and in which noise and drift problems are reduced.

Further objects and advantages of the invention will appear from the following disclosure, in which the embodiment discussed is presented for illustrative purposes, the scope of the invention being defined primarily by the appended claims.

In the drawings:

FIG. 1 is a schematic, partly in block diagram form, of a logarithmic amplifier according to the present invention;

FIG. 2 illustrates various voltage-current curves for portions of the circuit of FIG. 1;

FIG. 3 is a more detailed circuit representation of the device of FIG. 1;

FIG. 4 shows output voltage curves for the circuit of FIGS. 1 and 3; and

FIG. 5 shows a modification of the circuit of FIG. 1.

Referring firstly to FIG. 1, there is shown a schematic, partly in block form, of a logarithmic amplifier in accordance with the present invention. An input current *i* from an ionization chamber shown diagrammatically at 1 is directed over a cable 2 to the input terminal 3 of an insulated gate field effect transistor input stage 4. The output signal from the input stage 4 is directed to a conventional operational amplifier 6, to which is connected a conventional stabilizing network 8. The output from the operational amplifier 6 is next directed to a cascode follower output amplifier 10.

Output amplifier 10 provides a low impedance output into an output cable 12 to a differentiator shown in block form at 14. The differentiator 14 is commonly used in conjunction with nuclear reactors to differentiate the output signal e_o from the logarithmic amplifier and to shut down the reactor as a safety measure when such output signal (which is a measure of the current from the ionization chamber 1) increases too rapidly. The cascode follower output amplifier 10 is used to provide a low-output impedance because the output cable 12 will often be relatively long, with consequent high capacitance, and the differentiator 14 will normally include a series capacitance. The output signal must be able to charge the capacitances quickly in order to avoid errors and lags in the response of the differentiator 14, and thus a low-output impedance for the logarithmic amplifier is needed.

A feedback loop from the output amplifier 10 is provided, through the series combination of an attenuator 16 (containing resistors R15 and R16 in series, resistor R16 being adjustable), a temperature drift compensation network generally indicated at 18, and logarithmic elements generally indicated at 20, back to the input terminal 3 of the field effect transistor input stage 4. The logarithmic elements 20 consist of the series-connected emitter-base junction diodes of two silicon planar transistors Q1 and Q2. The collectors of transistors Q1 and Q2 are tied to their respective bases to reduce the effect of the body resistance of the base regions of these transistors.

The temperature compensation network 18 includes a pair of transistors Q3 and Q4 having the same characteristics as transistors Q1 and Q2 but connected in opposition thereto. The emitter currents of transistors Q3 and Q4 are set so that the average emitter current is approximately equal to the maximum current expected through the base-emitter diodes of transistors Q1 and Q2. Transistors Q3 and Q4 thus serve to cancel the "constant current" temperature drift of transistors Q1 and Q2. A temperature compensation resistor R1 is provided to compensate for the variation in temperature characteristics of transistors Q1 and Q2 with respect to the current flowing through these transistors. A, B, C and D are reference points.

FIG. 2 illustrates the principles of the temperature compensation network 18 in more detail. FIG. 2 plots voltage against the logarithm of the current through the feedback loop, with reference to the various points A, B, C, and D of FIG. 1. In FIG. 2A, curve 1 plots the voltage between points A and B at one temperature, e.g., 25° C., while curve 2 plots the voltage between points A and B at another higher temperature, e.g., 50° C. It will be noted that a change in temperature causes the voltage characteristics of transistors Q1 and Q2 to shift, and that a two-component correction will bring the two curves 1 and 2 back into coincidence (so that there will be no variation with temperature). The first correction needed is a translation of the curves so that they will intersect near the current range in question, and the second correction needed is a rotation about the intersection point (change in slope) of one of the curves so that the two curves will then coincide.

The first correction component is supplied by transistors Q3 and Q4. FIG. 2B plots voltage between points B and C as a function of the emitter currents of transistors Q3 and Q4, curve 3 being the 25° C. line and curve 4 being the 50° C. line, and the emitter currents of transistors Q3 and Q4 being set at the value indicated by the dotted line of FIG. 2B. To obtain the voltage between points A and C as a function of current through transistors Q1 and Q2, the voltage values of curves 3 and 4 at the fixed emitter currents of transistors Q3 and Q4 are added to curves 1 and 2 respectively, resulting in curves 5 and 6 respectively of FIG. 2C. Curves 7 and 8 of FIG. 2C are similar to curves 5 and 6 but show the voltage between points A and D instead of points A and C, curve 8 being plotted in the absence of the effect of temperature compensation resistor R1.

When the effect of resistor R1 is taken into account, curve 8 is rotated, i.e., its slope is changed, with the new result being shown as curve 8' in FIG. 2C. Thus, resistor R1 supplies the second correction component needed for temperature compensation.

The feedback network of the logarithmic amplifier illustrated in FIG. 1 also includes a time-constant capacitor C1 shown connected across the logarithmic elements Q1 and Q2. Capacitor C1 could of course be connected directly between the output of cascode follower amplifier 10 and terminal 3, but location of capacitor C1 as shown is more convenient from the point of view of routine construction and operation of the circuit.

The reason for the presence of time constant capacitor C1 is as follows. When the output current from the ionization chamber 1 is at a low level, for example, 10^{111} amperes, then normal statistical variations in the ionization measured in the ionization chamber will give rise to wide fluctuations in the current *i* therefrom. If such fluctuations in the current *i* were not smoothed the differentiator 14 would trigger safety devices (not shown) unnecessarily often, and the nuclear reactor (not shown) would be shut down at undesired times. Therefore, the fluctuations of current *i* at low current levels are averaged or filtered with the smoothing circuit formed by capacitor C1 and the resistance of transistors Q1 and Q2. At higher current levels, the statistical fluctuations in current *i* are much smaller in relation to the average current, so that little filtering is needed. However, less filtering occurs at higher levels because the resistance of logarithmic elements Q1 and Q2 drops greatly with an increase in current through these elements. If the resistance of the series base-emitter diodes of transistors Q1 and Q2 is denoted by R, then resistance R decreases as the current through transistors Q1 and Q2 increases, and hence the time constant RC1 of the filter con-

stituted by the combination of transistors Q1 and Q2, and capacitor C1, becomes smaller. At relatively high-input currents, the resistance R of the logarithmic elements Q1 and Q2 is so low that the effect of capacitor C1 is of little significance.

Although capacitor C1 is primarily intended as a smoothing capacitor, providing, with logarithmic elements Q1 and Q2 a variable (with input current) time constant, the choice of value for capacitor C1 is also affected by another factor. In practice, the input cable 2 from the ionization chamber 1 will normally be relatively long and hence will possess considerable capacity and it is found that the higher this capacity, the more high frequency amplifier noise there will be at the output of the logarithmic amplifier. However, it is also found that a higher value for feedback capacitor C1 assists in reducing the amplifier noise in the output signal.

Referring again to FIG. 1, it will be noted that there is provided a feedback path consisting of a diode D1, and resistors R2 and R3.

The purpose of this arrangement is to compensate for the following phenomenon: if the nuclear reactor (not shown) generating the ionization current has been shut down, the input current i will be very small. As previously mentioned, at very low signal currents the resistance of logarithmic elements Q1 and Q2 becomes extremely high. Then, after the reactor is restarted, the input current i increases and in the absence of resistor R3, would charge capacitor C1 for a period of time determined by time constant RC1, where R is as mentioned the equivalent resistance of logarithmic elements Q1 and Q2. Since R is large at this time, an undesirably long period of time would be required for the output of the logarithmic amplifier to reach equilibrium. If a fixed resistance having a lower value than that of logarithmic elements Q1 and Q2 were connected across capacitor C1 during the low-input current stages, then capacitor C1 would be charged by the input current to a voltage limited by this lower resistance and hence, upon restoration of the signal from the ionization chamber, would reach equilibrium much sooner. Such lower resistance is provided by resistor R3 which is connected into the feedback circuit when diode D1 becomes forward biased, this occurring when the output signal at cable 12 becomes sufficiently low.

In the exemplary circuit shown in FIG. 1 (and illustrated in more detail in FIG. 3, to be referred to shortly) the output voltage e_o at cable 12 varies from −5 volts at full scale input current (approximately 10^{14} amperes) to 0 volts at low-input currents (10^{111} amperes). At input currents below 10^{111} amperes, the output voltage e_o begins to go positive, i.e., reverses sign. Diode D1 then becomes forward biased and connects resistor R3 across capacitor C1 as mentioned. When the output voltage e_o begins to come back on scale, i.e., decreases below zero volts, diode D1 becomes reverse biased and disconnects resistor R3, so that logarithmic feedback through elements Q1 and Q2 is restored.

Resistor R3 may be thought of as a maximum time constant limiting resistor, limiting the maximum time constant of the feedback path to a selected value at times when the resistance R of logarithmic elements Q1 and Q2 approaches infinity. The switching-in of resistor R3 at very low-input currents has the further advantage that it reduces sudden jumps in the output voltage e_o that would otherwise tend to occur (because of the normal circuit characteristics of the logarithmic elements, Q1 and Q2, and the capacitor C1, in parallel) during the initial turn-on period. Sudden jumps in the voltage e_o are undesirable except where they indicate a danger condition in the reactor, because such sudden jumps will cause the differentiator 14 to provide a large output to trigger safety devices (not shown) to shut down the reactor.

The actual time constant of the feedback loop at times when diode D1 is forward biased and the resistance R of elements Q1 and Q2 approaches infinity, may be shown to be C1R1R3/(R1+R15+R16). This assumes that the gain of operational amplifier 6 is very high, so that input terminal 3 (reference point A) is very nearly at ground potential. It may be noted that the resistor R3, instead of being connected as shown, could be connected across capacitor C1 (with its value changed to the fraction R1/(R1+R15+R16) of its previous value, in order to maintain the same time constant). However, R3 is placed as shown, so that as few components as possible are utilized at very low currents, and so that as large a switching voltage as possible is available for switching diode D1.

A more detailed schematic of the logarithmic amplifier of FIG. 1 is presented in FIG. 3. In FIG. 3, the input amplifier 4 is shown as including two insulated gate field effect transistors Q5 and Q6 connected in a differential amplifier configuration. These transistors are of the *p*-channel type. The input cable 2 is connected through an input resistance R4 to the gate of transistor Q5, the gate of transistor Q6 being grounded. The source terminals of transistors Q5, Q6 are connected together through a balancing potentiometer R5, the tap of which is connected through a resistance R6 to a supply voltage +v., The drain terminals of transistors Q5 and Q6 are connected through resistors R7 and R8 to a supply voltage −v., and are also connected to input terminals 20 and 22 of the operational amplifier 6, which is shown as a differential amplifier in FIG. 3.

It will be appreciated that the input amplifier 4 need not be a differential amplifier as shown, but use of a differential input amplifier is convenient because in this way, the temperature drift in one field effect transistor Q5 is cancelled by the temperature drift in the other field effect transistor Q6. In addition, extra gain is achieved by providing differential inputs into the operational amplifier 6.

The operational amplifier 6 includes a stabilizing network consisting of capacitors C2, C3 and C4 and resistors R9 and R10. This network, which is conventional in design, stabilizes the operational amplifier over large changes in feedback due to the changes in resistance of the logarithmic elements Q1 and Q2. Power for the operational amplifier 6 is provided from terminal 24, which is connected to a zener diode Z1 leading to ground, and to a resistor R11 connected to the −v. supply. Power for the amplifier 6 is also provided from a terminal 26 which is connected to a zener diode Z2 connected to ground and to a resistor R12 connected to the +v. supply.

The operational amplifier 6 includes an output terminal 28 connected to the input of the cascode follower output amplifier 10, which is shown as including transistors Q7 and Q8. The collector of transistor Q7 is connected to the base of transistor Q8 and is also connected through a resistor R13 to the −v. supply, while the emitter of transistor Q7 is connected to the collector of transistor Q8. The emitter of transistor Q8 is connected through an inductor L1 to the −v. supply and through a capacitor C5 to ground.

The output signal from output amplifier 10 is taken at the emitter of transistor Q7. This output is directed to cable 12 and is also directed through diode D1, and through resistor R3 when diode D1 is turned on, to the collector of logarithmic element Q1. Resistor R2 enables diode D1 to become forward biased when the output signal e_o begins to go positive.

Connected to the emitter of transistor Q7 is a voltage divider chain consisting of zener diode Z3 and resistors R14, R15, R16 and R1. Zener diode Z3, which is connected between the emitter of transistor Q5 and resistor R14 (R14 in turn being connected to the +v. supply) provides a potential rise, i.e., in effect acts as a simple battery, in order that full scale output voltage will be obtained at the maximum input current and zero output voltage will be obtained at the minimum input current. The effect of zener diode Z3 is shown in FIG. 4, which plots the voltage between points A and E, point E being the point at which the output voltage is taken. (It will be recalled that point A is virtually at ground potential). Output voltage curves 9 and 10 appear in FIG. 4, and these curves are the same as curves 7 and 8′ respectively of FIG. 2C, but with the latter curves shifted upwardly by virtue of zener diode Z3, so that maximum and minimum output voltages will occur at maximum and minimum input currents respectively.

Resistor R14 acts primarily as a load for transistor Q7, while resistors R15 and R16 act, as mentioned, as an attenuator to assist in controlling the amount of feedback around the feedback loop. In particular, resistor R16 is used to set the desired span of measuring current range. Resistor R1 compensates for some of the temperature drift in logarithmic elements Q1 and Q2, as discussed.

The junction between resistors R16 and R1 is connected to the base of transistor Q3, and the emitter of transistor Q3 is connected in turn to the base of transistor Q4, the collectors of both these transistors being connected to the cathode of zener diode Z4 which controls the collector voltage of transistors Q3 and Q4. Zener diode Z4 is connected between ground and a resistor R17 which is connected to the +v. supply. The emitters of transistors Q3 and Q4 are connected through resistors R18 and R19 to the −v. supply. The emitter of transistor Q4 is also connected to the emitter of logarithmic element Q2, the base and collector of logarithmic element Q2 being connected in turn to the emitter of logarithmic element Q1, and the base and collector of logarithmic element Q1 being connected to input terminal 3.

In practice, the circuit shown in FIG. 3 has been found to operate satisfactorily with the following component values and types, the transistor and diode types being listed in standard notation:

Transistors	
Q1, Q2, Q3, Q4, Q8	2N1711
Q5, Q6	2N3608
Q7	2N2905
Diodes	
D1	FD300
Z1, Z4	1N429
Z2	1N716A
Z3	651C4
Resistors	
R1	2K temperature-compensating resistor
R2, R4, R13	10K
R3	10^{11} ohms
R5, R16	5K
R6, R9	6.8K
R7, R8	26K
R10, R14	1.8K
R11	820 ohms
R12	220 ohms
R15	5.6K
R17	680 ohms
R18, R19	selected for full scale input current
Capacitors	
C1	4,700 pf.
C2	1.0 μf.
C3	0.22 μf.
C4	0.047 μf.
C5	1,200 pf.
Inductor L1	1 mh.
Amplifier 1	Fairchild-type WA702 DC amplifier
Voltages +V and −V	+15 volts and −15 volts

With the values as noted above, the logarithmic amplifier described covers the range from 10^{111} to about 10^{14} amperes input current, with the output voltage e_o at cable 12 ranging from 0 volts at the low-range input current to −5 volts at about 10^{14} amperes current.

With the circuit values shown, the drain currents for the field effect input transistors Q5 and Q6 were held at about 0.5 milliamperes, i.e., to a value at which the temperature drift in characteristics of these transistors was low.

It may be noted that more than two logarithmic elements in series could be used, and this would naturally result in a higher voltage across the logarithmic elements, which in a sense is desirable since this tends to swamp the drift in the input amplifier 4. However, it is found that with too many logarithmic elements in series, their impedance becomes high, particularly at low-input currents, and it is then found that the time constant constituted by the product of the resistance of the series logarithmic elements and the capacitance of capacitor C1 becomes too high, degrading the response of the device. The value of capacitor C1 must therefore be lowered, but this causes an undesirably high degree of amplifier output noise when a long input cable 2 from the ionization chamber 1 is used. It is therefore found that two logarithmic elements in series provide a good compromise and lead to efficient operation of the circuit.

If desired, a low current correction facility may be built into the device, as shown in FIG. 5. In FIG. 5, a transistor Q9 has been inserted, biased from a potentiometer R20, to add a very low correction current to the current flowing through logarithmic elements Q1, and Q2, to improve their linearity at values of input current i towards the lower end of the range.

We claim:

1. A logarithmic amplifier for providing an output signal proportional to the logarithm of an input current signal within a range extending down to approximately 10^{111} amps, said amplifier comprising:

a. signal input means for said input signal,

b. amplifier means having amplifier input means, and having amplifier output means for said output signal,

c. said amplifier input means being connected to said signal input means,

d. logarithmic element feedback means coupled between said amplifier output means and said signal input means,

e. capacitor feedback means coupled between said amplifier output means and said signal input means for smoothing out input signal fluctuations at the lower end of said range,

f. and a passive circuit consisting of a combination of

i. a maximum time constant limiting resistance

ii. and switch means operative in response to a predetermined level of said output signal corresponding to an input signal at the extreme lower end of said range,

g. said passive circuit being coupled between said amplifier output means and said signal input means, said switch means being operative to insert said time constant limiting resistance in circuit between said amplifier output means and said signal input means to limit the time constant of the parallel connection of said logarithmic element feedback means and said capacitor feedback means upon occurrence of said predetermined level of said output signal.

2. A logarithmic amplifier according to claim 1 wherein said logarithmic element feedback means comprises a pair only of logarithmic elements, said logarithmic elements being transistors with the emitter-base junctions of said transistors connected in series, and each of said transistors having its collector connected to its base.

3. A logarithmic amplifier according to claim 2 including temperature compensation means connected in series with said pair of transistors, said temperature compensation means comprising:

h. a further pair of transistors having their emitter-base junctions connected in series with the emitter-base junctions of said first mentioned pair of transistors to provide a first temperature dependent compensating variation in feedback between said amplifier output means and said signal input means (a), and

i. temperature dependent resistance means connected to said further pair of transistors to provide a second temperature dependent compensating variation in feedback between said amplifier output means and said signal input means (a).

4. A logarithmic amplifier according to claim 3 wherein said signal input means (a) is a differential amplifier including a pair of insulated gate field effect transistors as input elements, said input signal being applied to the gate of one of said field effect transistors, and the gate of the other of said field effect transistors being grounded.

5. A logarithmic amplifier for providing an output voltage proportional to the logarithm of an input current over a range of input currents varying from a predetermined low value at least as low as approximately 10^{-11} amps to values greater than said predetermined low value, said output voltage having a predetermined level when said input current has said low value, said amplifier comprising:

a. signal input means for said input current and including an insulated gate field effect transistor as a current input element,

b. an operational amplifier connected to said signal input means,

c. a low impedance output amplifier connected to said operational amplifier and having output means for said output voltage,

d. feedback means connected between the output means of said output amplifier and said signal input means and comprising:

i. attenuator and temperature compensation means connected to said output means,

ii. a pair of logarithmic elements connected in series between said means (d) (i) and said signal input means,

iii. a time constant capacitor connected in parallel with said logarithmic elements for smoothing out input current fluctuations at said low value,

iv. diode switch means connected to said output means and operative in response to occurrence of said predetermined level of said output voltage,

v. and a time constant limiting resistance connected between said diode switch means and said signal input means, said diode switch means being operative to connect said resistance between said output means and said signal input means to limit the time constant of the parallel connection of said logarithmic elements and said time constant capacitor upon occurrence of said predetermined level of said output voltage.

6. A logarithmic amplifier according to claim 5 wherein

e. said pair of logarithmic elements consist of first and second planar transistors, the collector and base of said first transistor being connected to said signal input means (a) and the collector and base of said second transistor being connected to the emitter of said first transistor,

f. and said temperature compensation means includes

i. third and fourth transistors of the same type as said first and second transistors, the emitter of said third transistor being connected to the emitter of said second transistor and the emitter of said fourth transistor being connected to the base of said third transistor, said third and fourth transistors providing a first temperature dependent variation in feedback around said feedback means,

ii. and temperature sensitive resistance means connected to the base of said fourth transistor to provide a second temperature dependent compensating variation in feedback around said feedback means.