

[54] **AVERAGE TIMING METHOD AND
APPARATUS FOR INTERNAL
COMBUSTION ENGINES**

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[22] Filed: **Jan. 20, 1972**

[21] Appl. No.: **219,416**

[52] U.S. Cl. **324/16 R**, 73/118

[51] Int. Cl. **F02p 17/00**

[58] Field of Search...324/15-18; 73/116, 117.3, 118
R, 119 A

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[57] **ABSTRACT**

There is disclosed a method and apparatus for internal combustion engine timing based on measurement of the advance or retard of the firing of each spark plug with respect to a reference derived from the top dead center position of the piston for the number one cylinder. The engine timing is adjusted so that the average value of the advance or retard for all plugs equals a predetermined design value. A variable frequency oscillator is phase-locked by signals representing individual spark plug firing to operate at a frequency of 3,600 pulses per engine revolution. A reference related to the top dead center position of piston for the first cylinder is determined by sensing a notch in the engine damper or fan pulley, and is used to produce a series of pseudo damper pulses offset from the top dead center positions of the various pistons by 45 degrees by dividing the output of the variable frequency oscillator and selecting pulses to define the pseudo damper pulse interval based on the number of cylinders in the engine being timed. Timing measurement is achieved by counting the number of pulses between firing of a plug and the associated pseudo damper pulse over several complete engine operating cycles, averaging the result and removing the 45° offset. Digital display, printout, upper and lower limit computation and actual engine RPM measurements are also provided.

42 Claims, 18 Drawing Figures

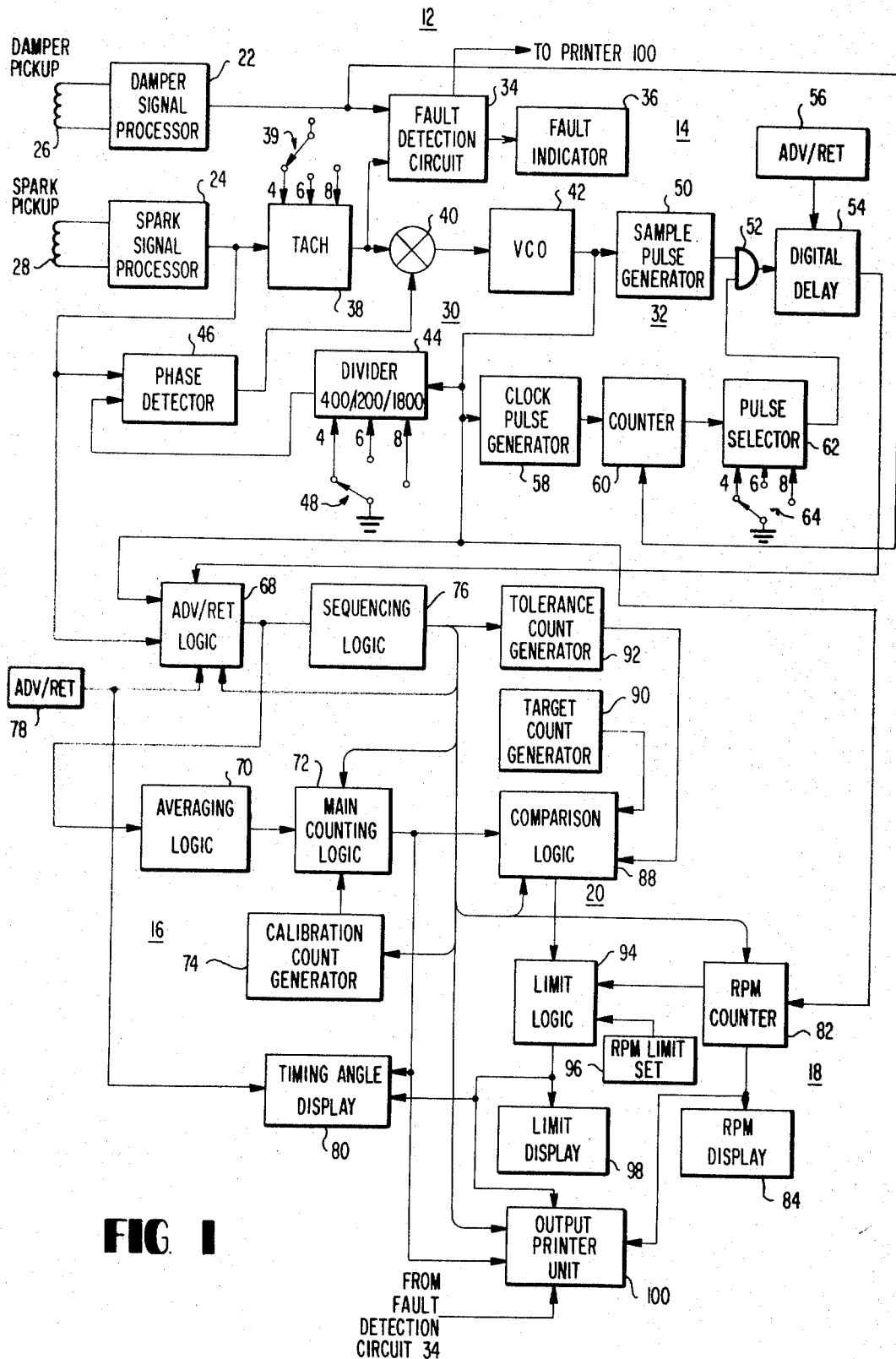
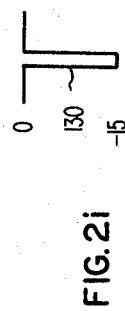
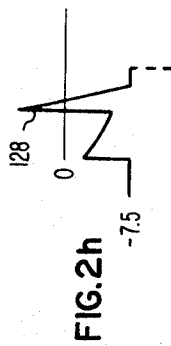
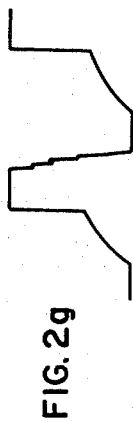
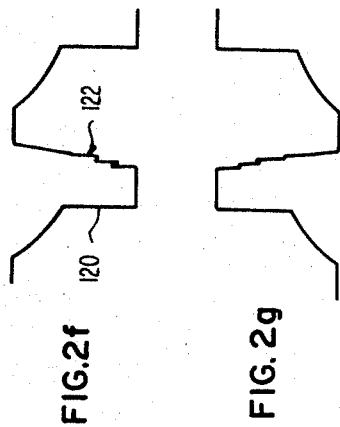
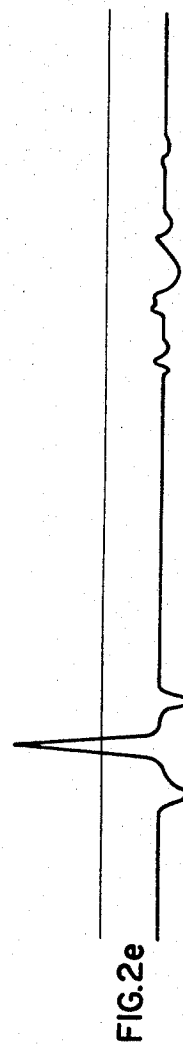
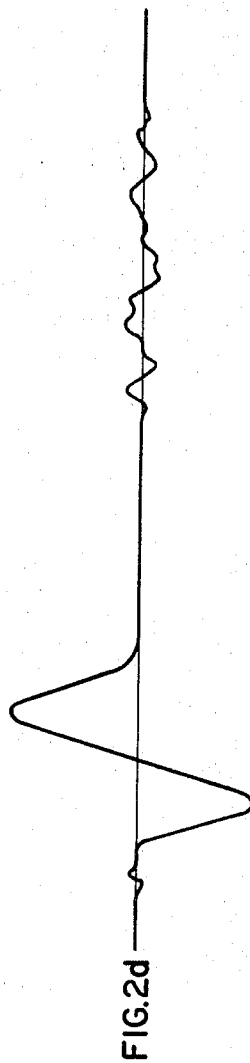
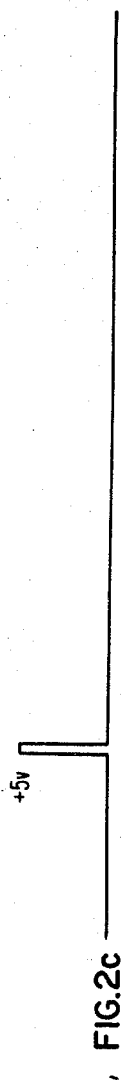
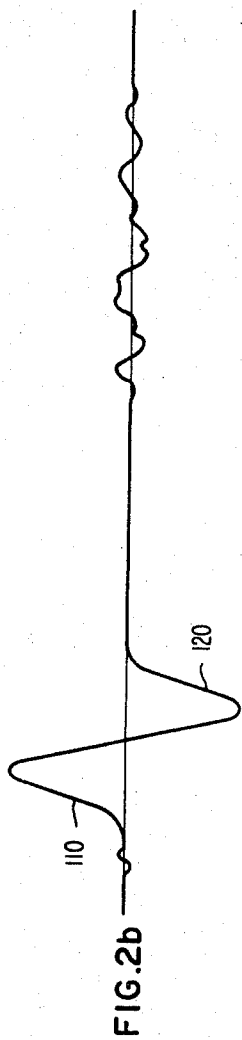


FIG. 1



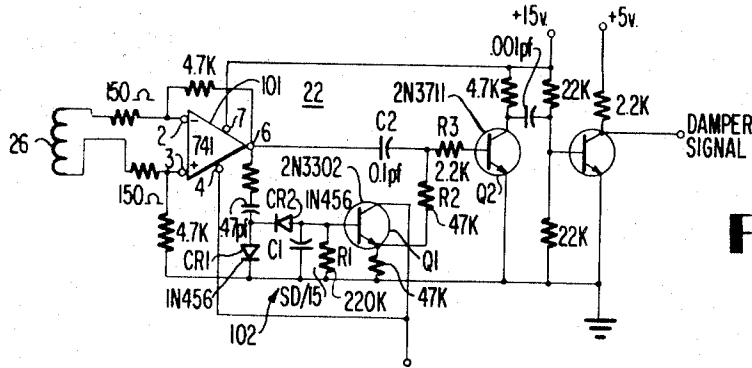


FIG. 3

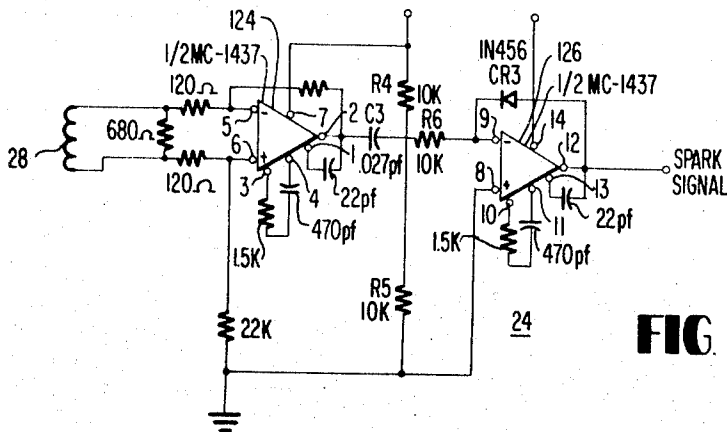


FIG. 4

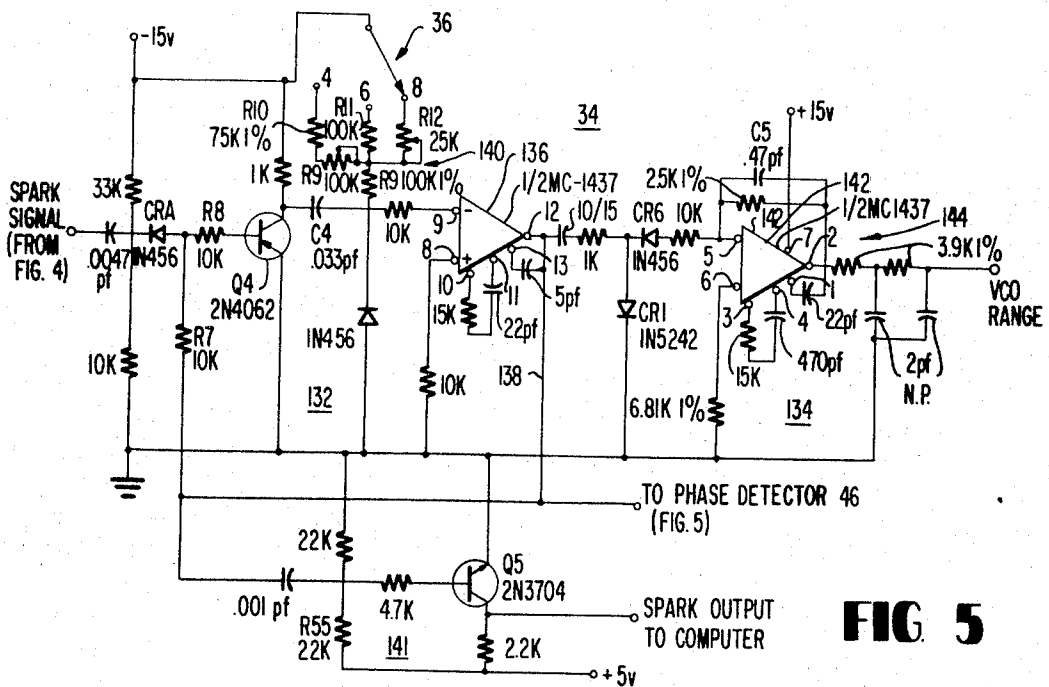


FIG. 5

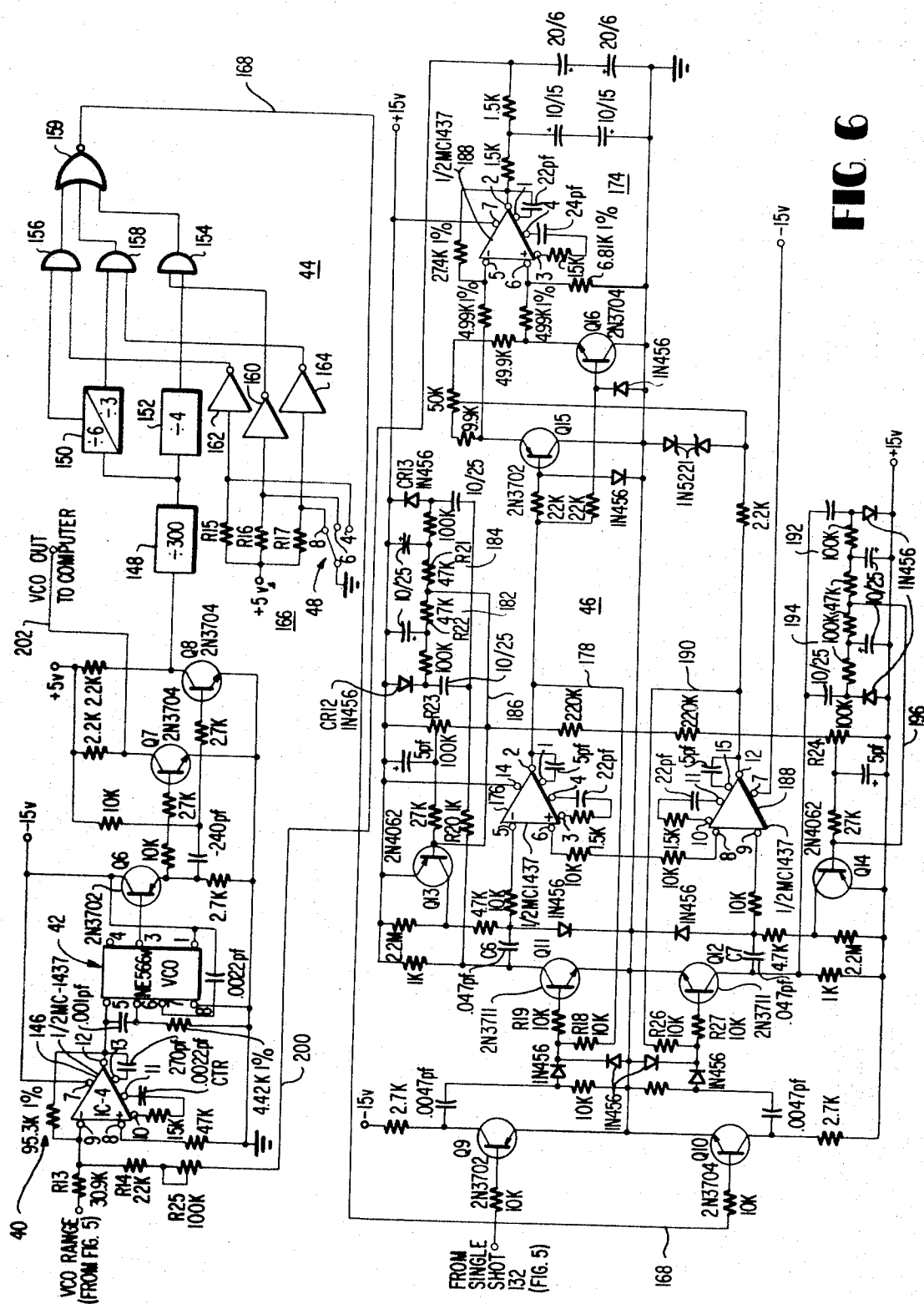


FIG. 6

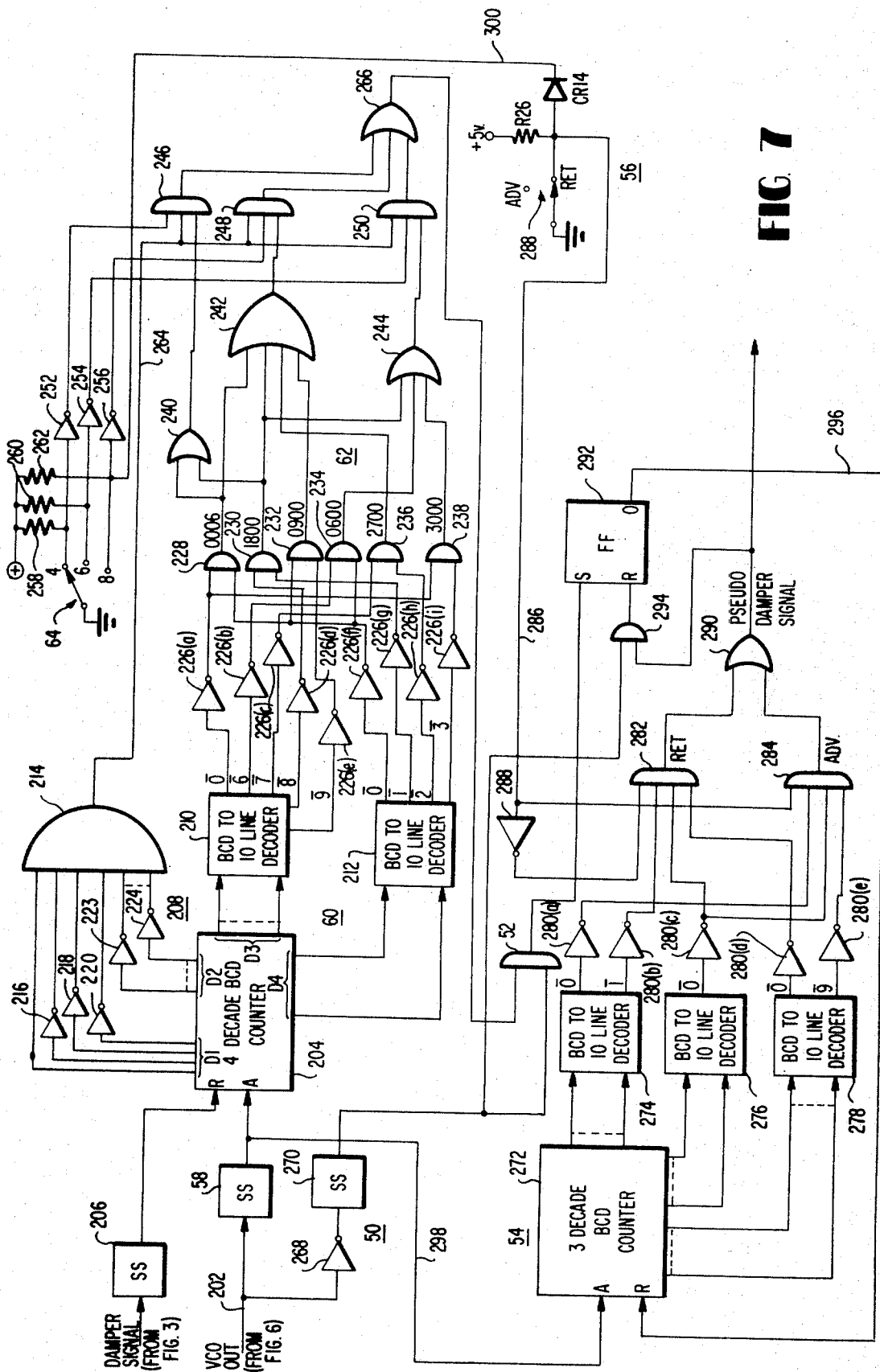
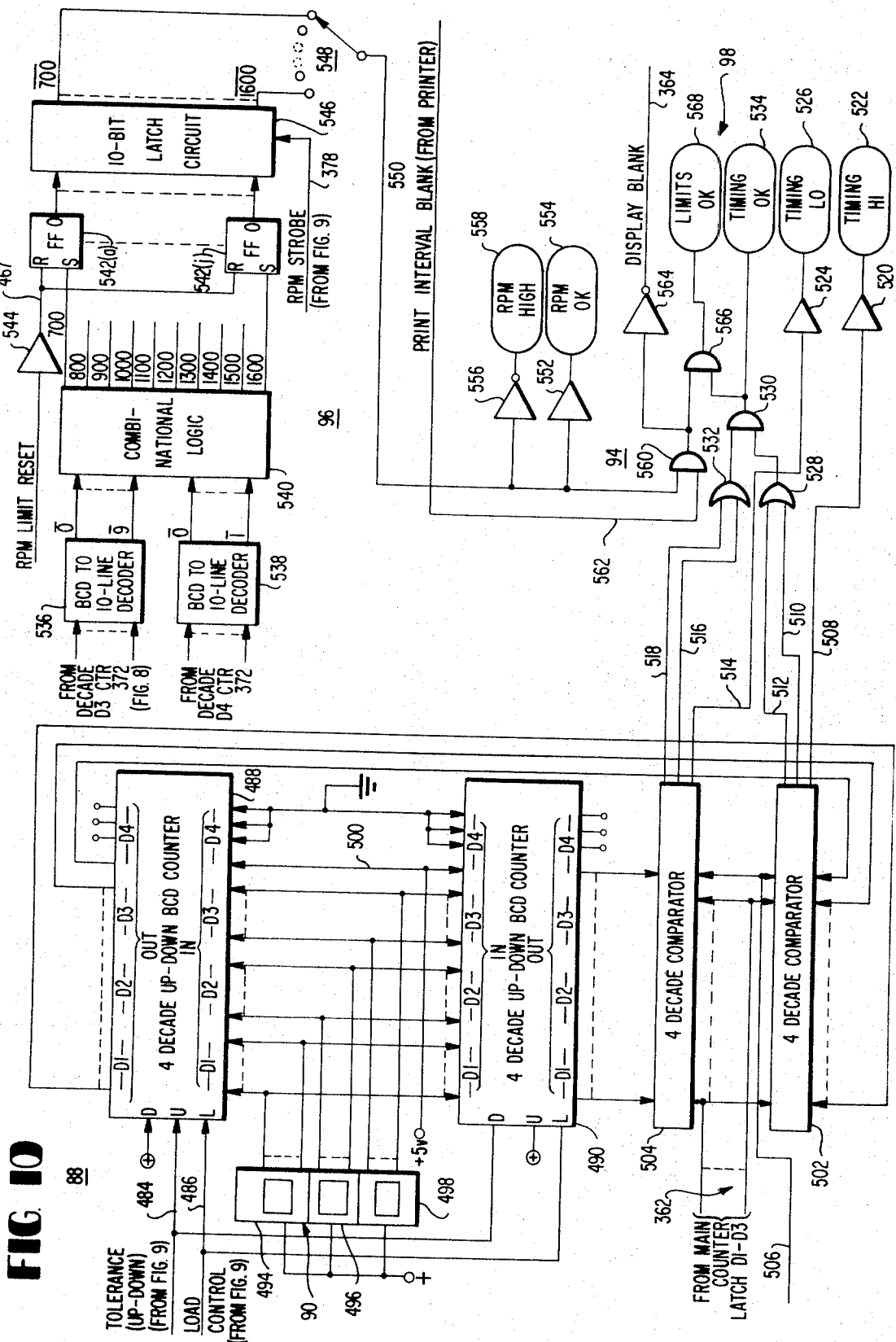


FIG. 7



AVERAGE TIMING METHOD AND APPARATUS FOR INTERNAL COMBUSTION ENGINES

INTRODUCTION

This invention relates to internal combustion engine timing, and more particularly to techniques and equipment for improving the accuracy of timing of engines such as automobile engines both in the assembly plant, and thereafter for purposes of routine maintenance.

Reference is made to a related patent application, Ser. No. 219,250, filed Jan. 20, 1972, entitled Engine Timing Computer, filed concurrently herewith in the name of Albert C. Abnett et al., which application claims certain subject matter disclosed herein, and related to the subject matter claimed in this application.

BACKGROUND

Briefly, by way of background, in a four-cycle engine of the type customarily employed in automobiles, each cylinder fires once for every two revolutions of the crankshaft. In most engines, a spark is provided for each cylinder slightly prior to the top dead center position for the piston on its compression stroke, although engines are occasionally designed to fire after the top dead center position.

Firing is controlled by a timing system. This includes a distributor having a rotating shaft coupled to the crankshaft by a 2:1 reduction gearing mechanism whereby the distributor shaft makes one complete rotation for every two crankshaft rotations. The distributor shaft carries a multi-lobed cam, (one lobe for each cylinder) which engages with a follower to operate a set of breaker points. These are shunted by a capacitor in a primary circuit of a spark coil connected to the battery. Opening of the points as the timing cam rotates provides rapid magnetic field changes in the secondary of the spark coil with resulting high voltage across the coil secondaries. The high voltage pulses are coupled to individual spark plugs by a rotating contact member carried by the distributor shaft and engaging with a series of fixed contacts in the distributor, each connected to one of the spark plugs.

Timing is normally adjusted in relation to the top dead center position of the number one piston by rotating a plate carrying the cam follower and breaker points in relation to the cam on the distributor shaft.

Accurate engine timing is extremely important because an improperly timed engine operates inefficiently and with less than optimum power and also, because timing errors increase the octane requirement of the fuel. Also of increasing importance is the fact that an improperly timed engine produces high exhaust emissions and consequent air pollution.

The normal procedure employed in engine timing utilizes a timing light which is a stroboscopic lamp fired by discharge of the number one spark plug. Firing of the lamp illuminates a pointer mounted on the engine in relation to a dial on the rotating damper pulley. The recurring momentary illumination of the pointer and dial indicates the relationship between the firing of the No. 1 cylinder and the top dead center position of its piston, ordinarily in terms of degrees before (or after) top dead center.

The foregoing system possesses several disadvantages. First, because of the positioning of the various measuring components, there can be substantial and unpredictable parallax in reading of the pointer and

markings on the damper pulley, thereby rendering the measurement inaccurate. Moreover, the stroboscopic timing equipment itself possesses inherent inaccuracies, due to the dynamic nature of the operation, and the visual nature of the observations. Further, measurements have been made with reference to a single cylinder on the assumption that each cylinder actually fires in precisely fixed relationship to the No. 1 cylinder. However, imperfections in the timing gears, the cam, and elsewhere in the timing mechanism can cause deviation of as much as plus or minus 3° from the design values. Thus, if the cam surface for cylinder No. 1 is inaccurate, the resulting offset may completely invalidate the timing reading. Even if the No. 1 cylinder is adjusted to fire exactly as specified, for example, at 6° before top dead center, adjustment of the timing for the No. 1 cylinder to achieve this ordinarily results in firing of the remaining cylinders anywhere between 3° and 9° before top dead center. This is totally unacceptable, particularly in view of increasing demands for reduced exhaust emissions.

For the foregoing reasons, several other techniques have been proposed to improve the accuracy of the engine timing operation, mostly involving electronically measuring the time interval between the firing and the top dead center position of the associated cylinder. Equipment of this type can provide a more accurate measurement of the timing angle for a particular cylinder, but totally fails to overcome the problem noted above regarding imperfection in the timing mechanism and its effect on the relationship between the firing angles for the cylinders.

Evidently in recognition of the foregoing, it has been proposed to measure the timing angle for each cylinder with respect to the top dead center position of its respective piston, and to adjust the distributor rotor until the average of all of the angles equals the design value as specified with respect to cylinder No. 1. The general concept of average timing appears to have excellent prospects as a means of improving engine efficiency and reducing exhaust emissions. However, the heretofore proposed implementation of the average timing concept known to applicant appears to be subject to several important disadvantages.

For example, average timing as heretofore proposed employs a fixed frequency reference oscillator and provides a measurement by counting the number of reference oscillator pulses between firing of each cylinder and a control signal representing the top dead center position for each cylinder. Since the frequency of the oscillator must bear a predetermined relation to the engine RPM at the time the measurement is made, means are provided to inhibit measurement unless the engine is running at the proper RPM. This presents difficulties since maintaining a constant engine RPM over even one revolution is almost impossible. While the variation in engine speed over a single revolution may not be great, nevertheless, even small changes produce substantial inaccuracy. For example, if the RPM at the time of measurement is as little as 2 percent high, a timing error exceeding the required plus or minus 0.1° accuracy will occur. For this reason, successful averaging has been found to require measurement of timing angles over several engine revolutions, which does not appear practical with the prior equipment.

Another difficulty with the heretofore proposed average timing technique is the necessity for providing a

pulse corresponding to the top dead center position for each cylinder. This is proposed to be accomplished in several way, for example a star wheel, or cam, or the like can be mounted on the front of the damper pulley, and an appropriate sensor mounted in fixed relationship on the engine. Alternatively, notches or the like could be cut directly in the damper pulley for interaction with a proximity sensor. Both of these techniques possess a significant economic disadvantage and in fact substantial resistance has been encountered in the industry. Placement of even a second notch on the damper pulley, i.e., for four-cylinder engine, is regarded as economically unattractive, and its use has been discouraged by the manufacturers.

A further problem with the previously proposed system is that under certain circumstances an engine designed to fire before top dead center may occasionally appear to fire after top dead center for a particular cylinder. The exact cause of such cross-over error is not clear but it is thought to be caused, for example, by a backfire, faulty plug, or other similar factors causing drastic transient changes in engine speed. Another possible cause may be inherent tracking imperfections in the measuring circuitry, though this may be more likely where, as described below, a constant number of pulses per engine revolution is employed. In any case, if logic circuitry designed to begin counting upon firing of the engine and to stop counting in response to the top dead center pulse is used under such circumstances, it will be appreciated that the count will begin with the engine firing but the top dead center pulse having already passed, the counting circuitry will continue to run until the next top dead center pulse. Even on an average basis, the resulting measurement would be so seriously affected as to be meaningless.

Yet an additional difficulty with the previously proposed device for average timing is its apparent inability to operate in the retard mode, as well as in the advance mode, without substantial inconvenience and possible unreliability. This presents a definite lack of flexibility.

BRIEF DESCRIPTION OF THE INVENTION

The present invention seeks to avoid both the technical and economic problems with the heretofore proposed average timing techniques by employment of a system including a variable frequency oscillator for generating a fixed number of counting pulses per engine revolution, (preferably 3,600 so each pulse represents 0.1°) and by averaging over several engine operating cycles, the number of pulses between the firing of each spark plug and the top dead center position for that cylinder, but based on a reference keyed to top dead center for the No. 1 cylinder. Elaborating on the foregoing, by using a fixed number of pulses per revolution, the time scale for measurement is automatically expanded or contracted to conform to engine RPM. By making all measurements with reference to the top dead center position for the No. 1 cylinder, the need for generating pulses corresponding to the top dead center position of the other cylinders is avoided and with it, the economic disadvantages of providing more than one notch or other indicator.

To eliminate the need for actually counting with respect to the top dead center position of the first cylinder, there is provided means for generating a series of pseudo damper pulses. This operates to count the oscillator pulses, and to provide reference pulses at prede-

termined intervals in accordance with the number of cylinders in the engine being timed. For example, for a four-cylinder engine, and with 3,600 counting pulses per revolution, the pseudo damper pulses would be spaced 1,800 counting pulses apart. Correspondingly, pseudo damper pulses for six and eight-cylinder engines would occur at 1,200 and 900 pulse intervals, respectively.

Aside from the economic advantages mentioned above, employment of pseudo damper pulses has two additional advantages. First, it permits measurement of the position of a notch in the damper (or fan pulley) as a reference in arbitrary relationship to the top dead center position for the No. 1 cylinder. Thus, if it proves to be convenient to position the proximity detector in such a manner that the notch passes the detector 100° before top dead center for the No. 1 cylinder, location of the actual top dead center position may be accomplished simply by counting 1,000 pulses following the pickup output.

More importantly, since the reference position is arbitrary, a timing angle of 6° before top dead center is equivalent to an angle of 16° before a reference 10° after the top dead center. This fact, and the fact that establishment of a reference is a simple matter of counting the desired number of pulses after the damper notch is sensed, completely avoids the possibility of a cross-over error.

Specifically, the reference for cylinder No. 1, is chosen to be 45° before top dead center for timing an engine designed to fire after top dead center (retard mode) and at 45° after top dead center for timing an engine designed to fire at or before top dead center (advance mode.)

The actual timing measurement is made by counting the number of variable frequency timing pulses between ignition of a cylinder and the associated pseudo damper pulse. This is accomplished by a counter activated either by the pseudo damper pulse for retarded firing or by the ignition pulse for advanced firing, and turned off by the ignition pulse for advanced firing.

The averaging operation is accomplished by maintaining a running count for the required number of ignitions. To reduce the required count capacity, the output of the reference clock is divided by the number of ignitions over which the average is taken before being coupled through the gating circuit to the counter.

The result is displayed digitally with the least significant figure being 0.1°. The 45° offset mentioned above is subtracted out prior to display.

Additional features of the invention include means for accurately locating the damper reference notch means for providing upper and lower limit indications with respect to the target timing angle, engine RPM readout, and means to provide an indication when the RPM exceeds a set limit. The system also includes fault detection means for providing an indication of system inoperativeness and an output printer, by which a permanent record of the timing operation can be produced.

Accordingly, among the objects of this invention are the following:

To provide improved techniques and apparatus for internal combustion engine timing;

To provide such techniques and apparatus utilizing average timing concepts but not subject to the disadvantages of heretofore proposed techniques;

To provide techniques and apparatus for average engine timing based on measurement of the angular interval between the ignition spark for each cylinder, and a reference angular position based on the top dead center position for the first cylinder;

To provide such average timing techniques and apparatus in which the average is taken over several complete engine cycles to compensate for nonuniformities of engine speed;

To provide average timing equipment and techniques utilizing a variable frequency oscillator adapted to produce a constant number of pulses per engine revolution and means for counting the number of pulses between ignition for each cylinder and a reference angular position based on the top dead center position for cylinder No. 1;

To provide such a system in which the variable frequency oscillator is phase-locked with the engine ignition pulses;

To provide average engine timing techniques and apparatus as described above in which the reference angular position is established by generation of a series of pseudo damper pulses at predetermined angular interval in relation to top dead center for cylinder No. 1;

To provide such pseudo damper pulses by selecting ones of the output pulses of the variable frequency oscillator at fixed intervals determined by the number of cylinders in the engine with the first of said pulses being related to the top dead center position for the first cylinder;

To provide average timing techniques and equipment as described above in which the reference position for cylinder No. 1 is a predetermined number of degrees before or after top dead center for said cylinder;

To provide average techniques and apparatus as described above in which the reference position is determined by a marker rotatable with the engine crankshaft, and a fixed sensor positioned to provide an output signal in response to passage of the marker and in predetermined angular relation to the top dead center position for the first cylinder;

To provide internal combustion engine timing techniques and apparatus as described above in which the average engine timing is determined by establishing a predetermined number of counting intervals representing the desired multiple of the number of cylinders over which the average is to be taken, generating a series of measuring pulses, the number of such pulses per engine revolution being constant, dividing the series of measuring pulses by the number of counting intervals, establishing a series of measuring intervals between ignition for a particular cylinder and a reference based on the top dead center position for one of the cylinders, counting the number of divided counting pulses for a number of measuring intervals equal to said predetermined number and displaying the result as the average timing of said engine; and

To provide average timing techniques and apparatus as described above in which the reference position with respect to the one cylinder is established by producing a reference pulse in known angular relationship to the top dead center position for that cylinder, dividing the pulse train to produce a series of pseudo reference pulses per revolution equal in number to one-half the number of cylinders, and using the so generated pseudo reference pulses in defining the succession of counting intervals.

The exact nature of this invention as well as other objects and advantages thereof will become apparent from consideration of the following detailed description together with the drawings in which:

FIG. 1 is an overall block diagram showing the organization of a preferred embodiment of the invention;

FIGS. 2a - 2c are waveform diagrams pertinent to the operation of certain portions of the system of FIG. 1;

FIGS. 3 through 6 show the circuit diagrams for the damper signal processor, the spark signal processor, the tachometer unit, and the phase locked loop shown in FIG. 1;

FIG. 7 is a circuit diagram of the pseudo pulse generator and digital delay units shown in FIG. 1;

FIG. 8 is a circuit diagram of the main counting logic, the advance-retard logic, the averaging logic, the RPM computing logic, and the timing angle and RPM display units;

FIG. 9 is a circuit diagram of the calibration and tolerance count generators, and the sequencing logic unit; and

FIG. 10 is a circuit diagram of the comparison and limit logic units, the RPM limit setting unit, and the limit display.

Referring now to FIG. 1, there is shown in block diagram form a preferred embodiment of the engine timing apparatus of this invention. The system, generally denoted at 12, may be regarded as comprised of four related sub-systems, namely a timing signal generating unit 14, a timing computer 16, an RPM computer 18, and an RPM and timing limit computer 20. The timing signal generator, illustrated in the upper half of FIG. 1 is comprised of input signal processors 22 and 24 for the damper notch pickup 26 and the spark coil pickup 28, a phase-locked loop 30 for generating a variable frequency pulse train comprising 3,600 pulses per engine revolution, and a pseudo damper pulse generator 32 which operates to select desired ones of the 3,600 pulses per revolution and to provide these as synthetic damper notch pulses in proper time relationship to the actual damper notch pulse provided by pickup 26.

Pickups 26 and 28 are constructed in any suitable fashion. Damper pickup 26 is preferably an eddy current or other magnetic field sensitive device while spark pickup 28 is either magnetic field or electric field sensitive (capacitive) as desired. The damper pickup operates as a proximity sensor to produce an output signal once per revolution of the damper as a notch cut in its periphery passes through the pickup field of view. To this end, there is advantageously provided a mounting fixture (not shown) on the engine to support the pickup in suitable relation to the damper so that the pickup senses the notch as the damper rotates. The mounting fixture itself may be of any suitable construction, and does not constitute part of this invention as such. However, it will be realized that placement of the fixture will depend on availability of an accessible mounting space. Any suitable mounting position may be employed, as long as the exact relationship between passage of the damper notch through the pickup field of sensitivity and the top dead center position for one of the pistons (for example, piston No. 1) is accurately known. In this connection, the system can readily accommodate any angular relationship between the position at which the damper notch is sensed and top dead center for the No. 1 piston. However, for simplicity, the following description assumes that the damper notch is

sensed by pickup 26 exactly 135° after piston No. 1 reaches its top dead center position. System adjustment to accommodate other positions is explained below.

Damper signal processor 22 converts the pickup output into a narrow pulse defining the center of the damper notch and thereby provides a precise reference for generation of a series of pseudo damper pulses from which timing measurement is actually made. The output of the damper signal processor is also coupled to a fault detection circuit 34 which operates an indicator 36 in the event of signal loss from the damper pickup.

Spark pickup 28 operates to provide a signal representing the magnetic field pattern associated with the spark coil output. In one preferred construction, the spark pickup is constructed to fit around the spark coil output wire, in the manner of a "clip on" type ammeter, but other constructions may also be employed, if desired.

Spark signal processor 34 responds to the pickup output to generate a pulse in precise time relationship with the opening of the distributor points. This signal is used directly by timing computer 16, and is also provided to a tachometer 38 which produces an analog signal representative of the frequency of the spark pickup output. Generation of the tachometer output is accomplished by integrating the series of pulses produced by spark signal processor 24. However, because a four-cylinder engine produces two spark pulses per revolution as compared to three spark pulses per revolution for a six-cylinder engine and four spark pulses per revolution of an eight-cylinder engine, tachometer 34 includes means to convert each of the incoming pulses from spark signal processor 24 into a pulse of different width in accordance with the number of cylinders in the engine. To this end, there is provided a three-position switch 39 which activates timing circuitry hereinafter described such that the pulse width for a six-cylinder engine is two-thirds the pulse width for a four-cylinder engine, while the pulse width for an eight-cylinder engine is one-half the pulse width for a four-cylinder engine.

The tachometer output is provided as a second input to fault detection circuit 34 which operates indicator 36 if the spark signal is lost. The output of tachometer also provides a control input for phase-locked loop 30. The latter comprises a summing unit 40, a voltage-controlled oscillator (VCO) 42 and a feedback loop comprising a variable frequency divider 44 and a phase detector 46. Summing unit 40 controls the frequency of VCO 42 in accordance with the sum of two DC voltages, one produced by the output of tachometer 38. The latter signal provides an approximate or coarse frequency control for the VCO while the former, representing the phase difference between the VCO pulse train and the pulse train produced by the spark signal processor 24, represents the normal phase error signal by which fine control of the phase-locked loop is achieved.

The system is so arranged that when operating properly, the output of VCO 42 provides 3,600 pulses per engine revolution. The VCO output is therefore 900 times the spark frequency for an eight-cylinder engine, 1,200 times the spark signal frequency for a six-cylinder engine, and 1,800 times the spark frequency for a four-cylinder engine. A control switch 48, cooperating with divider 44, assures the proper frequency relationship between the two inputs to phase detector 46

for four, six, or eight-cylinder engines according to the position of the switch.

The output of VCO 42 is provided to timing computer 16 as hereinafter described, and also to the pseudo damper pulse generator 32. This comprises a sample pulse generating unit 50, a gating circuit 42, a digital delay unit 54 controlled by an advance-retard switch 56, a clock pulse generator 58, counter 60, and a pulse rate selector 62, controlled by a switch 64.

Pseudo pulse generator 32 is described in detail below, but briefly stated, its function is to select particular ones of the 3,600 VCO pulses per engine revolution in accordance with the setting of a cylinder selection switch 64 and to delay the selected pulses for a predetermined count depending on whether the engine is to be timed with the spark plugs firing before or after the top dead center position of the piston (i.e., advance or retard operation, respectively.) The pulses are selected to provide the required two, three, or four pulses per engine revolution for a four-cylinder, six-cylinder, or eight-cylinder engine, respectively. Also, the selected pulses are adjusted in accordance with the previously noted 135° spacing between the top dead center position of cylinder No. 1 and the position at which the damper notch is sensed, and to provide the 45° calibration offset which prevents cross-over error as previously described.

The averaging and timing computation functions are provided by timing computer subsystem 16. This includes an advance-retard logic unit 68, and averaging logic unit 70, a main counting logic unit 72 and a calibration count generator 74. These cooperate under the control of a sequencing logic unit 76 to provide a digital representation of the average of the angle between ignition and the top dead center position of the piston for each cylinder. Ignition is represented by the output of spark signal processor 24 while the associated top dead center position is keyed to the top dead center position of the No. 1 cylinder, with the succession of pseudo damper pulses being provided by the output of digital delay unit 54. The average is taken over 128 firings, i.e., 16 complete cycles for an eight-cylinder engine. The angular interval is measured by counting the number of VCO pulses between the ignition pulse and the associated pseudo pulse. Since the VCO provides 3,600 pulses per engine revolution, each pulse counted represents 0.1°.

As will be appreciated, for an engine timed in the advance mode, the spark signal precedes the associated pseudo damper signal, while in the retard mode, the pseudo damper signal occurs first. Advance-retard logic unit 68 operates to select which of the two pulses defines the beginning of each counting interval in accordance with the position of an advance/retard selection switch 78.

During a succession of counting intervals, the number of VCO pulses is accumulated, and divided by the number of counting intervals to be employed in the averaging process. This is accomplished by averaging logic unit 70. The resulting average count is provided to main counting logic unit 72 which cooperates with calibration logic unit 74 to subtract 450 counts (i.e., representing 45° offset employed to prevent cross-over error), after which the result is visually displayed by means of timing angle display unit 80.

RPM and timing limit computer 20 is comprised of a comparison logic unit 88, target and tolerance count

generators 90 and 92, a limit logic unit 94, and an RMP limit setter 96. Comparison logic unit 88 provides a measure of the difference between the actual average timing angle as indicated by the output of main counting logic unit 72, and a target timing angle as indicated by unit 90, and provides signals indicating whether the difference is within a preset tolerance range established by tolerance count generator 92, or above or below the range. Limit logic unit 94 utilizes these signals to operate display 98, and also provides a comparison between the actual RPM as indicated by counter 82, and a maximum RPM suitable for timing measurement as indicated by limit setter 96. A limit display 98 also provides an indication if the actual RMP exceeds the acceptable limit.

In addition, there is provided a printer unit 100, controlled by sequencing logic unit 76 by which a permanent record of the measured timing may be produced. The printout may include such reference data as the date, the machine number, etc., as well as the timing angle and the RPM at the time of measurement (actually, the average RPM over the measuring interval, as explained below). The latter data are provided by main counting logic 72, and RMP counter 82. Control signals are provided by sequencing logic 76, fault detection circuit 34 and limit logic 94. Signals from the latter prevent printer operation if incorrect data is sensed.

FIGS. 3 through 10, taken in conjunction with the waveform diagram shown in FIG. 2 illustrate in more detail the construction and operation of a preferred embodiment of the apparatus illustrated generally in FIG. 1.

Referring to FIG. 3 there is shown the construction of damper signal processor 22. The circuit comprises an integrated circuit differential amplifier 101 (such as Motorola type MC 741, or equivalent) having its inputs resistance coupled to damper pickup 26. The output of amplifier 101 at pin 6 is coupled to an automatic level control unit 102 comprised of a transistor Q1 and a detector circuit including diodes CR1 and CR2, capacitor C1 and resistor R1.

Transistor Q1 provides a current path for a differentiator circuit comprised of a capacitor C2 and resistors R2 and R3 which couples the output of amplifier 101 to the base of a transistor Q2, the collector of which is, in turn, RC coupled to the base of an output transistor Q3.

Referring now to FIG. 2, lines (a)-(e), as well as FIG. 3, the damper notch 104 [FIG. 2, line (a)] may be regarded as a shallow rectangular cut-out having a leading edge 106 and a trailing edge 108. As notch 104 passes through the field of sensitivity of pickup 26, there is produced an output pulse such as illustrated in FIG. 2, line (b) having a positive-going leading edge 110 corresponding to the abrupt change in spacing between the pickup and the damper periphery as the leading edge 106 of the notch passes into the field of sensitivity of the pickup. As the leading edge passes the pickup, the output peaks, and returns toward zero, reaching the 0 level at about the time that the center of the notch passes the pickup. Then, as the trailing edge of the notch approaches the pickup, its output continues negative, and reaches a minimum value at about the time that the trailing edge 108 passes the pickup. Thereafter, the output again becomes positive-going, and returns to zero as the notch passes beyond the pickup.

The purpose of damper signal processor 22 is to convert the waveform shown in FIG. 2, line (a) to a narrow pulse such as shown in FIG. 2, line (c), as near as possible to the center of the damper notch.

Returning to FIG. 2, damper notch pickup 26 is coupled through amplifier 101 which inverts the pickup output, and at the same time converts it to a single-ended signal referenced to ground. The result is shown in FIG. 2, line (d). As this signal goes negative, it is rectified and smoothed by detector circuit 102. The resulting time varying DC signal operates transistor Q1 which applies a negative bias level at the base of a transistor Q2 through resistors R2 and R3. Because of capacitor C2, the output of amplifier 101 is differentiated to produce a pulse shown in FIG. 2, line (e), superimposed on the depressed bias level for the base of transistor Q2.

As will be understood, the negative bias creates an input threshold for transistor Q2 which maintains the same nonconductive until the input pulses [FIG. 2 line (e)] becomes sufficiently positive. By adjusting the threshold level properly, the conduction period of transistor Q2 is arranged to occur very close to the "zero" crossing of the damper pickup output, i.e., at approximately the peak of the derivative waveform which occurs at the time that the center of the damper notch passes the pickup.

With transistor Q2 nonconducting, transistor Q3 conducts, whereby the normal level for the output signal is zero [see FIG. 2, line (c)]. When transistor Q2 conducts, transistor Q3 cuts off, thereby producing the sharp positive pulse at the center of the damper notch shown in FIG. 2(c).

Referring to FIG. 2(f), there is shown the waveform sensed by spark pickup 28 for each spark plug ignition. A cycle begins when the breaker points open producing a negative going transition indicated at 120. Thereafter, when the points close, a fairly complicated waveform characterizing the magnetic field resulting from the spark itself occurs. This is indicated at 122. Since the timing measurement is made with reference to the opening of the points, it will be appreciated that spark signal processor 24 must be responsive to the opening of the points, i.e. at 120, but preferably not to the remainder of the waveform.

The circuitry required for accomplishing this result is shown in detail in FIG. 4. As illustrated, an input differential amplifier 124 such as one-half of a Motorola Type MC-1437, or the equivalent, is resistance coupled to spark pickup 28. Amplifier 124 operates to invert the polarity of the incoming spark signals, and at the same time to convert it to a single-ended signal referenced to ground. The resulting output of amplifier 124, at pin 2 is shown in FIG. 2(g). The inverter spark signal is coupled to the negative input of a second differential amplifier 126 which may be the other half of the integrated circuit comprising amplifier 124. As illustrated, the coupling circuit includes a capacitor C2 and a voltage divider comprising a pair of like resistors R4 and R5, coupled between the negative power supply and ground.

With the R4-R5 voltage divider connected to the negative power supply, it may be seen that a negative offset or bias is applied to the negative input of amplifier 126. With the positive input at pin 8 grounded, the negative bias at pin 9 tends to drive the amplifier output at pin 12 to a high level, but to prevent this, there

is provided a feedback diode CR3 which clamps the output to approximately 0 volts for all negative inputs.

From the AC standpoint, the RC coupling circuit operates to differentiate the spark waveform in FIG. 2 (g) to produce a waveform such as shown in FIG. 2(h) including a sharp positive going spike 128 coincident with the opening of the points. It will, however, be noted that because of the negative offset produced by the voltage divider, only the portion of spike 128 extending the offset voltage reaches the input of amplifier 126 as a positive level.

When the input to pin 9 of amplifier 126 exceeds the bias threshold, the amplifier operates to produce a negative output, and remains operative until the input falls below the threshold. The result is a straight-sided negative pulse such as shown in FIG. 2 (i), having a leading edge 130 coinciding with opening of the points.

The output of amplifier 126 is connected to the input of tachometer circuit 38, the construction of which is illustrated in FIG. 5. In essence, tachometer circuit 38 comprises a single shot multi-vibrator generally denoted at 132, having an adjustable operating period, and an integrator circuit 134 to produce a DC analog signal representative of the frequency of the ignition pulse train produced by spark signal processor 24.

Single shot 132 is comprised of a transistor Q4 and an amplifier 136, the latter comprising one-half of a Motorola Type MC-1437 integrated circuit, or the equivalent. A feedback path from the output of amplifier 136 at pin 12 is provided to the base of transistor Q4 over lead 138 through a pair of resistors R7 and R8.

Timing control for single shot 132 is provided by a timing capacitor C4 and a resistance circuit 140 including a series resistor R9 and three parallel resistors R10, R11, and R12 coupled in common to resistor R9, and to the fixed contacts of cylinder selection switch 36. The values of resistors R10 through R12 in relation to capacitor C4 and resistor R9 are so chosen that the sum of the pulse widths at the output of the single shot over one engine revolution is independent of the number of pulses. In other words, for a six-cylinder engine which produces three ignition pulses per revolution, the pulse width is two-thirds that for a four-cylinder engine which produces two ignition pulses per revolution. Correspondingly, for an eight-cylinder engine which produces four ignition pulses per revolution, the individual pulse width is one-half that for the four-cylinder engine.

The output of single shot 132 is provided as an input to phase detector 46 hereinafter described over lead 138, and also to an output circuit 141 comprising a transistor Q5, and associated circuitry. The collector of the transistor provides the spark output to timing computer subunit 16 (see FIG. 1) as described in detail below.

The output of single shot 132 also provides the input to VCO range integrator 134. The latter comprises a differential amplifier 142, preferably the second half of the integrated circuit comprising amplifier 136, provided with a feedback circuit including a capacitor C5 to integrate the pulse train output of single shot 132.

A shunt diode CR7 controls the maximum amplitude of the integrator input while a series diode CR6 blocks the passage of any positive signals. The output at pin 2 is therefore a DC level representative of the engine speed. Because the pulse width variation depending on the number of cylinders as explained above, the inte-

gration performed by circuit 134 is independent of the number of ignition pulses per engine revolution.

The output of amplifier 142 at pin 2 is coupled through an RC filter circuit 144 as the VCO range control signal for phase-locked loop 30, illustrated in detail in FIG. 6. As shown, the input from tachometer circuit 38 is provided to an integrated circuit amplifier 146 comprising summing circuit 40 (see FIG. 1). The input at pin 9 serves as a summing junction between the VCO range signal provided by a resistor R13 and by the output of phase detector 46 hereinafter described provided through a resistor R14. The output of amplifier 146 is connected to the control input of the voltage controlled oscillator which preferably is comprised of a commercially available integrated circuit unit such as the Signetics Type NE-556V, or its equivalent. The output at pin 3, having a frequency proportional to the amplitude of the control input at pin 5, is provided through an output amplifier comprising a transistor Q6, which in turn feeds a pair of output circuits comprising further transistors Q7 and Q8. The output of transistor Q7 provides the VCO output signal to the timing computer subsystem hereinafter described while transistor Q8 provides the input for divider 44 in the phase-locked loop feedback circuit.

As previously noted, the output of VCO 42 is controlled such that its output frequency varies with engine speed to produce exactly 3,600 pulses per engine revolution. As shown in FIG. 1, frequency control by means of phase detector 46 requires comparison of the output of spark signal processor 24 with the output of VCO 42. Thus, it is necessary to reduce the frequency of the VCO output to correspond to that of the spark signal processor. Since the spark signal processor produces 2, 3, and 4 spark pulses per engine revolution, for a four, six, and eight-cylinder engine respectively, and the VCO output is 3,600 pulses per revolution, it will be appreciated that divider unit 44 must divide the VCO output by 1,800 for a four-cylinder engine, by 1,200 for a six-cylinder engine, and by 900 for an eight-cylinder engine.

The foregoing result is accomplished by employment of digital dividers and associated combinational logic including a "divide by 300" unit 148 connected in parallel to a "divide by six" unit 150 and a "divide by four" unit 152. Each of the latter may be constructed in conventional fashion of commercially available integrated circuit counters. For example, divider 148 may be constructed of a series combination of two decade counters such as Texas Instruments Type 7490 and a "divide by 12" counter such as Texas Instruments Type 7492 wired to provide a "divide by three" function. Similarly, divider 150 may be a Texas Instruments Type 7492 counter wired to provide both a "divide by six" and "divide by three" functions. Divider 154 may be a Texas Instruments Type 7493 four bit binary counter wired to provide the "divide by four" function.

Considering dividers 148 and 152 as connected in series, it may be seen that the output of divider 152 effectively divides the output of VCO 42 by 1,200. Similarly, considering dividers 148 and 150 as connected in series, the "divide by six" output of divider 150 effectively divides the VCO output by 1,800 while the "divide by three" output divides the VCO output by 900.

Selection of the proper one of the outputs of dividers 150 and 152 is accomplished by an AND gate 154 connected to the output of divider 152, and two additional

AND gates 156 and 158 connected to the "divide by six" and "divide by three" outputs respectively of divider unit 150. The outputs of all of AND gates 154, 156, and 158 are connected to a NOR gate 159 to provide the output of the divider unit as a whole.

Control inputs for AND gates 154, 156, and 158 are provided respectively through three inverters 160, 162, and 164 by switch control circuit 166 comprising three resistors R16, R15, and R17 connected respectively to the inputs of inverters 160 through 164 and in common to the positive power supply. The inputs of each of inverters 160 through 164 are also connected to the fixed contacts of selection switch 48. The moving contact is grounded thereby providing a low level input to the selected one of inverters 160 through 164 and high inputs to the other two inverters. Since the outputs of the two unselected inverters are low, the corresponding ones of AND gates 154 through 158 are inhibited while the AND gate associated with the selected one of inverters 160 through 164 is activated. Thus, depending on the position of switch 48, divider 44 provides at the output of OR gate 159 a signal at two pulses per revolution for a four-cylinder engine (3,600 divided by 1,800), three pulses per revolution for a six-cylinder engine (3,600 divided by 1,200) and four pulses per engine revolution (3,600 divided by 900) for an eight-cylinder engine.

The output of divider 44 is provided over lead 168 as one input to the phase detector unit 46 through an input transistor Q10, the other input being provided through a transistor Q9 from single shot 132 in tachometer 38 previously described. In essence, phase detector unit 46 comprises a pair of variable frequency single shot multi-vibrators 170 and 172, each arranged to convert the incoming pulses (at 2, 3 or 4 pulses per engine revolution) into a square wave at the input frequency. An analog phase detector circuit 174 compares the phases of the resulting square waves.

Considering first the variable period single shot 170 associated with the spark signal input at transistor Q9, the two amplification stages are provided by a transistor Q11 and an integrated circuit differential amplifier 176. Feedback from the pin 2 output of amplifier 176 is provided over lead 178 and resistors R18 and R19 to the base of transistor Q11. Timing control is provided by a capacitor C6 and a charge control transistor Q13 operated by a diode-Rc biasing control circuit 180 which compares the duration of the on and off portions of the single shot output cycle and adjusts the charging time for capacitor C6 to maintain the two portions equal.

The above-described function is accomplished by a pair of polarized integrator circuits 182 and 184 coupled to the collector of single shot transistor Q11 by a resistor R20. Due to opposite polarization of diodes CR12 and CR13, integrator 182 responds only to one portion of the single shot cycle while integrator 184 responds only to the other portion. At the end of a cycle, a difference in the integrated signal levels indicates that the two portions of the single shot operating cycle are not of equal duration.

This difference, if any, is measured between a pair of resistors R21 and R22. The signal at the junction point is fed back over lead 186 to the base of transistor Q13. The latter also receives as a bias reference, the output of a potentiometer R23 connected between ground and the positive power supply to establish the current flow through transistor Q13 for zero bias on lead 186.

As will be appreciated, potentiometer R23 is set to produce a square wave output at some frequency trigger signal with zero feedback over lead 186. Thus, for other trigger frequencies, the bias on lead 186 varies the current through transistor Q13, and thus the charging current for capacitor C6, to maintain the active period of the single shot equal to half the period of the triggering pulses. The result, therefore, is a squarewave signal at pin 2 of amplifier 176 whose frequency is equal to the pulse rate of the incoming signal from tachometer 38.

The second single shot circuit 172 is comprised of a transistor Q12 and an integrated circuit amplifier 188 forming the other half of the integrated circuit comprising amplifier 176, connected by a feedback path 190. Single shot 172 is associated with the divider output provided over lead 168 through transistor Q10. Timing control for single shot 172 is provided by capacitor C7 and a charging current control transistor Q14 operated by a pair of diode-RC feedback circuits 192 and 194 like circuits 182 and 184. These monitor the waveforms at the collector of transistor Q12 and provide a signal on lead 196 representative of the difference between the two portions of the single shot cycle. A reference potentiometer R24 functions in the same manner as potentiometer R23. Changes in the bias level on lead 196 varies the charging current for capacitor C7 through transistor Q14 to maintain the single shot as a squarewave.

The outputs of single shots 170 and 172 are provided to the phase detection circuit 174. This comprises transistors Q15 and Q16, and a differential amplifier 198 which provides an output at pin 2 in a form of a DC signal representing the phase difference between the outputs of the single shots. The phase difference signal is provided over lead 200 through a potentiometer R25 and previously mentioned resistor R14 to the summing junction input of amplifier 146. Thus, it may be seen that the output frequency of VCO 42 is controlled by the sum of the VCO range signal provided by tachometer 34 and the signal representing the phase difference between the oscillator output and the spark pulse signal generated by single shot 132. The aforementioned arrangement is particularly advantageous since it allows establishing a coarse adjustment for the VCO related directly to the engine RPM, and a fine adjustment based on the phase difference between the oscillator output and the incoming spark pulses.

The VCO output is provided by previously mentioned transistor Q7 over lead 202 to the input of pseudo pulse generator 48, illustrated in detail, along with digital delay unit 54, in FIG. 7.

Before proceeding with the structural description, however, it is worthwhile to recall the functional requirements for the pseudo pulse generator and associated digital delay unit. To eliminate the possibility of cross-over error as described above, the timing system herein described measures the timing angle with respect to a reference 45° before the top dead center position of the associated cylinder for an engine operating in the retard mode, and 45° after the top dead center position of the associated cylinder for an engine operating in the advance mode. Signals representing each of these angular positions are to be generated with reference to the single actual pulse produced by the damper pulse sensor at a position 135° after the top dead center position for the cylinder No. 1.

Considering first the operating of a four-cylinder engine in the retard mode, the first pseudo damper pulse must appear 45° before the top dead center position for cylinder No. 1 and 180° thereafter, i.e., at 225° after top dead center for cylinder No. 1. This provides pseudo damper pulses for two of the four cylinders; the remaining pseudo damper pulses are to be generated at the same angular positions during the next revolution.

Correspondingly, for a six-cylinder engine operating in the retard mode, pseudo damper pulses are required 45° before top dead center for cylinder No. 1, and at 120° intervals thereafter, i.e., at 75° and 195° after top dead center for cylinder No. 1. Finally, for an eight-cylinder engine, four pseudo damper pulses per revolution must be provided at 45° before top dead center for cylinder No. 1, and at successive 90° intervals, i.e., at 45°, 135°, 225°, and 315° before top dead center for cylinder No. 1.

Because the single reference pulse is available only at 135° after top dead center, it may be seen that pseudo damper pulses may readily be referenced to 135° after top dead center for cylinder No. 1, rather than to the top dead center position. The required pseudo damper pulse angles for retard operation, taking into account the 45° offset to avoid cross-over errors, are listed below in TABLE ONE. The second column gives the angles with reference to top dead center, while the third column gives the angles with reference to the damper notch.

No. of Cylinders	Retard Mode (Ref. TDC1)	Retard Mode * (Ref. Damper Notch)
4	-45° (315°), 135°	0°, 180°
6	-45° (315°), 75°, 195°	60°, 180°, 300°
8	-45° (315°), 45°, 135°, 225°	0°, 90°, 180°, 270°

* 135° after TDC No. 1

TABLE ONE: PSEUDO PULSES FOR RETARD TIMING

Considering now the situation for operation in the advance mode, it will be appreciated that avoidance of cross-over error for a timing angle preceding the top dead center position requires the appearance of the pseudo pulse 45° after top dead center. Thus, for a four-cylinder engine, the pseudo damper pulses must appear at 45° and 225° after top dead center for cylinder No. 1, or at 90° and 270° with reference to the 135° offset between the sensing of the damper notch and top dead center for cylinder No. 1. Corresponding analysis shows that with respect to the top dead center position for cylinder No. 1, pseudo damper pulses for a six-cylinder engine must appear at 45°, 165°, and 282°, or at 30°, 150°, and 270° with reference to the damper notch. For an eight-cylinder engine, with reference to top dead center position for cylinder No. 1, damper pulses are required at 45°, 135°, 225° and 315°, corresponding to 0°, 90°, 180°, and 270° with reference to the damper notch. The foregoing results are summarized in TABLE II below.

No. of Cylinders	Advance Mode: (Ref. TDC No. 1)	Advance Mode: (Ref. Damper Notch) *
4	45°, 225°	90°, 270°
6	45°, 165°, 285°	30°, 150°, 270°
8	45°, 135°, 225°, 315°	0°, 90°, 180°, 270°

* 135° after TDC No. 1

TABLE TWO: PSEUDO PULSES FOR ADVANCE TIMING

Comparing TABLES I and II, it may be seen that in

each case, a pseudo damper pulse for retard mode timing appears 90° before the corresponding pseudo damper pulse for advanced mode timing. (This fact may also be appreciated from recognition that avoidance of cross-over error requires positioning the pseudo damper pulse 45 degrees before top dead center for retard timing and 45 degrees after top dead center for advance timing producing a net 90° offset.) Because of this, and in view of the availability of the reference pulse at 135°, it is found convenient to generate the pseudo damper pulses in relation to the damper notch according to the angular positions set forth in the right hand column of TABLE I and to provide the corresponding pseudo pulses for advance timing by delaying each of the retard mode pseudo damper pulses 90°, i.e., at the angular positions set forth in the right hand column of TABLE II.

The circuitry used to accomplish these functions is illustrated in FIG. 7. The pseudo pulse generating unit 32 includes counter 60 comprised of a four-decade binary coded decimal counter unit 204 constructed of integrated circuit units of any conventional or desired type. Counter 204 receives as its count input, the output of a single shot 58 comprising the clock pulse generator referred to in FIG. 1. The latter receives as its input, the VCO output signal described above in connection with FIG. 6. A reset input for counter 204 is provided by another single shot 206 receiving as its input, the damper signal provided by the output of transistor Q3 (see FIG. 3.) As will be appreciated, the VCO output constitutes a train of 3,600 pulses per engine revolution while the damper signal is pulse appearing once per revolution. Thus, counter 204 reaches to a count of 3,600 in binary coded decimal form before being reset for each engine revolution.

The BCD outputs of counter 204 for the two least significant decades are provided in binary coded decimal form to a one-count interval generator 208, while the outputs for the two most significant decades are provided respectively to a pair of BCD to 10-line decoders 210 and 212. One-count interval generator 208 comprises an AND gate 214 coupled directly to the output for the least significant bit (0.1 degree) of the first decade, while the outputs for the remaining bits of the first decade are coupled through respective inverters 216, 218, and 220. Similarly, all four bits comprising the second decade are coupled to AND gate 214 through inverters, two of which are shown at 222 and 224. Assuming counter 204 provides its outputs in a positive logic format, the inputs to AND gate 214 are all high only during the first count of every two decades, i.e., every one hundred counts.

BCD to 10-line converters 210 and 212 are preferably constructed of commercially available integrated circuit units such as Texas Instruments Type 7442. Such units provide ten outputs in response to a BCD input. The output corresponding to the input code is low; all the other outputs are high.

Decoder 210 is associated with the third decade of counter 204, and thus switches states every one hundred counts. Correspondingly, decoder 212 is associated with the fourth decade of counter 204 and thus switches states only every one thousand counts. However, the available outputs from third decade decoder 210, only the 000, 600, 700, 800, and 900 count outputs are required. From fourth decade decoder 212,

only the 0000, 1000, 2000, and 3000 count outputs are required.

Each of the above-mentioned outputs is provided through a respective one of inverters 226(a) through 226(i) to convert the signals to positive logic. Thus, the outputs of inverters 226(a) - (i) are high between the various counts set forth below in TABLE III.

Inverter	High Intervals	Inverter	High Intervals
226(a)	0-99, 1000-1099, etc.*	226(f)	0-999
226(b)	600-699, 1600-1699, etc.*	226(g)	1000-1999
226(c)	700-799, 1700-1799, etc.	226(h)	2000-2999
226(d)	800-899, 1800-1899, etc.	226(i)	3000-3599 **
226(e)	900-999, 1900-1999, etc.		

* Typical; repeats every 1000 ** Counter resets at 3600

TABLE III

The outputs of inverters 226(a) - (i) are connected to various ones of six AND gates 228-238 comprising part of pulse selector 62. AND gates 228-238 function to collect required ones of the hundred count signals and the thousand count signals to form six different 100 count intervals. In particular, the outputs of inverters 226(a) and (f) are coupled to AND gate 228 to produce a high output during counts 0-99. The outputs of inverters 226(d) and 226(g) are coupled to AND gate 230 to produce a high output for counts 1800-1899. The outputs of inverters 226(e) and (f) are provided to AND gate 232 to produce a high output for the counts 900-999. The outputs of inverters 226(b) and 226(f) are provided to AND gate 234 to produce a high output for the counts 600-699. The outputs of inverters 226(c) and (h) are provided to AND gate 236 to produce a high output for counts 2700-2701. Finally, the outputs of inverters 226(a) and 226(i) are coupled to AND gate 238 to produce a high output for counts 3000-3099.

The outputs of AND gates 228 and 230 are coupled to the inputs of an OR gate 240. AND gates 228 and 230 are also coupled as inputs to another OR gate 242, along with the outputs of AND gates 232 and 236. A third OR gate 244 receives as its inputs, the outputs of AND gates 230, 234, and 238. OR gate 240 thus operates counts 0-99 and 1800-1899, while OR gate 242 operates for counts 0-99, 900-999, 1800-1899, and 2700-2799. OR gate 244 operates for the counts of 600-699, 1800-1899, and 3000-3099.

The outputs of OR gates 240, 242, and 244 are connected respectively as inputs to three AND gates 246, 248, and 250. Second inputs for each AND gate 246 through 250 are provided through three inverters 252, 254, and 256, the inputs of which are connected to the positive power supply through three resistors 258, 260, 262, respectively. Each resistor is also connected to the fixed contacts of three-position switch 64 which has its moving contact grounded. As will be understood, resistors 258, 260, and 262 maintain the inputs to inverters 252 through 256 at a high level except for the inverter attached to the grounded switch contact. Thus, the outputs of two of the inverters are low while the output of the selected inverter is high to activate the associated AND gate. Thus, with switch 64 in the four-cylinder position, AND gate 246 is conditioned, with switch 64 in the six-cylinder position, AND gate 248 is conditioned and with switch 64 in the eight-cylinder position, AND gate 250 is conditioned.

The third inputs to each of AND gates 246 through 250 are provided in common over lead 264 by the output of AND gate 214. As previously described, AND

gate 214 operates to provide a high level output for a single count interval at the beginning of every 100 counts. Thus, AND gate 246 operates only at counts 0 and 1800, AND gate 248 operates only at counts 0, 900, 1800, and 2700, while AND gate 250 operates only at counts 600, 1800 and 3000.

Recalling that a cycle for counter 240 begins upon receipt of a damper signal (at which time the counter is reset through single shot 206) and that each count pulse represents 0.1° after the damper pulse, it may be seen that the pseudo pulses for a four-cylinder engine occur at 0° and 180° after the damper pulse. Similarly, for an eight-cylinder engine, the pseudo damper pulses occur at 0°, 90°, 180°, and 270° after the damper pulse. For a six-cylinder engine, the pseudo damper pulses occur at 60°, 180° and 300° after the damper pulse.

The outputs of AND gates 246-250 are coupled through an OR gate 266 to one input of AND gate 52 shown in FIGS. 1 and 7. The other input for AND gate 52 is provided by a sample pulse generator 50 comprised of a single shot 270 triggered by the VCO output on lead 202 through an inverter 268.

The output of AND gate 52 provides the input for digital delay unit 54. This is essentially a three-decade coded decimal counter 272 and associated decoding and steering logic. Counter 272 operates under control of the VCO clock pulses provided through clock generator single shot 58 over lead 298. The counter thus maintains a BCD count corresponding to tenths, units, and tens of degrees.

The BCD outputs of counter 272, in order of increasing significance, are connected to respective BCD to ten line decoders 274, 276 and 278. Decoders 274, 276, and 278 are constructed identically to previously described decoders 210 and 212, and provide a low level at the output corresponding to the BCD value of the input. Only selected ones of the ten available outputs are used, namely, the zero- and one-tenths outputs of decoder 274, the zero-units output of decoder 276, and the nine-tens output of decoder 278.

The aforementioned decoder outputs are connected through respective inverters 280(a)-280(e) as inputs to a pair of AND gates 282 and 284. Inverters 280(b), 280(c), and 280(d) are connected as inputs to AND gate 282, while the outputs of inverters 280(a), 280(c), and 280(e) are connected to AND gate 284. The control input for AND gate 284 is provided directly over a lead 286, while the same signal, coupled through an inverter 288, provides the control input for AND gate 282.

Lead 286 is connected to advance-retard unit 56 (also shown in FIG. 1) which comprises a resistor R26 coupled to the positive power supply, to lead 286, and to one of the fixed contacts of a two-position switch 288, the other contact of which is open, and the moving contact of which is grounded. The connected contact of switch 288 represents the retard mode of operation. Thus, with the switch in the "retard" position, the signal on lead 286 is low, inhibiting AND gate 284, and activating AND gate 282. Correspondingly, with switch 288 in the "advance" position, lead 286 is high, conditioning AND gate 284 and inhibiting AND gate 282.

From the above description of the interconnection between decoders 274-278, inverters 280, and AND gates 282 and 284, it may be seen that for retard mode timing, AND gate 282 operates to provide a high input to OR gate 290 only when the count contained in de-

cade counter 272 is 001, i.e., the minimum possible delay. For advance mode timing, AND gate 284 provides a high input to OR gate 290 only when counter 272 is at a count of 900, i.e., a delay of ninety degrees.

Operation of counter 272 is controlled by the pseudo pulse output of OR gate 266 coupled through AND gate 52. The output of AND gate 52 is connected to the set input of a set-reset flip-flop 292, the reset input to which is provided through an AND gate 294. The latter receives as its inputs the pseudo damper signal output of OR gate 290 and the sample pulse signal produced by single shot 270. The zero output of flip-flop 292 is coupled over lead 296 to the reset input of counter 272.

For a counter 272 constructed of three series-connected Texas Instruments type SN-7490 decade units, the counter advances on a negative to positive transition of the clock signal, while a high level at the reset input returns all of the outputs to zero. Thus, as long as flip-flop 292 is reset, its zero output is high and counter 272 is held at a count of zero.

Upon arrival at an output from pseudo pulse generator 32, AND gate 52 operates and sets flip-flop 292. The zero output of the flip-flop then goes low, freeing counter 272 to advance in response to the clock pulses on lead 298. Decoders 274-278, inverters 280, and AND gate 282 provide an output through OR gate 290 after a single advance of counter 272 for retard operation, while decoders 274-278, inverters 280, and AND gate 284 provide an output through OR gate 290 after 900 counts (i.e., ninety degrees) for advance mode operation. In either case, the output of OR gate 290 actuates AND gate 294 and reset flip-flop 292, thereby terminating the operation of counter 272. Since each pseudo pulse reactivates the counter by setting flip-flop 292, the result is a series of pulses delayed with respect to the output of the pseudo pulse generator, either by 1 count or 900 counts for retard or advance mode operation, respectively.

One further point may be noted. Referring to Tables 1 and 2 above, it may be seen that for an eight-cylinder engine, the advance and retard mode pseudo damper pulses coincide. Thus, delay of the pseudo pulse generator outputs for advance timing of an eight-cylinder engine is not actually necessary. Actuation of the delay unit is therefore inhibited for an eight-cylinder engine by means of a diode CR14 connected to the junction between lead 286 and resistor R26 and to the eight-cylinder position of selector switch 64 by means of lead 300. With switch 64 in the eight-cylinder position, lead 300 is grounded, which overrides the operation of advance-retard switch 288 and assures the presence of a low signal level on lead 286.

Turning to FIG. 8, there is illustrated the important functional aspects of advance-retard logic unit 68, averaging logic unit 70, main counting logic unit 72, advance-retard switch 78, timing angle display unit 80, RPM counter unit 82, and RPM display unit 84.

As previously explained, timing is measured by counting the number of VCO pulses (each of which corresponds to 0.1°) between a spark pulse and the pseudo damper pulse for the associated cylinder. For retard timing, the pseudo pulse initiates the counting interval and the spark pulse terminates the counting interval. Conversely, for advance timing, the spark pulse initiates the counting interval and the pseudo pulse terminates the counting interval.

As illustrated in FIG. 8, the counting interval is defined by a set-reset cycle flip-flop 302 formed of a pair of cross-coupled NOR gates 304 and 306. Flip-flop 302 is set through a NAND gate 308 and reset through another NAND gate 310. The inputs to NAND gate 308 are provided by a further pair of NAND gates 312 and 314, while the inputs to NAND gate 310 are provided by a pair of NAND gates 316 and 318. The spark pulse from spark signal processor 24 provides one input to NAND gates 314 and 316, while the pseudo damper pulse signal from digital delay unit 54 provides an input to NAND gates 312 and 318. Control inputs for NAND gates 312 and 316 are provided over lead 320; this signal is high when the system is operating in the retard mode. A separate control signal is provided over lead 322 for NAND gates 314 and 318; this signal is high when the system is operating in the advance mode.

The signal levels on leads 320 and 322 are controlled by advance-retard unit 78. This comprises a pair of inverters 324 and 326, the outputs of which are respectively connected to leads 320 and 322 and the inputs of which are connected to the positive power supply through separate resistors R27 and R28. Also connected to the inputs of inverters 324 and 326, respectively, are the fixed retard and advance contacts of a two-position switch 328, the moving contact of which is grounded. When switch 328 is in the retard position, the output of inverter 324 is high, conditioning NAND gates 312 and 316. Conversely, with switch 328 in the advance position, the signal on lead 322 is high, conditioning NAND gates 314 and 318.

NAND gates 308 and 310 operate as OR gates with inverted inputs, i.e., provide a high output if either input is low. Thus, for retard mode operation, flip-flop 302 is set through NAND gates 308 and 312 by the pseudo damper pulse and is reset through NAND gates 310 and 316 by the next spark pulse. For advance operation, flip-flop 302 is set through NAND gates 308 and 314 by the spark pulse and is reset through NAND gates 310 and 318 by the succeeding pseudo damper pulse.

The one output of cycle flip-flop 302 is connected over lead 330 to a further pair of NAND gates 332 and 334, control inputs for which are provided respectively over leads 322 and 320. NAND gates 332 and 334 are coupled to another NAND gate 336 which acts as an OR gate with inverted inputs and thus provides a high input to a further NAND gate 338 whenever cycle flip-flop 302 is set.

The other input to NAND gate 338 is provided over lead 340 by the VCO output signal from phase locked loop 30. The output of NAND gate 338 is coupled to the advance input of a "divide by 128" counter 342 comprising part of the averaging logic unit 70. Counter 342 may be constructed in conventional fashion of commercially available integrated circuit units to provide an output transition of desired polarity for every 128 input pulses.

The running count output of counter 342 is stored in an up-down counter 348 comprising part of main counting logic unit 72.

Up-down counter 348 may be constructed in well known fashion using commercially available integrated circuit units, such as Texas Instruments type SN-74192 up-down BCD decade counters, or the equivalent. Four such counters are connected in series to provide a four decade (9999 count) capacity. Each decade unit has a

count-up control input, a count-down control input, a reset control input, and a load (or preset) control input. Count direction is determined by pulsing either the count-up or count-down input while maintaining the other input at a high level, with state transition occurring at the negative-to-positive transition of the counting pulse. A high level for the reset input returns all the outputs to zero, while a low level for the load input allows preprogramming of each bit of the BCD output, i.e., presetting a particular count. For this purpose, each counter unit is provided with four data inputs corresponding to the four output bits. A low level for the load control input sets the counter to the levels then appearing on the data inputs.

Using four BCD counter units as described above, the "count-up" control input for the first decade is coupled over lead 346 to the output of "divide by 128" counter 342, through a single shot 344. This converts the counter level transition representing every 128th input into a narrow pulse to advance up-down counter 348. The reset inputs for the three least significant decades are provided in common over lead 349 for sequencing logic unit 76 as described below, while the same signal, coupled through an inverter 350, operates the load control input for the fourth or most significant decade. The load inputs for the first three decades are not employed, nor is the reset input for the fourth decade.

The data to be entered in response to the load input for decade four are provided at the inputs denoted B1-B4. Input B1, corresponding to the least significant bit (2^0) of the fourth decade, is coupled to a positive level while the three most significant bit inputs B2-B4 are grounded. This produces a count of 1 in the fourth BCD decade whenever the load input goes low. Note that the latter occurs simultaneously with the resetting of the first three decades. Thus, when the reset signal is provided over lead 349, decades 1-3 are reset, and decade 4 is set to a count of 1. In other words, counter 348 is reset to a BCD count corresponding to decimal 1000, rather than to a count of 0.

As will be recalled, NAND gate 338 operates only during the counting intervals between an ignition pulse and the associated pseudo damper pulse. Thus, the number of VCO pulses produced at the output of NAND gate 338 represents the total number of tenths or degrees of advance (or retard) of all of the cylinders which have fired from the time that counting began. Correspondingly, the number of pulses produced by the output of single shot 344 represents $1/128$ of the total number of tenths of degrees. Under these conditions, if it is assumed that counter 348 is reset every 128 counting intervals, it may be seen that the count stored in counter 348 just before reset equals the average value of the advance (or retard) of the cylinders firing since the last reset.

However, it will be recalled that counter 348 is reset to 1000 (decimal) rather than to zero, whereby the count stored is always 1,000 greater than the actual average count. This is to permit comparing the actual timing angle with a positive and negative tolerance for timing angles of zero degrees (i.e., at top dead center) to determine a level of acceptability. This is accomplished by comparison logic unit 88, hereinafter described.

Another point to be noted is that the pseudo pulses are not actually synchronous with the top dead center positions, but are displaced 45° . Thus, the count stored

in counter 348 exceeds the actual average by an additional 450 counts. There is always an excess, rather than a deficit since the pseudo pulse generator and the digital delay units described above provide the pseudo pulses 45° "early" for retard timing and 45° "late" for advance timing. The timing interval is thus always 45° too long.

The excess count is removed by subtracting 450 counts from counter 348 once during each 128 interval cycle. This is accomplished by pulsing the "count-down" input 450 times while holding the "count-up" input high. The circuitry for controlling this operation will be described shortly in connection with FIG. 9.

Utilization of the count stored in register 348 is accomplished by transferring the count just before reset (and after subtraction of the 450 count offset) to a 13 bit latch circuit 351. This may be constructed in conventional fashion of a plurality of multiple bit latch units, such as Texas Instruments type SN-7475 (4 bits), type SN-74100 (8 bits), etc. Latch circuit 351 is controlled by a "degree strobe" signal on lead 352 generated by sequencing logic unit 76, hereinafter described. The output of each latch follows the associated input when the strobe signal is high, and locks in and stores whatever count is then present at a high to low transition.

The count contained in the 12 bits of latch 351 corresponding to decades 1-3 of counter 348 are displayed visually by means of display unit 80. This is constructed conventionally of three seven-segment display elements 354, 356, and 358 providing a numerical display of the tenths, units, and tens digits, respectively, of the timing angle. Display units 354-358 are controlled by three binary coded decimal to seven-segment decoder units, such as Texas instruments type SN-7446. These are illustrated for convenience as a single block 360 which receives signal inputs over 12 leads collectively denoted 362 from 13 latch circuit 351. A display blanking input for extinguishing the numerical display is provided to decoder unit 360 over lead 364 from limit logic unit 94, hereinafter described, to blank the display if the preset RPM limit is exceeded or other error detected.

In addition to numerical display elements 354-358, there is also provided a polarity display element 366 which provides a plus or minus reference for the angle display. Polarity display element 366 is connected by lead 368 to the advance contact of advance-retard switch 328, previously referred to. When the signal on lead 368 is high, i.e., if the system is in the retard mode, polarity display unit 366 exhibits a minus sign. Correspondingly, if the signal on lead 368 is low, i.e., for advance mode operation, the plus sign is displayed. The result, therefore, is a three digit display, accurate to 0.1° with a plus or minus sign to indicate advance or retard mode timing.

Also illustrated in FIG. 8 are RPM counter and display units 82 and 84. In essence, RPM counter unit 82 operates by counting the number of VCO pulses during a fixed time interval, after which the resulting count is stored in a latch circuit and displayed. RPM computer unit 82 comprises a "divide by 48" counter 370 constructed in conventional fashion and having its input provided by the VCO signal on lead 340. The output of counter 370 is provided to the advance input of a four decade BCD counter 372. A reset input is provided over lead 374 from sequencing logic unit 76, as herein-

after described. RPM display unit 84 is arranged to provide a four digit display but for convenient viewing, resolution to within only 10 RPM is provided. Thus, the outputs for the three most significant decades of counter 372 are provided to a 12 bit latch circuit 376 identical to latch circuit 351, previously described. A control input is provided over lead 378 from sequencing logic unit 78, as hereinafter described, to store the counts contained in the three most significant decades of counter 372 when the RPM counting interval is completed.

12 bit latch circuit 376 is connected to a BCD to seven-segment decoder unit 380 having separate decoder units for the respective decades. These drive three seven-segment display elements 382, 384, and 386 constituting the thousands, hundreds, and tens digits, respectively, of the RPM display. An additional seven-segment display unit 388 is provided for the units digit, but this is wired to show a constant zero output.

Turning now to FIG. 9, there are illustrated calibration count generator 74, sequencing logic unit 76, and tolerance count generator unit 92.

As mentioned above, every 128 counting intervals there must be subtracted from the count accumulated in average timing register 348 the 450 counts corresponding to the 45° offset employed to avoid the possibility of cross-over error. Removal of the offset is achieved by means of calibration count generator unit 74. As illustrated in FIG. 9, this is comprised of a "divide by 128" counter unit 390 constructed in any conventional or desired way. The counter input is provided by the one output of cycle flip-flop 302 over lead 392. Counter 390 advances on a positive-to-negative transition of the input, i.e., each time flip-flop 302 is reset, and thus counts complete cycles of flip-flop operation which define the count intervals.

The output of counter 390 is connected to single shot 394 which provides a single pulse every 128 count intervals. These pulses are provided to the set input of a set-reset flip-flop 396. The one output of flip-flop 396 is connected as a control input to an AND gate 398, the other input to which is provided by the VCO output on lead 399. The output of AND gate 398 is connected to the input of a three decade binary coded decimal counter unit 400, the decades of which are connected to three separate BCD to ten line decoders 402, 404, and 406, such as Texas Instruments type SN-7442. These are wired respectively to provide low outputs for the zero, five, and four BCD input values. Decoders 402-406 are respectively associated with the least significant and the most significant decade of counter 400. Thus, the outputs of all three decoders 402-406 are simultaneously low for a binary coded decimal count of 450 stored in counter 400.

The outputs of decoders 402-406 are coupled through respective inverters 408, 410, and 412 as three inputs to an AND gate 414. The fourth input to AND gate 414 is provided over lead 416 from the output of AND gate 398. This serves as an actuating signal for AND gate 414 in synchronism with the VCO pulses when flip-flop 396 is set.

The output of AND gate 414 is connected to a single shot 418, the positive output of which is connected over lead 420 to reset counter 400, while the negative output is provided over lead 422 to reset flip-flop 396.

Considering the above-described construction, it may be seen that every 128 counting intervals flip-flop

396 is set by counter 390 and single shot 394. This permits counter 400 to advance under control of the VCO pulses provided through AND gate 398. As the counter advances, and ultimately reaches a count of 450, the outputs of decoders 402, 404, and 406 all go low providing high inputs to AND gate 414, which then operates to trigger single shot 418. Operation of the single shot resets flip-flop 396, which disables AND gate 398. Single shot 418 also resets counter 400, returning its count to zero. Further advance in response to the VCO pulses is prevented as long as AND gate 398 remains reset.

The VCO pulses which advance counter 400 are coupled over lead 424 and inverter 426 (see FIG. 8) to the "count down" input of up-down counter 348 in main counting logic unit 72. Thus, every 128 counting intervals, counter 400 advances to a count of 450, and the advance pulses are simultaneously used to reduce the count stored in counter 348.

It should also be noted that calibration logic unit 74 may also serve to eliminate any calibration errors elsewhere in the system. These could be caused, for example, by variations in sensitivity of pickups 26 or 28, imprecise adjustment of signal processors 22 or 24, etc. In any case, by adjusting calibration unit 74 to subtract more or less than 450 pulses, e.g. 451 or 448 counts, any pickup variation or other calibration errors are thereby eliminated.

During the subtraction of the 450 calibration pulses, it is desired to prevent further operation of cycle counting flip-flop 302 and advance retard logic unit 68. For this purpose, the one output of flip-flop 396 is provided over lead 428 to a pair of inverters 430 and 432 (see FIG. 8), the outputs of which are connected respectively to leads 322 and 320. When flip-flop 396 is set, operation of inverters 430 and 432 forces the signal on leads 320 and 322 to be held low, thereby inhibiting all of NAND gates 312 through 318, 332 and 334. Thus, flip-flop 302 can not be set and NAND gate 338 cannot be conditioned to respond to VCO pulses on lead 340. Thus, neither averaging logic unit 70 nor "divide by 128" counter 390 can operate as long as flip-flop 396 is set. Thereafter, a new 128 cylinder averaging interval is permitted to begin.

Also illustrated in FIG. 9 are the essential functional features of sequencing logic unit 76. This includes an input "divide by 256" counter 434 driven by the VCO output on lead 399. The output of counter 434 is coupled to the advance input of a three decade BCD counter 438 cooperating with three BCD to ten line decoder units 440, 442, and 444, respectively associated with the least significant, middle, and most significant decades of counter 438. Decoder 440 is wired to provide separate low outputs for input counts of 1, 2, 4, and 6 while decoders 442 and 444 provide low outputs for input counts of 0 and 3, respectively. Inverters 446(a), 446(e), and 446(f) are coupled as inputs to an AND gate 448, while the outputs of inverters 446(b), 446(e), and 446(f) provide inputs to a second AND gate 450. A third AND gate 452 receives as inputs the outputs of inverters 446(c), 446(e) and 446(f), while a fourth AND gate 454 receives as inputs the outputs of inverters 446(d), 446(e) and 446(f).

All of AND gates 448-454 receive a control input over lead 456 through an inverter 458 from the output of "divide by 256" counter 434; this, in effect, strobes

all of the AND gates in synchronism with the input to counter 438.

From the above description, it may be seen that AND gates 448-454 provide outputs at counts of 301, 302, 304, and 306 of a counting cycle for counter 438. Reset, i.e., the end of each cycle, is established by providing a high level on lead 460 to the counter reset input. This is connected to the one output of flip-flop 396; thus, it may be seen that during the time that flip-flop 396 is set, i.e., during the calibration pulse count-back interval, counter 438 is maintained in a reset condition. Accordingly, the counting cycle for counter 438 begins when flip-flop 396 is reset, making the signal on lead 460 go low and permitting the counter to operate.

Counter 438 operates in response to the VCO signal on lead 436 after passing through "divide by 256" circuit 434. Thus, at counts of 301, 302, 304, and 306 after the end of the calibration count-back interval, respective AND gates 448, 450, 452, and 454 operate with the entire cycle repeating every 128 counting intervals.

The output of AND gate 448, appearing 301 counts after the beginning of the sequencing cycle for counter 438, provides the "degree strobe" signal over lead 449. This operates 13 bit latch circuit 351 to store the count there accumulated in four decade counter 348. One count later in the sequencing cycle for counter 438 (i.e., after count 302), AND gate 450 provides the "reset degree counter" signal over lead 349, previously mentioned, to reset decades 1-3 of counter 438, and through inverter 350 to actuate the load control input of counter unit 348. This presets the fourth decade of counter 348 to count the 1, completes the 128 counting interval cycle for the averaging operation. A new averaging cycle thus begins while the data previously accumulated in counter 348 for the previous averaging cycle is displayed by display unit 80.

The outputs of AND gates 452 and 454 at the 304th and 306th counts of the sequencing cycle for counter 438 are used in conjunction with the operation of comparison logic unit 88 and tolerance count generator 92, hereinafter described.

It should be noted that the relationship between the rate at which counter 438 advances, and the time required for 128 counting intervals, must be such that counter 438 does not complete its 3 decade (1000 count) operating cycle before being reset. This, or course, is to prevent generation of the sequence of pulses at the 301st, 302nd, 304th and 306th counts of the operating cycle more than once for each 128 timing intervals. Since there are always 3,600 VCO pulses per revolution, and since the maximum number of revolutions for 128 timing intervals occurs with a four-cylinder engine (i.e., two intervals per revolution or 64 revolutions per 128 counting intervals,) it may be seen that the VCO will produce up to $64 \times 3,600 = 230,400$ VCO pulses for an entire 128 timing interval cycle. Since counter 438 is driven by the VCO pulses, the input must be divided down by sufficient amount before operating the counter that the counter is advanced less than 1000 counts for 64 revolutions. Thus, the division ratio for divide-down counter 434 must exceed $230,400 \div 1,000$ or 230.4. This may be accomplished quite simply using a multiple bit binary counter. The next integral power of two greater than 230.4 is 256 (2^8), whereby the required division by 256 may be accomplished by cascade connection of a pair of 4-bit bi-

nary counters such as Texas Instruments Type SN-7493 or the equivalent.

Another important point to be noted with respect to counter 438, and the timing of the sequencing control signals provided by AND gates 448 through 454 is that any desired number of timing intervals less than 128 may elapse between the beginning of the cycle for counter 438, and the first control output, i.e., the "degree strobe" signal provided by AND gate 448. The reason for this is that even though the count contained in main up-down counter 348 advances as additional timing intervals occur between counts of 0 and 301 for counter 438, reset for counters 348 and 438 occurs regularly in a fixed relationship every 128 counting intervals. Thus the averaging process is not disturbed by the fact that an averaging cycle is not completed when the 450 count offset is subtracted out.

Stated another way, since any ignition intervals which occur during the 450 count subtraction are prevented from actuating main counter unit 348, or "divide by 128" counter 390, it may be seen that the only practical effect of ending an averaging cycle at the 301st count of the operating cycle of counter 438 is to implant the 450 count subtraction at some point within a 128 timing interval averaging cycle.

Even the actual position within the averaging cycle is of no particular concern. For example for a four-cylinder engine, 33 additional ignition intervals occur between completion of the 450 count subtraction and the "data strobe" signal since ignitions occur every 1,800 VCO pulses for a four-cylinder engine. correspondingly, for a six-cylinder engine, 64 ignition intervals pass between subtraction of the 450 count offset and the end of an averaging period while for an eight-cylinder engine, approximately 86 ignition intervals pass.

Referring still to FIG. 9, the circuitry for generating the "RPM strobe" and "RPM reset" signals is comprised of a free-running multivibrator constructed in conventional or desired way, to produce a squarewave having a period of 800 milliseconds. For example squarewave generator 462 may be constructed of a pair of single shot multi-vibrators having equal active periods coupled in a closed loop. A triggering input to assure that such a multivibrator begins to run when power is applied to the system is provided over lead 463 by the output of "divide by 128" counter 390.

The squarewave output is provided through a single shot multi-vibrator 454 to provide a pair of complementary pulse trains at the same frequency as the output of the squarewave generator. The positive output of single shot 454 (i.e., the one which goes high when the single shot is triggered) is coupled over lead 378 as the "RPM strobe" signal to 12-bit latch circuit 376 while the complementary output (which goes low when the single shot is triggered) is provided as the triggering input to a second single shot 464. The positive output of the latter provides the "RPM reset" signal over lead 374, while the complementary output constituting the "RPM limit reset" signal, and provided over lead 467, is employed by the RMP limit setting unit 96 described below. Thus, it may be seen that the "RPM strobe" and "RPM reset" signals are both positive pulse trains having a period of approximately 800 milliseconds, and delayed with respect to each other by the triggering interval of single shot 464, while the "RPM limit reset" sig-

nal is synchronous with the "RPM reset" signal but of opposite polarity.

Decade counter 372 operates for successive 800 millisecond periods to count the number of VCO pulses (divided by 48) occurring during the counting interval. The 800 milliseconds computation interval and the division by 48 to divide counter 372 are chosen because these values will conveniently produce an exact numerical value of RPM at the end of a computation interval. For example, at 100 RPM VCO 42 produces 360,000 pulses per minute or 6,000 pulses per second. If the VCO output is divided by 48 and counted for 800 milliseconds, the count accumulated in counter 372 will be $(6,000/48) \times 0.8 = 100$, i.e., the actual RPM. However other division bases and computation intervals producing the same result may obviously be used instead.

At the end of the counting interval, the "RPM strobe" signal causes 12-bit latch circuit 376 to store the count from counter unit 372, after which the counter is reset by the "RPM reset" signal. At the end of the reset interval, as determined by the active period of single shot 466, counter 372 is again permitted to run and a new count is accumulated. As previously described, the count stored in 12-bit latch circuit 376 is decoded by unit 380 and provided to the seven-segment display elements 382 through 388 to provide a measure of the average RPM over the counting interval. Still referring to FIG. 9 tolerance count generator unit 74 is comprised of a set-reset flip-flop 468 receiving its set input through a single shot 470 from the output of AND gate 454, previously described. The reset input is provided by a NOR gate 472 coupled through a further single shot 474. The ONE output of flip-flop 468 is coupled as a control input to an AND gate 476. This receives as its other input, the VCO signal over lead 436. The output of AND gate 476 provides the "tolerance (up-down)" signal for use by comparison logic unit 88 (see FIG. 1) hereinafter described.

The output of AND gate 476 is also coupled through an inverter 478 as one input to NOR gate 472, and also as the advance input to a one decade BCD counter 480. The four outputs of counter 480 are coupled to the inputs of a BCD to ten line decoder 482, the non-zero outputs of which are connected to nine fixed contacts of a tolerance selection switch 484, respectively labelled in tenths of a degree. The arm of switch 484 is coupled over lead 486 as the second input to NOR gate 472. The latter provides the triggering input for single shot 474 as previously mentioned, the signal shot output being provided as the reset input to flip-flop 468, and also to BCD counter 480.

In operation, at the 306th count of the operating cycle of three decade counter 438, AND gate 454 operates and causes flip-flop 468 to be set. The VCO pulses are coupled through AND gate 476, and inverter 478 to advance counter 480 which causes the individual outputs of decoder 482 to go low in sequence. When the particular output corresponding to the position of switch 484 is reached a low output is provided over lead 486 to NOR gate 472. Simultaneously, the inverted output of AND gate 476 is also coupled to NOR gate 472, and the latter acts as an AND gate with inverted inputs to produce a high output which triggers single shot 474. Thus, in response to the activating pulse from AND gate 454, AND gate 476 provides a succession of tolerance count pulses determined by the setting of power switch 484.

The aforementioned tolerance pulses are utilized by comparison logic unit 88 illustrated in FIG. 10. Comparison logic unit 88 is comprised of a pair of four decade up-down counters 488 and 490, preferably constructed in the same manner as previously described four decade up-down counter 348. As in the case of counter 348, counters 488 and 490 are provided with separate "count up" and "count down" control inputs, respectively labeled U and D, and load control inputs respectively labeled L. Four decade outputs denoted D1-D4 provide a maximum binary coded decimal output count of 9999. A set of preprogramming inputs, correspondingly labeled D1-D4, permit the output count to be preset when the load control input goes low. Sequential state transitions, either up or down, occur on negative to positive transitions for the U or D input with the other input held high.

Counter 488 is wired as follows: The "count up" control input is coupled over lead 484 to the "tolerance (up-down)" signal provided by AND gate 476 in tolerance count generator unit 92. The load inputs for all four decades are connected in common over lead 486 to the "load limit counters" signal provided through an inverter 492 from AND gate 454. The "count down" input is hard wired to an appropriate positive power supply level.

The "load limit counters" signal on lead 486 is also provided to the load control input for decade counter 490. However, the "tolerance (up-down)" signal is provided to the "count down" input of counter 490, while the "count up" input is hard wired to the power supply. Thus, for sequential counting, counter 488 counts up in response to the "tolerance (up-down)" signal while counter 490 counts down in response to the "tolerance (up-down)" signal.

The preprogramming inputs for both of counters 488 and 490 are provided by target count generator 90 by which the target timing angle is manually set. Generator 90 comprises three separate binary coded decimal thumbwheel switches 494, 496, and 498. Switches of this type are commercially available from a variety of sources, and are constructed to provide a binary coded decimal output pattern in accordance with a manual digit setting. The outputs are positive or negative, depending upon the signal input provided over a common input lead.

For target count generator 90, the four BCD outputs of thumbwheel switch 494 are coupled to the four D1 inputs of counters 488 and 490. Correspondingly, the respective BCD outputs of thumbwheel switches 496 and 498 are coupled respectively to the D2 and D3 inputs of counters 488 and 490. The common inputs to all of switches 494-498 are hard wired to an appropriate positive power supply level whereby the BCD outputs are in positive logic form.

With reference to the fourth decade of counters 488 and 490, it may be seen that one of the four inputs for each counter corresponding to the least significant bit of that decade is hard wired over lead 500 to an appropriate positive power supply level, while the remaining three bits of the fourth decade in both counters are grounded.

From the foregoing, it may be seen that whenever the "load limit counters" signal on lead 486 goes low, the first three decades of counters 488 and 490 are preset to the target timing angle as manually set on thumb-

wheel switches 494-496, while the fourth decade is preset to a count of 1.

Referring back to FIG. 9, it will be recalled that the "load limit counters" signal is generated at the 304th count of the operating sequence for counter 438, while the generation of tolerance pulses does not begin until the 306th count. Thus, for each cycle of counter 438, a count corresponding to the timing angle target is loaded into both of counters 488 and 490. Immediately thereafter, the tolerance pulses are provided over lead 484. Since this is coupled to the "count up" input of counter 488 and to the "count down" input of counter 490, it may be seen that the tolerance pulses increase the count stored in counter 488 and decrease the count stored in counter 490. Thus, at the end of the tolerance count interval, there is stored in counter 488 the upper limit acceptability for the timing angle, while counter 490 stores the lower acceptable limit for the timing angle.

Note, however, that because the fourth decade of each of counters 488 and 490 is preset to a count of 1, (i.e., a decimal count of 1000), the limit stored in counters 488 and 490 are in both cases 1,000 counts (or 100°) too high. The purpose of providing this offset will be appreciated by considering a situation in which it is desired to time an engine exactly at top dead center (i.e., a target angle of 00.0°) with the tolerance of plus or minus 0.5°. In that case, tolerance switch 484 (see FIG. 9) is set at 0.5, and thumbwheel switches 494-498 are set at 000. Decades D1-D3 are thus loaded with zero counts, and adding the tolerance counts to counter 488 produces a decimal count of 005. Correspondingly, subtracting the tolerance counts from counter 490 produces a count of 995, rather than (-) 005.

Since the upper and lower limit counts contained in counters 488 and 490 must be compared with the actual count contained in main up-down counter 348, considerable simplification of the comparison operation is achieved simply by adding an additional 1000 counts to the limit references and correspondingly adding 1000 counts to the actual timing angle information for purposes of comparison. As will be appreciated, this avoids the need to create polarity information for the comparison. Thus, for a target angle of 0° and a tolerance of 0.5°, upper limit counter 488 contains a count of 1005 and counter 490 contains a count of 995.

Referring back to FIG. 8, it will be recalled that main counter 348 also provides four decade capacity and is arranged to be preset to a decimal count of 1000. This is accomplished by loading a 1 into the last significant bit of the fourth decade, and zeros into the remaining bits of the fourth decade, while resetting all decades 1-3 to a zero count. Thus, the average count stored in main counter 348 is also offset by 1000, and comparison between the actual count and the target count, plus or minus the tolerance, is readily and simply achieved. However, since only the three least significant decades of the main counter 348 are coupled to the timing angle display unit 80, it will be understood that the 1000 count offset is suppressed for purposes of display, thereby avoiding possible confusion.

As previously mentioned, the limit counts stored in counters 488 and 490 are compared with the actual average timing angle to determine a range of acceptability. For this purpose, there are provided a pair of four decade comparator circuits 502 and 504 associated re-

spectively with counters 488 and 490. These comparators may be constructed in any conventional or desired way using commercially available integrated circuit components, such as Texas Instruments Type SN-74L85 4-bit comparators. These may be connected in cascade and are constructed to provide separate high level outputs indicating that a first input exceeds a second input, that the first input is less than the second input, or that the two inputs are equal.

Since comparators 502 and 504 provide individual bit matching, it may be seen that the input coding is of no concern, as long as the two inputs are similarly coded. Thus, the binary coded decimal outputs of main counter latch circuit 351 corresponding to the first three decades of main counter 348 are coupled over leads 362 to the first 12 bit positions of comparators 502 and 504 while the 13th bit output of latch circuit 351, corresponding to the least significant bit of the fourth decade of counter 348, is coupled over lead 506 to a 13th bit position of comparators 502 and 504.

Referring to FIG. 9, it will be recalled that the sequence of operations initiated by programming counter 438 include storing in latch circuit 351 (see FIG. 8) the average of the timing angle for the preceding 128 ignition intervals at count 301, followed at count 304 by the loading of limit counters 488 and 490 with the target timing angle. Thereafter, beginning at count 306, counter 488 is advanced and counter 490 is counted down in response to the tolerance pulses to define the acceptable timing angle.

The upper limit reference contained in counter 488 is compared with the actual timing angle data appearing on lead 362 and 605, while the lower limit reference in counter 490 is compared with the actual timing angle data by comparator 504. Considering first comparator 502, if the actual timing angle A exceeds the upper limit L_U , lead 508 is high and leads 510 and 512 are low. If A is less than L_U , lead 510 is high and leads 508 and 512 are low. If A equals L_U , lead 512 is high and leads 508 and 510 are low.

Considering now comparator 504, if the average timing angle A is less than the lower acceptable limit L_L , lead 514 is high, while leads 516 and 518 are low. If A is greater than L_L , lead 516 is high and leads 514 and 518 are low, while if A equals L_L , lead 518 is high and leads 514 and 516 are low.

The signal pattern appearing on leads 508-518 is utilized by limit logic unit 94 to provide a number of qualitative limit status indications by means of limit display unit 98. Limit logic unit 94 is simply a group of combinational logic elements wired to interpret the limit data provided by comparators 502 and 504. For example, if lead 508 is high, then it is known that the actual timing angle exceeds the acceptable limit. Thus, a high signal level on lead 508 is coupled through a driver amplifier 520 to operate a "timing high" display light 522. Correspondingly, if the signal on lead 514 is high, then it is known that the actual timing angle is below the acceptable limit and the resulting low signal level is coupled through a driver amplifier 524 to operate a "timing low" display light 526.

As will be understood, the actual timing angle is acceptable if it is equal to either limit, or less than the upper limit and above the lower limit. These conditions are met if either lead 510 or 512 is high and either lead 516 or 518 is high. To determine the foregoing, leads 510 and 512 are coupled through an OR gate 528 to

one input of an AND gate 530. Correspondingly, leads 516 and 518 are coupled through an OR gate 532 as one input to AND gate 530. If the output of AND gate 530 is high, then it is known that the actual timing angle falls within the limits set by target thumbwheels 494-496 and tolerance switch 484. This condition is indicated by a "timing OK" display light 534.

The remaining function of the circuitry illustrated in FIG. 10 is to establish a maximum acceptable RPM level (to within a resolution of 100 RPM) and to provide an appropriate indication when the preset limit is exceeded. This function is accomplished by RPM limit setting unit 96 which comprises a pair of BCD to ten line decoder units 536 and 538, the inputs of which are respectively connected to the outputs for the third and fourth decades of RPM counter 372 (see FIG. 8). Output connections for decoder 526 are wired to provide separate low level indications for each of the ten available input combinations, while outputs for decoder 538 are provided only for input counts of 0 and 1.

The above-mentioned outputs of decoders 536 and 538 are coupled through a combinational logic circuit illustrated for simplicity as a single unit 540. This is comprised of appropriate logic elements, such as NOR gates operating with inverted inputs, or NAND gates and associated inverters. Logic circuit 540 is connected to appropriate ones of the outputs of decoders 536 and 538 and operates to provide separate high level outputs corresponding to BCD inputs for decoders 536 and 538 of 700 RPM, 800 RPM, . . . up to 1,600 RPM in 100 RPM intervals.

Each of the outputs of combinational logic unit 540 is coupled to the set input of a respective one of 10 set-reset flip-flops 542, two of which (associated with the 700 count output and the 1600 output) are illustrated at 542(a) and 542(j). The reset inputs for flip-flop 542 are connected in common over lead 468 to the "RPM limit reset" signal generated by single shot 466 (see FIG. 9) coupled through an inverter 544.

The ZERO output of each of flip-flops 542 is connected to one bit position of the 0 bit latch circuit 546. The control inputs for each of the latch elements are provided in common over lead 378 by the "RPM strobe" signal previously described. The outputs of each of the individual latch elements are connected to one of 10 fixed contacts of a 10 position single pole switch 548, the moving contact of which is connected over lead 550 to limit logic unit 94.

Referring to FIGS. 8, 9, and 10, it will be recalled that the RPM averaging cycle begins when four decade RPM counter 378 (see FIG. 8) is reset, after which counter 372 advances under control of the VCO signals coupled through divide down circuit 370 for approximately 800 milliseconds. As will be appreciated, as counter 72 advances, the BCD outputs steadily advance, reaching a maximum at the end of the counting interval. Thus, considering the outputs of decoders 536 and 538, it may be seen that the output patterns change for every 100 counts accumulated in counter 372. Correspondingly, the outputs of combinational logic unit 540 change as the number of counts in counter 372 increases. In particular with inputs to decoders 536 and 538 corresponding to counts less than 700, all of the outputs of combinational logic unit 540 are low. Since flip-flops 542 are all reset, together with RPM counter 372 at the beginning of an RPM count cycle, flip-flops all have high outputs at this time.

When the inputs to decoders 536 and 538 reach a count of 700, the first output of combinational logic unit 540 goes high, and flip-flop 542(a) is set. Then, as the input counts increase by 100, successive ones of the outputs of combinational logic unit 540 go high in turn, setting successive ones of flip-flops 542. As the flip-flops are set, successive ones of the ten bit positions of latch circuit 546 receive low inputs. However, "RPM strobe" signal on lead 378 is still low, so the outputs of the latch circuit are unaffected.

The above-described operation continues with successive ones of the latch inputs going low until the "RPM strobe signal" is generated. At that time, the outputs of latch circuit 546 go low if the corresponding flip-flop 542 has been set, but are high otherwise. As will be understood, if the RPM count at the time of the "data strobe" signal is 950, then the 700, 800, and 900 outputs of combinational logic unit 540 will have gone high to set the first three of flip-flops 542, whereby the inputs to the first three latches in latch circuit 546 will be low, while the other inputs will still be high. In response to the "data strobe" signal, these three low inputs are stored in the latches and the first three fixed contacts of switch 548 are low. The remaining contacts, of course, are high. After the "RPM strobe" signal, the "RPM limit reset" signal is generated, and all the flip-flops 542 are again reset in preparation for another RPM counting cycle. The previous counts, however, are retained by the latches.

Considering still the situation in which the RPM count is between 900 and 1000, if the moving contact of switch 548 is in the 700, 800, or 900 position, the signal provided over lead 550 will be low, which indicates that the actual RPM count exceeds maximum selected count. On the other hand, if the moving contact of switch 548 is on the 1,000 RPM position, or one of the higher RPM positions, the output on lead 550 is high, indicating that the actual average RPM is still below the acceptable maximum.

Referring again to limit logic unit 94, a high input on lead 550 is coupled through a driver amplifier 552 to operate an "RPM OK" light 554, while a low level on lead 550 is coupled through an inverter amplifier 556 to operate an "RPM High" light 558. The signal on lead 550 is also coupled to an AND gate 560 which may receive an external blanking signal, e.g., from a printer, over lead 562. This signal would be high unless a printout is actually in progress, while the signal on lead 550 is high unless the preset maximum RPM is exceeded. Thus, if AND gate 560 operates, the actual average RPM is acceptable. [The output of AND gate 560 is coupled through an inverter 564 and lead 364 to extinguish the timing angle display 80 when the RPM is not acceptable or simply to blank the display during a printout.]

The output of AND gate 560 is also coupled to another AND gate 566 which receives as its second input the output of AND gate 530. Since a high output for AND gate 530 indicates that the timing angle is within acceptable limits and a high output of AND gate 560 indicates a similar condition for the RPM, the conjunction of the two indicates all limits to be acceptable. This is indicated by a "limits OK" light 568 connected to the output of AND gate 566.

OPERATION

While the operation of the individual components

has been described above, a brief overall operating description is given below by way of recapitulation.

To begin operation, the advance-retard controls 56 and 78, the target timing angle switches 494-498, tolerance switch 484, and the cylinder selection switches 39, 48, and 64, are set to the required positions. Damper and spark pickups 26 and 28 are connected, and power applied to the system.

Depending on the position of the cylinder switches and the advance-retard switches, a series of pseudo damper pulses offset by 45° from the actual top dead center positions for the cylinders are generated and provided to advance-retard logic unit 68. Concurrently, the spark signal operates to lock the frequency of oscillator 42 to produce exactly 3600 outputs pulses per revolution.

Timing angle intervals defined by the spark pulse and associated pseudo damper pulses operate cycle counting flip-flop 302 to establish a succession of counting intervals during which VCO pulses are passed through NAND gate 338, divided by 128, and accumulated in up-down counter 348. Each time cycle flip-flop 302 resets, divide-down counter 390 (see FIG. 9) advances by one count. When a count of 128 is reached, flip-flop 396 is set, which resets sequencing counter 438 and activates calibration count generator 74, to subtract a total of 450 pulses from the count contained in main up-down counter 348. At the same time, both cycle flip-flop 302 and averaging counter 342 are inhibited.

When subtraction of the 450 pulses has been completed, programming counter 438 is released, and flip-flop 302 and averaging counter 342 are reactivated. When counter 438 reaches a count of 301, the "degrees strobe" signal is generated. This activates 13 bit latch circuit 351 and stores the count contained in main counter 348. Immediately thereafter, up-down counter 348 is reset by the "reset degree counter" signal, whereby the count returns to 1000 and the average value of the timing angle for the next 128 timing intervals begins to accumulate.

Thereafter, the "load limit counters" signal operates counters 488 and 490 to load the target angle. Then the tolerance count is added to counter 488 and subtracted from counter 490, and the results compared with the count stored in latch circuit 351.

Concurrently with the above, squarewave generator 462 causes operation of RPM counter 380 which updates the computed value of the average RPM every 0.8 second. If the resulting count is below the setting on maximum RPM switch 548, the RPM OK light 554 remains illuminated.

To time an engine, the operator adjusts the position of the distributor rotor and observes the value of the timing angle indicated by display unit 80. Adjustment continues until the "timing OK" light 534 goes on. The engine is then timed to within the preset tolerance limits of the target angle.

In the foregoing, there has been presented a description of apparatus for utilizing the concept of average engine timing which overcomes various objectionable features of previously proposed systems. It should be understood, however, that the description has been simplified somewhat to highlight essential features. A variety of different implementations for achieving the logical functions described are possible and within the scope of the invention, as will be apparent to one skilled in the art in light of the foregoing description.

Also, it should be noted that the system has been described in terms of a position of the damper notch pickup such that the notch is detected 130° after top dead center for cylinder No. 1 and in terms of a 45° offset of the pseudo damper pulses to avoid the possibility of crossover error. Selection of either or both of these angles is quite arbitrary and the system may readily be adapted to accommodate other angles. For example, to accommodate placement of the damper pickup in some other angular relationship to top dead center for the No. 1 cylinder, it is only necessary to rewire the outputs of decoders 210 and 212 (see FIG. 7.) Such an operation may be readily accomplished by means of suitable switches, or by jumper wires.

Correspondingly, to establish an offset other than 45° the outputs of decoders 274-278 may be wired differently than shown.

Therefore, the invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiment is therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

What is claimed and desired to be secured by United States Letters Patent is:

1. An internal combustion engine timer comprising: reference position sensing means to cooperate with an engine under adjustment to generate a reference pulse at a predetermined angular position of the engine crankshaft for each engine revolution; ignition sensing means to cooperate with the engine under adjustment to generate a pulse coincident with the firing of each spark plug; means responsive to the succession of spark pulses to generate a master pulse train having a constant number of pulses per engine revolution, each pulse thereby representing a predetermined fraction of an entire 360 degree revolution; means responsive to each reference position pulse for selecting groups of said master pulses to define a set of pseudo reference pulses, each of said pseudo reference pulses representing a predetermined angular position of the engine crankshaft with reference to top dead center position for the respective pistons, said set of pseudo reference pulses including a pulse for each cylinder of the engine; means for establishing a timing interval between each of the spark pulses and the pseudo reference pulse for the associated cylinder, said timing interval establishing means comprising means for producing a train of timing pulses and means for counting the number of said timing pulses between each spark pulse and its associated pseudo reference pulse; and means for counting the average number of master pulses generated during a succession of timing intervals as a measure of the average firing angle for all of the cylinders.

2. Engine timing apparatus as defined in claim 1 wherein said ignition sensing means comprises a pickup adapted to be electrically coupled to the output of the spark coil of the engine under adjustment, said pickup being responsive to the energy fields caused by the opening and closing of the distributor points; signal processing means coupled to said pickup and responsive to that portion of the pickup output corresponding to the opening of said distributor points to generate said spark signal.

3. Engine timing apparatus as defined in claim 2 wherein said signal processing means comprises amplifier means; circuit means for differentiating said pickup output to produce a derivative waveform including a portion corresponding to the opening of said points, the latter being characterized by a level substantially exceeding that of other portions of said derivative waveform; means for establishing an operating threshold for said amplifying means above the magnitude of all portions of said derivative waveform except the portion corresponding to the opening of said points; and means for coupling said derivative waveform to the input of said amplifying means whereby said amplifier operates only during an interval corresponding to the opening of the points.

4. An internal combustion engine timer comprising: reference position sensing means to cooperate with an engine under adjustment to generate a reference pulse at a predetermined angular position of the engine crankshaft for each engine revolution; ignition sensing means to cooperate with the engine under adjustment to generate a pulse coincident with the firing of each spark plug; means responsive to the succession of spark pulses to generate a master pulse train having a constant number of pulses per engine revolution, each pulse thereby representing a predetermined fraction of the entire 360° revolution; means responsive to each reference position pulse for selecting groups of said master pulses to define a set of pseudo reference pulses, each of said pseudo reference pulses representing a predetermined angular position of the engine crankshaft with reference to the top dead center position for the respective pistons said set of pseudo reference pulses including a pulse for each cylinder of the engine; means for establishing a timing interval between each of the spark pulses and the pseudo reference pulse for the associated cylinder, said timing interval establishing means comprising means for producing a train of timing pulses and means for counting the number of said timing pulses between each spark pulse and its associated pseudo reference pulse; and means for counting the number of master pulses during said timing interval as a measure of the firing angle for the cylinders corresponding to the respective counting intervals.

5. Engine timing apparatus as defined in claim 4 wherein said reference position sensing means comprises a pickup adapted to be positioned in non-contacting proximity to a member rotating with the crankshaft of the engine under adjustment, said pickup being responsive to the passage within its field of sensitivity of a predetermined portion of said member to generate an output pulse; and signal processing means responsive to said pickup output pulse for generating said reference pulse approximately coincident with the center of the pickup output pulse.

6. Engine timing apparatus as defined in claim 5 wherein said pickup output pulse is characterized by positive and negative portions of approximately equal duration separated by a zero signal level crossing; and wherein said signal processing means includes means responsive to said zero crossing to generate said reference pulse.

7. Engine timing apparatus as defined in claim 6 wherein said signal processing means comprises a first transistor circuit; means responsive to the level of the pickup output pulse to generate a control signal for said first transistor circuit; means to differentiate the pickup

output signal and to apply the resulting derivative signal to said transistor circuit; biasing means responsive to said control signal to establish a conduction threshold for said transistor at a predetermined level below the peak value of the derivative signal; a normally conductive second transistor circuit; means coupled to the output of said second transistor circuit for providing said reference pulse; means coupling the signal output of said first transistor circuit to the signal input of the second transistor circuit; and means for biasing said second transistor circuit to be non-conductive when said first transistor circuit is conductive, and to be conductive when said first transistor circuit is nonconductive.

8. Engine timing apparatus as defined in claim 4 wherein said master pulse train generating means comprises a digital phase locked loop responsive to said spark pulses to generate said train of master pulses at a frequency equal to a selected multiple of the spark repetition frequency.

9. Engine timing apparatus as defined in claim 8 wherein digital phase locked loop is operative to generate 3,600 pulses per engine revolution.

10. Engine timing apparatus as defined in claim 8 further including means to vary the ratio of the repetition frequency of the master pulse train to the spark repetition frequency in accordance with the number of cylinders in the engine under adjustment such that said pulse train contains a substantially constant number of pulses per engine revolution, independent of the number of cylinders.

11. Engine timing apparatus as defined in claim 8 wherein said phase locked movement comprises a voltage controlled oscillator for generating said pulse train; divider means coupled to the output of said voltage controlled oscillator; phase detector means having one input coupled to the output of said divider, and the other input coupled to said spark pulses and means coupling the output of said phase detector to said voltage controlled oscillator to adjust the frequency thereof in accordance with the phase difference between the succession of spark pulses and the output of said divider.

12. Engine timing apparatus as defined in claim 11 further including means responsive to said spark pulse to generate a DC analog of the repetition rate thereof; and means for coupling said DC analog to said voltage controlled oscillator further to control the frequency of its output.

13. Engine timing apparatus as defined in claim 12 wherein said DC analog signal generator comprises means responsive to each spark pulse to generate a further pulse of predetermined duration depending on the number of cylinders in the engine under adjustment; and means to integrate the resulting train of further pulses.

14. Engine timing apparatus as defined in claim 13, further including means to adjust the duration of said further pulses in accordance with the ratio 1:2/3:1/2 for four, six, and eight-cylinder engines, respectively.

15. Engine timing apparatus as defined in claim 13 wherein said further pulse generating means comprises a single shot multi-vibrator, means for selectively adjusting the operating period of said single shot multi-vibrator in accordance with the number of cylinders in the engine under adjustment such that the width of said

further pulses are in the ratio 1:2/3:1/2 for engines having four, six, and eight cylinders, respectively.

16. Engine timing apparatus as defined in claim 14 wherein said divider comprises counter means, means for selecting the counting base of said counter means in accordance with the number of cylinders in the engine under adjustment in accordance with the ratio 1:2/3:1/2 for engines having four, six, and eight cylinders, respectively.

17. Engine timing apparatus as defined in claim 11 wherein said divider comprises variable base counting means; and means for adjusting the base of said counting means in accordance with the ratio 1:2/3:1/2 for engines having four, six, and eight cylinders, respectively.

18. Engine timing apparatus as defined in claim 11 wherein said phase detector comprises first pulse stretching means coupled to the output of said divider and operative to convert the succession of divider output pulses into a squarewave; second pulse stretching means coupled to said spark signal generator and operative to convert the succession of spark pulses into a squarewave; a phase detector circuit coupled to the outputs of said first and second pulse stretching circuits and operative to generate a DC analog of the phase error between said squarewaves.

19. Engine timing apparatus as defined in claim 18 wherein each of said first and second pulse stretching means comprises a variable period single shot multi-vibrator; means respectively coupling said divider output and said spark pulse signals as the triggering inputs for said single shot multi-vibrators; a sensing means coupled to the output of each of said multi-vibrators, and responsive to the on and off time of the outputs thereof to provide respective DC signals representative of the difference between said on and off times; and feedback means for each multivibrator responsive to said difference signals for adjusting the period of the respective multi-vibrator to minimize the values of said difference signals.

20. Engine timing apparatus as defined in claim 19 wherein each of said sensing means comprises a first circuit responsive to the level of the single shot output when triggered; second circuit means responsive to the level of said single shot output when in its rest condition, said first circuit means including means to block a signal level corresponding to the triggered condition of said single shot, and a second circuit means including means to block the signal level corresponding to the untriggered condition of said single shot, each of said sensing means further including integrator means coupled to the output of the respective first and second circuits to generate DC analog signals corresponding to the durations of the on and off times for the associated single shots; and means coupled to the output of said integrator circuits to provide a signal representative of the difference between said DC pulse width analogs; and wherein said feedback means comprises a time constant circuit coupled to the associated single shot, a signal controlled impedance element connected in the current path of said time constant circuit, and means coupling said difference signal to said signal controlled impedance element to adjust the impedance thereof, thereby effectively varying the time constant of the time constant circuit.

21. Engine timing apparatus as defined in claim 8 wherein said phase locked loop includes a voltage controlled oscillator to produce said master pulse train;

means for comparing the output of said voltage controlled oscillator with the train of spark pulses to generate a first control signal for said voltage controlled oscillator; means to generate a DC analog of the speed of the engine under adjustment; and means for coupling said DC speed analog as a further control signal for said voltage controlled oscillator.

22. Engine timing apparatus as defined in claim 21 wherein said means for generating said DC engine speed analog comprises means responsive to each spark pulse to generate a further pulse of predetermined duration as a function of the number of cylinders of the engine under adjustment; and means to integrate the resulting train of further pulses to generate said DC analog.

23. Engine timing apparatus as defined in claim 22 wherein said further pulse generating means comprises a single shot, means for selectively adjusting the operating period of said single shot such that the pulse width varies in accordance with the ratio 1:2/3:1/2 for engines having four, six, and eight cylinders, respectively.

24. Engine timing apparatus as defined in claim 4 wherein said pseudo reference pulse generating means comprises a counter; means coupling the master pulse train as the input to said counter; pulse collecting means to provide a succession of pulses as said pseudo reference pulses corresponding to selected output count states of said counter; and means to reset said counter in response to each engine reference pulse.

25. Engine timing apparatus as defined in claim 24 wherein said pulse collecting means includes a first logic circuit to select two counts per engine revolution corresponding to two of the four pseudo reference pulses for a four-cycle engine; second logic means to select three counts per engine revolution corresponding to three of the six pseudo reference pulses for a six-cylinder engine; a third logic circuit to select four counts per engine revolution corresponding to four of the eight pseudo reference pulses for an eight-cylinder engine; and means for selectively actuating said first, second, or third logic circuits.

26. Engine timing apparatus as defined in claim 25 wherein said master pulse train is a frequency of 3,600 pulses per engine revolution; and further including means coupled to said counter to generate a strobe pulse having a duration equal to one pulse of said master pulse train each time the state of said counter increases by 100 counts; and means to condition said first, second, and third logic circuits in response to said succession of strobe pulses.

27. Engine timing apparatus as defined in claim 24 adapted to measure the timing angles of engines designed to fire before or after the top dead center position for each piston and including means to select retard mode operation for said apparatus corresponding to an engine designed to fire after top dead center, and to select advance mode operation for said apparatus corresponding to an engine designed to fire before top dead center; means responsive to selection of the advance mode of operation to delay each pseudo reference pulse for an interval corresponding to a predetermined number of pulses of said master pulse train; and responsive to selection of the retard mode of operation to pass said pseudo reference pulses with essentially no delay.

28. Engine timing apparatus as defined in claim 27 wherein said delay means comprises a further counter;

means for coupling said master pulse train to the input of said counter; logic circuit means coupled to the output of said counter to generate a pulse at a predetermined count corresponding to the desired delay interval; means to reset said counter in response to said delay pulse; and means to restart said counter in response to the next pseudo reference pulse following a reset.

29. Engine timing apparatus as defined in claim 24 wherein said apparatus is adapted to measure the timing of engines designed to fire both before and after the top dead center position of its pistons and including means to select retard mode operation for adjusting an engine designed to fire after top dead center, and to select advance mode operation for adjusting an engine designed to fire before top dead center; means responsive to selection of the retard mode of operation to generate each of said pseudo reference pulses at a position in the engine revolution cycle corresponding to 45 degrees before top dead center for each piston; and means responsive to selection of the advance mode of operation to delay each pseudo pulse such that the same appears at a point in the engine revolution 45° after top dead center for the associated cylinder.

30. Engine timing apparatus as defined in claim 29 wherein said delay means comprises a further counter means for coupling said master pulse train to the input of said counter; logic circuit means coupled to the output of said counter to generate a delayed pulse at a predetermined count corresponding to the desired delay interval; means to reset said counter in response to said delayed pulse; and means to restart said counter in response to the next pseudo reference pulse following a reset.

31. Engine timing apparatus as defined in claim 24 wherein said apparatus is adapted to measure the timing of engines designed to fire both before and after the top dead center position of its pistons and including means to select retard mode operation for adjusting an engine designed to fire after top dead center, and to select advance mode operation for adjusting an engine designed to fire before top dead center; means responsive to selection of the retard mode of operation to generate each of said pseudo reference pulses at a position in the engine revolution cycle corresponding to 45° before top dead center for each cylinder; means responsive to selection of the advance mode of operation to delay each pseudo pulse such that the same appears at a point in the engine revolution 45° after top dead center for the associated cylinder; means for selecting the number of cylinders in the engine being adjusted, and means responsive to selection of an eight-cylinder engine to inhibit the operation of said delay circuit, thereby preventing said delay for advance mode operation.

32. Engine timing apparatus as defined in claim 24 adapted to measure the timing angles of engines designed to fire before or after the top dead center position for each piston and including means to select retard mode operation for said apparatus corresponding to an engine designed to fire after top dead center, and to select advance mode operation for said apparatus corresponding to an engine designed to fire before top dead center; means responsive to selection of the advance mode of operation to delay each pseudo reference pulse for an interval corresponding to a predetermined number of pulses of said master pulse train; and

responsive to selection of the retard mode of operation to pass said pseudo reference pulses with substantially no delay; means for selecting the number of cylinders in the engine under adjustment; and means responsive to selection of an eight-cylinder engine for inhibiting operation of said delay circuit whereby said pseudo reference pulses are not delayed for advance mode operation.

33. A method of timing an internal combustion engine comprising the steps of: sensing a predetermined reference position of the engine crankshaft in relation to the top dead center position for a particular cylinder; sensing the occurrence of each ignition; generating a master pulse train having a constant number of pulses per engine revolution; selecting predetermined ones of said master pulses following the sensing of the reference position during a revolution to form a set of pseudo reference pulses each having a particular angular relationship to the top dead center position for one of the cylinders of the engine being timed; establishing a timing interval between each spark pulse and the associated pseudo reference pulse; and averaging the number of master pulses during a predetermined number of timing intervals as a measure of the average timing angle for all the cylinders.

34. A method of timing an internal combustion engine as defined in claim 33 further including the steps of displaying a visual representation of said average value of said timing angle; and adjusting the distributor rotor of the engine until the average value of the timing angle is acceptably close to the specified design value.

35. A method of timing an internal combustion engine as defined in claim 33 further including the steps of selecting the particular angular relationship between the pseudo reference pulses and the top dead center position for the associated cylinder such that, for retard operation, in which the engine is adjusted to fire after top dead center, the spark pulse always follows the associated pseudo reference pulse, and for advance operation, in which the engine is adjusted to fire prior to top dead center, the spark pulse always occurs prior to the associated pseudo reference pulse.

36. The method of timing an internal combustion engine as defined in claim 35 wherein each of said pseudo reference pulses are selected to occur 45° after top dead center for advance operation, and 45° before top dead center for retard operation.

37. The method of timing an internal combustion engine as defined in claim 36 further including the steps of displaying a visual representation of said average timing angle; and adjusting the distributor rotor of the engine until the average value of the timing angle is acceptably close to the specified design value.

38. A method of timing an internal combustion engine as defined in claim 33 wherein said step of generating said master pulse train comprises the steps of phase locking an oscillator to a train of spark pulses coincident with the ignitions of the engine under adjustment.

39. A method of timing an internal combustion engine as defined in claim 38 wherein said steps of phase locking said oscillator comprises comparing the output of said oscillator with said succession of spark pulses; and controlling the operating frequency of said oscillator in accordance with the phase difference between said oscillator output and said spark pulses.

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40. A method of timing an internal combustion engine as defined in claim 39 further including the steps of generating a DC analog representative of the speed of the engine being timed, and further controlling the frequency of said oscillator based on said DC analog signal.

41. A method of timing an internal combustion engine as defined in claim 40 wherein the steps of generating said DC analog comprises the steps of integrating the succession of spark pulses; and compensating for the different number of pulses per revolution in engines having different numbers of cylinders such that, at a

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given RPM, the result of the integration is independent of the number of cylinders.

42. The method of timing an internal combustion engine as defined in claim 41 wherein the step of compensating for said different number of cylinders comprises generating a variable width pulse in response to each spark pulse; and adjusting the width of said variable width pulse according to the ratio 1:2/3:1/2 for timing engines having four, six, and eight cylinders, respectively.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,753,082 Dated August 14, 1973

Inventor(s) Arthur R. Crawford, Glenroy W. Barnett, Richard E. Porter and Joseph R. Pottebaum

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

- Col. 2, line 57, "revoltuion" should read --revolution--.
- Col. 4, line 24, "face" should read --fact--.
- Col. 5, line 52, "particlar" should read --particular--;
- line 64, "umber" should read --number--.
- Col. 6, line 60, "throuhh" should read --through--.
- Col. 7, line 19, "34" should read --24--; line 27, "becaue" should read --because--; line 47, "(vCO)" should read --(VCO)--.
- Col. 8, line 2, "swtich" should read --switch--; line 6, "42" should read --52--; line 39, "No. 1 1" should read --No. 1--.
- Col. 11, line 1, "didode" should read --diode--; line 9-10, "extending" should read --exceeding--.
- Col. 12, line 35, "revlution" should read --revolution--.
- Col. 13, line 57, "ene" should read --end--.
- Col. 15, line 1, "operating" should read --operation--.
- Col. 17, line 4, "thorough" should read --through--.
- Col. 19, line 33, "reset" should read --resets--.
- Col. 20, line 24-25, "respectivley" should read --respectively--.
- Col. 22, line 8, "substracting" should read --subtracting--;
- line 38, "latch" should read "bit latch--.
- Col. 25, line 33, "completes" should read --and completes--.
- Col. 26, line 14, "regularly" should read --regularly--;
- line 32-33, "correspondingly" should read --Correspondingly--.
- Col. 27, line 5, "occuring" should read --occurring--.
- Col. 28, line 4, "deacde" should read --decade--; line 44, "wth" should read --with--; line 48, "otputs" should read --outputs--.
- Col. 29, line 17, "limit" should read --limit of--; line 51, "last" should read --least--.

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,753,082 Dated August 14, 1973
Inventor(s) Arthur R. Crawford
et al (PAGE 2)

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 30, line 11, "tht" should read --that--; line 66, "leds" should read --leads--.

Col. 31, line 2, "ate" should read --gate--; line 8, "illustated" should read --illustrated--; line 10, "ang" should read --and--; line 37, "coenected" should read --connected--; same line, "th" should read --the--; line 41, "0 bit" should read --10 bit--; line 55, "72" should read --372--.

Col. 32, line 2, "combination" should read --combinational--; line 23, "latchs" should read --latches--.

Col. 34, line 3, "130⁰" should read --135⁰--.

Col. 40, line 24, Claim 33, "as a a" should read --as a--.

Signed and sealed this 16th day of April 1974.

(SEAL)

Attest:

EDWARD M. FLETCHER, JR.
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