



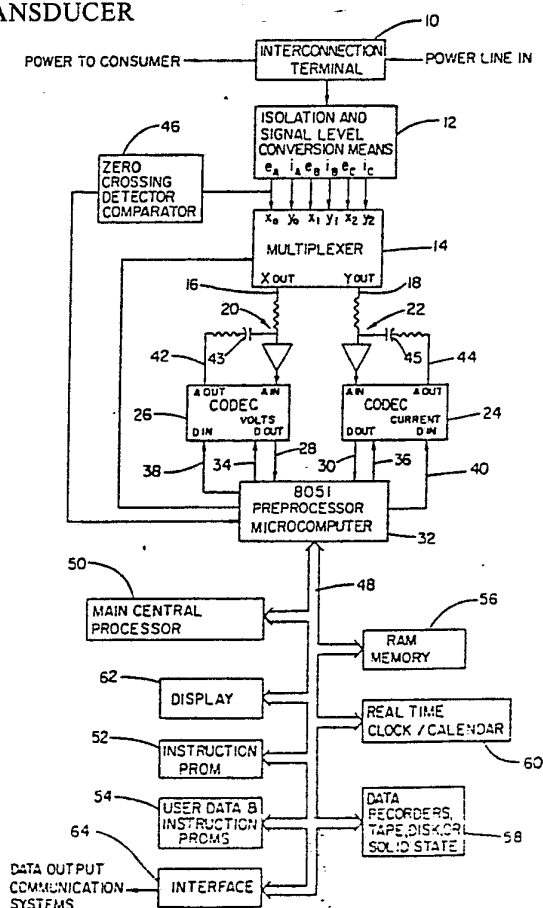
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ³ : G01R 21/06	A1	(11) International Publication Number: WO 83/ 03011 (43) International Publication Date: 1 September 1983 (01.09.83)
(21) International Application Number: PCT/US83/00232 (22) International Filing Date: 23 February 1983 (23.02.83) (31) Priority Application Number: 352,106 (32) Priority Date: 25 February 1982 (25.02.82) (33) Priority Country: US (71) Applicant: SCIENTIFIC COLUMBUS, INC. [US/US]; 1900 Arlingate Lane, Columbus, OH 43228 (US). (72) Inventor: HAFERD, James, E. ; 3827 Habitat Drive, Columbus, OH 43228 (US). (74) Agent: FOSTER, Frank, H.; Kremblas & Foster, 50 West Broad Street, Columbus, OH 43215 (US). (81) Designated States: AT (European patent), AU, BE (Eu- ropean patent), BR, CH (European patent), DE (Eu- ropean patent), DK, FR (European patent), GB (Eu- ropean patent), JP, LU (European patent), NL (Euro- pean patent), SE (European patent).		Published <i>With international search report.</i>

(54) Title: MULTI-FUNCTION ELECTRICITY METERING TRANSDUCER

(57) Abstract

An electricity metering transducer which samples voltages and currents at an interconnection terminal (10) of an electrical energy distribution system, converts those samples to digital form and computes selected electricity metering quantities. In a multiphase system current and voltage signals are multiplexed to a pair of codecs (24 & 26), one for current signals and one for voltage signals. The period of the signals being sampled is detected and used to generate a substantially nonsynchronous sampling signal so that a sample migration system is created which provides a large number of samples of a composite waveform. The steps of a digitally generated stepwise approximation of a sawtooth waveform are summed with the sequential analog samples and then removed from the digital value of each sample by software operation in order to increase the resolution of the digital to analog conversion.



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TITLE: MULTI-FUNCTION ELECTRICITY METERING
TRANSDUCER

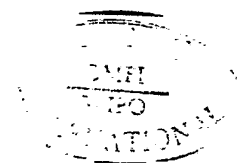
Technical Field

5 This invention relates to metering for
electricity energy distribution systems and more
particularly relates to an electronic, solid-state,
multi-function meter which can be used as a multi-
function transducer or combined with additional
10 components to provide a revenue or billing meter.

Background Art

 This application is a continuation-in-part
of my previously filed co-pending application
15 serial no. 256,058 filed April 21, 1981.

 In the electrical energy industry various
quantitative measurements are needed and are
traditionally obtained from a variety of different
devices. Each device is designed and constructed
20 to meter a particular quantity. For example, the
historic Ferraris rotating meter was used in a
variety of forms to measure real or reactive energy
and with uniquely designed attachments measures
the rate and power demand quantities. Electronic
25 kilowatt and kilovar transducers when coupled with
circuitry for integrating with respect to time are
also used for these purposes.



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With conventional technology, a power company orders and installs those devices or transducers which provide the quantities which are desired. Some manufacturers have combined more than one type of transducer into an aggregation of such devices in a single piece of equipment. Patent 4,218,737 shows two different transducers combined in a circuit which converts each of their analog outputs to digital form and then processes, stores, communicates and displays the processed data.

Prior art analog/digital conversion techniques include the sampling of a periodic analog signal such as an audio signal in a communication system.

We have found that one of the major difficulties which is experienced in attempting to apply sampling techniques to electricity metering is in obtaining metered quantities with the high accuracy which is needed for revenue metering.

Brief Summary Of The Invention

A high degree of accuracy is obtained, especially for distorted waveforms with the features and techniques of the present invention. The sampling rate is increased to improve accuracy, by utilizing high speed A/D converters called codecs which are manufactured for communication purposes. Multiphase signals are preferably multiplexed to a pair of such codecs, one for currents, one for voltages. A sample migration technique is used which effectively provides a great number of sample positions spaced throughout a composite cycle of the electricity distribution system signal. Resolution of the codecs is increased by summing the analog samples with the



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levels of a stepwise approximation of a sawtooth and then digitally subtracting the sawtooth.

Brief Description Of The Drawings

5 Fig. 1 is a block diagram illustrating the preferred embodiment of the invention.

 Fig. 2 is a table of equations illustrating some arithmetic operations performed in the preferred embodiment of the invention.

10 Fig. 3 is a schematic diagram showing the detail of a portion of the circuitry of Fig. 1.

 Fig. 4 is a graphical representation of the operation of the preferred embodiment of the invention.

15

Description Of Block Diagram Circuitry

 Fig. 1 illustrates the preferred embodiment of the invention connected into a power distribution system. It may be connected, for example, to
20 meter the energy supplied to a particular customer or it may be connected at an interconnect between two different utilities.

 An interconnection terminal 10 is provided by which the metering circuitry of the present
25 invention is interconnected to the power distribution system. An isolation and signal level conversion means 12, such as the conventional plurality of transformers, is connected to the interconnection terminal 10 for providing DC
30 isolation from the power distribution system and amplitude reduction to amplitudes which are compatible with the solid state circuitry. At its outputs it provides voltages and currents for each of the input phases.



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These output voltages and currents are applied to the inputs of a multiplexer 14. As illustrated, the voltage signals are multiplexed to a voltage output terminal 16 while the current signals are multiplexed to the current output terminal 18. The multiplexer is operated to simultaneously connect the voltage and current of a single phase to the multiplexer output and to periodically sequence through these voltages and currents of all the phases on a rotational basis.

These simultaneous voltage and current output pairs at the terminals 16 and 18 are applied to analog summing circuits 20 and 22. Each analog output signal from the multiplexer is summed with a periodic sawtooth signal.

The sum of the sawtooth signal and the analog signal is applied to a coder/decoder type of A/D converter known as a codec. One codec 24 receives the current signal sum and the other codec 26 receives the voltage signal sum. The sums are applied to the analog input of the A/D portion of each codec. The digital output terminals 28 and 30 of the codecs 26 and 24 are connected to input ports of a preprocessing microcomputer 32 which is preferably a type 8051.

The control inputs 34 and 36 to the codecs 26 and 24 are connected to output ports of the preprocessor 32 so that they are controlled by the preprocessor 32. Similarly, the multiplexer is also connected to the preprocessor 32 for control by it.



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As described more completely below preprocessor 32 generates in digital form a step wise approximation of a sawtooth signal. This digital sawtooth is generated as a series of digital words which are serially output to the digital inputs 38 and 40 of the D/A portions of the codecs 26 and 24. Each codec then converts each word to its corresponding level and together they provide the sawtooth which is applied from the codec analog outputs 42 and 44 through DC removing capacitances 43 and 45 to the analog summing circuits 20 and 22. The analog sawtooth signals are summed with the analog signals appearing at the outputs 16 and 18 of the multiplexer 14.

A comparator circuit 46 is used as a zero crossing detector. Its input is connected to one of the outputs of the isolation and signal level conversion means 12. As illustrated it is preferably connected to a signal which is proportional to the voltage of one phase of the power distribution system. The zero crossing detector 46 compares that instantaneous voltage to zero volts for detecting when the voltage of that phase makes a transition from a positive voltage to a negative voltage, that is when it passes through the zero volt level. Upon detection of that zero volt transition, the output state of the zero crossing detector 46 changes and that change of state is applied to an input port of the preprocessor 32.

As also illustrated in Fig. 1, the preprocessor 32 is connected through a conventional data, address and control bus 48 to a main central processing unit 50 as well as a variety of memory



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components in the form of an instruction prom 52,
other data and instruction proms 54, ram memory
56 and data recorders 58 such as tape, discs or
solid state memories. The bus also connects the
5 central processor 50 with a real time clock and
calendar 60, display circuitry 62 and an interface
64 for permitting the output of data from the
system in communication with other systems.

The codecs 24 and 26 are preferably companding
10 codecs such as the MK5116 sold by Mostek. A
companding codec has a transfer characteristic
which results from the fact that its range of
analog values is divided into amplitude intervals
called chords. The chords are arranged
15 logarithmically to the base two. The range or span
of each chord is double that of its immediate lower
predecessor. Each chord is divided into 16 step
values. There are 8 positive and 8 negative chords.
Each analog level is specified by a 0 or a 1
20 indicating a plus or minus signal, three chord
bits and four step value bits.

Each codec is a coder/decoder which means one
portion of each codec encodes an analog signal,
that is converts it from analog to digital form,
25 and the other portion decodes it, that is converts
it from digital to analog form. The analog to
digital portion uses the conventional rounding off
technique. It converts each analog sample level
to the nearest adjacent discrete incremental level
30 in accordance with the bit resolution of the A/D
converter.



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Instead of using a multiplexer, one codec could be used for each of the current and voltage signals of each phase. In that event the multiplexing function would effectively be performed by the preprocessing microcomputer 32.

Circuit Operation

In the operation of the preferred embodiment illustrated in Fig. 1, the current and voltage signals of each phase are sequentially applied by the multiplexer in simultaneous pair for each phase to the summing circuits 20 and 22.

Although the analog current and voltage signals are summed with the sawtooth referred to above, for purposes of initial discussion it may be assumed that the analog signals from the multiplexer 14 are essentially the same at the analog inputs to the codecs. Thus, for purposes of initial explanation, the sawtooth signal may be considered to be small relative to the analog signals.

The analog current and voltage signals are converted to digital form by codecs 24 and 26 under the control of the preprocessor 32. Although analog input signals are continuously applied to the analog input terminals of the codecs, the actual sample taking over a short interval is accomplished in the control of the codec by the preprocessor 32 which actuates the sample taking by each codec. The data for each sample is then serially output from the codec to the preprocessor 32.



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For each voltage sample the preprocessor 32 computes the square of the voltage and adds it to an accumulator. A single accumulator sums the voltage square for all phases. Because the voltages for all phases are approximately equal, the per phase voltage can later be determined to a reasonable approximation. The real power and the reactive power are also computed for each phase in accordance with the equations I and II and then added to the appropriate one of six accumulators, one for real power for each phase and one for reactive power for each phase. In addition to the seven accumulated quantities described above, a timer/counter accumulates the elapsed time interval over which the samples were taken. This correspond to N in the equations of Fig. 2. Therefore, in summary, there are preferably eight accumulators for a three phase system.

To use the circuitry as a transducer, each of these quantities may then be output either by display or communication to further circuitry so that the device at the output of the preprocessor 32 would provide data for voltage, current, real power and reactive power. We prefer that it also be connected to the main computer 50 and other circuitry structure illustrated in Fig. 1 so that further computations can be made from this data to provide all of the variety of data which is used by the art for billing purposes.



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Fig. 2 illustrates the equations used by the preprocessor 32 and the main microprocessor 50 in computing the voltage, current, power and reactive power for all three phases. The results of those computations may be used in making further computations of the other quantities desired by the art. The preprocessor 32 illustrated in Fig. 1 does not do all of the calculations. Instead, the values described above together with the elapsed time are merely output through the bus 48 to the main processor 50 when a request signal is transmitted by the main computer 50. It then completes the calculations and makes the additional ones. The accumulations in the preprocessor 32 are reset to zero and operation continues.

Because even codecs are limited in the speed with which they can perform their operations, only a limited number of samples may be taken during each cycle of the electricity distribution system. However, by taking the samples at different positions in successive cycles, a considerably greater number of sample positions are used over a composite cycle. It is therefore desirable that the sample position migrate along the composite waveform as succeeding samples are taken in order to obtain a large number of sample positions.

This is accomplished in the present invention by choosing a sampling frequency which is relatively asynchronous with the electricity distribution system. The frequency of the distribution system signal is continuously monitored and from it a frequency is calculated which is not an integral multiple of the distribution system frequency. This causes the sample positions to migrate throughout the composite waveform cycle.



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By selecting the sampling frequency in accordance with the present invention, sample migration may be accomplished for improving the accuracy of the metered quantities and at the same time permitting simple yet accurate determination of the quantities of current voltage, volt-amps, real power and reactive power at an interconnection point in the supply line regardless of whether the load is wye or delta connected.

As is well known to those skilled in the art, the line currents observed at an interconnection point in the line are not the same as the currents in a delta connected three phase load. Therefore, metered quantities such as VA, which depend upon current cannot be obtained directed from the current samples.

However, the values of reactive power in Vars and real power in Watts as calculated from equations I and II of Fig. 2 can be used to compute volt-amperes in accordance with equation III.

As can be seen in equation II, real power for each phase is computed by multiplying the instantaneous voltage and current samples for each sample pair for each phase and summing or accumulating these N products for each phase and dividing the accumulated products by N, the number of samples.

As seen in equation I, reactive power is the component in quadrature with the real power. Reactive power is therefore the product of an instantaneous voltage sample multiplied by the current which leads the voltage by 90° , that is with an instantaneous current sample which is 90° ahead of the voltage sample.



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Therefore, if the consecutive samples for each phase can be taken at 90° intervals, then the reactive power may be determined by multiplying each voltage sample by the immediately preceding current sample for the same phase. Because the samples of each phase are taken in rotational sequence, if a sample is taken every 30° then each phase will be sampled every 90° . This is illustrated in Fig. 4(D).

10 This is accomplished by first detecting the period of the distribution system signal. The period is detected by the preprocessor which times the time elapsed between the detected zero crossings. This is done simply by initiating the operation of a timer at one zero crossing and stopping the timer when the next zero crossing is detected. The elapsed time is thus the period of the distribution signal.

20 The preprocessor then divides that period of the distribution signal by four times the number of phases times an integer to give a sample period which will space the samples for each phase very 90° . For a three phase system, the distribution signal period is divided by 12 to space the samples every 30° which is every 90° for each phase. For example, if the distribution system signal is exactly 60Hz the sample period which would give exactly a 90° spacing of samples in each phase will be 1.388 milliseconds (not rounded off).

30 In order to accomplish the desired sample migration, a second time interval is then added to the first time interval. The second time interval is small relative to the first time interval and in



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the preferred embodiment in one microsecond. This sum of the small second time interval and the first time interval is then used by the preprocessor 32 as the period of the sampling signal when it generates the sampling signal.

In the preferred embodiment, if the distribution system signal is exactly 60Hz the sample period would become 1.389 milliseconds. It should be noted that adding a small time interval would include adding a negative small time interval, for example subtracting one microsecond to give a sample period of 1.387 milliseconds.

The result of adding this small second time interval is that each sample is spaced 1 microsecond beyond the spacing which would give exactly 30° spacings between all samples. Thus, for each phase, samples are 3 microseconds from being exactly 90° apart. However, this error has an insignificant effect on accuracy yet causes the sample migration which greatly increases the accuracy of the metered quantities.

It should be remembered that, although the samples migrate, all samples are migrating so that a particular sample of a phase is always no more than 3 microseconds away from being 90° phase shifted from its immediately preceding sample. Due to the migration of the samples during successive cycles of the distribution system signal, samples will be spaced every one microsecond over a composite cycle representing many cycles of distribution system signals.



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The migration sequence will repeat each time a sample migrates through a total of 90° . Therefore, if the distribution system signal is exactly 60Hz then 90° represents 4,166 microseconds. Since the samples are spaced at 1 microsecond intervals, there will be 4,166 spaced sample positions for the composite cycle. Since one sample is taken every 1.389 milliseconds then 4,166 samples will require 5.78 seconds. Thus, the samples will migrate through all 4,166 samples each 5.78 seconds.

We have found a source of inaccuracy with the codecs which is related to the fact that they, like most A/D converters, round-up or round-down an analog sample to whichever of the adjacent, discrete, incremental levels is nearest. Because the digital samples are accumulated, the error is also cumulative.

This error is significantly reduced in the present invention by generating a pair of analog sawtooth signals, one for voltage and one for current. Different levels of the sawtooth are added at different times to different samples of the identical signal. Each sum is converted to digital form and then the value of the sawtooth in digital form is subtracted out. The differences are then time integrated.

In order to accomplish this the sawtooth is generated in digital form by the preprocessor 32. The sawtooth is generated by first detecting the peak amplitude of the voltage signal and the peak amplitude of the current signal from one phase of the electrical energy signal. These peak values are then used to generate two different sawtooths,



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one for the volts summing circuit 20 and one for the current summing circuit 22. The peak value is detected by the preprocessor by examination of all of the samples in companded form to determine the largest.

After obtaining the peak sample in digital, companded form the preprocessor then decrements the four chord bits for the largest sample by four if the peak is located in the 5th, 6th, 7th or 8th chord. If the peak is in the 3rd or 4th chord the chord word is decremented to the first chord and if the peak is in the 1st or 2nd chord no sawtooth is generated. The chord word, decremented as described, is then used as the chord word for the sawtooth.

The purpose of decrementing the chord word is to obtain a sawtooth having a peak to peak value which is equal to the amplitude interval between the discrete incremental levels of the chord in which the peak was measured.

The preprocessor 32 also generates successive 4 bit step value words for generating the sawtooth by incrementing a 4 bit counter. Each step value word corresponds to a different one of the 16 levels of the chord. The chordword derived as described is output with each of the 16 step value words to generate in digital form a step wise approximation to a sawtooth signal illustrated in Fig. 4a.

This digital step wise approximation of a sawtooth signal illustrated in Fig. 4a is applied to the digital input of the digital to analog section of the codec. The codec converts this companded digital input to an analog output signal which is illustrated in solid lines in Fig. 4b.



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Because of the companding transfer function of the codec, the sawtooth has a substantial average or DC value corresponding to the center of the chord. This average value is eliminated from the analog
5 form by the capacitances 43 and 45 to provide a sawtooth 101 illustrated in broken lines Fig. 4b which is then summed with the analog signal from the multiplexer.

Fig. 4c illustrates an analog sample 103 which
10 is intermediate two adjacent discrete incremental levels, 105 and 107 which are characteristic of A/D converters.

As is well known in the art, the A/D converter, for each sample having the amplitude of sample 103,
15 will always generate a digital word corresponding to the discrete level 105 because of the rounding characteristic. The error of the difference between level 103 and level 105 will accumulate in the accumulators as the data is accumulated.

20 If, however, successive samples of the signal of level 103 are summed with each of 16 levels of the sawtooth 101, then some of the digital output words from the A/D converter will correspond to level 105 while others will correspond to level 107.
25 The number of samples falling at the positions 105 and 107 levels respectively will be proportional to the proportional spacing of the level 103 from the levels 105 and 107. Therefore the accumulated error described above is eliminated and resolution
30 is increased to the resolution of the 16 steps of the sawtooth.



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The sawtooth is generated in synchronism with the sample frequency computed as above. Thus, due to the sample migration, each of the 16 different ramp levels will be summed with sequential samples for the same voltage or current for the same phase in sequential rotation.

Since the peak to peak amplitude of the sawtooth is selected to be equal to the distance between discrete incremental levels of the A/D converter only for the peak of a signal, it follows that for most samples the peak to peak value will be greater than the difference between the incremental levels. However, since the sawtooth is centered about zero the same proportional principle as described above will continue to apply.

It is desirable to subtract from each digital sample of the sum of the sawtooth level and a voltage or current signal, the digital value of the particular sawtooth level which was summed with the analog signal prior to the A/D conversion.

To determine the digital word representing the sawtooth level which was added to the analog sample, the 8 bit companded word used to generate that sawtooth level must be operated upon. Because a capacitance removed the DC level from the analog signal generated by that digital word, the digital value of the DC must first be subtracted from the digital word. This may be simply accomplished by providing a look-up table for the center level of each possible chord value of the companded 8 bit words. Because there are four chord bits and four step values, a look-up table can be prepared and stored in memory for each of the 256 different



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digital words. For each digital word representing the total sawtooth level, the look-up table provides the DC value to be subtracted from it to give the sawtooth level actually added to the analog sample. After that subtraction, the result is subtracted from the total detected sample to give the digital value of the sampled voltage or current before the sawtooth was added to it.

As stated above, the real power for each phase, the reactive power for each phase, the summation time of N samples and the accumulated voltage squared for all three phases are accumulated in the memory associated with the preprocessor 32. These are then used by the main processor 50 to determine voltage in accordance with equation IV, volt-amperes in accordance with equation III, current by dividing volt-amperes by voltage and all the other metering quantities which are well known to those skilled in the art.

Fig. 3 is a schematic diagram illustrating in detail the preferred embodiment of the invention. Reference numerals identical with those of Fig. 1 are inserted to point out the corresponding circuitry. Conductors 201, 202 and 203 additionally connect to the main microcomputer 50 for control of the preprocessor 32 and together with the data outputs D0 through D7 form a part of the data, control and address bus 48 illustrated in Fig. 1.

A scaling circuit 205 is connected to the data input ports of the preprocessor 32 to provide a series of manually selectable switches 207. The appropriate scaler input is manually selected for each installation so that the digital data may be



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multiplied by the proper conversion factor to convert the digital data bits to data representing the actual voltage and current values in the distribution system.

- 5 It is to be understood that while the detailed drawings and specific examples given describe preferred embodiments of the invention, they are for the purposes of illustration only, that the apparatus of the invention is not limited
- 10 to the precise details and conditions disclosed and that various changes may be made therein without departing from the spirit of the invention which is defined by the following claims.



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CLAIMS

1. An electricity metering transducer for periodically sampling the voltages and currents at interconnection terminals of an electrical energy distribution system and for converting the samples to digital data signals and then machine computing selected electricity metering quantities from said digital data signals, said transducer comprising:
- 5 (a) an isolation and signal level conversion means having its inputs connected to said interconnection terminals of said distribution system for providing at its outputs a plurality of analog signals which are proportional to instantaneous voltages and currents at said terminals;
- 10 (b) a multiplexer having its inputs connected to the output of said isolation and signal level conversion means for simultaneously applying a selected voltage analog signal and a selected current analog signal at its inputs to a pair of output ports;
- 15 (c) a pair of analog to digital converters each having an input connected to one of the output ports of the multiplexer; and
- 20 (d) a microcomputer connected to said A/D converters and multiplexer for controlling them and for receiving digital data signals from said A/D converters.
- 25



2. A transducer in accordance with claim 1 further including a zero crossing detector means having an input connected to one of said inputs to said multiplexer and an output connected to said microcomputer for detecting the zero crossing of an electrical energy signal.
3. A transducer in accordance with claim 2 wherein said A/D converters comprise a pair of companding codecs.
4. A transducer in accordance with claim 3 further comprising:
- (a) a pair of analog signal summing means each one interposed between one of said multiplexer outputs and a different one of said codec A/D converter inputs, the other input of each of said summing means connected through a different dc removing capacitor to the analog output terminal of its associated codec; and
 - (b) means including said microcomputer for generating a companded, digital, stepped ramp function at a pair of data output ports, said data output ports being connected to the D/A input of a different one of said codecs.



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5. An electricity metering transducer for periodically sampling the voltages and current at interconnection terminals of an electrical energy distribution system and for converting said samples to digital data signals and then machine computing selected electricity metering quantities from said digital data signals, said transducer comprising:

- (a) an isolation and signal level conversion means having its input connected to said interconnection terminals of said distribution system for providing at its outputs a plurality of analog signals which are proportional to instantaneous voltages and currents at said terminals;
- (b) a plurality of companding codecs each having its A/D converter input connected to a different one of the outputs of said conversion means; and
- (c) a microcomputer connected to said codecs for controlling them and for receiving digital data signals from them.

6. A transducer in accordance with claim 5 further comprising:

- (a) a pair of analog signal summing means each one interposed between one of said conversion means outputs and a different one of said codec A/D converter inputs and the other input of each of said summing means connected through a different dc removing capacitor to the analog output terminal of its associated codec; and
- (b) means including said microcomputer for generating a companded, digital, stepped ramp function at data output ports, said data output ports being connected to the D/A input of different ones of said codecs.



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7. A method for metering an electricity distribution system comprising:

- (a) simultaneously sampling current and voltage signals of said system;
- 5 (b) sequentially applying the current signals to at least one A/D converter and sequentially applying the voltage signals to at least one other A/D converter;
- 10 (c) converting each of said applied signals to digital data form to provide a plurality of samples; and
- (d) machine computing selected electricity metering quantities from said samples.

15 8. A method in accordance with claim 7 wherein a signal for controlling the sample rate is generated by:

- (a) periodically detecting the period of said system signals;
- 20 (b) dividing said system signal period by at least ten to obtain a first time interval; and
- (c) adding a second time interval to said first time interval to obtain said control signal, said second time interval being small
- 25 relative to said first time interval.

9. A method in accordance with claim 8 wherein said period is detected within 1 μ sec interval and wherein said second time interval is also 1 μ sec.

30



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10. A method in accordance with claim 7 further comprising:

- 5 (a) generating a sampling period signal for initiating the sampling at the period of said sampling period signal by periodically detecting the period of said electricity distribution system, dividing said system period by an integral multiple of four times the number of phases and adding a second time interval to said first time interval to obtain
10 the period of said sampling period signal, said second time interval being small relative to said first time interval; and
- 15 (b) detecting instantaneous reactive power for one phase by multiplying a voltage sample of the phase by a current sample of the phase taken substantially 90° preceding the voltage sample.

- 20 11. A method in accordance with claim 10 wherein the integral multiplier is one and said current sample was the immediately preceding sample for the phase.



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12. A method in accordance with claim 7 wherein said A/D conversion includes rounding an analog sample amplitude to the nearest adjacent discrete incremental level and wherein said method further comprises:

- (a) generating a pair of periodic sawtooth signals which are frequency synchronized to said samples, one for current and one for voltage,
- each sawtooth signal having a peak to peak amplitude at least equal to substantially the magnitude of the spacing between discrete incremental levels of said A/D conversion;
- (b) before converting the analog sample signals to digital form interposing the step of summing sequentially incoming analog sample signals to sequential levels of said ramp signal and applying the resulting sum to said A/D converter;
- (c) subtracting the associated digital value of each ramp level from said digital value of each sum signal; and
- (d) time integrating the differences of said subtraction.

13. A method in accordance with claim 12 wherein said A/D conversion is a companded A/D conversion and wherein each of said ramps is generated by:

- (a) generating a digital companded, periodic stepped ramp function;
- (b) converting said digital ramp function to an analog ramp signal by means of a companding D/A conversion; and
- (c) removing any dc component from said analog ramp signal to provide said periodic stepped ramp function signal.



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14. A method for increasing the resolution of an A/D converter of the type which has characteristic discrete incremental levels and which rounds an analog sample amplitude which is interposed
5 between the incremental levels to the nearest incremental level, said method comprising:
- (a) generating a periodic stepped ramp function signal having a peak to peak amplitude at least equal to substantially the
10 magnitude of the spacing between said discrete incremental levels and having a frequency synchronized with the sampling frequency of the A/D converter;
 - (b) summing sequentially incoming analog
15 sample signal to said A/D converter with sequentially generated levels of said ramp signal;
 - (c) subtracting the digital value of each ramp signal level from the digital value of
20 its sum with an analog sample; and
 - (d) time integrating the digital difference values.



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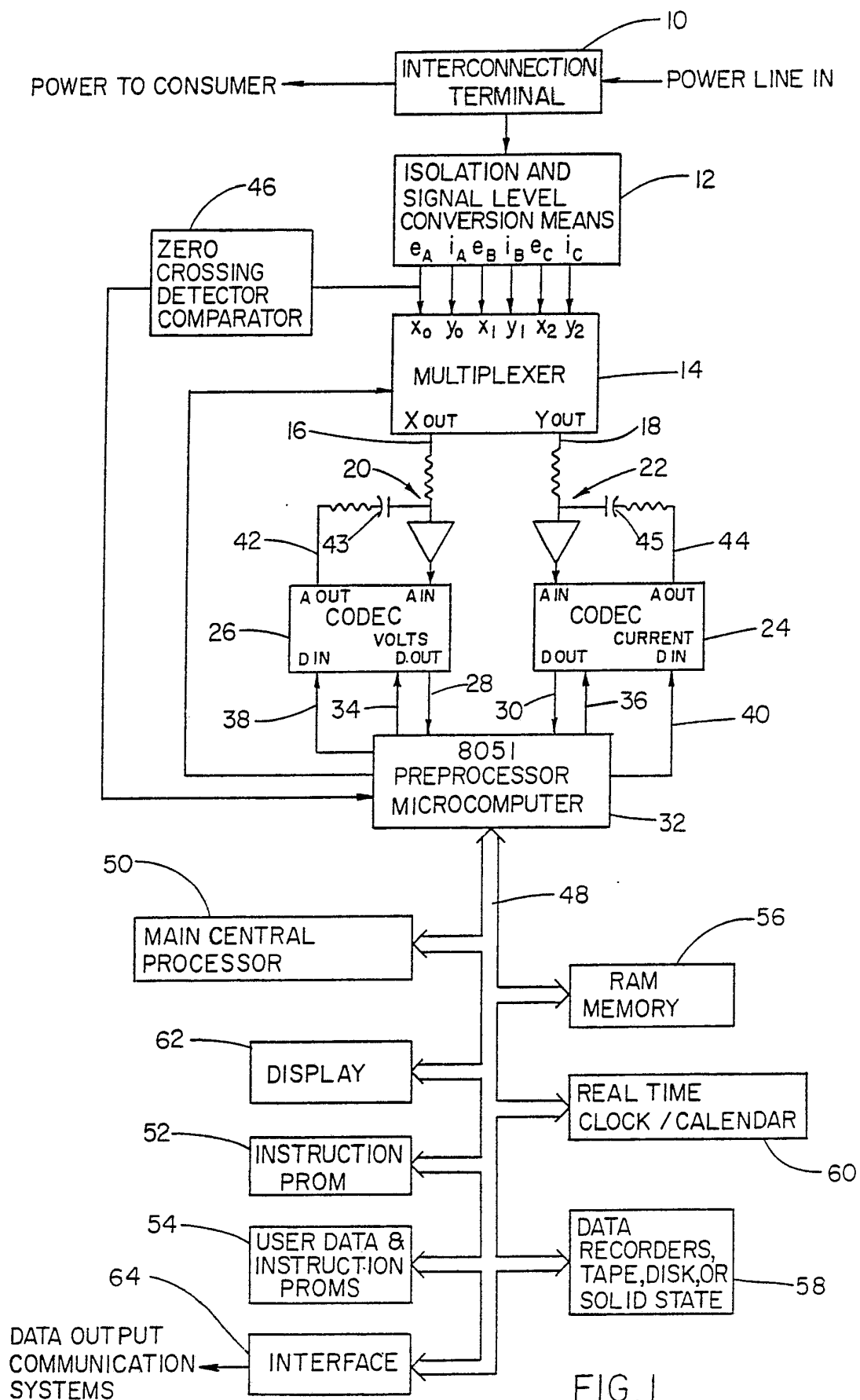


FIG. 1

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$$(I) \text{ REACTIVE POWER (VARS)} = \left(\frac{1}{N} \sum_{t=0}^N e_{\phi,t} i_{\phi,t-1} \right)$$

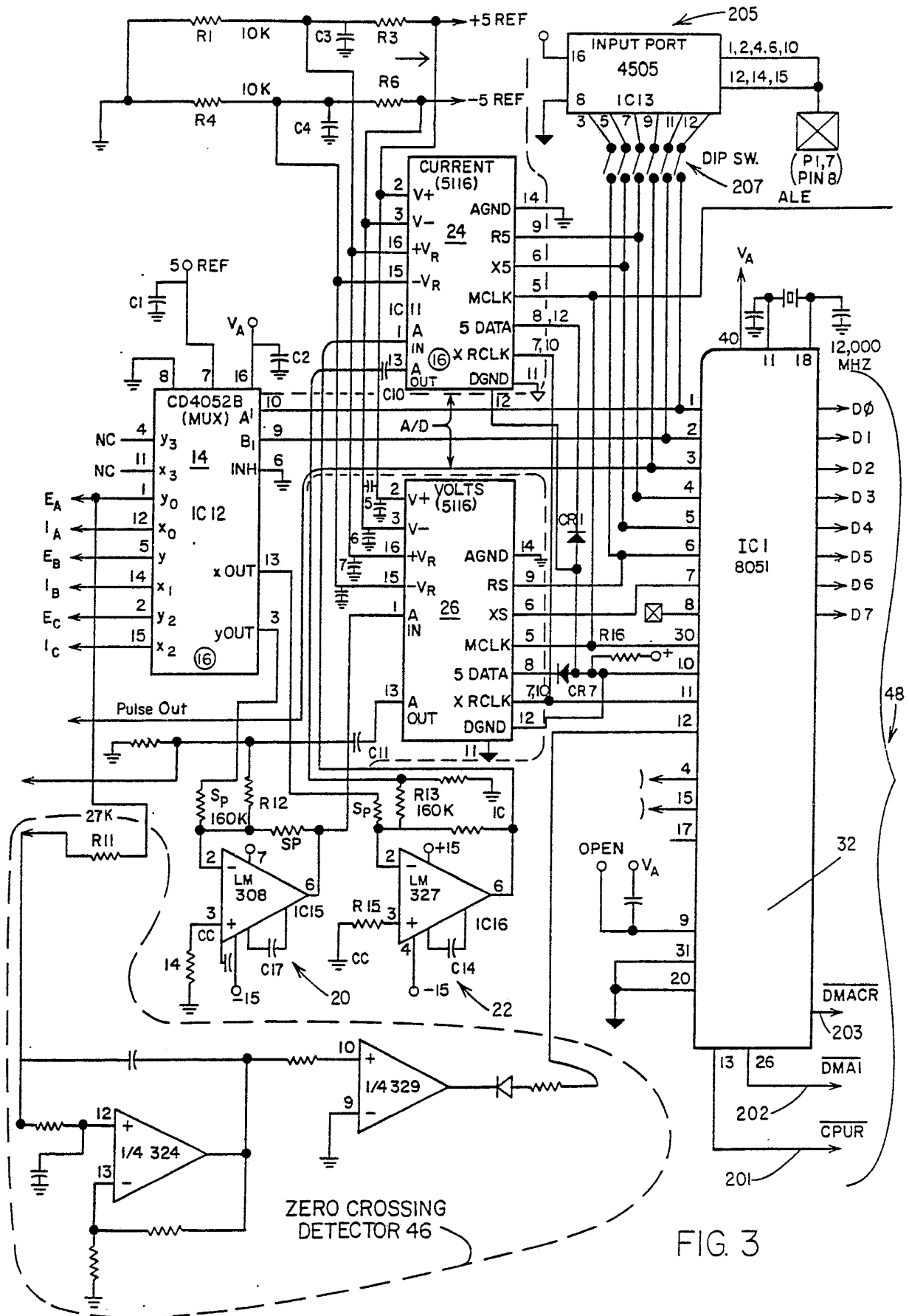
$$(II) \text{ REAL POWER (WATTS)} = \left(\frac{1}{N} \sum_{t=0}^N e_{\phi,t} i_{\phi,t} \right)$$

$$(III) \text{ VA} = \sum_{\phi=a}^c \sqrt{(\text{WATTS}_{\phi})^2 + (\text{VARS}_{\phi})^2}$$

$$(IV) \text{ V} \approx \sqrt{\frac{1}{3} \sum_{\phi=a}^c \frac{1}{N} \sum_{t=0}^N V_{\phi,t}^2}$$

FIG. 2

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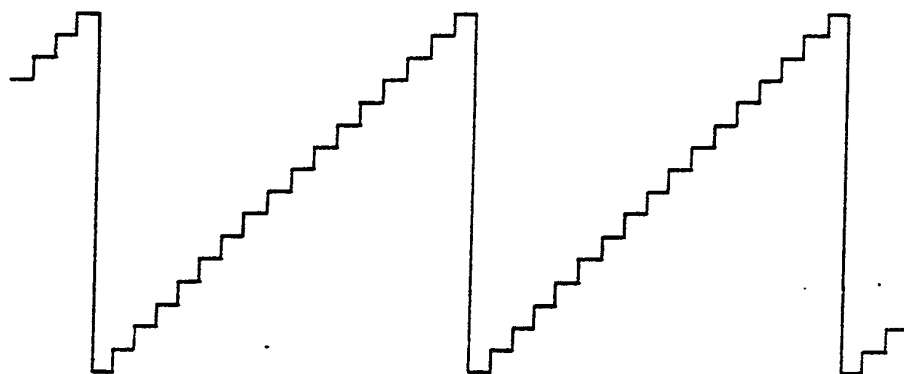


FIG. 4A

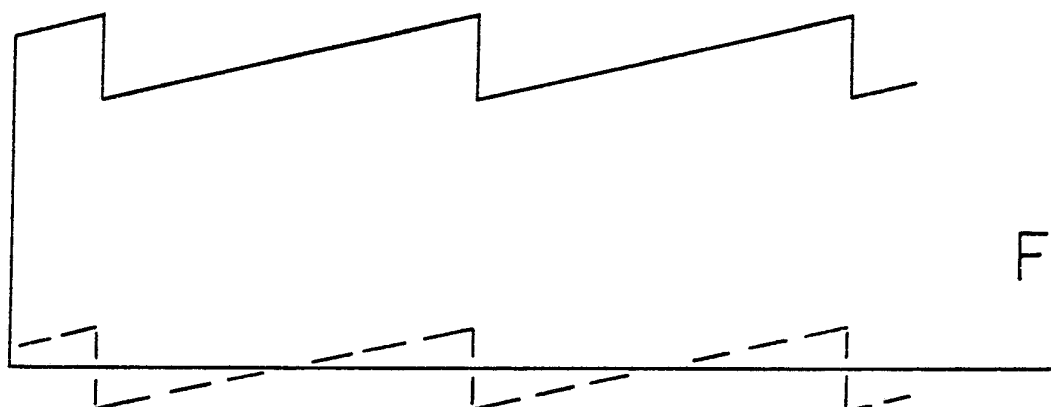


FIG. 4B

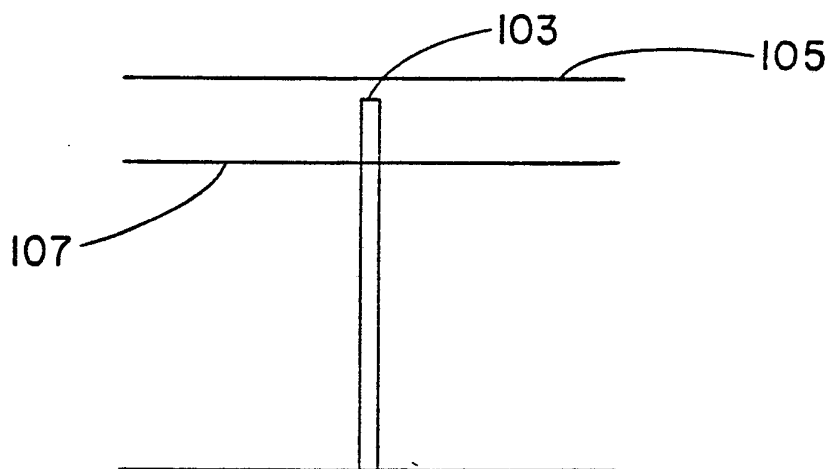


FIG. 4C

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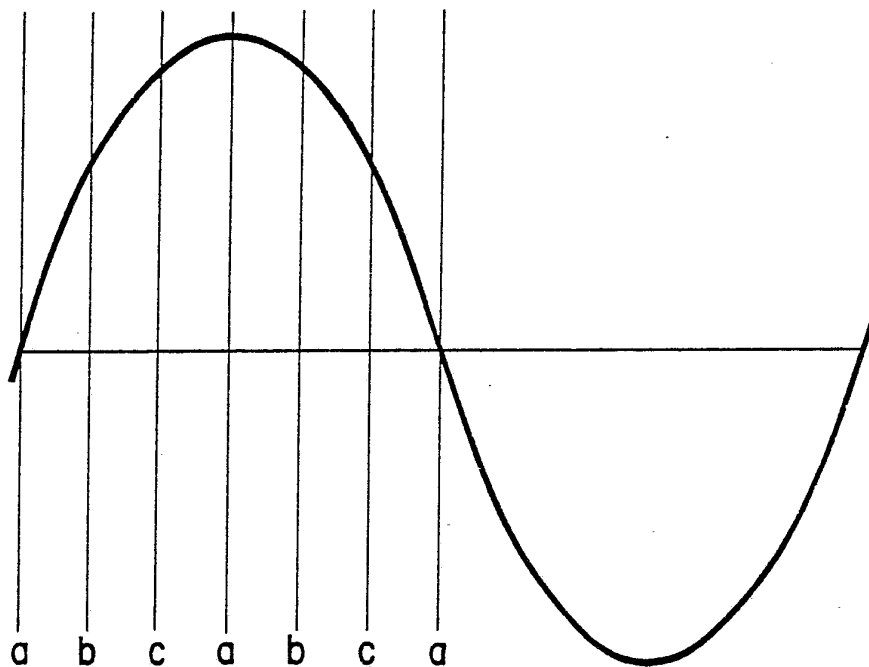


FIG. 4D

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US83/00232

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ³		
According to International Patent Classification (IPC) or to both National Classification and IPC		
INT. CL. G01R 21/06		
U.S. CL. 364/483		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁴		
Classification System	Classification Symbols	
U.S.	364/483 324/142 340/347AD, 347M, 347CC, 347SH	
Documentation Searched other than Minimum Documentation to the extent that such Documents are Included in the Fields Searched ⁵		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ¹⁴		
Category ⁶	Citation of Document, ¹⁶ with indication, where appropriate, of the relevant passages ¹⁷	Relevant to Claim No. ¹⁸
Y, P	US, A, 4,345,311; Published 17 August 1982; Fielden	1 & 7
Y	US, A, 4,213,134; Published 15 July 1980; Chen	2
Y	US, A, 3,984,829; Published 5 October 1976; Zwack	3-6
Y	US, A, 3,484,591; Published 16 December 1969; Trimble	8-10
Y	US, A, 3,244,808; Published 5 April 1966; Roberts	4, 6 & 12-14
Y	US, A, 4,276,605; Published 30 June 1981; Okamoto et al.	1 & 5
Y	US, N, ALTERNATING CURRENT CIRCUITS; Published in 1938; Kirchner et al.	4, 6, 10, 11 & 13
<p>* Special categories of cited documents: ¹⁵</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"Z" document member of the same patent family</p>		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search ¹	Date of Mailing of this International Search Report ²	
2 June 1983	07 JUN 1983	
International Searching Authority ¹	Signature of Authorized Officer ²⁰	
ISA/US	T. J. Sloyan <i>T. J. Sloyan</i>	