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*[Continued on next page]*

(54) **Title**: METHOD AND APPARATUS FOR MAINTAINING DC BIAS

(57) **Abstract**: A direct current (DC) bias maintenance circuit operably couples to the input of a primary amplifier. The DC bias maintenance circuit employs feedback to maintain the desired DC bias but lacks any coupling to the output of the primary amplifier. By one approach the DC bias maintenance circuit includes a secondary amplifier that replicates at least some near real-time performance characteristics of the primary amplifier. For example, the secondary amplifier can replicate at least certain DC properties of the primary amplifier such that DC-based changes appearing at the output of the primary amplifier are mirrored at an output of the secondary amplifier notwithstanding a lack of any coupling between the output of the primary amplifier and the DC bias maintenance circuit.

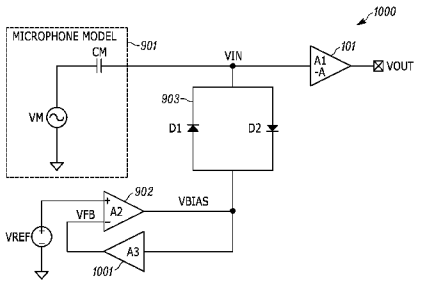



FIG. 10

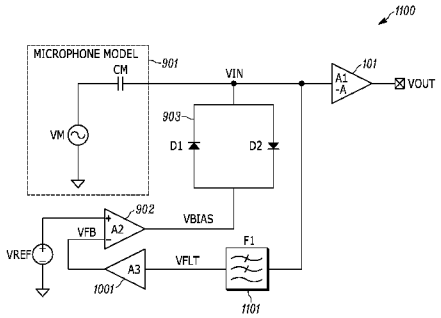



FIG. 11

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DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

**Published**:

— *with international search report (Art. 21(3))*

# METHOD AND APPARATUS FOR MAINTAINING DC BIAS

## Technical Field

**[0001]** These teachings relate generally to DC biasing of amplifiers.

## Background

**[0002]** Amplifiers are known in the art. In many cases it can be useful to set and/or otherwise control the so-called DC operating point of the amplifier in order to mitigate, for example, clipping of the incoming signal. Unfortunately, at least some known approaches in these regards are either somewhat ineffective for the intended task and/or give rise to other unintended consequences that can negatively impact the signal in other ways.

## Brief Description of the Drawings

**[0003]** The above needs are at least partially met through provision of the method and apparatus for maintaining DC bias described in the following detailed description, particularly when studied in conjunction with the drawings, wherein:

**[0004]** FIG. 1 comprises a schematic diagram as configured in accordance with the prior art;

**[0005]** FIG. 2 comprises a schematic diagram as configured in accordance with the prior art;

**[0006]** FIG. 3 comprises a graph as configured in accordance with the prior art;

**[0007]** FIG. 4 comprises a graph as configured in accordance with the prior art;

**[0008]** FIG. 5 comprises a graph as configured in accordance with the prior art;

**[0009]** FIG. 6 comprises a graph as configured in accordance with the prior art;

**[0010]** FIG. 7 comprises a graph as configured in accordance with the prior art;

**[0011]** FIG. 8 comprises a graph as configured in accordance with the prior art;

**[0012]** FIG. 9 comprises a schematic diagram as configured in accordance with the prior art;

**[0013]** FIG. 10 comprises a schematic diagram as configured in accordance with various embodiments of these teachings; and

**[0014]** FIG. 11 comprises a schematic diagram as configured in accordance with various embodiments of these teachings.

**[0015]** Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions and/or relative positioning of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of various embodiments of the present teachings. Also, common but well-understood elements that are useful or necessary in a commercially feasible embodiment are often not depicted in order to facilitate a less obstructed view of these various embodiments of the present teachings. Certain actions and/or steps may be described or depicted in a particular order of occurrence while those skilled in the art will understand that such specificity with respect to sequence is not actually required. The terms and expressions used herein have the ordinary technical meaning as is accorded to such terms and expressions by persons skilled in the technical field as set forth above except where different specific meanings have otherwise been set forth herein.

Detailed Description

**[0016]** Generally speaking, pursuant to these various embodiments, a direct current (DC) bias maintenance circuit operably couples to the input of a primary amplifier. The DC bias maintenance circuit employs feedback to maintain the desired DC bias but lacks any coupling to the output of the primary amplifier. By one approach the DC bias maintenance circuit includes a secondary amplifier that replicates at least some near real-time performance characteristics of the primary amplifier. For example, the secondary amplifier can replicate at

least certain DC properties of the primary amplifier such that DC-based changes appearing at the output of the primary amplifier are mirrored at an output of the secondary amplifier notwithstanding a lack of any coupling between the output of the primary amplifier and the DC bias maintenance circuit.

**[0017]** By one approach the DC bias maintenance circuit includes a comparator having one input coupled to the output of the aforementioned secondary amplifier and another input coupled to a reference voltage that comprises a desired output DC operating point of the primary amplifier.

**[0018]** These teachings are highly flexible in practice and will accommodate a variety of modifications. For example, by one approach the output of the aforementioned comparator operably couples to the input of the primary amplifier via a pair of anti-parallel diodes. As another example in these regards, the input of the secondary amplifier can operably couple to the input of the primary amplifier via a low-pass filter.

**[0019]** So configured, the DC bias maintenance circuit can effectively bias an amplifier to achieve a useful linear range while also minimizing distortion due to clipping without the use of global negative feedback. Those skilled in the art will appreciate that these teachings can be employed without involving any alternating current signal and accordingly can avoid any corresponding distortion-inducing behavior in those regards.

**[0020]** These and other benefits may become clearer upon making a thorough review and study of the following detailed description. Referring now to the drawings, it may be helpful to first describe and explain an illustrative application setting and some corresponding illustrative prior art circuits and behavior in those regards.

**[0021]** Referring first to FIG. 1, a first circuit 100 includes an amplifier 101. For the sake of simplicity this amplifier 101 comprises a single-ended amplifier but it will be understood that the present teachings are not so limited. For example, these teachings can be similarly applied with differential amplifiers and other configurations.

**[0022]** This circuit 100 illustrates an incoming signal voltage VSRC and a source impedance represented by ZSRC. In a typical application setting that source impedance is

designed to be considerably less than the input impedance of the amplifier 101 in voltage amplification application settings. A corresponding bias voltage is represented by VSRC_DC. DC biasing has the advantage of facilitating signal processing at frequencies that are arbitrarily close to 0 Hz. That said, the properties of the biasing may be unknown to the amplifier designer and potentially incompatible for some operating conditions. For example, this bias may vary undesirably with temperature. Such variances can result in shifting the corresponding DC operating point for the amplifier 101 and this, in turn, can result in or increase distortion.

**[0023]** FIG. 2 illustrates a prior art circuit 102 that attempts to mitigate unknown bias voltage behavior by AC coupling the signal voltage through a capacitor C. This capacitor effectively blocks any bias voltage from the source. The amplifier designer can now design and employ a DC bias circuit that includes a DC bias voltage source VBIAS and the corresponding bias voltage impedance ZBIAS. In a typical application setting the bias voltage impedance is considerably larger than the input impedance of the amplifier 101 to prevent unwanted signal attenuation of the input signal VIN itself.

**[0024]** FIG. 3 through FIG. 8 illustrate the importance of setting and/or maintaining a proper DC operating point. FIG. 3 illustrates a plot representing the amplifier's 101 DC transfer function VOUT/VIN. The resultant plot has three main regions. A linear region 301 represents an area where VOUT = A*VIN + VOUT(DC). For the sake of simplicity, in this example the gain A is unity and the output DC bias point is zero (i.e., VOUT(DC) = 0). As a result, in this linear region 301 VOUT = VIN. The other two regions 302 and 303 represent low and high saturation regions, respectively. In these saturation regions VOUT remains constant regardless of VIN and equal to VOUT(MIN) and VOUT(MAX) respectively.

**[0025]** Referring to FIG. 4, a sine wave has been applied to the input of the amplifier 101 and a resultant sine wave 401 appears at the output thereof. This sine wave 401 is centered around VOUT(DC) 304. In this case the amplitude of the incoming sine wave does not exceed VOUT(MAX) or VOUT(MIN) and accordingly the output signal shown in FIG. 4 is undistorted and hence is identical to the input signal.

**[0026]** FIG. 5 illustrates the same assumptions as are discussed above in FIG. 3 except that VOUT(DC) 304 is increased. In this case, and referring to FIG. 6, since the sine wave 401 remains centered around VOUT(DC), and since the latter has increased, the positive peaks 601 of the sine wave 401 are now clipped when the output voltage attempts to exceed VOUT(MAX). FIGS. 7 and 8 illustrate that much the same occurs when VOUT(DC) 304 decreases, in which case the negative peaks 801 of the sine wave 401 are now clipped when the output voltage attempts to decrease below VOUT(MIN). In either case the resultant clipping results in distortion.

**[0027]** In many cases it may not be especially helpful to design VBIAS to be constant. This is because the amplifier 101 itself can be sensitive to changes in supply voltage, temperature, and even random manufacturing variations that themselves result in shifts to the operating point even if the bias remains constant. Accordingly, it is known to design the bias to compensate for such variations such that the DC operating point of the amplifier 101 itself remains constant.

**[0028]** FIG. 9 presents a prior art circuit 900 that seeks to set and reset as appropriate the amplifier's DC operating point. In this example the bias voltage VBIAS is generated using a global negative feedback loop (i.e., a feedback loop that includes the amplifier 101 itself). In this example a comparator 902 compares VOUT as provided by the amplifier 101 with VREF to generate the bias. The comparator 902 applies the bias to the input VIN of the amplifier 101 through a pair of anti-parallel diodes 903. These diodes 903 present a very high ZBIAS as discussed above when the voltage difference between VIN and VBIAS is zero.

**[0029]** So configured, VOUT can match VREF and accordingly this circuit can set the DC operating point for the amplifier 101, at least when no signal is applied. In practice, such an approach has been proposed for use in decreasing the settling time of the amplifier 101 when used in conjunction with a microphone 901 and the microphone 901 experiences an impulse event such as the slamming of a door. In particular, this circuit operates to apply a signal that is negatively related to VIN to the bottom of the diodes 903.

This forward biases one of the diodes (depending on the polarity of VIN) to thereby decrease the diode impedance to bring VIN (and therefore VOUT) back to its quiescent point.

**[0030]** Unfortunately, this same behavior will persist in the presence of a continuous incoming signal. Accordingly, this circuit can act to limit the signal in a way that introduces in and of itself distortion at the input of the amplifier 101.

**[0031]** The present teachings address such concerns by employing a circuit that sets and stabilizes the DC operating point of an amplifier (such as a microphone amplifier) without using global negative feedback. Though employing many of the same components as the circuit 900 described above in FIG. 9, the circuit 1000 shown in FIG. 10 further includes a secondary amplifier 1001 (in contrast to the aforementioned amplifier 101 which is hereafter referred to as the primary amplifier 101).

**[0032]** This secondary amplifier 1001 can comprise a scaled replica of the primary amplifier 101. Accordingly, this secondary amplifier 1001 can have identical DC properties as compared to the primary amplifier 101. These teachings will of course accommodate having the secondary amplifier 1001 be an exact duplicate of the primary amplifier 101 in these regards if desired. Such exactness, however, is not necessarily required for many application settings. For example, it may not be necessary or even useful that the secondary amplifier 1001 be identical to the primary amplifier 101 with respect to non-essential attributes such as physical size or current drain.

**[0033]** In this illustrative example the secondary amplifier 1001 has its input coupled through the aforementioned diodes 903 to the input VIN of the primary amplifier 101. The output of the secondary amplifier 101 connects to one input of the comparator 902, the remaining input of which couples to a reference voltage VREF that is set to the desired DC operating point VOUT(DC). So configured the output of the secondary amplifier 1001 represents a feedback voltage VFB. Accordingly, the comparator 902 compares the reference voltage VREF to a feedback voltage VFB to develop a resultant VBIAS signal.

**[0034]** Because the secondary amplifier 1001 is enclosed in a feedback loop and has the same essential properties as the primary amplifier 101 as described above, any changes in

VOUT(DC) will be mirrored in the VFB signal. When VFB is not equal to VREF, negative feedback will adjust VBIAS to thereby restore the condition VREF = VFB = VOUT(DC). Those skilled in the art will note and appreciate that, unlike the solution described above in FIG. 9, this biasing scheme does not involve any AC signals and therefore has no corresponding distortion-inducing behavior.

**[0035]** If desired, and should it be deemed useful to adjust VBIAS below and/or above the minimum/maximum voltage in the circuit 1000 (as established, for example, by ground and VDD) using a charge pump. The comparator 902 can also be biased with a charge pump. Such an approach is readily accommodated in microphone application settings where the primary amplifier 101 is often implemented as a source follower. Also if desired, it may be useful to set VBIAS beyond the available supply limits.

**[0036]** In the foregoing discussion of the circuit 1000 shown in FIG. 9, the average input voltage VIN(AVG) is assumed to equal VBIAS. In practice, however, the two diodes 903 may not be identical diode types. Accordingly, it is possible that the impedance presented by the cross-coupled diodes may not be the same for positive voltages as for negative voltages. In this case the average value of VIN may vary with signal amplitude and hence result in some rectification. Should this occur, the average input will not equal VBIAS and therefore VOUT(DC) will not equal VREF.

**[0037]** FIG. 11 presents a circuit 1100 that corrects the foregoing by including the diodes 903 in the bias feedback loop that is otherwise described above. In particular, the input to the secondary amplifier 1001 now connects to the input of the primary amplifier 101 (i.e., VIN) via a low-pass filter 1101. For many application settings the corner frequency for the low-pass filter 1101 can be below 20Hz but not as low as the filter formed from the diodes 903 and the microphone 901 which needs to be less than 1Hz for good noise performance in a typical application setting. So configured, the low-pass filter 1101 removes the AC content of VIN so that the resultant filtered signal VFLT is at least approximately equal to VIN(AVG). (These teachings would accommodate, if desired, instead tying the filter 1101 to the output of the primary amplifier 101 to achieve much the same effect.) When VIN

constitutes an AC signal, the average value of VIN may not equal VBIAS, but since VFB is now derived from VIN(AVG), the aforementioned negative feedback will now adjust VBIAS such that the desired result (i.e., that VREF = VFB = VOUT(DC)) is achieved.

**[0038]** These teachings can be implemented in a variety of useful application settings and typically in a very economical and reliable manner. Configuring an amplifier circuit pursuant to these teachings results in desired DC biasing of the amplifier without requiring global negative feedback and hence avoids the performance issues that are inherently associated with global negative feedback techniques in these application settings.

**[0039]** Those skilled in the art will recognize that a wide variety of modifications, alterations, and combinations can be made with respect to the above described embodiments without departing from the scope of the invention, and that such modifications, alterations, and combinations are to be viewed as being within the ambit of the inventive concept.

What is claimed is:

1. An apparatus comprising:

a primary amplifier having an input and an output;

a direct current (DC) bias maintenance circuit operably coupled to the input of the primary amplifier, the DC bias maintenance circuit including a secondary amplifier that replicates at least some near real-time performance characteristics of the primary amplifier.

2. The apparatus of claim 1 wherein the input of the primary amplifier further operably couples to a microphone.

3. The apparatus of claim 1 wherein the secondary amplifier replicates at least DC properties of the primary amplifier such that DC-based changes appearing at the output of the primary amplifier are mirrored at an output of the secondary amplifier.

4. The apparatus of claim 1 wherein the DC bias maintenance circuit further comprises a comparator having a first input operably coupled to an output of the secondary amplifier.

5. The apparatus of claim 4 wherein a second input of the comparator operably couples to a reference voltage comprising a desired output DC operating point of the primary amplifier.

6. The apparatus of claim 5 wherein an input to the secondary amplifier operably couples to an output of the comparator.

7. The apparatus of claim 6 wherein the output of the comparator further operably couples to the input of the primary amplifier via a pair of anti-parallel diodes.

8. The apparatus of claim 5 wherein the output of the comparator further operably couples to the input of the primary amplifier via a pair of anti-parallel diodes and an input to the secondary amplifier operably couples to the input of the primary amplifier other than through the pair of anti-parallel diodes.

9. The apparatus of claim 8 wherein the input of the secondary amplifier operably couples to the input of the primary amplifier via a low pass filter.

10. A method comprising:

operably coupling a direct current (DC) bias maintenance circuit to an input of a primary amplifier, the DC bias maintenance circuit including a secondary amplifier that replicates at least some near real-time performance characteristics of the primary amplifier.

11. The method of claim 10 further comprising operably coupling the input of the primary amplifier to a microphone.

12. The method of claim 10 further comprising using the secondary amplifier to replicate at least DC properties of the primary amplifier such that DC-based changes appearing at an output of the primary amplifier are mirrored at an output of the secondary amplifier.

13. The method of claim 10 wherein the DC bias maintenance circuit further comprises a comparator having a first input operably coupled to an output of the secondary amplifier.

14. The method of claim 13 wherein a second input of the comparator operably couples to a reference voltage comprising a desired output DC operating point.

15. The method of claim 14 wherein an input to the secondary amplifier operably couples to an output of the comparator.

16. The method of claim 15 wherein the output of the comparator further operably couples to the input of the primary amplifier via a pair of anti-parallel diodes.

17. The method of claim 14 wherein the output of the comparator further operably couples to the input of the primary amplifier via a pair of anti-parallel diodes and an input to the secondary amplifier operably couples to the input of the primary amplifier other than through the pair of back-to-back diodes.

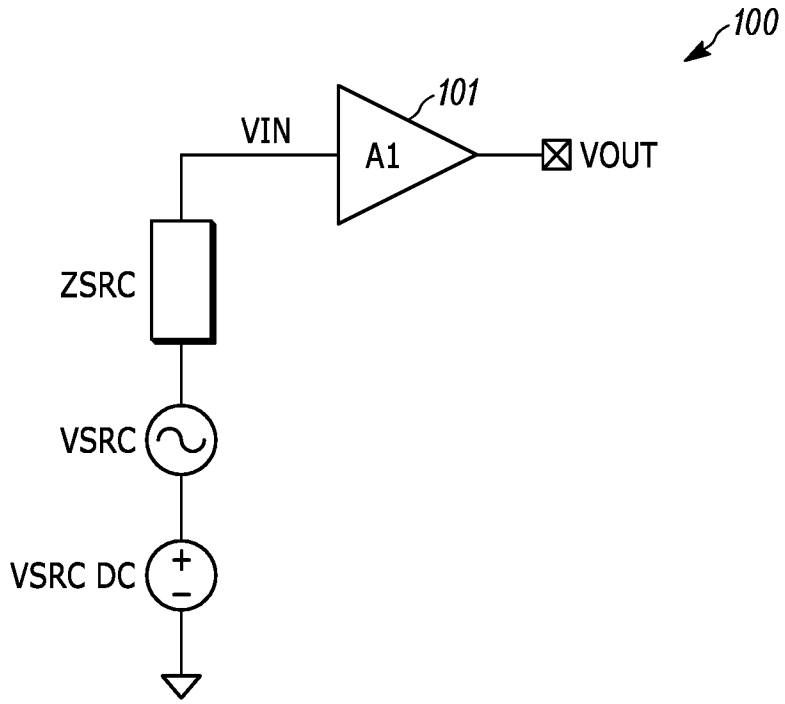
18. The method of claim 17 wherein the input of the secondary amplifier operably couples to the input of the primary amplifier via a low pass filter.

19. An apparatus comprising:

a primary amplifier having an input and an output;

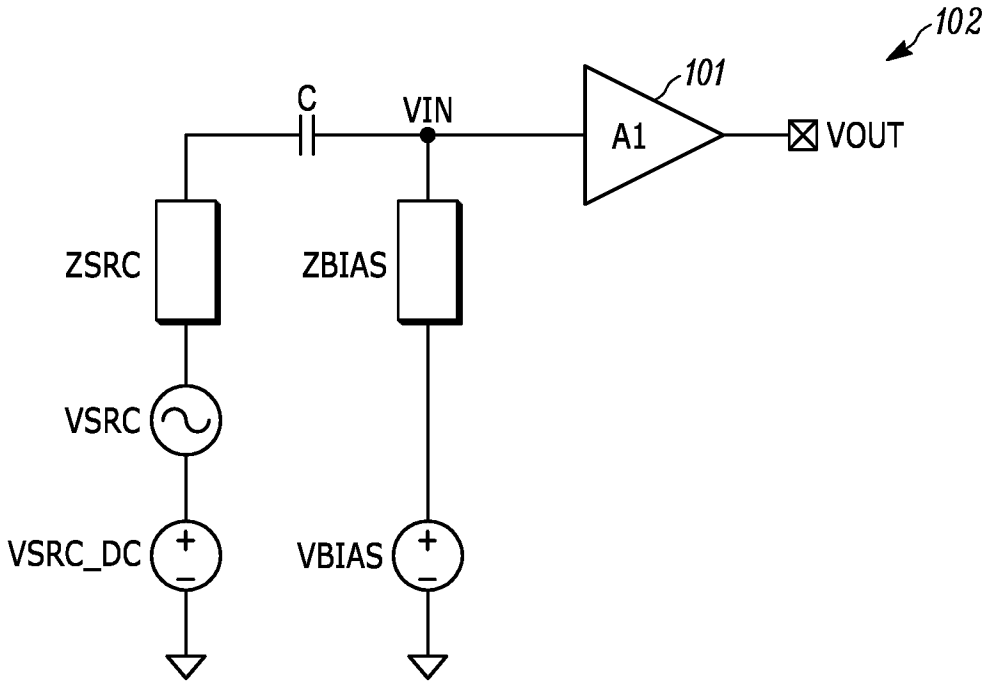
a direct current (DC) feedback-based bias maintenance circuit operably coupled to the input of the primary amplifier, the DC feedback-based bias maintenance circuit lacking any coupling to the output of the primary amplifier.

20. The apparatus of claim 19 wherein the DC feedback-based bias maintenance circuit is configured to mirror DC-based changes that appear at the output of the primary amplifier.



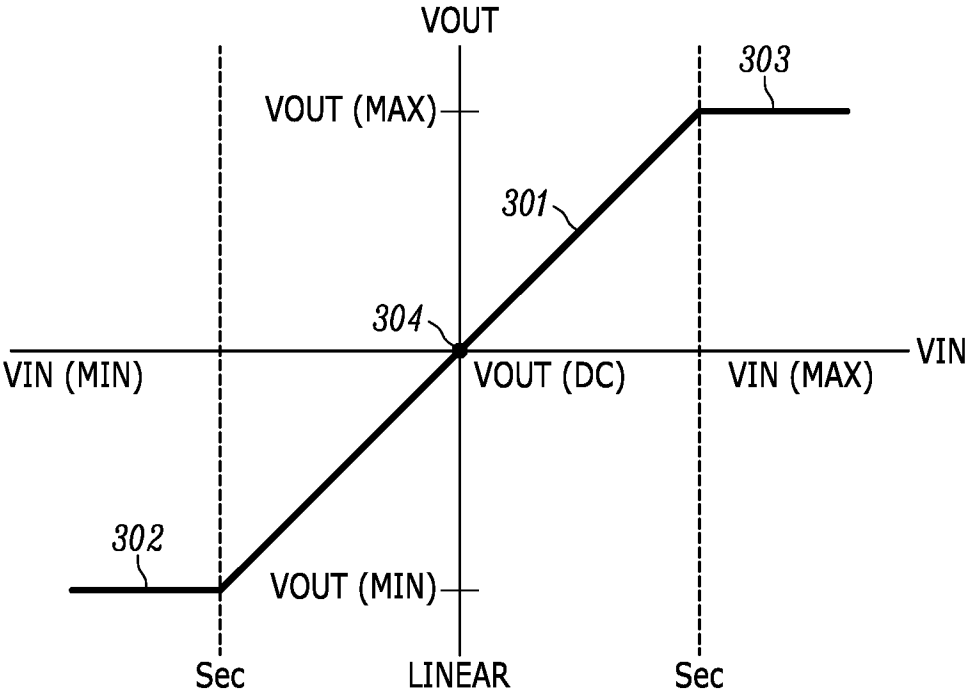

PRIOR ART

FIG. 1



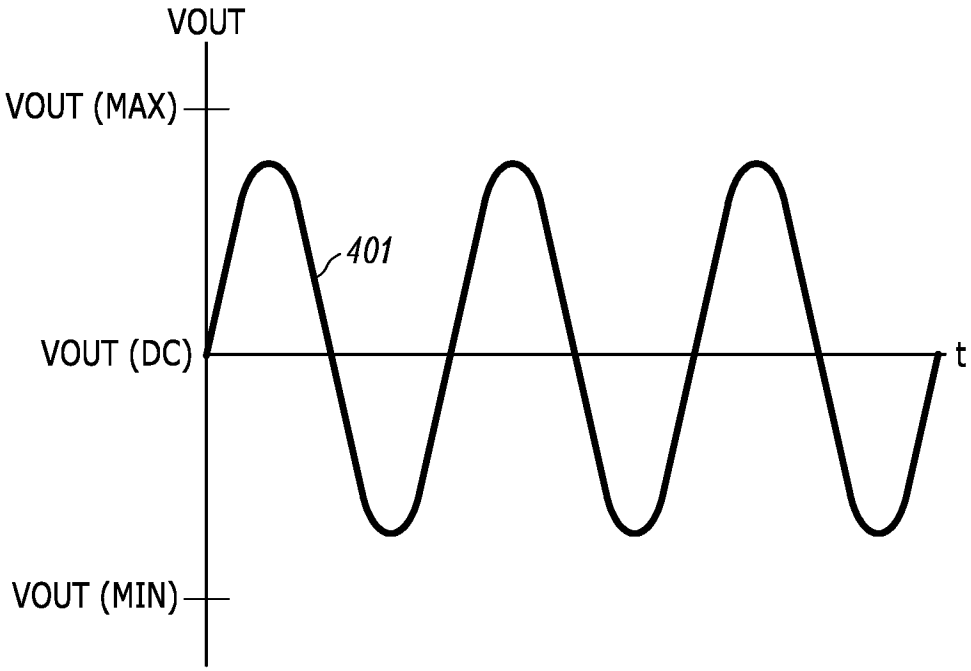

PRIOR ART

FIG. 2



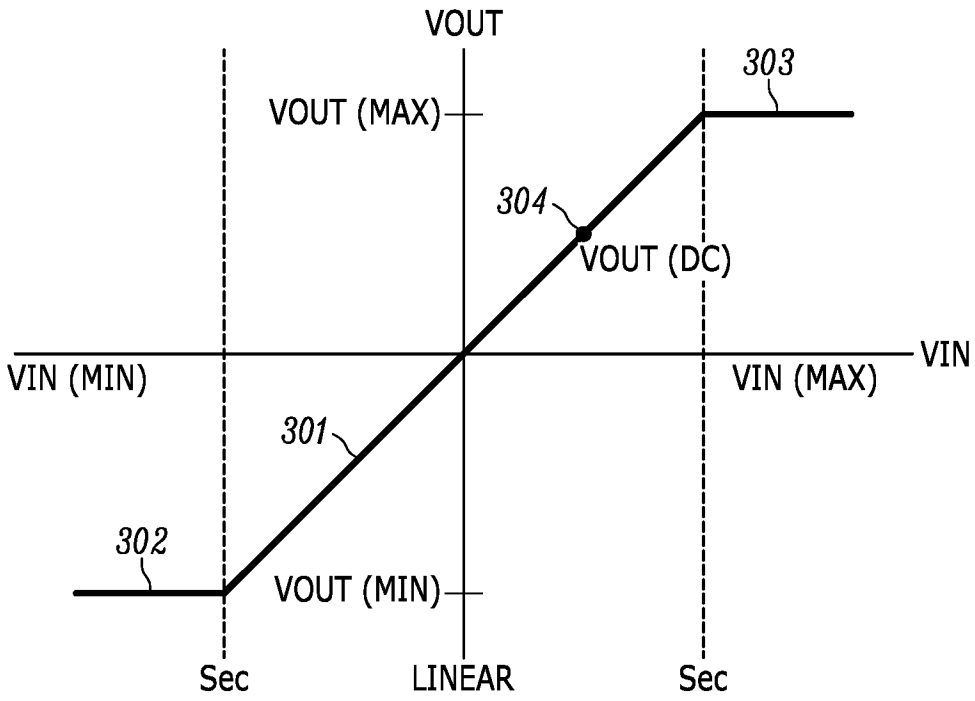

PRIOR ART

FIG. 3



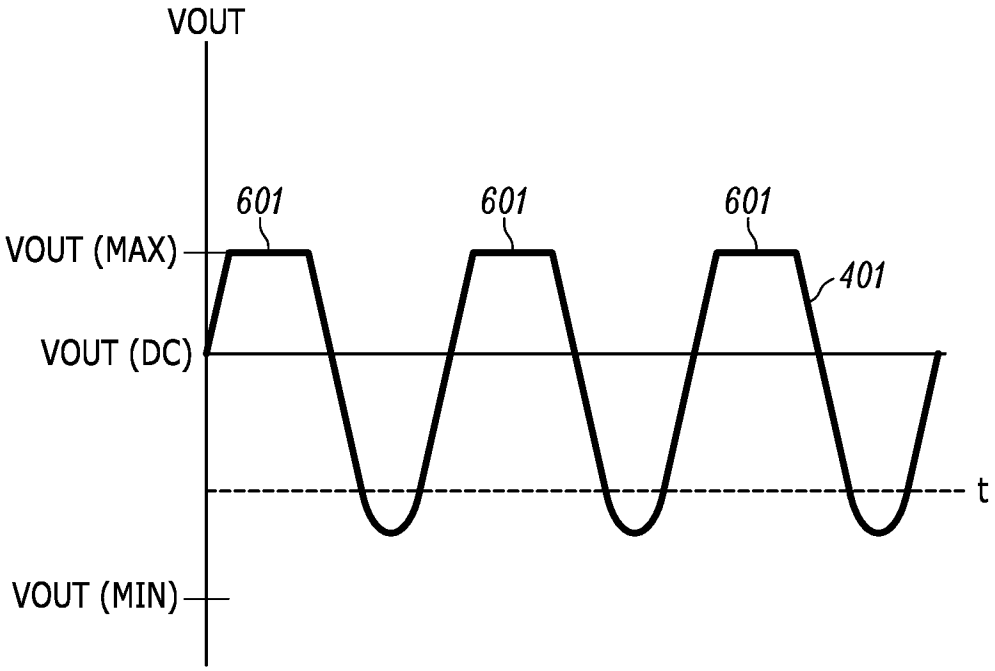

PRIOR ART

FIG. 4



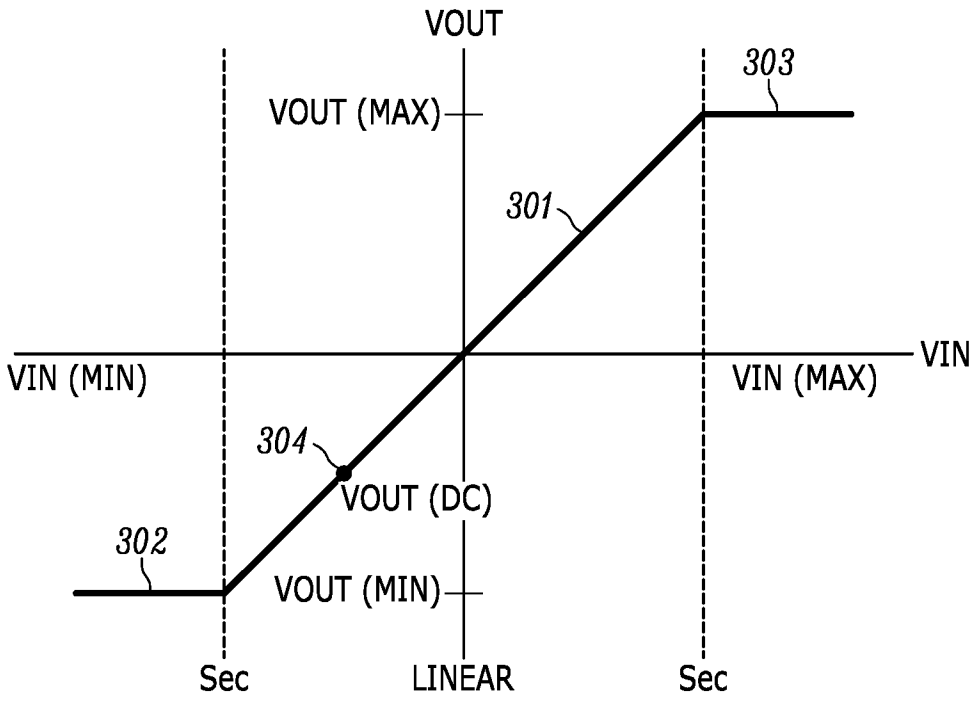

PRIOR ART

FIG. 5



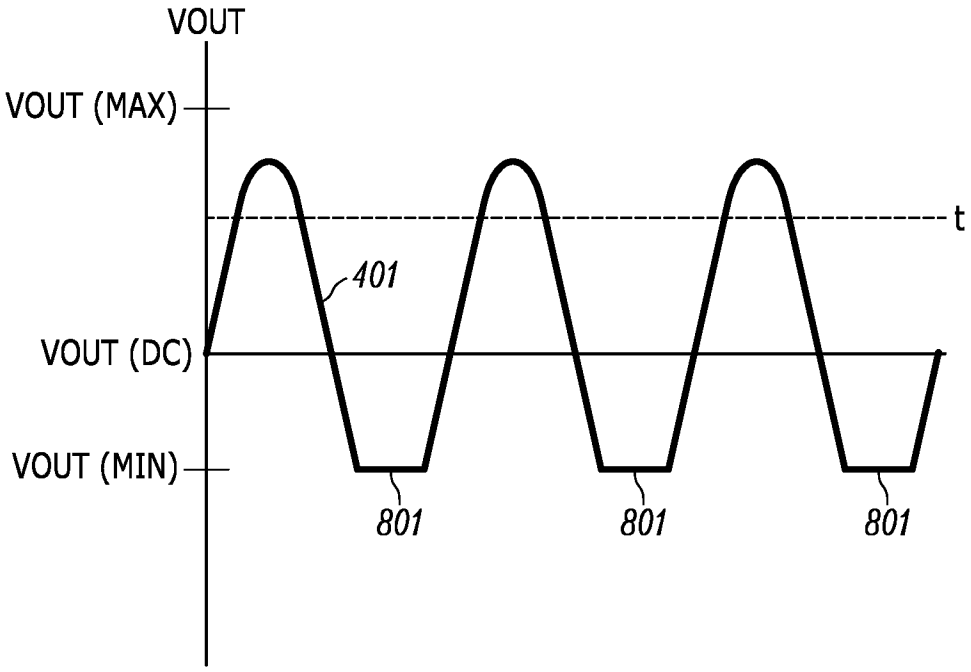

PRIOR ART

FIG. 6



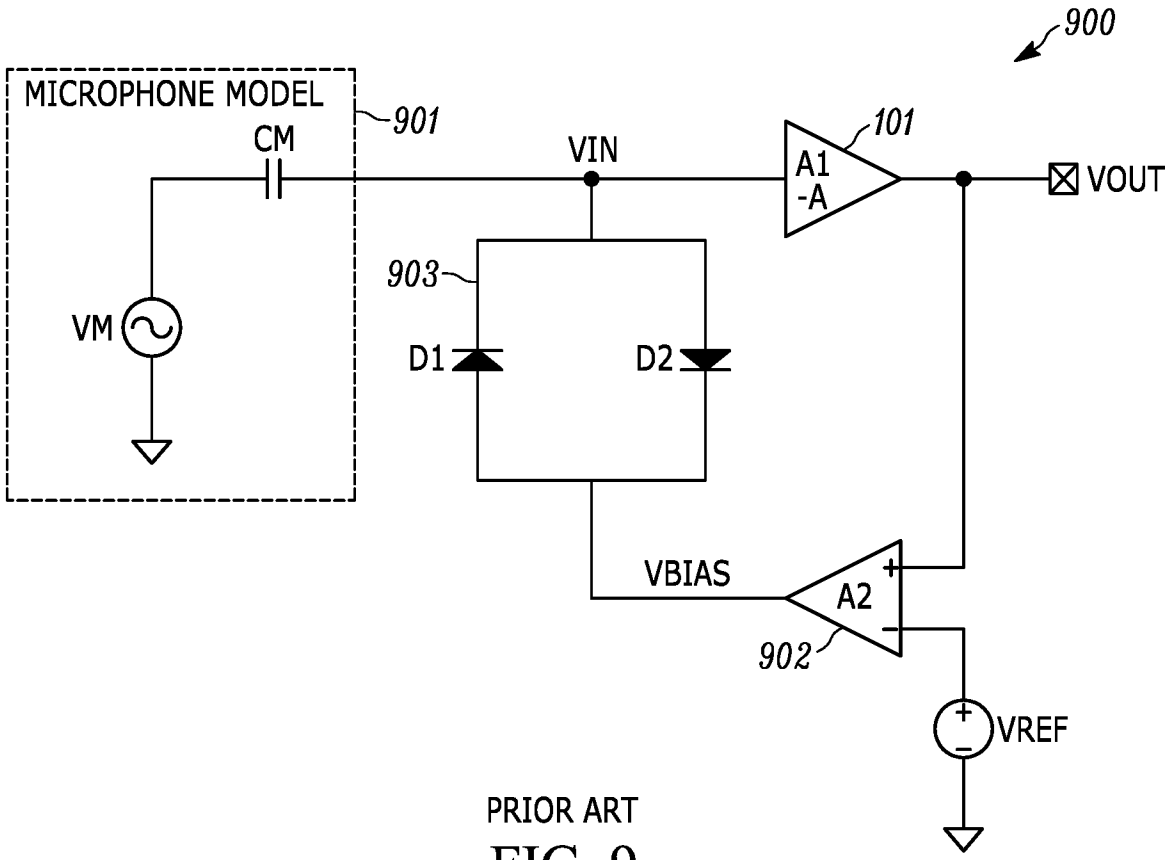

PRIOR ART

FIG. 7




PRIOR ART

FIG. 8




PRIOR ART

FIG. 9

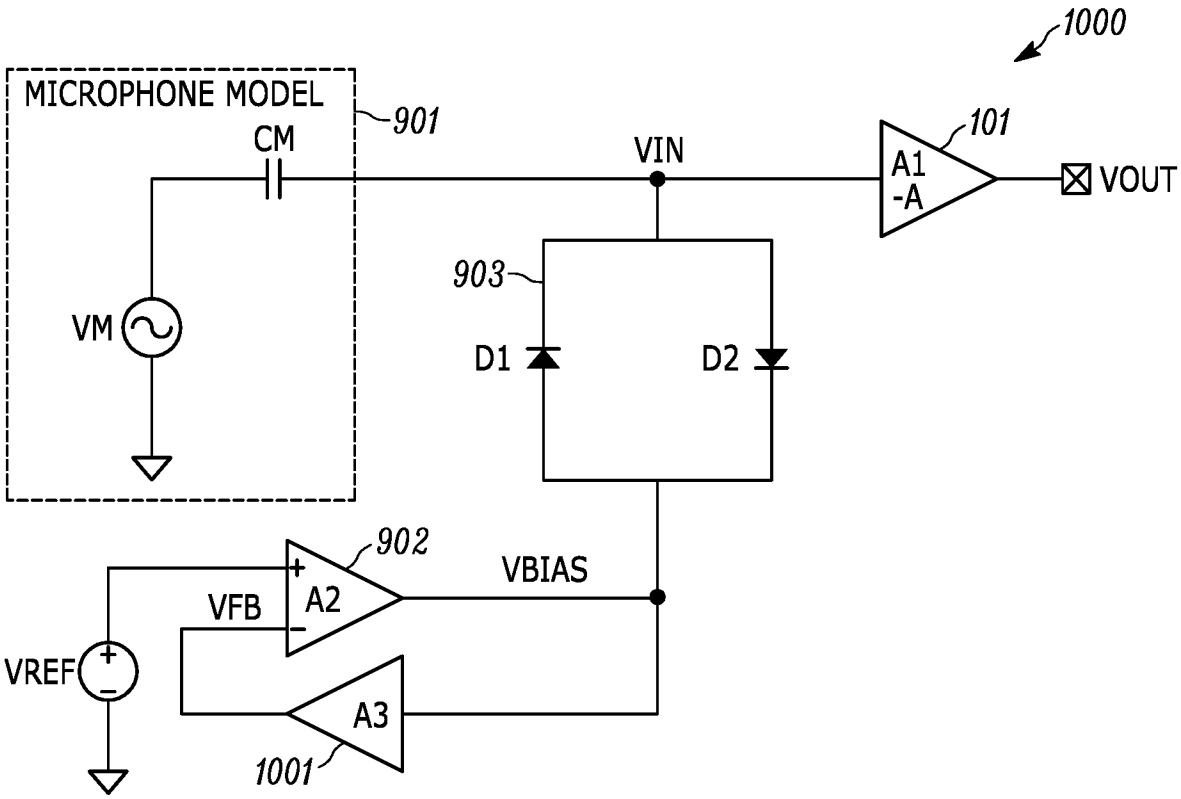



FIG. 10

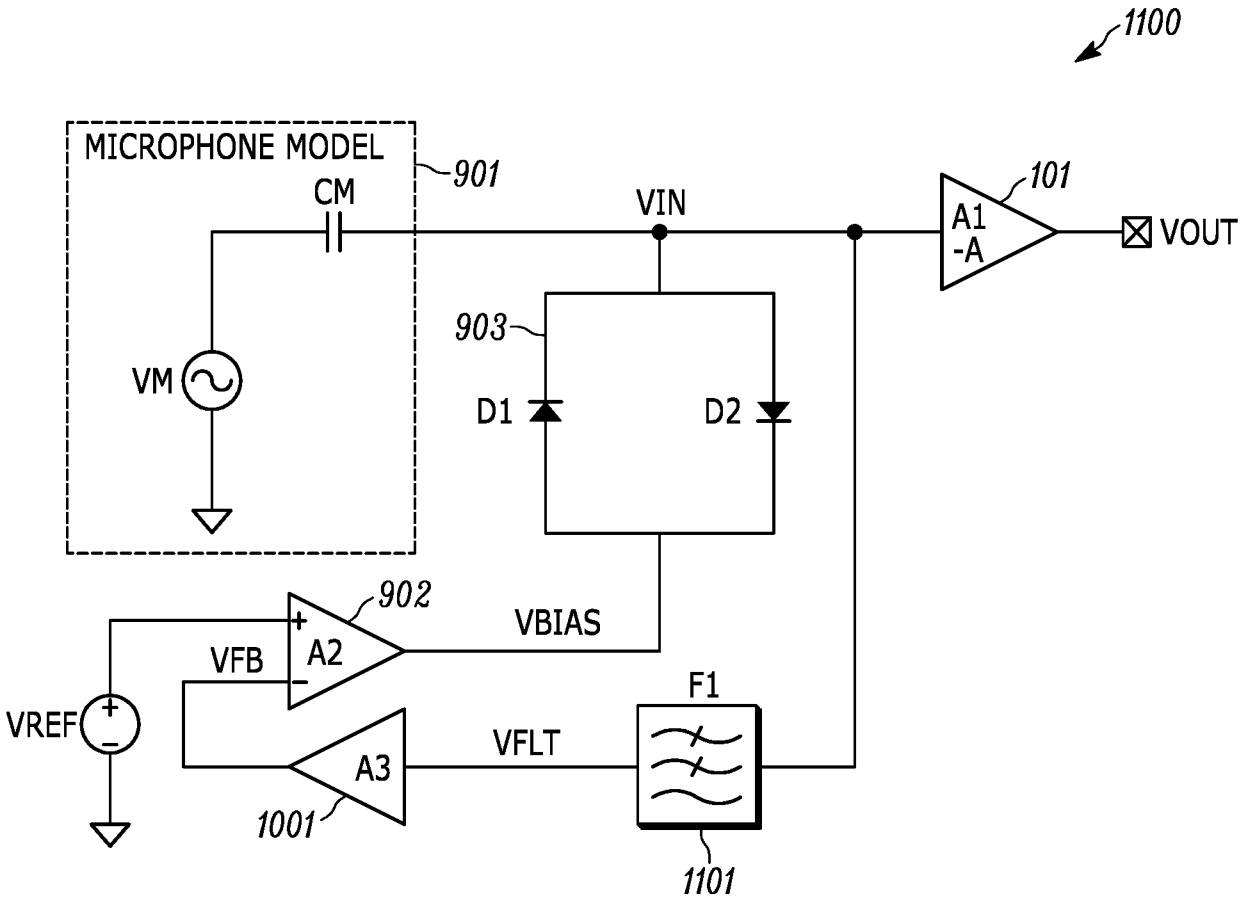

1100
MICROPHONE MODEL
901
CM
VIN
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A1
-A
VOUT
903
VM
D1
D2
902
VBIAS
VFB
A2
VREF
F1
VFLT
A3
1001
1101

FIG. 11

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/053728

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/30
ADD. H03F3/181 H04R3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F H04R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 2005/242791 A1 (RAJAPANDIAN SARAVANAN [US] ET AL) 3 November 2005 (2005-11-03)<br>figures 2-5<br>paragraphs [0003] - [0024]<br>paragraph [0038]<br>----- | 1-20 |
| X<br><br><br>A | WO 2007/103401 A1 (ANALOG DEVICES INC [US]; STRANGE JONATHAN RICHARD [US])<br>13 September 2007 (2007-09-13)<br>page 1, lines 20-24;<br>figure 6<br>page 11, lines 2-20<br>----- | 1,10,19, 20<br><br><br>2-9, 11-18 |
| X | US 7 679 448 B1 (MCADAM MATTHEW W [CA] ET AL) 16 March 2010 (2010-03-16)<br>figures 3,7<br>column 2, lines 1-31<br>column 3, line 52 - column 4, line 39<br>-----<br>-/-- | 1-20 |

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Form PCT/ISA/210 (second sheet) (April 2005)

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