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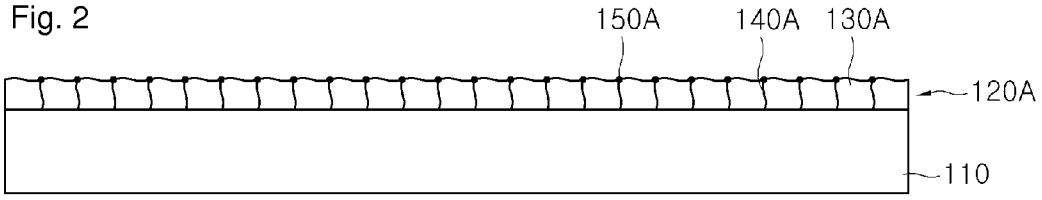
Fig. 2



(57) Abstract: Provided are a polysilicon film and a method of manufacturing the same, and a flash memory device employing the polysilicon film and a method of manufacturing the flash memory device. After the polysilicon film grows to a thickness that is the same as a grain size, an impurity gas is supplied to provide a lot of impurities into boundaries of grains, thereby suppressing the continuous growth of grains and forming the polysilicon film having small, uniform, nano-size grains whose size is less than 10 nm. The impurities existing in the boundaries suppress the growth of grains in subsequent processes. By using the polysilicon film as a floating gate of the flash memory device, it is possible to increase a program or erase speed and improve thermal stability, thereby enhancing the reliabilty of the device.

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Description

POLYSILICON FILM AND METHOD OF FORMING THE SAME, FLASH MEMORY DEVICE AND MANUFACTURING METHOD USING THE SAME

Technical Field

[1] The present invention relates to a polysilicon film and a method of manufacturing the same, and more particularly, to a polysilicon film having nano-size grains and a method of forming the same, and a flash memory device employing the polysilicon film and a method of manufacturing the flash memory device.

Background Art

[2] A flash memory device is a non-volatile memory device that can program and erase data, and read out the programmed data. Thus, the flash memory device has a cell structure that includes a gate electrode insulated from a semiconductor substrate by a tunnel oxide layer and formed with a dielectric layer interposed between a floating gate and a control gate, and source/drain junction regions disposed at both sides of the gate electrode.

[3] The flash memory device is programmed and erased performing an operation of injecting charge onto the floating gate and pulling the charge off the floating gate. That is, a positive voltage applied to the control gate is coupled to the floating gate and thus the flash memory device is programed by electrons that are captured into the floating gate through the tunnel oxide layer from the substrate through Fowler-Nordheim (FN) tunneling or hot-carrier injection. On the other hand, in the erase operation, the electrons within the floating gate are moved into the substrate by a negative voltage applied to the control gate.

[4] The floating gate of the flash memory device may include a polysilicon film. However, as a design rule decreases, in a flash memory device having a design rule less than 40 nm, it is required to increase the number of grains in a polysilicon film used as a floating gate as well as increasing a tunneling field in order to perform a high-speed program by reducing a threshold voltage. For this purpose, the grain size of the polysilicon film should be reduced. As the grain size is reduced, the number of grain boundaries is increased and thus an erasing speed of the flash memory device becomes high. That is, a programming speed and the erasing speed of the flash memory device can be improved by reducing the grain size of the polysilicon film used as the floating gate. Furthermore, as the grain size of the polysilicon film is reduced to especially a nano size, thermal stability of the floating gate is enhanced and thus the performance of the device can be improved.

[5] The polysilicon film is formed through several phases such as an incubation phase, a nucleation and growth phase, a growth dominated phase, and a complete coalescence phase. In the incubation phase, silicon adatom reaches onto a surface of the tunnel oxide layer and a first stable nucleus is generated. In the nucleation and growth phase, new nucleuses are consecutively generated while the previously generated nucleuses grow into nanocrystals. In the growth dominated phase, the generation of new nucleuses is stopped and the generated nucleuses keep on growing before the nanocrystals are merged. In the complete coalescence phase, all nanocrystals are merged to form a film.

[6] In order to reduce the grain size of the polysilicon film, until the coalescence occurs, it is required to minimize a size of an individual grain by increasing nucleus generation density in the nucleation and growth phase. However, the grain growth is continued through the nucleation and growth phase, the growth dominated phase and the complete coalescence phase. The grain growth is continued during the film being deposited after the coalescence occured. After the deposition is even completed, during a post thermal process that is performed at the temperature of 900 ℃ for 11our, the grain growth is continued by a solid phase diffusion phenomenon, thereby increasing the grain size.

[7] As the grain size of the polysilicon film is continuously increased as described above, the flash memory device has the difficulty in performing high-speed programming and the deterioration of the thermal stability.

Disclosure of Invention

Technical Problem

[8] The present invention provides a polysilicon film having small, uniform, nano-size grains less than 10 nm, and a method of forming the same.

[9] The present invention provides a polysilicon film having small, uniform, nano-size grains less than 10 nm that is obtained through suppressing the continuous grain growth by supplying an impurity gas in a growth dominated phase and a complete coalescence phase during forming the polysilicon film, and a method of forming the same.

[10] The present invention provides a flash memory device using a polysilicon flim, which has small, uniform, nano-size grains less than 10 nm, as a floating gate, and a method of forming the same.

Technical Solution

[11] In accordance with one aspect of the present invention, a polysilicon film includes a plurality of polysilicon layers stacked to each other, wherein each of the polysilicon layers includes a plurality of grains and contains impurity atoms in boundaries of the grains to suppress the growth of the grains.

[12] The grain may have a size of approximately 5 nm to approximately 10 nm.

[13] The impurity atoms may include nitrogen atoms or oxygen atoms, or both.

[14] In accordance with another aspect of the present invention, a method of manufacturing a polysilicon film includes forming a polysilicon layer including a plurality of grains by supplying a silicon source gas, and providing impurity atoms into boundaries of the grains by supplying an impurity gas.

[15] The impurity gas may be supplied after the supplying of the silicon source gas is stopped.

[16] The silicon source gas may be purged before the impurity gas is supplied.

[17] The impurity gas and the silicon source gas may be simultaneously supplied.

[18] supplying the silicon source gas and supplying the impurity gas may be repeated.

[19] Forming the polysilicon layer and providing the impurity atoms may be performed at the temperature ranging from approximately 450 ℃ to approximately 800 ℃ and in the pressure of approximately 1E-5 Torr to approximately 760 Torr.

[20] The impurity gas may use a gas including nitrogen atoms or oxygen atoms, or both.

[21] In accordance with still another aspect of the present invention, a flash memory device includes a gate electrode including a stack structure of a tunnel insulation layer, a floating gate, a dielectric layer and a control gate, which is formed over a certain region of a semiconductor substrate, and source/drain junction regions formed at both sides of the gate electrode in the semiconductor substrate, wherein the floating gate is formed by stacking a plurality of polysilicon layers, and each of the polysilicon layers includes a plurality of grains and contains impurity atoms in boundaries of the grains to suppress the growth of the grains.

[22] The grain may have a size of approximately 5 nm to approximately 10 nm.

[23] The impurity atoms may include nitrogen atoms or oxygen atoms, or both.

[24] In accordance with still another aspect of the present invention, a method of manufacturing a flash memory device includes forming a tunnel insulation layer over a semiconductor substrate and forming a polysilicon film containing impurities in boundaries of grains, patterning the polysilicon film to form a resultant structure, forming a dielectric layer and a conductive layer over a whole surface of the resultant structure, patterning the conductive layer, dielectric layer, the polysilicon film and the tunnel insulation layer to form a gate electrode incuding a stack structure of a floating gate and a control gate, and forming junction regions by injecting impurity ions into the semiconductor substrate at both sides of the gate electrode.

[25] Forming the polysilicon film may include forming a polysilicon layer including a plurality of grains by supplying a silicon source gas, and stopping the supplying of the silicon source gas and supplying an impurity gas to provide impurity atoms into the boundaries of the grains.

[26] Forming the polysilicon film may include forming a polysilicon layer including a plurality of grains by supplying a silicon source gas, and supplying the silicon source gas and an impurity gas to provide impurity atoms into the boundaries of the grains.

[27] Forming the polysilicon layer and providing the impurity atoms may be performed at the temperature ranging from approximately 450 ℃ to approximately 800 ℃ and in the pressure of approximately 1E-5 Torr to approximately 760 Torr.

[28] The impurity gas may use a gas including nitrogen atoms or oxygen atoms, or both.

Advantageous Effects

[29] In accordance with the present invention, in the growth dominated phase or the complete coalescence phase during forming the polysilicon film, i.e., after the polysilicon film grows to a thickness that is the same as a grain size, the impurity gas is supplied to provide a lot of impurities into boundaries of grains, thereby suppressing the continuous growth of grains and forming the polysilicon film having small, uniform, nano-size grains that is less than 10 nm. The impurities existing in the boundaries suppresses the growth of grains after depositing the polysilicon film in a desired thickness or during a thermal budget.

[30] By using the polysilicon film as a floating gate of a flash memory device, it is possible to increase a program or erase speed and improve thermal stability, thereby enhancing the reliabilty of the device.

Brief Description of the Drawings

[31] FIGs. 1 to 5 illustrate cross-sectional views of a method of forming a polysilicon film in accordance with an embodiment of the present invention;

[32] FIG. 6 is a flow chart illustrating a method of forming the polysilicon film in accordance with the embodiment of the present invention; and

[33] FIG. 7 illustrates a cross-sectional view of a flash memory device in accordance with an embodiment of the present invention.

Best Mode for Carrying Out the Invention

[34] Hereinafter, specific embodiments will be described in detail with reference to the accompanying drawings. The present invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present invention to those skilled in the art. In the figures, the dimensions of layers and regions are exaggerated for clarity of illustration. Like reference numerals refer to like elements throughout. It will also be understood that when a layer, a film, a region or a plate is referred to as being 'on' another one, it can be directly on the other one, or one or more intervening layers, films, regions or plates may also be present.

[35] FIGs. 1 to 5 illustrate cross-sectional views of a method of forming a polysilicon film in accordance with an embodiment of the present invention, and FIG. 6 is a flow chart illustrating a method of forming the polysilicon film.

[36] Referring to FIGs. 1 and 6, a semiconductor substrate 110 including a certain structure formed thereon is loaded into a chmical vapor deposition (CVD) chamber such as a thermal CVD chamber, a low-pressure chemical vapor deposition (LPCVD) chamber or a plasma-enhanced chemical vapor deposition (PECVD) chamber in step S100. Then, a silicon source gas is supplied to the chamber to form a first polysilicon layer 120A in step S200. The first polysilicon layer 120A is formed in conditions of increasing nucleus density, e.g., at the temperature ranging from approximately 450 ℃ to approximately 800 ℃ and in the pressure of approximately 1E-5 Torr to approximately 760 Torr. Herein, the silicon source gas includes SiH_4, Si_2H_6 or $Si_2H_2Cl_2$. In those conditions, stable nucleuses can be generated after silicon adatom reaches onto the surface of the semiconductor substrate 110 and the generated nucleuses grow to nanocrystals and then grains 130A while new nucleuses are continuously generated. Grain boundaries 140A are formed between the grains 130A. A deposition thickness of the first polysilicon layer 120A is controlled by an inflow amount and time of the silicon source gas supplied to the chamber. For instance, the grain 130A grows in size of approximately 5 nm to approximately 10 nm and the first polysilicon layer 120A is formed in thickness of approximately 5 nm to approximately 10 nm that is substantially the same as the size of the grain 130A.

[37] Referring to FIGs. 2 and 6, after the grain 130A is formed in a certain size and the first polysilicon layer 120A is formed in a thickness identical to the size of the grain 130A and, before the grains 130A are fused each other, the inflow of the silicon source gas is stopped and an impurity gas is supplied in step S300. At this time, to remove the silicon source gas remaining in the chamber, a purge process may be performed using, e.g., a purge gas or an exhaust gas. The impurity gas may use a gas containing one of nitrogen atoms, oxide atoms and a combination thereof. For example, the impurity gas includes one of NH_3, O_2, N_2O and a combination of. The reason the impurity gas uses the nitrogen atoms or the oxide atoms, those atoms do not damage a gate oxide layer and can be combined with the polysilicon without making bad influence on electrical performance of a layer although they are diffused into and exist within crystalloid. Besides the nitrogen or oxide atoms, other atoms may be used if they can maintain the performance of the polysilicon film. By the supplied impurity gas, an impurity atom 150A including one of nitrogen atom, oxide atom and a combination thereof may be contained in the grain boundary 140A. Since the impurity atom 150A is contained in the grain boundary 140A, the growth of the grain 130A is suppressed and thus the grain 130A maintains a nano size of, e.g., approximatley 5 nm to approximately 10

nm. The impurity gas is supplied at the temperature ranging from approximately 450 ℃ to approximately 800 ℃ and in the pressure of approximately 1E-5 Torr to approximately 760 Torr, which are substantially the same conditions as the first polysilicon layer 120A is deposited. Since the content of the impurities supplied to the grain boundary 140A can be controlled according to the temperature and pressure, the temperature and the pressure are adjusted depending on a desired grain size to be obtained by containing the impurities. In addition, by controlling the inflow amount and time of the impurity gas, the impurity atom 150A is contained into the grain boundary 140A unless a layer is formed by the impurity gas.

[38] Referring to FIGs. 3 and 6, in step S400, it is determined whether a desired thickness of the polysilicon film is obatined. If the desired thickness is not acquired, the silicon source gas is supplied again to form a second polysilicon layer 120B. The second polysilicon layer 120B may be formed in substantially the same conditions as the first polysilicon layer 120A is formed. That is, the second polysilicon layer 120B is formed at the temperature ranging from approximately 450 ℃ to approximately 800 ℃ and in the pressure of approximately 1E-5 Torr to approximately 760 Torr, thereby increasing the nucleus density. A thickness of the second polysilicon layer 120B is adjusted by controlling an inflow amount and time of the silicon source gas and a grain 130B grows within the second polysilicon layer 120B, forming a grain boundary 140B. It is preferable that the second polysilicon layer 120B has substantially the same thickness as the size of the grain 130B. For instance, the grain 130B grows in a size of approximately 5 nm to approximately 10 nm and the second polysilicon layer 120B is deposited to have a thickness of approximately 5 nm to approximately 10 nm. At this time, the grain 130A of the first polysilicon layer 120A does not continuously grow with the grain 130B of the second polysilicon layer 120B by the impurity atom 150A contained in the boundary 140A, so that the size of the grain 130A does not increase anymore.

[39] Referring to FIGs. 4 and 6, the inflow of the silicon source gas is stopped and an impurity gas is supplied, so that an impurity atom 150B is contained in the grain boundary 140B of the second polysilicon layer 120B in step S300. The impurity gas supplied to provide the impurity atom 150B into the grain boundary 130B uses a gas containing one of nitrogen atoms, oxide atoms and a combination thereof. For example, the impurity gas includes one of NH_3, O_2, N_2O and a combination of. By the supplied impurity gas, the impurity atom 150B including one of nitrogen atom, oxide atom and a combination thereof is contained in the grain boundary 140B. Since the impurity atom 150B is contained in the grain boundary 140B, the growth of the grain 130B is suppressed in subsequent processes.

[40] Referring to FIGs. 5 and 6, the processes for growing the polysilicon layer and

providing the impurity atom into the grain boundary are iterated by repeatedly supplying the silicon source gas and the impurity gas, thereby forming a polysilicon film 160 having a desired thickness in step S400.

[41] In the above embodiment, the impurity gas is supplied when coalescence of the grains starts, i.e., the polysilicon layers are deposited. However, in order to obtain a smaller size of grains, the impurity gas may be supplied when the nanocrystal is formed not when the coalescence of the grains starts. Furthermore, the silicon source gas and the impurity gas may be simultaneously supplied to provide the impurity atom into the grain boundary. In this case, it is possible to mainly oxidize the grain boundary using an energy barrier between the grain and the grain boundary when a small amount of impurity gas is supplied. However, in case of simultaneously supplying the silicon source gas and the impurity gas, an amount of impurity atoms existing inside a polysilcon crystalloid may be increased. That is, the impurity atoms may exist in an undesired part of the crystalloid not in the grain boundary. Therefore, compared to simultaneously supplying the silicon source gas and the impurity gas, it is more effective to supply the impurity gas after stopping the supply of the silicon source gas.

[42] The polysilicon film that is formed in size of 5 nm to 10 nm as illustrated above may be used as a floating gate of a flash memory device, thereby increasing a program and erase speed, improving thermal stability and enhancing the reliability of the device. Hereinafter, there will be described the flash memory device that uses the polysilicon film having nano-size grains as its floating gate.

[43] FIG. 7 illustrates a cross-sectional view of a flash memory device empolying a polysilicon film that has nano-size grains and grain boundaries containing impurities therein.

[44] Referring to FIG. 7, the flash memory device includes a gate electrode 200 having a stack structure of a tunnel insulation layer 210 formed over a certain region of a simconductor substrate 110, a floating gate 220 formed of a polysilicon film having nano-size grains whose boundaries contain impurity atoms, a dielectric layer 230 and a control gate 240, and source/drain junction regions 250 formed at both sides of the gate electrode 200 in the semiconductor substrate 110.

[45] The semiconductor substrate 110 is formed of one selected from a group consisting of Si, Ge, SiGe, GaP, GaAs, SiC, SiGeC, InAs, InP and a combination thereof.

[46] The tunnel insulation layer 210 is formed of one selected from a group consisting of SiO_2, SiON, Si_3N_4, $Ge_xO_yN_z$, $Ge_xSi_yO_z$, a material having high permittivity and a combination thereof. For instance, the tunnel insulation layer 210 may include a structure formed by sequentially stacking two or more materials selected from the above materials. Herein, the SiO_2 layer may be formed by oxidation such as dry oxidation performed using an O_2 gas at the temperature of approximately 1000 ℃ to ap-

proximately 1100 ℃, wet oxidation performed in moisture atmosphere at the temperature of approximately 1000 ℃ to approximately 1100 ℃, HCl oxidation using a mixed gas of an O_2 gas and a HCl gas, oxidation using a mixed gas of an O_2 gas and a $C_2H_3Cl_3$ gas, oxidation using a mixed gas of an O_2 gas and a $C_2H_2Cl_2$ gas, and so on. The material having high permittivity may include one of HfO_2, ZrO_2, Al_2O_3, Ta_2O_5, hafnium silicate, zirconium silicate and a combination thereof to form a layer having the high permittivity by performing an atomic layer deposition method.

[47] The floating gate 220 is formed using the polysilicon film having grains whose boundaries contain impurity atoms, wherein a size of the grain ranges from approximately 5 nm to approximately 10 nm. The polysilicon film for forming the floating gate 220 is made by stacking a plurality of polysilicon layers and each of the polysilicon layers contains the impurity atoms in its grain boundaries. For this, a silicon source gas and an impurity gas are repeatedly supplied to form the polysilicon film having a desired thickness. The polysilicon layer is formed by supplying the silicon source gas at the temperature ranging from approximately 450 ℃ to approximately 800 ℃ and in the pressure of approximately 1E-5 Torr to approximately 760 Torr, wherein the silicon source gas includes one of SiH_4, Si_2H_6, $Si_2H_2Cl_2$ and a combination thereof. It is preferable that the thickness of the polysilicon layer is controlled to a grain size by adjusting an inflow amount and time of the silicon source gas. Then, the inflow of the silicon source gas is stopped at the time of coalescence of the grains and the impurity gas is supplied at the temperature ranging from approximately 450 ℃ to approximately 800 ℃ and in the pressure of approximately 1E-5 Torr to approximately 760 Torr. At this time, the temperature and pressure may be substantially the same as those required for performing a process of depositing polysilicon. Since it is possible to control the content of impurities provided into the grain boundaries by adjusting the temperature and the pressure, the temperature and the pressure are adjusted according to a desired grain size obtained by containing the impurities. Furthermore, by adjusting the inflow amount and time of the impurity gas, the impurity atoms are contained in the grain boundaries unless a film is formed by the impurity gas. By this way, the impurity atoms are contained in the grain boundaries of the polysilicon layer and thus growth of grains is suppressed in subsequent processes.

[48] The dielectric layer 230 may use an ONO layer or, like the tunnel insulation layer 210, it may use one selected from a group consisting of SiO_2, SiON, Si_3N_4, $Ge_xO_yN_z$, $Ge_xSi_yO_z$, a material having high permittivity and a combination thereof. The dielectric layer 230 may be formed to have a thickness greater than that of the tunnel insulation layer 210.

[49] The control gate 240 includes a conductive layer such as a polysilicon layer, a metal layer of W, Pt or Al, a metal nitride layer such as a TiN layer, a metal silicide layer

made of refractory metal such as Co, Ni, Ti, Hf and Pt, or a stack layer thereof. For instance, the control gate 240 may be formed by stacking a polysilicon layer and a metal silicide layer, or a polysilicon layer and a metal layer. Herein, the polysilicon layer may be formed using a silicon source gas such as a SiH_2Cl_2 gas and an impurity source gas such as a PH_3 gas, and performing an LPCVD method.

[50] The source/drain junction regions 250 are formed by injecting an n-type or p-type impurity into the semiconductor substrate 110 according to a desired type of a flash memory cell. The source/drain junction regions 250 may be formed with a lightly doped drain (LDD) region slightly formed performing a low concentration ion injection process and a heavily doped drain region deeply formed performing a high concentration ion injection process, wherein the heavily doped drain region is formed after the LDD region is formed. It is possible to effectively suppress the occurrence of a breakdown although a high voltage is supplied to the source/drain junction regions 250 since the source/drain junction regions 250 include the LDD region. In addition, a halo region may be formed beneath the heavily doped drain region and the LDD region by doping an impurity of a conductive type opposite to the conductive type of the source/drain junction regions 250. By including the halo region, it is possible to effectively maintain thermal electrons in a program operation.

[51] Furthermore, spacers 260 may be formed on sidewalls of the gate electrode 200. The spacers 260 may be formed before forming the heavily doped drain region when the source/drain junction region 250 includes the LDD region and the heavily doped drain region.

[52] The flash memory device in accordance with the embodiment of the present invention may be a NOR-type flash memory device or a NAND-type flash memory device according to a manufacturing method and the layout of peripheral circuits. The NAND-type flash memory device may be formed using various methods such as a self align shallow trench isolation (SASTI) method or a self align floating gate (SAFG) method.

[53] Although the present invention has been described with reference to the specific embodiments, they are not limited thereto. Therefore, it will be readily understood by those skilled in the art that various modifications and changes can be made thereto without departing from the spirit and scope of the present invention defined by the appended claims.

[54]

Claims

[1] A polysilicon film, comprising:
a plurality of polysilicon layers stacked to each other,
wherein each of the polysilicon layers includes a plurality of grains and contains impurity atoms in boundaries of the grains to suppress the growth of the grains.

[2] The polysilicon film of claim 1, wherein the grain has a size of approximately 5 nm to approximately 10 nm.

[3] The polysilicon film of claim 1, wherein the impurity atoms include nitrogen atoms or oxygen atoms, or both.

[4] A method of manufacturing a polysilicon film, the method comprising:
forming a polysilicon layer including a plurality of grains by supplying a silicon source gas; and
providing impurity atoms into boundaries of the grains by supplying an impurity gas.

[5] The method of claim 4, wherein the impurity gas is supplied after the supplying of the silicon source gas is stopped.

[6] The method of claim 5, wherein the silicon source gas is purged before the impurity gas is supplied.

[7] The method of claim 4, wherein the impurity gas and the silicon source gas are simultaneously supplied.

[8] The method of claim 4, wherein supplying the silicon source gas and supplying the impurity gas are repeated.

[9] The method of claim 4, wherein forming the polysilicon layer and providing the impurity atoms are performed at the temperature ranging from approximately 450 ℃ to approximately 800 ℃ and in the pressure of approximately 1E-5 Torr to approximately 760 Torr.

[10] The method of claim 4, wherein the impurity gas includes a gas including nitrogen atoms or oxygen atoms, or both.

[11] A flash memory device, comprising:
a gate electrode including a stack structure of a tunnel insulation layer, a floating gate, a dielectric layer and a control gate, which is formed over a certain region of a semiconductor substrate; and
source/drain junction regions formed at both sides of the gate electrode in the semiconductor substrate,
wherein the floating gate is formed by stacking a plurality of polysilicon layers, and each of the polysilicon layers includes a plurality of grains and contains impurity atoms in boundaries of the grains to suppress the growth of the grains.

[12] The flash memory device of claim 11, wherein the grain has a size of approximately 5 nm to approximately 10 nm.

[13] The flash memory device of claim 11, wherein the impurity atoms include nitrogen atoms or oxygen atoms, or both.

[14] A method of manufacturing a flash memory device, the method comprising:
forming a tunnel insulation layer over a semiconductor substrate and forming a polysilicon film containing impurities in boundaries of grains;
patterning the polysilicon film to form a resultant structure;
forming a dielectric layer and a conductive layer over a whole surface of the resultant structure;
patterning the conductive layer, dielectric layer, the polysilicon film and the tunnel insulation layer to form a gate electrode incuding a stack structure of a floating gate and a control gate; and
forming junction regions by injecting impurity ions into the semiconductor substrate at both sides of the gate electrode.

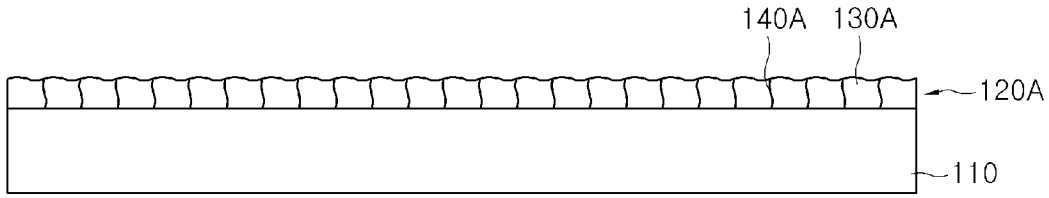
[15] The method of claim 14, wherein forming the polysilicon film comprises:
forming a polysilicon layer including a plurality of grains by supplying a silicon source gas; and
stopping the supplying of the silicon source gas and supplying an impurity gas to provide impurity atoms into the boundaries of the grains.

[16] The method of claim 14, wherein forming the polysilicon film comprises:
forming a polysilicon layer including a plurality of grains by supplying a silicon source gas; and
supplying the silicon source gas and an impurity gas to provide impurity atoms into the boundaries of the grains.

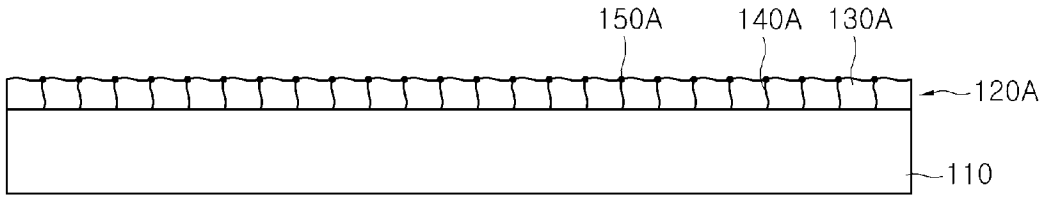
[17] The method of claim 15 or 16, wherein forming the polysilicon layer and providing the impurity atoms are performed at the temperature ranging from approximately 450 ℃ to approximately 800 ℃ and in the pressure of approximately 1E-5 Torr to approximately 760 Torr.

[18] The method of claim 15 or 16, wherein the impurity gas uses a gas including nitrogen atoms or oxygen atoms, or both.

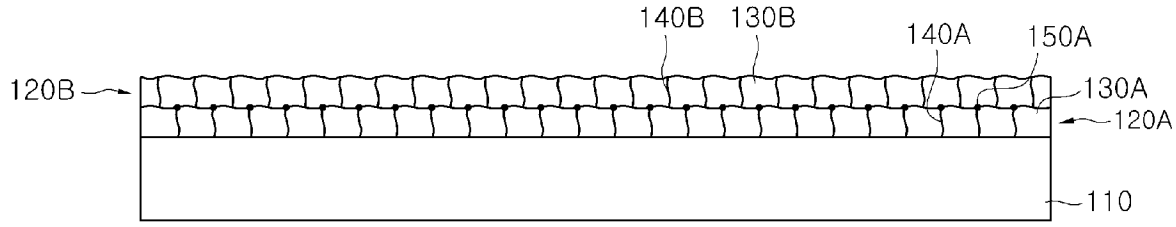
[Fig. 1]



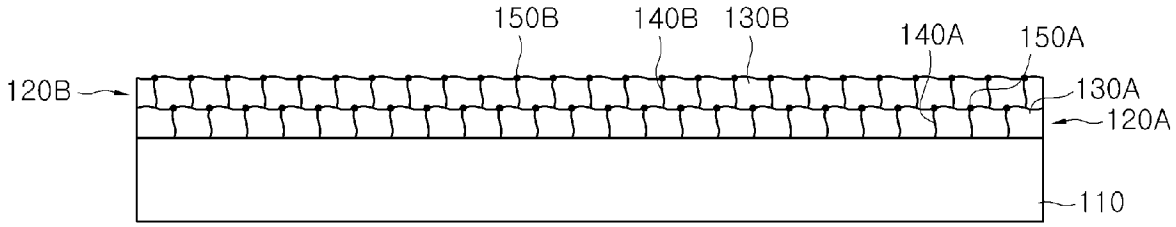
[Fig. 2]



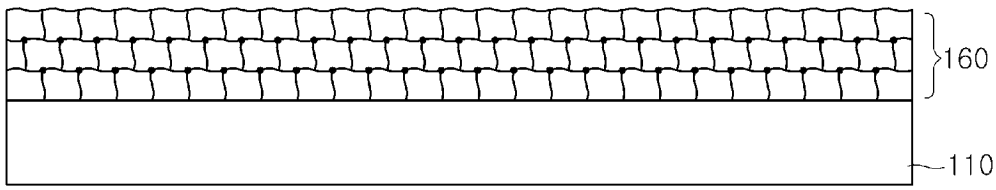
[Fig. 3]



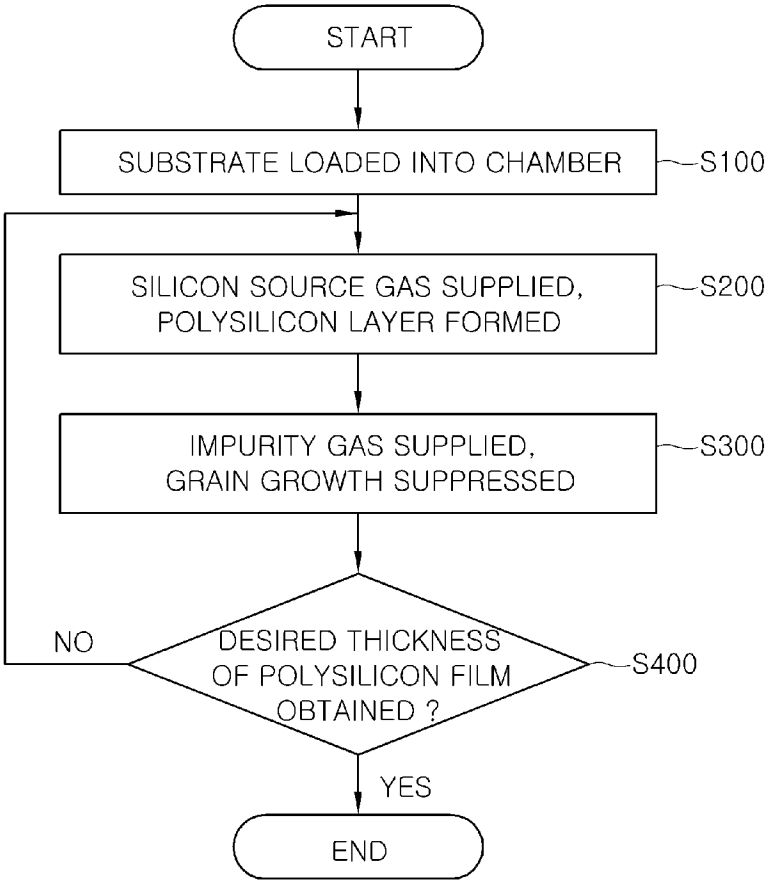
[Fig. 4]



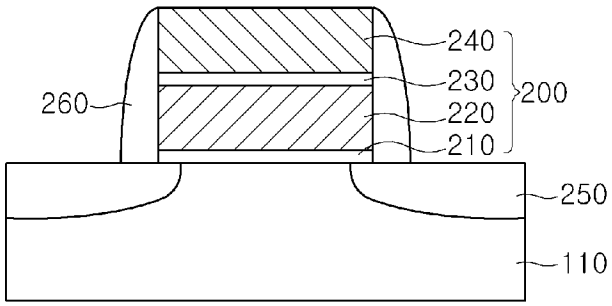
[Fig. 5]



[Fig. 6]


START
SUBSTRATE LOADED INTO CHAMBER
S100
SILICON SOURCE GAS SUPPLIED, POLYSILICON LAYER FORMED
S200
IMPURITY GAS SUPPLIED, GRAIN GROWTH SUPPRESSED
S300
NO
DESIRED THICKNESS OF POLYSILICON FILM OBTAINED ?
S400
YES
END

[Fig. 7]


240
230
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260
250
110