

May 19, 1959

B. J. WARMAN

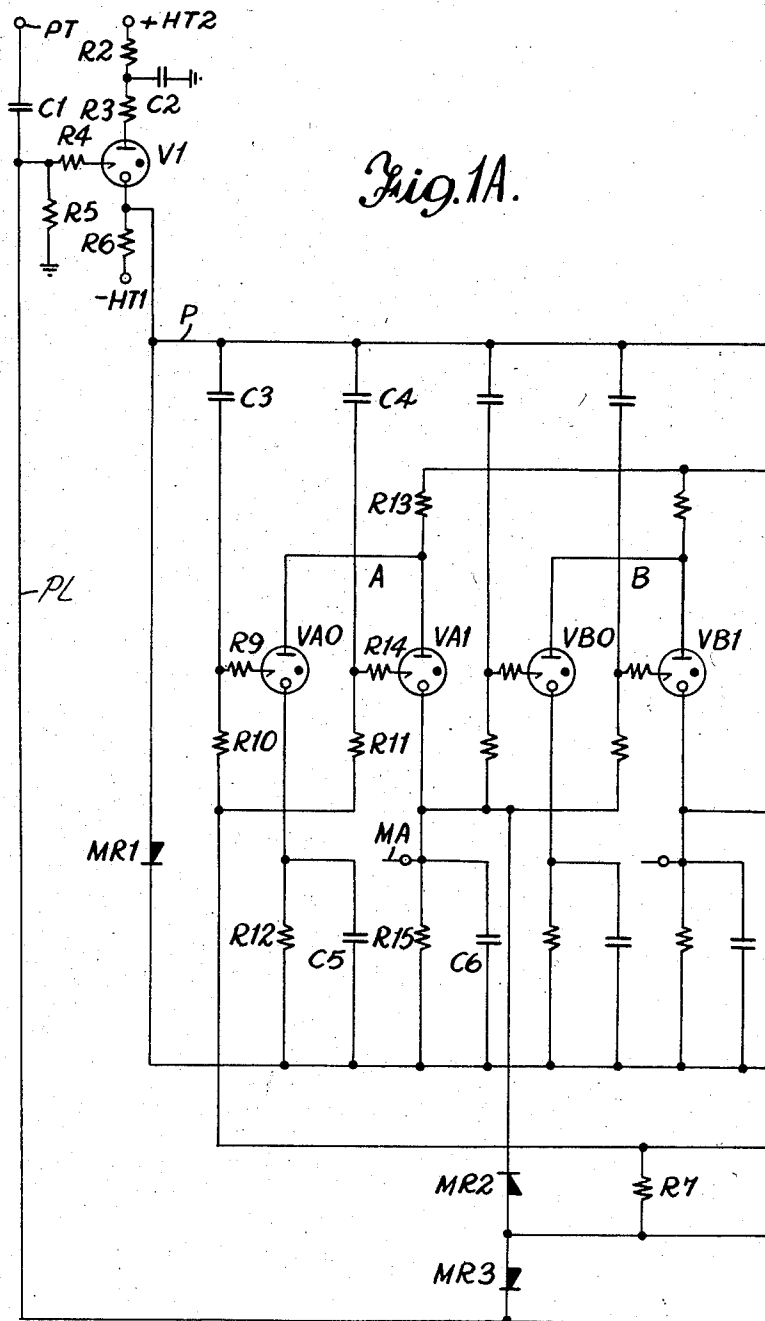
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ELECTRICAL IMPULSE COUNTERS

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Fig. 1A.



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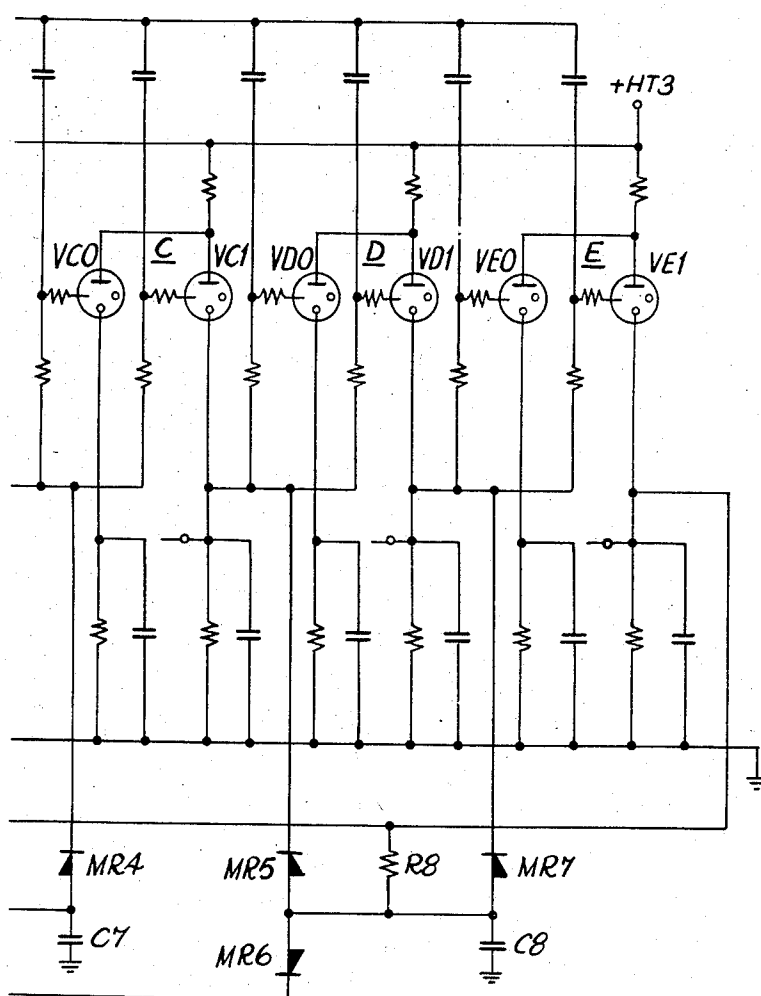
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Fig. 1B.



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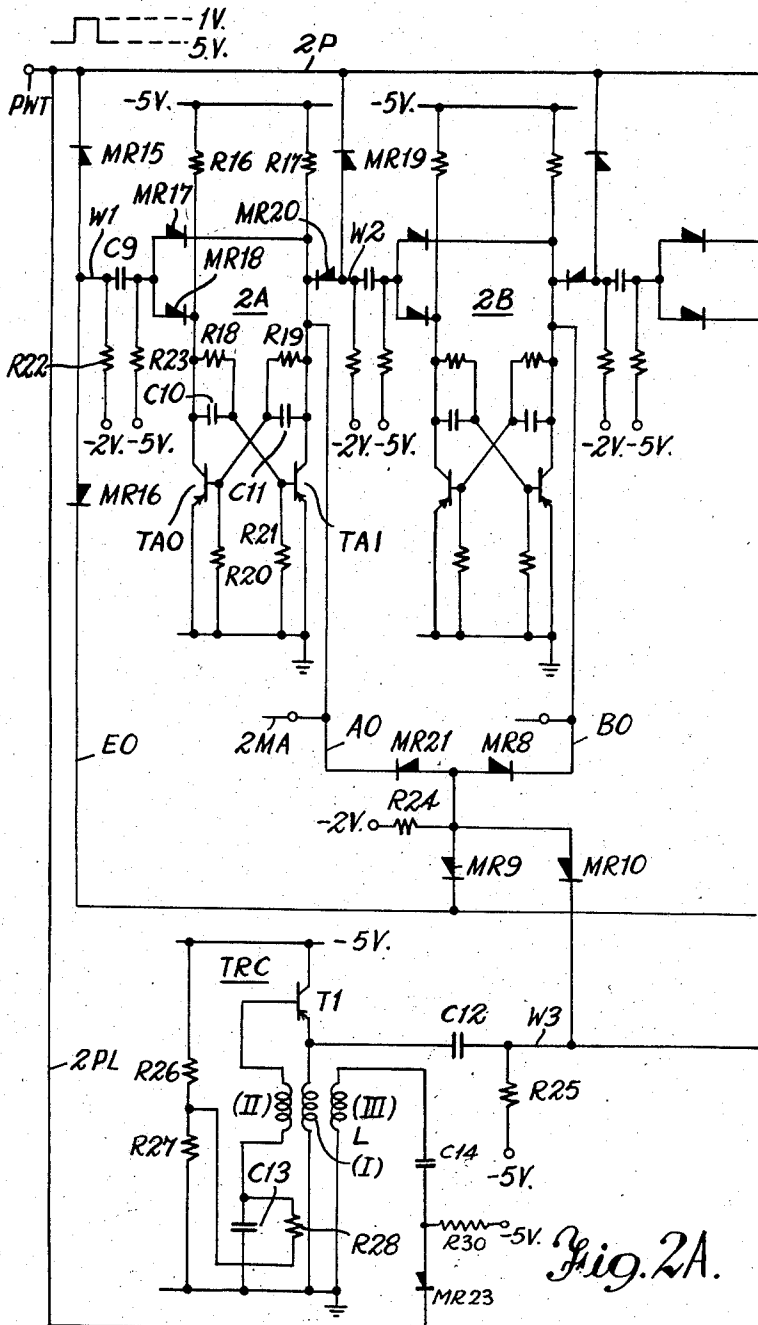
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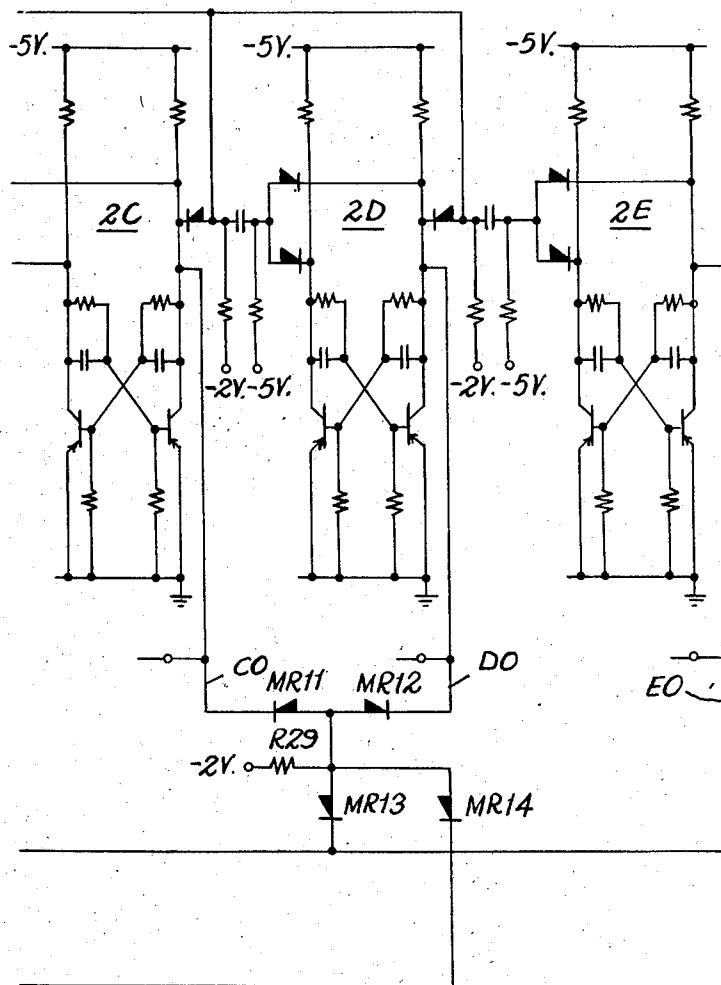


Fig. 2B.

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ELECTRICAL IMPULSE COUNTERS

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3 Claims. (Cl. 307—88.5)

This invention relates to electrical impulse counters, and has in view the provision of improved electrical impulse counters of the type adapted to furnish a code signal representing the result of a count. By a code signal is meant a signal such that different signals are constituted by the application of a signal condition to different combinations of code signalling wires. Impulse counters of the type referred to find applications in automatic telephone and like selective systems.

Electrical impulse counters are known which are arranged to count on a binary scale basis, counting being effected by a chain of binary counting elements each having a normal condition and a registering condition and each being arranged so that an impulse fed to it serves to reverse its condition.

Unless special provision is made, the code signals produced by a counter comprising a chain of binary counting elements counting on a strict binary scale basis and having an outgoing code signalling wire per counting element include signals constituted by the application of the signal condition to different kinds of combinations (e.g. one-at-a-time, two-at-a-time, and three-at-a-time combinations) of the wires, and arrangements have been proposed whereby unwanted or undesirable combinations are, in effect, skipped during the counting action. For some purposes it is required or desirable that the code signals utilised should be confined to signals constituted by the application of the signal condition to two-at-a-time combinations of a set of code signalling wires, and to obtain ten such code signals at least five counting elements are needed in a counter comprising a chain of counting elements. A counter counting on a strict binary scale basis and comprising a chain of five binary counting elements and having an outgoing code signalling wire per counting element will produce in one counting cycle thirty-one code signals, ten being code signals of the kind constituted by the application of the signal condition to two-at-a-time combinations of the five code signalling wires and twenty-one being code signals of kinds involving the application of the signal condition to other combinations of these wires including single wires. For a count of ten with the code signals utilised confined to signals constituted by the application of the signal condition to two-at-a-time combinations of the five code signalling wires, such a counter would have to be provided with means for skipping or otherwise eliminating twenty-one code signals, which would cause the counter to be so complicated and cumbersome as to be impracticable.

The present invention provides electrical impulse counters of a kind which, while providing on five code signalling wires ten code signals of the kind constituted by the application of a signal condition to two-at-a-time combinations of the wires, provides only a few code signals involving other combinations of these wires, thereby enabling comparatively simple means to be employed to effect the skipping or elimination of the last-mentioned code signals if required.

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According to a main feature of the present invention, there is provided an electrical impulse counter, of the type adapted to furnish a code signal representing the result of a count, wherein five similar counting elements each having a normal condition and a registering condition are connected to form a closed chain, and wherein in the general case when the counter is in operation performing a count electric pulses appearing on a pulse wire are applied to the counting elements to produce counting operation of the chain of counting elements, each such pulse being applied to all of the counting elements simultaneously, and wherein the chain of counting elements is arranged so that each counting element changes its condition, from its normal condition to its registering condition or vice versa, in response to an applied pulse from the pulse wire if, and only if, the immediately preceding counting element in the chain is in the registering condition at the time of application of this pulse, and wherein each counting element applies a signal condition to a corresponding one of five code signalling wires whilst the element is in the registering condition. To bring such a counter into a starting condition ready for counting it is necessary to bring, by a preliminary operation, any one or a combination of the counting elements less than the whole five elements to the registering condition, and this has the advantage that the starting condition may be chosen to suit the requirements of any particular application. A counter according to the invention will produce in one counting cycle fifteen code signals, ten being code signals of the kind constituted by the application of a signal condition to two-at-a-time combinations of the five code signalling wires, and five being code signals of the kind involving a signal condition on four-at-a-time combinations of these wires.

Designating, for the sake of description, the five counting elements of a counter according to the invention, taken in order around the closed chain, A, B, C, D, and E respectively, and representing, using the notation of the binary scale, the normal condition of a counting element by a "0" and the registering condition by a "1," the following table sets out a typical full counting cycle of such a counter, this cycle being one started with the counting element E in the registering condition:

Count	Condition of Counting Elements					Number of Code Signalling Wires Marked
	A	B	C	D	E	
0	0	0	0	0	1	Starting condition
1	1	0	0	0	1	2
2	0	1	0	0	1	2
3	1	1	1	0	1	4
4	0	0	0	1	1	2
5	1	0	0	1	0	2
6	1	1	0	1	1	4
7	0	0	1	1	0	2
8	0	0	1	0	1	2
9	1	0	1	1	1	4
10	0	1	1	0	0	2
11	0	1	0	1	0	2
12	0	1	1	1	1	4
13	1	1	0	0	0	2
14	1	0	1	0	0	2
15	1	1	1	1	0	4
1	1	0	0	0	1	2

If it is required, in the case of a counter according to the invention, that the counter should be adapted to perform counts of up to ten with the code signals utilised confined to signals constituted by the application of a signal condition to two-at-a-time combinations of the five code signalling wires, at least four of the five code signals of the kind involving a signal condition on four-at-a-time combinations of these wires must be skipped to exclude them from the count.

According to a further feature of the invention, an electrical impulse counter, constituted and arranged in accordance with the feature previously set forth, is provided with arrangements which operate to produce an auxiliary electric pulse on the pulse wire in response to the production, by the chain of counting elements when the counter is in operation performing a count, of an unwanted or undesirable code signal constituted by the application of the signal condition to four of the five code signalling wires, the said auxiliary pulse serving to change the condition of the chain of counting elements so that the condition giving rise to the unwanted or undesirable code signal is in effect skipped. The preferred manner of carrying out the invention as regards this feature is to employ a coincidence-of-three gating circuit which is connected so that when, during the performance of a count, the chain of counting elements is brought to a condition in which a particular three of the counting elements are all in the registering condition simultaneously, the gating circuit produces an output signal which serves to bring about the production of an auxiliary electric pulse on the pulse wire. Whilst the skipping of four of the five code signals of the kind involving a signal condition on four-at-a-time combinations of the five code signalling wires can be readily catered for by the provision of two coincidence-of-three gating circuits, additional apparatus would be required to bring about the skipping of the remaining such code signal. However, by arranging that one such code signal is produced at the end of the full counting cycle, as occurs in the typical full counting cycle to which the previously-given table relates, this particular code signal may be neglected or alternatively it may be made use of for giving a special or distinctive signal.

As counting elements any devices may be employed which are of a kind capable of assuming a normal and a registering condition. Suitable bi-stable elements may for example be constituted by electro-magnetic relays, thermionic valves, cold cathode electric discharge tubes, or transistors.

The features of the invention are exemplified in the two specific embodiments of its which will now be described with reference to the accompanying drawings. Figs. 1A and 1B together constitute a circuit diagram illustrating an electrical impulse counter according to the invention in which each of the five counting elements comprises a pair of three-electrode cold cathode electric discharge tubes, and Figs. 2A and 2B together constitute a circuit diagram illustrating an electrical impulse counter according to the invention in which each of the five counting elements comprises a pair of transistors.

Referring firstly to Figs. 1A and 1B, these two figures should be viewed with Fig. 1B placed to the right of Fig. 1A to constitute a single circuit diagram. The counter to which this diagram pertains comprises five identical counting elements A, B, C, D, and E which are connected in an endless chain. Each of the counting elements comprises two three-electrode cold cathode electric discharge tubes, the pairs of tubes being VA0, VA1 to VE0, VE1 which are arranged as bi-stable pairs. One of the tubes of a bi-stable pair will conduct in the normal or non-registering condition of the element and the other tube of the pair will conduct in the registering condition of the element, the two tubes being suffixed "0" and "1" respectively, using the notation of the binary scale. Since the five counting elements are identical, the connections in respect of element A only will be described, these serving also to typify the similar connections of the other counting elements. The anodes of the two tubes VA0 and VA1 are connected over a common anode resistor R13 to a source of anode voltage +HT3. The cathodes of these two tubes are connected to earth over parallel-connected resistor-capacitor combinations R12 and C5, and R15 and C6, respectively, the cathode of the tube VA1 being further connected to an outgoing

code signalling wire MA. The trigger electrodes of these two tubes are connected to serially-connected current limiting and coupling resistors R9 and R10, and R14 and R11, respectively, the ends of the coupling resistors R10 and R11 remote from the tubes being connected together and to the cathode of the "1" tube VE1 in the preceding element in the chain, and the junctions of the current limiting and coupling resistors being connected over coupling capacitors C3 and C4 respectively to a pulse wire P over which pulses for the operation of the counting elements of the counter are applied to these elements. Connected between the pulse wire P and earth is a pulse restoring rectifier MR1 poled so as to permit flow of current to earth.

Each of two "coincidence-of-three" gating circuits included in the counter circuit consists of a resistor and two rectifiers, rectifiers MR2 and MR4 and resistor R7 serving to constitute one gating circuit, and rectifiers MR5 and MR7 and resistor R8 serving to constitute the other gating circuit. The resistor in each gating circuit is connected, at its end remote from the junction of the gating circuit components, to the cathode of the "1" tube of an element providing a registration in each of four different four-wire registrations that are to be skipped, i.e. to the cathode of the tube VE1. The rectifiers MR2 and MR4 of one gating circuit are connected to the cathodes of the "1" tubes in the elements A and B respectively, and the rectifiers MR5 and MR7 of the other gating circuit are connected to the cathodes of the "1" tubes in the elements C and D respectively. These gate rectifier and gate resistor connections cover the four-wire registration combinations 3, 6, 9 and 12 so that whenever any one of these obtains one or other of the gating circuits produces an output signal. The resistor-rectifier junctions of the two gating circuits are connected to a local pulse wire PL through rectifiers MR3 and MR6 respectively. These rectifiers mutually isolate the resistor-rectifier junctions of the two gating circuits when the potential of either of these junctions is raised to produce a positive output signal on the local pulse wire PL. The resistor-rectifier junctions of the two gating circuits are also connected to one side of capacitor C7 and to one side of capacitor C8 respectively, the other sides of these capacitors being connected to earth. When the potential of the resistor-rectifier junction of either of the two gating circuits is raised the corresponding capacitor C7 or C8 is charged with the result that in effect the output impedance of the gating circuit concerned is lowered.

The pulses to be counted, and the locally-derived auxiliary stepping pulses that are constituted by the outputs of the two "coincidence-of-three" gating circuits, are applied to the pulse wire P via a trigger circuit which consists of the three-electrode cold cathode electric discharge tube V1 and associated components. The anode of the tube V1 is connected through resistors R3 and R2 joined in series to a source of positive potential +HT2, and the junction of these two resistors is connected to earth via capacitor C2. The cathode of the tube V1 is connected through resistor R6 to a source of negative potential -HT1, and to the pulse wire P. The trigger electrode of the tube V1 is connected through resistors R4 and R5 to earth, with the result that a bias potential, which is positive with respect to the normal potential at the cathode, is permanently applied to the trigger electrode. The junction of the resistors R4 and R5 is connected via capacitor C1 to an input terminal PT to which the pulses to be counted are applied, and to the local pulse wire PL.

In operation, the tube V1 will fire on the application of a pulse (either one to be counted or an auxiliary stepping pulse) through resistor R4 to its trigger electrode, and the resultant output voltage which is produced at its cathode is applied to the pulse wire P. The tube is made self-extinguishing, in the well known manner, by the

action of resistor R2 and capacitor C2 so that the said output voltage persists on the pulse wire P for a short period of time only, thereby producing an amplified input pulse on this wire. Such pulses on the pulse wire P are applied to the trigger electrode of each of the tubes VA0 to VE1 via the associated capacitor such as C3 or C4, but these pulses are of insufficient amplitude to fire a tube unless the tube already has its trigger electrode biased positive to some suitable potential. Assuming that the starting condition of the previously-given table obtains, the tubes VA0 and VA1, of which VA0 is already fired, will have their trigger electrodes biased positively by the potential from the cathode of the tube VE1, so that the first pulse applied to the pulse wire P causes tube VA1 to fire which is effective in the well known manner to extinguish the tube VA0. Counting elements A and E are now both in the registering condition to signify a count of 1 as shown in the table. On the application of the second pulse to the pulse wire P element B is changed to the registering condition since tube VB1 is fired and element A is changed to the non-registering condition since tube VA0 is fired. Elements B and E are now both in the registering condition to signify a count of 2. On the application of the third pulse to the pulse wire P what first happens is that elements A and C are changed to the registering condition and elements B and E remain in the registering condition so that for a brief period a four-wire registering condition obtains. However, since rectifiers MR2 and MR4 are backed off by the positive condition of the cathodes of tubes VA1 and VB1 respectively and resistor R7 has a positive potential applied to it from the cathode of the tube VE1, the potential of the resistor-rectifier junction of the gating circuit constituted by rectifiers MR2 and MR4 and resistor R7 is raised causing rectifier MR3 to conduct to produce an auxiliary stepping pulse on the local pulse wire PL. This auxiliary stepping pulse serves to fire tube V1 and thereby cause a further pulse to appear on the pulse wire P so that the four-wire registering condition is stepped over or skipped and the succeeding two-wire condition, in which elements D and E only are in the registering condition, obtains. This procedure continues on the application of further pulses to the pulse wire P, with one or other of the two "coincidence-of-three" gating circuits producing an auxiliary stepping pulse each time a four-wire registering condition obtains. The rectifier MR1 which is connected between the pulse wire P and earth is included to discharge the capacitors such as C3 and C4 after each pulse on the pulse wire P.

Referring now to Figs. 2A and 2B, these two figures should be viewed with Fig. 2B placed to the right of Fig. 2A to constitute a single circuit diagram. The counter to which this diagram pertains is similar in many respects, so far as its general organization and scheme of operation are concerned, to that of Figs. 1A and 1B except that transistor circuit elements are employed in place of cold cathode triode circuit elements.

The counter comprises five identical counting elements 2A, 2B, 2C, 2D and 2E corresponding respectively to the elements A, B, C, D, and E in Figs. 1A and 1B. Considering by way of example the counting element 2A, this is a bi-stable trigger circuit employing two transistors TA0 and TA1. These transistors have respective collector resistors R16 and R17, the ends of which remote from the transistors are connected to a suitable source of negative potential (for example -5 volts as shown in the figure). The base of the transistor TA0 is connected to the collector of the transistor TA1 through the parallel combination of a resistor R19 and a capacitor C11. Similarly, the base of the transistor TA1 is connected to the collector of the transistor TA0 through the parallel combination of a resistor R18 and a capacitor C10. The bases of the two transistors are further con-

nected to earth through respective resistors R20 and R21. The emitter of each transistor is connected directly to earth. The collector of the transistor TA1 is connected to an outgoing code signalling wire 2MA. A common input wire W1 is connected through capacitor C9 to the collectors of the two transistors via respective rectifiers MR18 and MR17 which are poled so as to conduct current towards the collectors. The side of the capacitor C9 connected to the common input wire W1 is further connected through a resistor R22 to a source of negative potential of value (for example -2 volts as shown in the figure) just less than half that of the source of negative potential to which resistors R16 and R17 are connected and the other side of the capacitor C9 is connected through a resistor R23 to the last-mentioned source of negative potential. The input wire W1 is connected to a pulse wire 2P through a rectifier MR15, and to the output wire E0 from the previous element 2E in the chain through a rectifier MR16, both rectifiers being poled so as to conduct current away from the input wire W1. Assuming that a starting condition corresponding to that of the previously-given table obtains, the counting element 2A is in the non-registering condition so that transistor TA0 is conducting and transistor TA1 almost cut-off, the potential of the collector of the transistor TA0 being raised towards earth, owing to the flow of collector current, to hold the base of the transistor TA1 at a potential such that no effective current flows in the collector circuit of this latter transistor, the collector of which is consequently held negative at a value approaching that of the source of negative potential to which resistors R16 and R17 are connected. With the starting condition referred to obtaining, the rectifier MR16 is backed off since the transistor similar to transistor TA1 in the counting element 2E is fully conducting so that its collector potential is positive with respect to the potential of the source of negative potential to which resistor R22 is connected. Although rectifier MR16 is thus backed off and rendered non-conducting, this does not in itself serve to raise effectively the potential of the input wire W1, since the quiescent potential of the pulse wire 2P is that of the source of negative potential to which resistors R16 and R17 are connected so that rectifier MR15 remains conducting to clamp the input wire W1 to a potential approaching that of the last-mentioned source of negative potential. On the application to the pulse wire 2P of a pulse positive with respect to the potential of the source of negative potential to which resistor R22 is connected, and of suitable amplitude, rectifier MR15 also becomes backed off and rendered non-conducting, with the result that the potential of the input wire W1 rises. This rise of potential of the input wire W1, transmitted through the capacitor C9 and the rectifier MR17, serves to raise the potential of the collector of the transistor TA1, thereby increasing the flow of current in the circuit of this collector and initiating the changing over of the counting element from the non-registering condition to the registering condition in which transistor TA0 is almost cut-off and transistor TA1 is conducting. This changing over is accelerated and completed by the now well-known regenerative action due to the couplings between the two transistors.

The rectifiers MR19 and MR20 connected to the input wire W2 of the counting element 2B correspond respectively to the rectifiers MR15 and MR16 connected to the input wire W1 of the counting element 2A. The general manner of operation of the counter of Figs. 2A and 2B in response to pulses to be counted applied to input terminal PWT will now be apparent from the description of counting element 2A which has just been given, and from the description already given with reference to Figs. 1A and 1B. It is, however, necessary to refer briefly to the means provided for skipping the four-wire registering conditions. These means comprise two

"coincidence-of-three" gating circuits corresponding, so far as their effects are concerned, to the two "coincidence-of-three" gating circuits of Figs. 1A and 1B, and also comprise a trigger circuit TRC of a known kind having only one stable condition. Rectifiers MR8, MR9, and MR21 and resistor R24, constitute one gating circuit, and rectifiers MR11, MR12, and MR13, and resistor R29 constitute the other gating circuit. In the case of each of these two gating circuits, the resistor is connected, at its end remote from the junction of the gating circuit components, to the source of negative potential to which resistor R22 is connected. The rectifiers MR21, MR8, and MR9, are connected to the output wires A0, B0, and E0 of the counting elements 2A, 2B, and 2E respectively, and the rectifiers MR11, MR12, and MR13 are connected to the output wires C0, D0, and E0 of the counting elements 2C, 2D, and 2E respectively. These gate rectifier connections cover the four-wire registration combinations 3, 6, 9, and 12 so that whenever any one of these obtains one or other of the two gating circuits produces an output signal. The resistor-rectifier junctions of the two gating circuits are connected to the input wire W3 of the trigger circuit TRC through isolating rectifiers MR10 and MR14 respectively. Whenever one of the said four-wire registration combinations obtains, the resulting rise of potential of the input wire W3 of the trigger circuit TRC triggers this circuit to its unstable condition with the result that the requisite auxiliary stepping pulse is produced on the output wire 2PL and hence on the pulse wire 2P.

The trigger circuit TRC comprises a transistor T1, a transformer L, an input resistor R25, an input capacitor C12, an output capacitor C14, an output resistor R30, an output rectifier MR3, a capacitor C13, and three resistors R26, R27, and R28. Whenever one of the said four-wire registrations obtains, the resulting rise of potential of the input wire W3, transmitted through the input capacitor C12, serves to raise the potential of the emitter of the transistor T1, with the result that the emitter current begins to increase. Consequently, the current in winding (I) of transformer L begins to increase and, the transformer windings being arranged to this end, a pulse tending to lower the potential of the base of the transistor T1, and thereby still further increase the emitter current, is produced in winding (II) of the transformer. Eventually, however, the capacitor C13 assumes a state of charge at which the potential of the base of the transistor becomes too high (i.e. too positive with respect to the potential of the source of negative potential to which the collector is directly connected) for the high emitter current to be maintained, whereupon the trigger circuit reverts to its normal condition. Upon the increase of emitter current referred to, the output winding (III) of the transformer produces the requisite auxiliary stepping pulse on the output wire 2PL.

When used as an impulse counter in an automatic telephone system, a counter according to the invention would be arranged to have applied to its pulse wire one pulse to be counted (i.e. distinct from any auxiliary stepping pulse or pulses) in respect of each received impulse from a dial or other source of impulses.

What I claim is:

1. An electrical impulse counter comprising a pulse wire on which electric pulses appear when the counter is in operation performing a count, first and second and third and fourth and fifth counting elements each having a normal condition and a registering condition, said five counting elements being similar to one another and being connected to form a closed chain of counting elements in which the counting elements appear in cyclic order

means for applying each pulse appearing on said pulse wire to all said counting elements simultaneously, means involving interconnections between counting elements for causing each said counting element to change its condition, from whichever of its two conditions it happens to be in to the other, in response to an applied pulse from said pulse wire when, and only when, the immediately preceding counting element in said chain is in the registering condition at the time of application of this pulse, for each said counting element a code signalling wire to which the counting element applies a signal condition whilst the counting element is in the registering condition, a first coincidence-of-three gating circuit connected to produce an output signal in response to the assumption by said chain of counting elements of a condition in which said first and second and fifth counting elements are all in the registering condition simultaneously, a second coincidence-of-three gating circuit connected to produce an output signal in response to the assumption by said chain of counting elements if a condition in which said third and fourth and fifth counting elements are all in the registering condition simultaneously, and a trigger circuit, responsive to the production of an output signal by either of said first and second coincidence-of-three gating circuits, for producing on said pulse wire an auxiliary electric pulse serving to change the condition of said chain of counting elements to cause a condition of this chain giving rise to an unwanted code signal to be in effect skipped.

2. An electrical impulse counter comprising a pulse wire on which electric pulses appear when the counter is in operation performing a count, five similar counting elements each having a normal condition and a registering condition, said counting elements being connected to form a closed chain of counting elements, means for applying each pulse appearing on said pulse wire to all said counting elements simultaneously, means involving interconnections between counting elements for causing each said counting element to change its condition, from whichever of its two conditions it happens to be in to the other, in response to an applied pulse from said pulse wire when and only when, the immediately preceding counting element in said chain is in the registering condition at the time of application of this pulse, for each said counting element a code signalling wire to which the counting element applies a signal condition whilst the counting element is in the registering condition, and means, responsive to the assumption by said chain of counting elements of a condition in which it produces an unwanted code signal constituted by the application of the signal condition to four of said code signalling wires, for producing on said pulse wire an auxiliary electric pulse serving to change the condition of said chain to cause the particular condition giving rise to the unwanted code signal to be in effect skipped.

3. An electrical impulse counter as claimed in claim 2 in which said means for producing an auxiliary electric pulse includes a coincidence-of-three gating circuit connected to produce an output signal in response to the assumption by a combination of said counting elements comprising a particular three of these elements of a condition in which all three elements of the combination are in the registering condition simultaneously.

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