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(54) Title: A SOC DESIGN WITH CRITICAL TECHNOLOGY PITCH ALIGNMENT

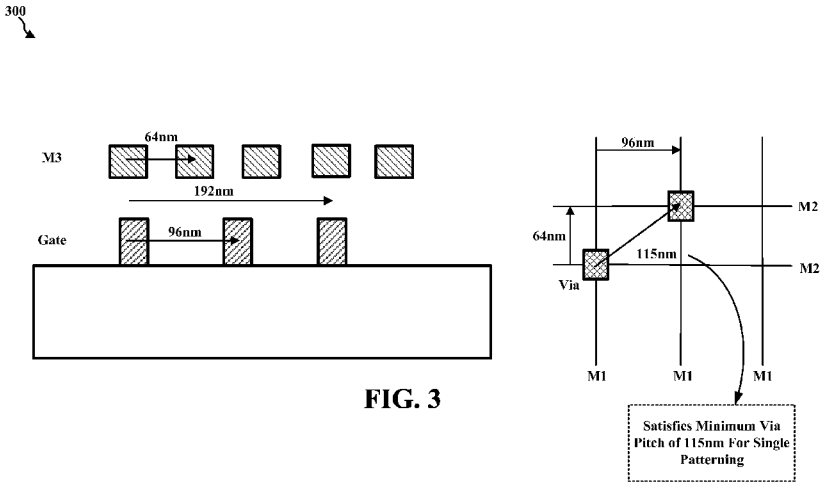

FIG. 3

(57) Abstract: An SOC apparatus includes a plurality of gate interconnects with a minimum pitch g, a plurality of metal interconnects with a minimum pitch m, and a plurality of vias interconnecting the gate interconnects and the metal interconnects. The vias have a minimum pitch v. The values m, g, and v are such that $g^2+m^2 \geq v^2$ and an LCM of g and m is less than 20g. The SOC apparatus may further include a second plurality of metal interconnects with a minimum pitch of $m2$, where $m2 > m$ and the LCM of g, m, and m^2 is less than 20g.

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A SOC DESIGN WITH CRITICAL TECHNOLOGY PITCH ALIGNMENT

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims the benefit of U.S. Provisional Application Serial No. 61/858,567, entitled "A SOC DESIGN WITH CRITICAL TECHNOLOGY PITCH ALIGNMENT" and filed on July 25, 2013, and U.S. Non-Provisional Application Serial No. 14/338,229, entitled "A SOC DESIGN WITH CRITICAL TECHNOLOGY PITCH ALIGNMENT" and filed on July 22, 2014, which are expressly incorporated by reference herein in their entirety.

BACKGROUND

Field

[0002] The present disclosure relates generally to a circuit layout, and more particularly, to a system on a chip (SOC) design with critical technology pitch alignment.

Background

[0003] A pitch is the distance between the same type of adjacent elements. To achieve cost, power, and performance benefits of scaling a pitch by x%, an area scaling of approximately x^2% should be obtained. For example, to achieve the full cost, power, and performance benefits of a 70% pitch scaling, approximately a 50% area scaling should be obtained. However, given a requirement to obtain an x^2% area scaling, an x% pitch scaling may not provide the best cost, power, and performance benefits. As such, methods and apparatuses are needed for determining a pitch or pitch scaling given a desired area scaling.

SUMMARY

[0004] In an aspect of the disclosure, a method and an apparatus are provided. An SOC apparatus includes a plurality of gate interconnects with a minimum pitch g, a plurality of metal interconnects with a minimum pitch m, and a plurality of vias interconnecting the gate interconnects and the metal interconnects. The vias have a minimum pitch v. The values m, g, and v are such that $g^2 + m^2 \geq v^2$ and an LCM of g and m is less than $20g$.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 is a diagram illustrating pitch scalings.

[0006] FIG. 2 is a diagram illustrating gate interconnect, metal interconnect, and via pitches.

[0007] FIG. 3 is a diagram illustrating a first set of exemplary gate interconnect, metal interconnect, and via pitches.

[0008] FIG. 4 is a diagram illustrating a second set of exemplary gate interconnect, metal interconnect, and via pitches.

[0009] FIG. 5 is a flow chart of a method of operating an SOC apparatus.

DETAILED DESCRIPTION

[0010] The detailed description set forth below in connection with the appended drawings is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of various concepts. However, it will be apparent to those skilled in the art that these concepts may be practiced without these specific details. In some instances, well known structures and components are shown in block diagram form in order to avoid obscuring such concepts. Apparatuses and methods will be described in the following detailed description and may be illustrated in the accompanying drawings by various blocks, modules, components, circuits, steps, processes, algorithms, elements, etc.

[0011] FIG. 1 is a diagram 100 illustrating pitch scalings. As shown in FIG. 1, in a 28nm manufacturing process technology, the gate interconnect (may also be referred to as "POLY" interconnect) may have a minimum pitch of g_1 (the distance between any two gate interconnects is at the minimum g_1). Upon scaling in a 20nm, 16nm, 14nm, and/or other manufacturing process technology, the gate interconnect may have a minimum pitch of g_2 (the distance between any two gate interconnects is at the minimum g_2). In one example, g_1 may be 130nm. A 70% scaling of the gate interconnect pitch would result in a g_2 of 90nm. In a 28nm manufacturing process technology, the first metal layer M1 may have a minimum pitch of $m1_1$ (the distance between any two first metal layer M1 interconnects is at the minimum $m1_1$). Upon scaling in a 20nm, 16nm, 14nm, and/or other manufacturing process technology, the first metal layer M1 may have a minimum pitch of $m1_2$ (the distance between any

two first metal layer M1 interconnects is at the minimum $m1_2$). In one example, $m1_1$ may be 90nm. A 70% scaling of the first metal layer M1 interconnect pitch would result in an $m1_2$ of 64nm. In a 28nm manufacturing process technology, other metal layers Ma (e.g., M2, M3, M4, M5) may have a minimum pitch of ma_1 (the distance between any two metal layer Ma interconnects is at the minimum ma_1). Upon scaling in a 20nm, 16nm, 14nm, and/or other manufacturing process technology, the metal layer Ma may have a minimum pitch of ma_2 (the distance between any two metal layer Ma interconnects is at the minimum ma_2). In one example, ma_1 may be 90nm. A 70% scaling of the metal layer Ma interconnect pitch would result in an ma_2 of 64nm. In the 20nm, 16nm, 14nm, and/or other manufacturing process technology, the Mb metal layer may have a pitch of mb. The Mb metal layer is higher than the Ma metal layer and may be wider than the Ma metal layer. For example, the Ma metal layer may include an M2 metal layer and an M3 metal layer, and the Mb metal layer may include an M4 metal layer. For another example, the Ma metal layer may include an M2 metal layer, an M3 metal layer, and an M4 metal layer, and the Mb metal layer may include an M5 metal layer. In one example, mb is 80nm. In a 28nm manufacturing process technology, vias may have a minimum pitch of v_1 (the distance between any two vias is at the minimum v_1). Upon scaling in a 20nm, 16nm, 14nm, and/or other manufacturing process technology, the vias may have a minimum pitch of v_2 (the distance between any two vias is at the minimum v_2). In one example, v_1 may be 130nm. Maintaining a process limit due to a single patterning process (using only one mask rather than multiple masks in a double patterning process) limits the minimum pitch of any two vias. Assuming a 115nm minimum pitch (i.e., assuming v_2 is 115nm) results in an 88% scaling of the vias. In this example, the via pitch is not necessarily scaled similar to other elements, such as the gate and metal interconnects.

[0012] In the aforementioned example of FIG. 1, given an 88% pitch scaling limit for the vias, scaling all of the other metal layers by 70% is not ideal because the interconnects and vias are not aligned. As discussed *supra*, to achieve cost, power, and performance benefits of scaling a pitch by x%, an area scaling of approximately x^2% should be obtained. For example, to achieve the full cost, power, and performance benefits of a 70% pitch scaling, approximately a 50% area scaling should be obtained. However, as discussed further in relation to FIG. 2, given a

requirement to obtain an x^2% area scaling, an x% pitch scaling may not provide the best cost, power, and performance benefits when limiting the via pitch scaling.

[0013] FIG. 2 is a diagram 200 illustrating gate interconnect, metal interconnect, and via pitches. In FIG. 2, the two shown metal layer M1 interconnects extend in the same direction as the gate interconnects, are connected to the gate interconnects, and have the same pitch as the gate interconnects. Other metal layer M1 interconnects may have a smaller pitch, such as 64nm. Accordingly, as shown in FIG. 2, when the gate interconnect pitch g_2 is a minimum 90nm and the metal layer M2 pitch ma_2 is a minimum 64nm, the via pitch v_2 is 110nm. If the process limit for single patterning is 115nm for the via pitch, a via pitch of 110nm would not satisfy the minimum via pitch requirements for single patterning. Assuming a via pitch of 115 nm and a 70% pitch scaling for the gate interconnect and the metal layer M2, the gate interconnect, vias, and metal interconnect pitches would not align, which can cause pin access difficulty, degrade place and route efficiency, and cause a low place and route utilization (the area utilized may not be reduced to 50%). In one configuration, the scaling of the gate interconnect pitch g_2 and/or the metal layer M2 interconnect pitch ma_2 may be increased in order to satisfy the requisite scaling of the via pitch v_2, and allow for improved pin access, place and route efficiency, and place and route utilization.

[0014] FIG. 3 is a diagram 300 illustrating a first set of exemplary gate interconnect, metal interconnect, and via pitches. As discussed *supra*, the scaling of the gate interconnect pitch g_2 and/or the metal layer M2 interconnect pitch ma_2 may be increased in order to satisfy the requisite scaling of the via pitch v_2. For example, as shown in FIG. 3, the scaling of the gate interconnect pitch g_2 is increased to 73.85%. When the gate interconnect pitch g_2 is a minimum 96nm and the metal layer M2 pitch ma_2 is a minimum 64nm, the via pitch v_2 is 115nm, which satisfies the aforementioned 115nm via pitch limit. As shown in FIG. 3, the metal layer M3 pitch may also be a minimum of 64nm. The least common multiple (LCM) (also referred to as lowest common multiple) of 96nm and 64nm is 192nm. In one configuration, the LCM of the minimum gate and metal interconnect pitches may be constrained to be less than 20 times the minimum gate interconnect pitch. For example, the LCM of the minimum gate and metal interconnect pitches may be constrained to be less than 1920nm (20*96nm). In this case, the minimum gate and

metal interconnect pitches of 96nm and 64nm, respectively, satisfy such a requirement.

[0015] FIG. 4 is a diagram 400 illustrating a second set of exemplary gate interconnect, metal interconnect, and via pitches. In this example, the minimum gate interconnect pitch may be 96nm, the minimum metal layers M2 may be 64nm, the minimum metal layer M3 pitch may be 72nm, and the minimum metal layer M5 pitch may be 80nm. The LCM of 96nm, 72nm, and 80nm is 1440nm.

[0016] In one configuration, an SOC apparatus may have a plurality of gate interconnects with a minimum pitch g, a plurality of metal interconnects with a minimum pitch m, and a plurality of vias interconnecting the gate interconnects and the metal interconnects. The vias have a minimum pitch v. The pitches g, m, and v are such that $g^2 + m^2 \geq v^2$ and an LCM of g and m is less than $20g$. In one example, g is equal to or is approximately equal to 96nm, m is equal to or is approximately equal to 64nm, and v is equal to or is approximately equal to 115nm. With pitches of g=96nm and m=64nm, the LCM is 192nm, which is less than 1920nm. The pitches g, m, and v are constrained by the equations $g^2 + m^2 \geq v^2$ and LCM(g,m)<20g. In one configuration, a via pitch v is assumed, and the gate interconnect pitch g and metal interconnect pitch m are adjusted to satisfy the equations. The plurality of metal interconnects are on at least one of a first interconnect level or a second interconnect level, and the vias interconnect the metal interconnects between the first interconnect level and the second interconnect level. The first interconnect level may be a first metal layer M1 and the second interconnect level may be a second metal layer M2.

[0017] The SOC apparatus may further include a second plurality of metal interconnects with a minimum pitch of m_2, where $m_2 > m$ and the LCM of g, m, and m_2 is less than $20g$. In one example, g is equal to or is approximately equal to 96nm, m is equal to or is approximately equal to 72nm, v is equal to or is approximately equal to 115nm, and m_2 is equal to or is approximately equal to 80nm. With pitches of g=96nm, m=72nm, and m_2=80nm, the LCM is 1440nm. The pitches g, m, m_2, and v are constrained by the equations $g^2 + m^2 \geq v^2$ and LCM(g,m,m_2)<20g. In one configuration, a via pitch v is assumed, and the gate interconnect pitch g, metal interconnect pitch m, and metal interconnect pitch m_2 are adjusted to satisfy the equations. The plurality of metal interconnects may be on a third interconnect level (e.g., metal layer M3) and the second plurality of metal interconnects may be on a

fifth interconnect level (e.g., metal layer M5) higher than the third interconnect level. The vias interconnect metal interconnects between the plurality of metal interconnects and the second plurality of metal interconnects. The third interconnect level may be a third metal layer M3 and the fifth interconnect level may be a fifth metal layer M5.

[0018] FIG. 5 is a flow chart 500 of a method of operating an SOC apparatus. At step 502, a current is flowed through a plurality of gate interconnects with a minimum pitch g. At step 504, a current is flowed through a plurality of metal interconnects with a minimum pitch m. At step 506, a current is flowed through a plurality of vias interconnecting the gate interconnects and the metal interconnects. The vias have a minimum pitch v. The pitches of the gate interconnects, metal interconnects, and vias satisfy $g^2 + m^2 \geq v^2$. In addition, an LCM of g and m is less than $20g$. The plurality of metal interconnects may be on at least one of a first interconnect level or a second interconnect level, and the vias may interconnect the metal interconnects between the first interconnect level and the second interconnect level. The first interconnect level may be a first metal layer and the second interconnect level may be a second metal layer. At step 508, a current is flowed through a second plurality of metal interconnects with a minimum pitch of m_2, where $m_2 > m$ and the LCM of g, m, and m_2 is less than $20g$. The plurality of metal interconnects may be on a third interconnect level and the second plurality of metal interconnects may be on a fifth interconnect level. The vias may interconnect metal interconnects between the plurality of metal interconnects and the second plurality of metal interconnects. The third interconnect level may be a third metal layer and the fifth interconnect level may be a fifth metal layer.

[0019] In one configuration, an SOC apparatus includes means for flowing a current through a plurality of gate interconnects with a minimum pitch g, means for flowing a current through a plurality of metal interconnects with a minimum pitch m, and means for flowing a current through a plurality of vias interconnecting the gate interconnects and the metal interconnects. The vias having a minimum pitch v, $g^2 + m^2 \geq v^2$, and an LCM of g and m is less than $20g$. The means for flowing a current through a plurality of gate interconnects is the plurality of gate interconnects, the means for flowing a current through a plurality of metal interconnects is the plurality of metal interconnects, and the means for flowing a current through a plurality of vias is the plurality of vias. The SOC apparatus may further include

means for flowing a current through a second plurality of metal interconnects with a minimum pitch of m_2, where $m_2 > m$ and the LCM of g, m, and m_2 is less than $20g$. The means for flowing a current through a second plurality of metal interconnects is the second plurality of metal interconnects.

[0020] As provided *supra*, given a requirement to obtain an x^2% area scaling, greater than x% pitch scaling may be used for some interconnects. The minimum pitch scaling may be determined based on minimum via pitch limits. Such a scaling may provide improved cost, power, and performance benefits over an x% pitch scaling for all interconnects.

[0021] It is understood that the specific order or hierarchy of steps in the processes disclosed is an illustration of exemplary approaches. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the processes may be rearranged. Further, some steps may be combined or omitted. The accompanying method claims present elements of the various steps in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

[0022] The previous description is provided to enable any person skilled in the art to practice the various aspects described herein. Various modifications to these aspects will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other aspects. Thus, the claims are not intended to be limited to the aspects shown herein, but is to be accorded the full scope consistent with the language claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless specifically so stated, but rather "one or more." The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any aspect described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other aspects." Unless specifically stated otherwise, the term "some" refers to one or more. Combinations such as "at least one of A, B, or C," "at least one of A, B, and C," and "A, B, C, or any combination thereof" include any combination of A, B, and/or C, and may include multiples of A, multiples of B, or multiples of C. Specifically, combinations such as "at least one of A, B, or C," "at least one of A, B, and C," and "A, B, C, or any combination thereof" may be A only, B only, C only, A and B, A and C, B and C, or A and B and C, where any such combinations may contain one or more member or members of A, B, or C. All structural and functional equivalents to the elements of the various aspects described throughout this disclosure that are known

or later come to be known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the claims. Moreover, nothing disclosed herein is intended to be dedicated to the public regardless of whether such disclosure is explicitly recited in the claims. No claim element is to be construed as a means plus function unless the element is expressly recited using the phrase "means for."

WHAT IS CLAIMED IS:

CLAIMS

1. A system on a chip (SOC) apparatus, comprising:

a plurality of gate interconnects with a minimum pitch g;

a plurality of metal interconnects with a minimum pitch m; and

a plurality of vias interconnecting the gate interconnects and the metal interconnects, the vias having a minimum pitch v,

wherein $g^2 + m^2 \geq v^2$ and a least common multiplier (LCM) of g and m is less than $20g$.

2. The apparatus of claim 1, wherein g is approximately 96nm, m is approximately 64nm, and v is approximately 115nm.

3. The apparatus of claim 1, wherein the plurality of metal interconnects are on at least one of a first interconnect level or a second interconnect level, and the vias interconnect the metal interconnects between the first interconnect level and the second interconnect level.

4. The apparatus of claim 3, wherein the first interconnect level is a first metal layer and the second interconnect level is a second metal layer.

5. The apparatus of claim 1, further comprising a second plurality of metal interconnects with a minimum pitch of m_2, wherein $m_2 > m$ and the LCM of g, m, and m_2 is less than $20g$.

6. The apparatus of claim 5, wherein g is approximately 96nm, m is approximately 72nm, v is approximately 115nm, and m_2 is approximately 80nm.

7. The apparatus of claim 5, wherein the plurality of metal interconnects are on a third interconnect level and the second plurality of metal interconnects are on a fifth interconnect level, wherein the vias interconnect metal interconnects between the plurality of metal interconnects and the second plurality of metal interconnects.

8. The apparatus of claim 7, wherein the third interconnect level is a third metal layer and the fifth interconnect level is a fifth metal layer.

9. A method of operating a system on a chip (SOC) apparatus, comprising:

flowing a current through a plurality of gate interconnects with a minimum pitch g;

flowing a current through a plurality of metal interconnects with a minimum pitch m; and

flowing a current through a plurality of vias interconnecting the gate interconnects and the metal interconnects, the vias having a minimum pitch v,

wherein $g^2 + m^2 \geq v^2$ and a least common multiplier (LCM) of g and m is less than $20g$.

10. The method of claim 9, wherein the plurality of metal interconnects are on at least one of a first interconnect level or a second interconnect level, and the vias interconnect the metal interconnects between the first interconnect level and the second interconnect level.

11. The method of claim 10, wherein the first interconnect level is a first metal layer and the second interconnect level is a second metal layer.

12. The method of claim 9, further comprising flowing a current through a second plurality of metal interconnects with a minimum pitch of m_2, wherein $m_2 > m$ and the LCM of g, m, and m_2 is less than $20g$.

13. The method of claim 12, wherein the plurality of metal interconnects are on a third interconnect level and the second plurality of metal interconnects are on a fifth interconnect level, wherein the vias interconnect metal interconnects between the plurality of metal interconnects and the second plurality of metal interconnects.

14. The method of claim 13, wherein the third interconnect level is a third metal layer and the fifth interconnect level is a fifth metal layer.

15. A system on a chip (SOC) apparatus, comprising:

means for flowing a current through a plurality of gate interconnects with a minimum pitch g;

means for flowing a current through a plurality of metal interconnects with a minimum pitch m; and

means for flowing a current through a plurality of vias interconnecting the gate interconnects and the metal interconnects, the vias having a minimum pitch v,

wherein $g^2 + m^2 \geq v^2$ and a least common multiplier (LCM) of g and m is less than $20g$.

16. The apparatus of claim 15, wherein the plurality of metal interconnects are on at least one of a first interconnect level or a second interconnect level, and the vias interconnect the metal interconnects between the first interconnect level and the second interconnect level.

17. The apparatus of claim 16, wherein the first interconnect level is a first metal layer and the second interconnect level is a second metal layer.

18. The apparatus of claim 15, further comprising means for flowing a current through a second plurality of metal interconnects with a minimum pitch of m_2, wherein $m_2 > m$ and the LCM of g, m, and m_2 is less than $20g$.

19. The apparatus of claim 18, wherein the plurality of metal interconnects are on a third interconnect level and the second plurality of metal interconnects are on a fifth interconnect level, wherein the vias interconnect metal interconnects between the plurality of metal interconnects and the second plurality of metal interconnects.

20. The apparatus of claim 19, wherein the third interconnect level is a third metal layer and the fifth interconnect level is a fifth metal layer.

FIG. 1

100

	28nm	20/16/14nm
Gate	g_1 (e.g., 130nm)	g_2 (e.g., 90nm (70%))
M1	$m1_1$ (e.g., 90nm)	$m1_2$ (e.g., 64nm (70%))
Ma	ma_1 (e.g., 90nm)	ma_2 (e.g., 64nm (70%))
Mb		mb (e.g., 80nm)
Via	v1 (e.g., 130nm)	v2 (e.g., 115nm (88%))

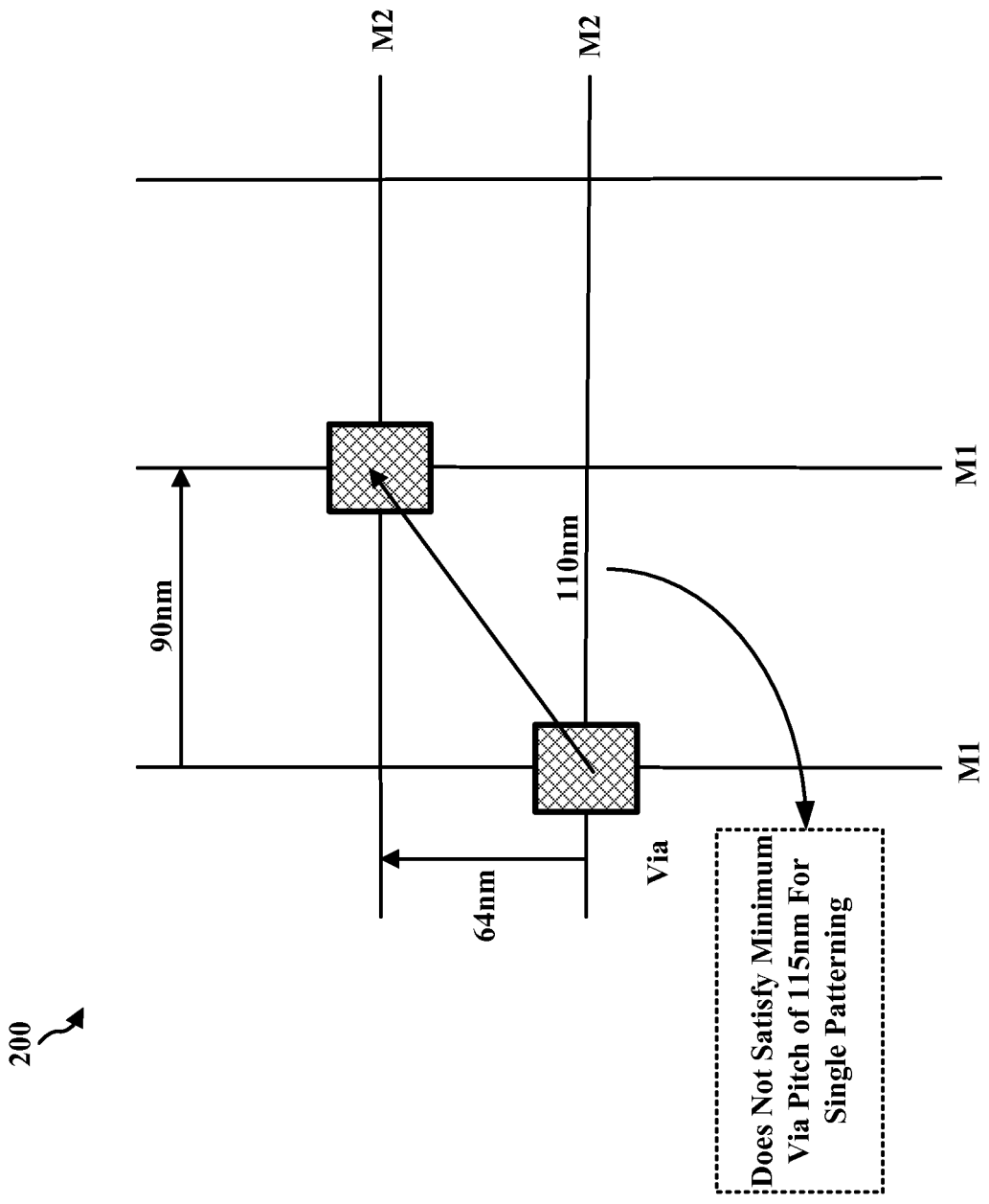
200
M2
M2
M1
M1
90nm
110nm
64nm
Via
Does Not Satisfy Minimum Via Pitch of 115nm For Single Patterning

FIG. 2

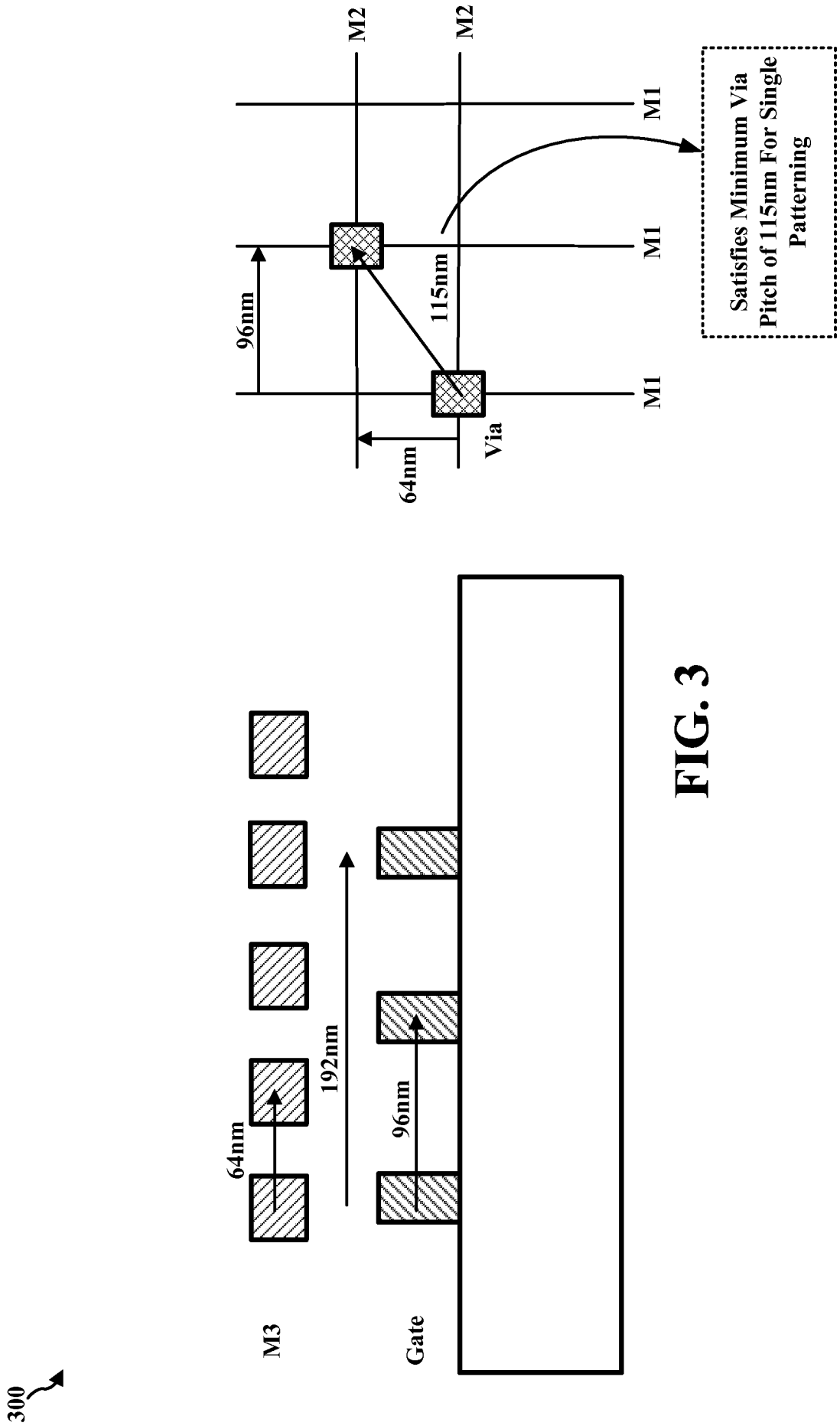
300
M3
Gate
64nm
192nm
96nm
M2
M2
M1
M1
M1
96nm
115nm
64nm
Via
Satisfies Minimum Via Pitch of 115nm For Single Patterning

FIG. 3

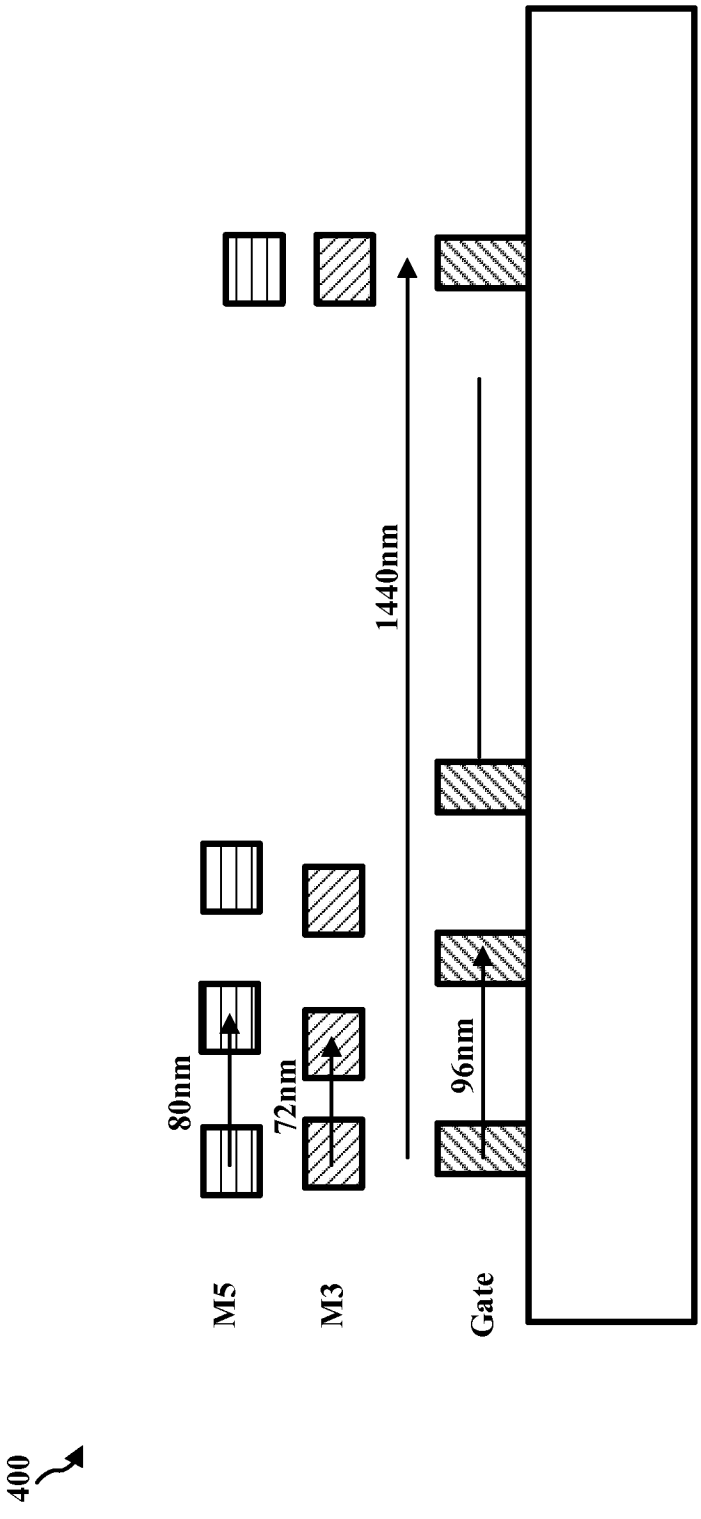

FIG. 4

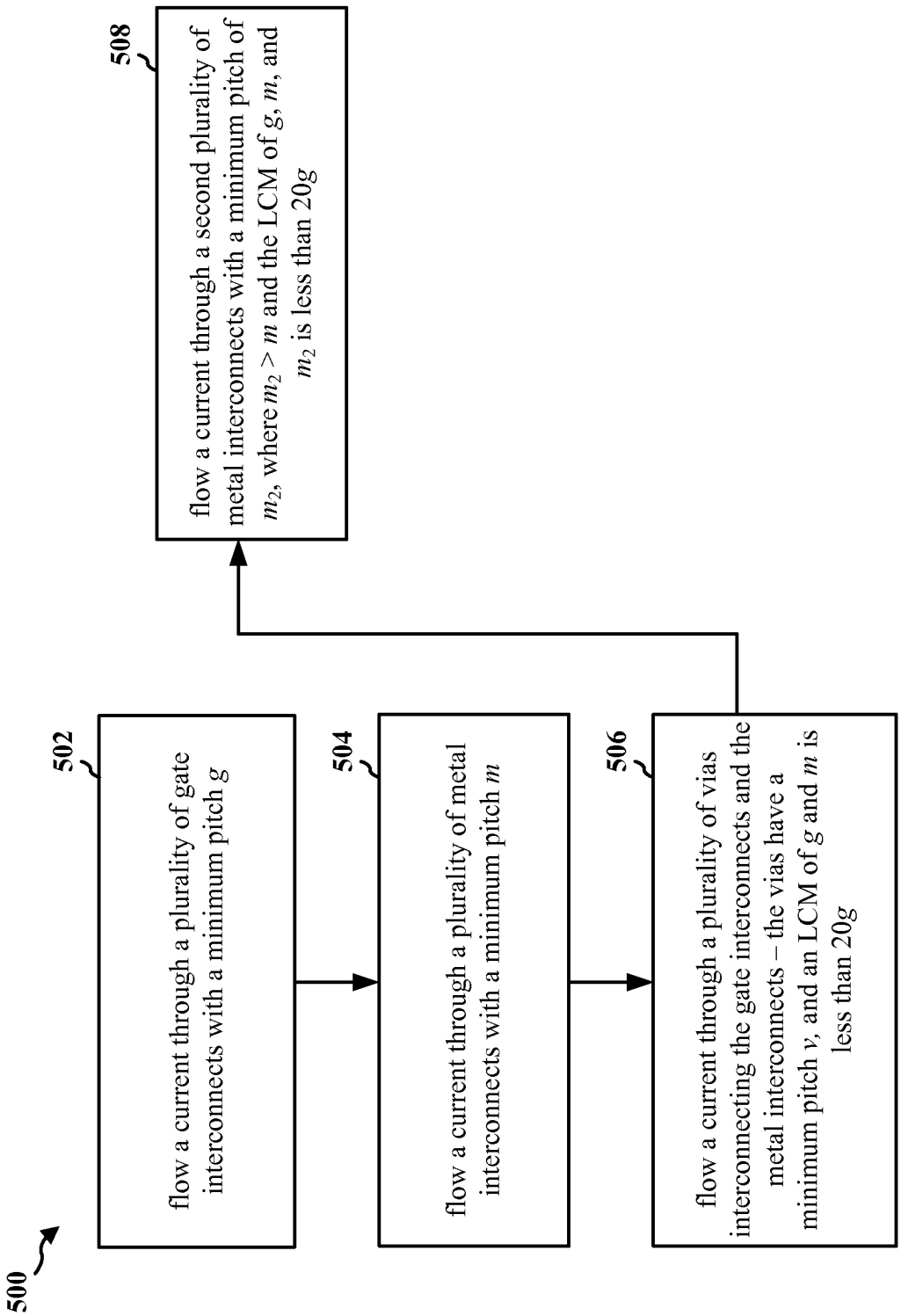
500
502
flow a current through a plurality of gate interconnects with a minimum pitch g
504
flow a current through a plurality of metal interconnects with a minimum pitch m
506
flow a current through a plurality of vias interconnecting the gate interconnects and the metal interconnects – the vias have a minimum pitch v, and an LCM of g and m is less than 20g
508
flow a current through a second plurality of metal interconnects with a minimum pitch of m_2, where $m_2 > m$ and the LCM of g, m, and m_2 is less than 20g

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/047834

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/02 H01L21/768 H01L23/498 H01L23/522
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013/072020 A1 (BLATCHFORD JAMES WALTER [US]) 21 March 2013 (2013-03-21) abstract; claims; figures 1-6 paragraph [0024]; table 1	1-20
Y	US 2006/289861 A1 (CORREALE ANTHONY JR [US] CORREALE JR ANTHONY [US]) 28 December 2006 (2006-12-28) abstract; claims; figures 2,5 paragraphs [0006], [0039] - [0060]	1-20
A	US 2010/006951 A1 (BECKER SCOTT T [US] ET AL) 14 January 2010 (2010-01-14) abstract; claims; figures	1-20
A	US 5 471 093 A (CHEUNG ROBIN W [US]) 28 November 1995 (1995-11-28) abstract; claims; figures	1-20

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
5 November 2014	12/11/2014

Name and mailing address of the ISA/	Authorized officer
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004/068710 A1 (MIYAKAWA YASUHIRO [JP]) 8 April 2004 (2004-04-08) abstract; claims; figures -----	1-20
A	US 2008/061441 A1 (LIU CHUNG-SHI [TW]) 13 March 2008 (2008-03-13) abstract; claims; figures -----	1-20

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/US2014/047834

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013072020 A1	21-03-2013	NONE	
US 2006289861 A1	28-12-2006	US 2006289861 A1	28-12-2006
		US 2007264758 A1	15-11-2007
		US 2009114952 A1	07-05-2009
US 2010006951 A1	14-01-2010	NONE	
US 5471093 A	28-11-1995	TW 259909 B	11-10-1995
		US 5471093 A	28-11-1995
US 2004068710 A1	08-04-2004	NONE	
US 2008061441 A1	13-03-2008	CN 101140921 A	12-03-2008
		US 2008061441 A1	13-03-2008