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(71) Applicant *(for all designated States except US)*: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **HERAGU, Keerthinarayan, P.** [US/US]; 3560 Alma Road #1021, Richardson, TX 75080 (US). **PK, Nisha** [IN/IN]; Flat No D201, Rohan Vasantha Apartments, Varthur Main Road, Marthahalli, Bangalore PIN 560037 (IN).

(74) Agents: **STEWART, Alan, K.** et al.; Texas Instruments Incorporated, Deputy General Patent Counsel, P.O. Box 655474, MS 3999, Dallas, TX 75265-5474 (US).

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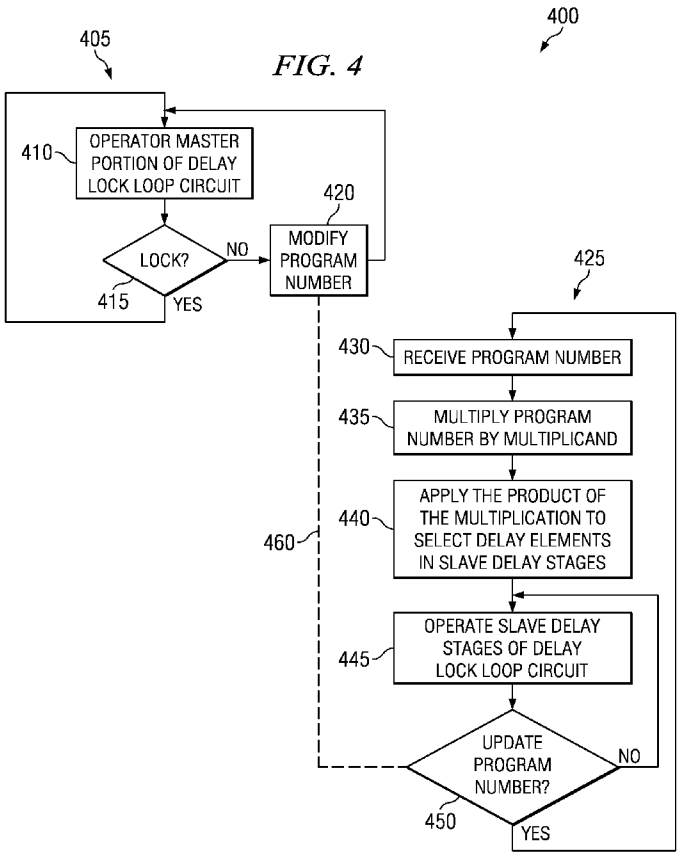


FIG. 4

(57) **Abstract:** Various systems and methods (400) for signal synchronization are disclosed. For example, some embodiments of the invention provide methods for reduced area delay signal timing. Such methods include providing a delay lock loop circuit with a plurality of selectable delay elements. The methods further include operating the delay lock loop circuit in a first mode (410) where a program number is established in relation to a reference frequency. The program number corresponds to a number of the plurality of selectable delay elements used to establish a first delay time at the reference frequency. The program number is multiplied by a multiplicand (435), and the product of the multiplication is used while operating the delay lock loop circuit in a second mode (445) to select the number of delay elements utilized in delaying an input signal. In the second mode, an input signal is delayed by a second delay time that is approximately the first delay time multiplied by the multiplicand.

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SYSTEMS AND METHODS FOR REDUCED AREA DELAY LOCKED LOOP

The invention is related to event synchronization, and more particularly to systems and methods for synchronizing one signal to another signal in a semiconductor device.

BACKGROUND

Synchronizing one electrical signal to another often involves applying the signal to a data input of a flip-flop, and clocking the flip-flop using a clock to which the signal is to be synchronized. The signal to be synchronized generally must be applied to the data input of the flip-flop for a defined period before the clock transitions (i.e., setup time), and must remain for a defined period after the clock transitions (i.e., hold time). By assuring that the setup and hold times are met, predictable circuit operation is achieved.

In some cases, a delay lock loop circuit has been used to delay a signal in relation to a synchronizing clock to assure that setup and hold times are met. Such delay lock loops may be iteratively updated until a desired delay is achieved. Implementation of such a delay lock loop typically requires substantial circuitry and a corresponding amount of chip area. This leads to increased chip costs and in some cases reduced yield.

Thus, for at least the aforementioned reasons, there exists a need in the art for advanced systems and devices for implementing a signal delay.

SUMMARY

The invention is related to event synchronization, and more particularly to systems and methods for synchronizing one signal to another signal in a semiconductor device.

Various embodiments of the invention provide methods for reduced area delay signal timing. Such methods include providing a delay lock loop circuit with a plurality of selectable delay elements. The methods further include operating the delay lock loop circuit in a first mode where a program number is established in relation to a reference frequency. The program number corresponds to a number of the plurality of selectable delay elements used to establish a first delay time at the reference frequency. The program number is multiplied by a multiplicand, and the product of the multiplication is used while operating the delay lock loop circuit in a second mode to select the number of delay elements utilized in delaying an input signal. In the second mode, an input signal is delayed by a second delay time that is approximately the first delay time multiplied by the multiplicand. In some instances of the aforementioned embodiments, the multiplicand is a power of two, and the

multiplication process is accomplished by shifting the program number to the right or to the left. In one particular instance of the aforementioned embodiments, the multiplicand is the integer 2, and multiplying the program number by the multiplicand includes shifting the program number to the left by one bit. In another particular instance of the aforementioned embodiments, shifting the program number is accomplished by aligning the program number with delay elements such that an effective shift is incurred. In yet another particular instance of the aforementioned embodiments, multiplication includes applying the multiplicand and the program number to a multiplier circuit. As yet a further instance of the aforementioned embodiments, multiplication includes replicating delay element enable signals.

In various instances of the aforementioned embodiments, the first mode is a master mode and the second mode is a slave mode. In some instances of the aforementioned embodiments, the delay lock loop circuit may be implemented in relation to a DDR memory. In such instances, the reference frequency may be obtained by using a 2x clock implemented as part of the DDR memory interface. In some instances of the aforementioned embodiments, the delay lock loop circuit is operable to provide a particular delay using a reduced area when compared with a non-multiplying delay lock loop circuit.

In one or more instance of the aforementioned embodiments, the plurality of selectable delay elements is a first plurality of selectable delay elements incorporated in a first delay stage. In such instances, the delay lock loop circuit may further include a second plurality of selectable delay elements incorporated in a second delay stage. In master mode, a reference clock operating at the reference frequency is applied to the first delay stage and an output of the first delay stage is applied to the second delay stage. In some such cases, the output signal is a first output signal, and operating the delay lock loop circuit in the second mode may include applying the first input signal to the first delay stage programmed with the program number multiplied by the multiplicand such that the first delay stage provides a first delay output. The methods may further include applying a second input signal to the second delay stage programmed with the program number multiplied by the multiplicand, wherein the second delay stage provides a second delay output.

Other embodiments of the invention provide delay lock loop circuits that include at least a first delay stage and a second delay stage. In addition, the delay lock loop circuits include a register, a feedback loop, and a multiplication circuit. The first delay stage includes

a first plurality of selectable delay elements, and is operable to receive an input clock and to provide a stage clock that is a delayed derivative of the input clock. The second delay stage includes a second plurality of selectable delay elements, and is operable to receive an input signal. The register maintains a program number that determines a number of the plurality of selectable delay elements used in the delay stage. The feedback loop that is operable to establish the program number corresponding to a desired delay time, and the multiplication circuit multiplies the program number by a multiplicand. A selected number of the second plurality of selectable delay elements are used to delay the input signal to derive an output signal, and wherein the output signal is delayed the desired delay time multiplied by the multiplicand.

Yet other embodiments of the invention provide methods for signal synchronization. Such methods include providing at least a first delay stage and a second delay stage. The first delay stage includes a first selectable plurality of delay elements, and the second delay stage includes a second plurality of delay elements. The methods further include applying a reference clock to the first delay stage such that an output of the first delay stage is a first derivative of the reference clock, and applying the first derivative of the reference clock to the second delay stage such that an output of the second delay stage is a second derivative of the reference clock. The second derivative of the reference clock is a phase shift delayed from the reference clock. The methods further include, repeatedly selecting a number of the first plurality of delay stages and the second plurality of delay stages until the phase shift is at a desirable amount; multiplying the number of the first plurality of delay elements and the second plurality of delay elements by a multiplicand; and applying the product of the multiplication to a slave stage such that the product of the multiplication determines a number of utilized delay elements in the slave stage. In some instances of the aforementioned embodiments, the delay lock loop circuit operates in a master mode and a slave mode. In such cases, a portion of circuitry may be reused in both the first delay stage and the slave stage depending upon whether the delay lock loop circuit is operating in the master mode or the slave mode. In one or more instances of the aforementioned embodiments, the delay lock loop circuit is implemented in relation to a DDR memory interface that includes a 2x clock and a 1x clock. In such cases, the DDR memory interface includes a 1x clock and a 2x clock. The reference clock is the 2x clock, and the 1x clock is applied to the slave stage.

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This summary provides only a general outline of some embodiments according to the invention. Many other objects, features, advantages and other embodiments will become apparent from the following description and accompanying drawings, wherein:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1a shows a memory system that utilizes a combination memory controller and delay lock loop circuit in accordance with one or more embodiments of the invention;

FIG. 1b depicts a strobe signal delayed in relation to a data signal;

FIGS. 2a-2e show a delay lock loop circuit locking to a 2x reference signal in accordance with some embodiments of the invention;

FIG. 3 depicts a slave delay stage along with an interface circuit that may be implemented in relation to various embodiments of the invention; and

FIG. 4 is a flow diagram showing a method in accordance with embodiments of the invention for signal synchronization.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Turning to FIG. 1a, a memory system 100 is shown that utilizes a combination memory controller 110 and a delay lock loop circuit 120 in accordance with one or more embodiments of the invention. It should be noted that delay lock loop circuit 120 may be implemented on the same semiconductor die as memory controller 110, or may be implemented on a different die. Further, it should be noted that delay lock loop circuit 120 may be integrated with memory controller 110 or may be implemented as separate modules of the same circuit design. As shown, memory controller 110 includes a number of signals that are generated to allow access to one or more memory modules. Generation of such signals may be accomplished in various ways as are known in the art. For example, the same strobe signal may be used for both read and write signals, or a strobe signal for the read and a strobe signal for the write may be created internal to memory controller 110 and only at the interface of memory controller 110 are the two signals combined to drive the strobe I/O of the external memory. Delay lock loop circuit 120 includes a master portion consisting of one or more delay stages 142, 144, 146, 148, 150; and a feedback loop consisting of a phase comparator circuit 152 and a delay control circuit. Delay lock loop circuit 120 also includes a slave portion consisting of one or more slave delay stages 162, 164.

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As shown, memory system 100 includes a bank 130 of double data rate memory blocks 134, 138. It should be noted that other memory types may be used in accordance with different embodiments of the invention. Each of memory blocks 134, 138 includes an interface consisting of an address bus, a data bus, a strobe and a read/write control line. In operation, when data is to be written to memory block 134, the appropriate address is applied to the address bus, the read/write control line is asserted to indicate a write operation, data is placed on the data bus, and the strobe signal for memory block 134 (i.e., strobe 0) is asserted. The same process is done to write data to memory block 138, except that the strobe signal for memory block 138 (i.e., strobe 1) is asserted. In contrast, when data is to be read from memory block 134, the appropriate address is applied to the address bus, the read/write control line is asserted to indicate a read operation. Memory block 134 then asserts the strobe associated memory block 134 (i.e., strobe 0) coincident with applying data to the data bus. The same process is used for reading data from memory block 138, except that the strobe associated with memory block 138 is asserted. Both a 1x reference clock 123 (i.e., a clock that is capable of operating at approximately the frequency as either strobe 0 or strobe 1) and a 2x reference clock 122 (i.e., a clock that is capable of operating at least two times as fast as either strobe 0 or strobe 1) is associated with memory blocks 134, 138. Based on the disclosure provided herein, one of ordinary skill in the art will recognize a variety of interfaces or signal sets that may be used in accordance with different embodiments of the invention.

In some cases, the strobe and the data are not properly aligned during the read and write cycles. In such cases, delay lock loop circuit 120 may be used to delay one or more strobe signals to create the appropriate alignment. As shown, a slave delay stage 162 is used to delay the strobe associated with memory block 134, and a slave delay stage 164 is used to delay the strobe associated with memory block 138. It should be noted that depending upon the configuration, slave delay stage 162 may be designed to delay a strobe received from memory block 134 by a particular amount, or slave delay stage 162 may be designed to delay a strobe provided to memory block 134 from memory controller 110. Similarly, depending upon the configuration, slave delay stage 164 may be designed to delay a strobe received from memory block 138 by a particular amount, or slave delay stage 164 may be designed to delay a strobe provided to memory block 138 from memory controller 110. The amount of

delay applied by slave delay stage 162 and slave delay stage 164 is controlled by delay lock loop circuit 120. It should be noted that delay lock loop circuit 120 may be implemented in relation to a circuit other than a memory controller. Based on the disclosure provided herein, one of ordinary skill in the art will recognize a variety of applications that may benefit from use of such a delay lock loop circuit.

The aforementioned process of delaying strobes using slave delay stages 162, 164 is graphically displayed in FIG. 1b. Turning to FIG. 1b, a timing diagram 190 shows data 192 applied to the aforementioned data bus and a corresponding strobe in 194. As shown, strobe in 194 transitions coincident with the change in data 192. In some cases such an immediate transition results in a setup or hold problem in either memory blocks 134, 138 or a device receiving data from memory blocks 134, 138. By introducing a controlled time delay 198 to strobe in 194, any setup or hold problems may be averted. As more fully discussed below, time delay 198 is programmable by selecting a different number of delay elements implemented as part of slave delay stages 162, 164.

The number of delay elements utilized in slave delay stages 162, 164 is determined through delay locking to 2x reference clock 122 using delay lock loop circuit 120. Delay lock loop circuit 120 includes delay stage 142, delay stage 144, delay stage 146, delay stage 148 and delay stage 150. In some instances, all of delay stages 142, 144, 146, 148, 150 are substantially identical including the same number of delay elements. As shown, 2x reference clock 122 and 1x reference clock 123 are applied as inputs to a multiplexer 127. Depending upon the assertion level of a select signal 121, one of 2x reference clock 122 or 1x reference clock 123 is applied as an input to delay stage 142. The output of delay stage 142 is the input of delay stage 144, the output of delay stage 144 is the input of delay stage 146, the output of delay stage 146 is the input of delay stage 148, and the output of delay stage 148 is the input of delay stage 150.

By providing an ability to select between 2x reference clock 122 and 1x reference clock 123 using multiplexer 127, a wide operational range with a desired resolution may be achieved. In particular, when high frequency operation is desired, 1x reference clock 123 is selected. When low frequency operation is desired, 2x reference clock 122 is selected. When high frequency operation is selected using select signal 121, a multiplier circuit 102 is bypassed. In contrast, when low frequency operation is selected using select signal 121,

multiplier circuit 102 is used to modify the number of delay elements utilized by slave delay stages 162, 164. The use of multiplier circuit 102 decreases the resolution offered, but this is not as important during low frequency operation. Allowing for both high frequency and low frequency operation reduces the number of delay elements required to meet a three-hundred, sixty degree locking capability.

The output of delay stage 150 (or in some cases, an output of one of the other delay stages 142, 144, 146, 148) is compared with the output of multiplexer 127 by a phase comparator 152. The output of phase comparator 152 indicates whether the number of delay elements currently utilized in each of delay stages 142, 144, 146, 148, 150 is to be incremented, decremented or left constant in order to achieve the desired delay lock. In particular, phase comparator 152 provides an increment/decrement signal 153 to a delay control circuit 154. Based on increment/decrement signal 153, delay control circuit 154 controls the number of delay elements used by each of delay stages 142, 144, 146, 148, 150. The number of delay elements used by each of delay stages 142, 144, 146, 148, 150 is multiplied by a multiplier circuit 102. The product of multiplier circuit 102 is used to select the number of delay elements utilized in each of delay stages 162, 164.

As an example, the delay elements utilized in each of delay stages 142, 144, 146, 148, 150 each provide approximately the same incremental delay (i.e., resolution) as the delay elements used in slave delay stages 162, 164. Thus, where delay lock loop 120 is synchronized to a clock (i.e., 2x Reference Clock 122) that operates at approximately twice the frequency of the signals (i.e., strobe 0 and strobe 1) delayed by slave delay stages 162, 164, then the number of delay elements used by each of delay stages 142, 144, 146, 148, 150 may be approximately half the number of delay elements used by slave delay stages 162, 164 to produce a corresponding delay. In this case, multiplier circuit 102 may be set to apply a two times (i.e., the multiplicand is two) multiplication. In such a case, multiplier circuit 102 may be implemented as any multiplier circuit known in the art that is capable of multiplying an input by two and providing a product of the multiplication to select the number of delay elements used in slave delay stages 162, 164. In one particular case, multiplier circuit 102 may be a shift register that is operable to shift the number of delay elements used by delay stages 142, 144, 146, 148, 150 left by one bit position. As another particular case, multiplier circuit 102 may be a register that is aligned with the number of delay elements used by delay

stages 142, 144, 146, 148, 150 such that the number is shifted to the left by one bit position. Based on the disclosure provided herein, one of ordinary skill in the art will recognize a number of multiplier circuits 102 that may be used in relation to one or more embodiments of the invention. As one advantage, by locking delay lock loop circuit 120 to a 2x frequency signal, delay stages 142, 144, 146, 148, 150 may be implemented with half of the delay elements as would otherwise be needed to produce a delay number to be used by slave delay stages 162, 164.

As another example where the delay elements utilized in each of delay stages 142, 144, 146, 148, 150 each provide approximately the same incremental delay as the delay elements used in slave delay stages 162, 164, delay lock loop 120 may be synchronized to a clock that operates at approximately four times the frequency of the signals delayed by slave delay stages 162, 164. In such a case, the number of delay elements used by each of delay stages 142, 144, 146, 148, 150 may be approximately one quarter the number of delay elements used by slave delay stages 162, 164 to produce a corresponding delay. In this case, multiplier circuit 102 may be set to apply a four times (i.e., a multiplicand of four) multiplication. In such a case, multiplier circuit 102 may be implemented as any multiplier circuit known in the art that is capable of multiplying an input by four and providing a product of the multiplication to select the number of delay elements used in slave delay stages 162, 164. In one particular case, multiplier circuit 102 may be a shift register that is operable to shift the number of delay elements used by delay stages 142, 144, 146, 148, 150 left by two bit positions. As another particular case, multiplier circuit may be a register that is aligned with the number of delay elements used by delay stages 142, 144, 146, 148, 150 such that the number is shifted to the left by two bit positions. Again, based on the disclosure provided herein, one of ordinary skill in the art will recognize a number of multiplier circuits 102 that may be used in relation to one or more embodiments of the invention. As one advantage, by locking delay lock loop circuit 120 to a 4x frequency signal delay stages 142, 144, 146, 148, 150 may be implemented with one quarter of the delay elements as would otherwise be needed to produce a delay number to be used by slave delay stages 162, 164.

While examples of multiplying the number of delay elements utilized by delay stages 142, 144, 146, 148, 150 by two and by four, it should be noted that based on the disclosure provided herein, one of ordinary skill in the art will recognize a number of different

multiplicands that may be used in accordance with different embodiments of the invention. Such multiplicands may be, but are not required to be, powers of two (2^n). Such powers of two may include, but are not limited to, ¼, 1/2, 2, 4 and 8. Any of such powers of two may be achieved by shifting an input value to the right or left. Again, it should be noted that the multiplicand may be any value where multiplier circuit 102 is designed as a traditional multiplier circuit rather than a simple shift register.

Turning to FIGS. 2a-2e, a delay lock loop circuit 200 locking to a 2x reference signal 201 in accordance with some embodiments of the invention is shown. Delay lock loop circuit 200 may be used in place of the master portion of delay lock loop circuit 120 where the 2x reference clock has been selected using multiplexer 127. It should be noted that delay lock loop circuit 200 includes circuitry for reducing glitches that may or may not be included in relation to different embodiments of the invention. Delay lock loop circuit 200 includes a set of delay stages 242, 244, 246, 248, 250. Further, delay lock loop circuit 200 includes a feedback loop that includes a phase comparator 210, an enable generator 220, and a unified selector register 230. Delay lock loop circuit 200 also includes a reference signal gate 202, and a phase selector multiplexer 252. In one particular embodiment of the invention, each of the aforementioned delay stages is designed to implement a phase delay of about seventy-two degrees. In such cases, phase selector multiplexer 252 provides an ability to select between a one stage seventy-two degree phase shift or a one stage ninety degree phase shift depending upon whether a selector input 253 is set such that phase selector multiplexer 252 causes stage output 249 or stage output 251 to drive a multiplexer output 254. Based on the disclosure provided herein, one of ordinary skill in the art will recognize a variety of embodiments that do not employ a multiplexer 252, or that employ additional multiplexers to allow for selection of different stage outputs.

Reference signal gate 202 receives 2x reference signal 201 and provides a gated reference signal 203. One particular embodiment of the invention includes an AND gate that ANDs an inverted version of gate control output 222 with 2x reference signal 201. In some cases, circuitry is included that controls the timing of gate control output such that producing gated reference signal 203 from 2x reference signal 201 does not result in glitches on gated reference signal 203. Delay stage 242 receives gated reference signal 203, and provides a stage output 243. Stage output 243 is gated reference signal 203 delayed by a determined

amount. Delay stage 244 receives stage output 243, and provides a stage output 245. Stage output 245 is stage output 243 delayed by a determined amount. Delay stage 246 receives stage output 245, and provides a stage output 247. Stage output 247 is stage output 245 delayed by a determined amount. Delay stage 248 receives stage output 247, and provides a stage output 249. Stage output 249 is stage output 247 delayed by a determined amount. Delay stage 250 receives stage output 249, and provides a stage output 251. Stage output 251 is stage output 249 delayed by a determined amount. Each of delay stages 242, 244, 246, 248, 250 includes a number of delay elements that may be selectably incorporated in a delay chain.

Gated reference signal 203, stage output 245, and one of stage output 249 or stage output 251 are provided to an up/down generator 216 of phase comparator 210. Up/down generator 216 provides an output to an increment generator 214 that indicates whether a number of delay elements used in each of delay stages 242, 244, 246, 248, 250 should be incremented, decremented or maintained constant to achieve the desired phase shift. Increment generator 214 provides an output to a lock generator 212 that provides a lock output 213.

In addition, increment generator 214 provides an increment/decrement signal 215 to an enable generator 220. Enable generator 220 controls the modification of a unified selector register 230 via a set of control signals 221. In one particular embodiment of the invention, control signals 221 include an enable signal and an increment/decrement signal. In such a case when the increment/decrement signal indicates an increment and the enable signal is asserted, the value maintained in unified selector register 230 is incremented. Alternatively, when the increment/decrement signal indicates a decrement and the enable signal is asserted, the value maintained in unified selector register 230 is decremented. In such an embodiment, a lock condition may be indicated (i.e., lock output 213 is asserted) when the value in selector register is to be maintained constant. In such cases, the enable signal is not asserted when the lock condition is indicated.

In some embodiments of the invention, enable generator 220 includes a counter circuit that is synchronized to 2x reference signal 201. The counter circuit periodically asserts an enable signal (part of control signals 221). In one particular embodiment of the invention, the counter circuit asserts the enable signal once for every four cycles of 2x reference signal

201 when the lock condition has not been established. In such a case, a gate control output 222 derived from the counter may be provided to reference signal gate 202 such that gated reference signal 203 does not assert when the enable of control signals 221 is asserted. In this way, glitches are avoided when the value in unified selector register 230 is updated.

An X-bit selector value 232 maintained in unified selector register 230 is provided to each of delay stages 242, 244, 246, 248, 250. In operation, X-bit selector value 232 selects the number of the delay elements in each of delay stages 242, 244, 246, 248, 250 that are used in a delay chain implemented by the respective delay stage. In one particular embodiment of the invention, X-bit selector register is sixty-three bits wide, and the number of selectable delay elements in each of delay stages 242, 244, 246, 248, 250 is also sixty-three. It should be noted that the aforementioned delay width and register width is related to a particular implementation. It should also be noted that in contrast to the preceding example, the width of unified selector register 230 need not necessarily match the number of delay elements implemented in each of delay stages 242, 244, 246, 248, 250. Further, it should be noted that each of delay stages 242, 244, 246, 248, 250 do not necessarily need to include the same number of delay elements. Based on the disclosure provided herein, one of ordinary skill in the art will recognize a number of different delay widths and register widths that may be used in accordance with different embodiments of the invention.

X-bit value 232 multiplied by a multiplicand using a multiplier circuit 285 may be used to select a number of delay elements of one or more slave delay stages (not shown). In such cases, X-bit value 232 may be stored in a register 290. An output 293 of register 290 is combined with a fixed least significant bit 283 from an LSB circuit 280. Combining output 293 with fixed least significant bit 283 in this way causes results in a program number output 292 that is the X-bit value 232 multiplied by two. Again, it should be noted that multiplier circuit 285 may be any multiplier circuit known in the art, and may be designed to multiply X-bit value 232 by any number depending upon the particular design in which it is implemented.

Operation of delay lock loop circuit 200 is described in relation to a timing diagram 295 of FIG. 2b. Turning to FIG. 2b, 2x reference signal 201 is shown as a repeating clock with approximately a fifty percent duty cycle. As shown, enable generator 220 asserts gate control output 222 once every four cycles of 2x reference signal 201. Reference signal gate

202 gates 2x reference signal 201 with gate control output 222 to produce gated reference signal 203. In this example, gate control output 222 and the enable that is part of signals 221 have the same characteristics. In particular, gated reference signal 203 is 2x reference signal 201 that is not asserted whenever gate control output 222 is asserted.

Whenever the value in unified selector register 230 is to be incremented, increment generator 214 asserts increment/decrement signal 215 to indicate an increment operation (e.g., a logic '1' in this example). Alternatively, whenever the value in unified selector register 230 is to be decremented, increment generator 214 asserts increment/decrement signal 215 to indicate a decrement operation (e.g., a logic '0' in this example). Increment/decrement signal 215 is re-clocked by enable generator 220 as increment signal (part of signals 221). Signals 221 are passed by enable generator 220 to unified selector register 230 where they cause either an increment or decrement of X-bit value 232 upon the next positive edge of 2x reference signal 201. As previously stated, X-bit value 232 causes a change in the number of delay elements utilized in delay stages 242, 244, 246, 248, 250 (i.e., a change in the delay incurred through each of the respective delay stages).

Turning to FIG. 2c, a detailed schematic of one implementation of a delay stage 260 and a selector register 231 is shown. Delay stage 260 may be used in place of any or all of delay stages 242, 244, 246, 248, 250 discussed above in relation to FIG. 2a or delay stages 142, 144, 146, 148, 150 discussed above in relation to FIG. 1a. Similarly, selector register 231 may be used in place of selector register 232 discussed above in relation to FIG. 2a. As shown, delay stage 260 includes a number of delay elements 261 that can be configured as a chain of delay elements including one delay element up to the total number of delay elements depending upon the value maintained in selector register 231. Delay stage 260 receives an input signal 264 and provides an output signal 265. As an example, where delay stage 260 is used in place of delay stage 242, input signal 264 corresponds to gated reference signal 203 and output signal 265 corresponds to stage output 243. Similarly, inputs from selector register 231 correspond to X-bit value 232.

Each delay element 261 includes a delay buffer 263 that may be, but is not limited to an inverting buffer, a logic gate, or a non-inverting buffer. Based on the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuits that may be used to cause a signal delay. In addition, each delay element 261 includes a multiplexer 262 that is

controlled by an input from selector register 231 and is used to control whether the particular delay element is included in an overall delay chain implemented by delay stage 260. In particular, when the value provided from selector register 231 is a logic '1', the particular delay element is not selected. In contrast, when the value provided from selector register 231 is a logic '0', the particular delay element is selected. As each delay element 261 drives a subsequent delay element 261 (i.e., the output of delay element 261d, drives the output of delay element 261c), the value provided from selector register 231 includes a series of logic '1's followed by a series of logic '0's, with the transition between logic '0's and logic '1's being positioned such that it corresponds to the overall delay line length implemented in delay stage 260.

Selector register 231 is implemented as a shift register that causes a series of logic '1's followed by a series of logic '0's to shift right whenever the delay implemented by delay stage 261 is to be increased, and to shift left whenever the delay implemented by delay stage 261 is to be decreased. In particular, selector register 231 includes a number of flip-flops 233 configured in series. Each of flip-flops 233 includes a shift enable input 236, a scan input 237, a data input 238 and an output 239. In operation, when a shift right is to occur, an increment signal input (e.g., part of signals 221) is asserted high, and upon the next assertion of a clock input (e.g., 2x reference signal 201) the block of logic '1's followed by the block of logic '0's shifts right. In contrast, when a shift left is to occur, the increment signal input (e.g., part of signals 221) is asserted low, and upon the next assertion of a clock input (e.g., 2x reference signal 201) the block of logic '1's followed by the block of logic '0's shifts left. In some cases, an additional enable signal may be added to each of flip-flops 233 that enables both right and left shifting. Based on the disclosure provided herein, one of ordinary skill in the art will recognize other designs for implementing selector register 231. The outputs of flip-flops 233 are collectively referred to as delay element enable signals.

It should be noted that where X-bit value 232 is derived from selector register 231, multiplier circuit 285 may be designed such that it doubles (i.e., replicates each bit one time) each of the logic '1's and logic '0's of X-bit value 232 to achieve the desired multiplication by two. Alternative, X-bit value 232 may be encoded to provide a binary representation of the number of logic '1's that are included, and the binary value may be left shifted or otherwise multiplied as discussed above. Again, based on the disclosure provided herein, one

of ordinary skill in the art will recognize a variety of multiplier circuits that may be used in relation to different embodiments of the invention.

Turning to FIG. 2d, an exemplary up/down and increment generator circuit 270 that may be used in relation to one or more embodiments of the invention is depicted. Up/down and increment generator circuit 270 may be used in place of up/down generator 216 and increment generator 214 discussed above in relation to FIG. 2a. Up/down and increment generator circuit 270 includes a number of flip-flops 271 that are each clocked using different outputs and inputs from delay stages 242, 244, 246, 248, 250. In particular, a flip-flop 271a is clocked by stage output 245, a flip-flop 271b is clocked by multiplexer output 254 that is either stage output 249 or stage output 251, and a flip-flop 271c is clocked by gated reference signal 203. A flip-flop 271d is clocked by the output of flip-flop 271c. The data input of both flip-flop 271b and flip-flop 271c are connected to the output of flip-flop 271a. The output of flip-flop 271b (i.e., a down signal 273) and the output of flip-flop 271c (i.e., an up signal 274) are applied as inputs to a NAND gate 272, and the output of NAND gate 272 is applied to the input of flip-flop 271a. The output of flip-flop 271 b is also applied to the input of flip-flop 271d. The output of flip-flop 271d is increment/decrement signal 215.

Operation of up/down and increment generator circuit 270 is described in relation to a timing diagram 297 of FIG. 2b. As shown, gated reference signal 203 is a gated version of a cock signal with two out of every four clock cycles gated out by reference signal gate 202. Gated reference signal 203 is passed through delay stage 242 and delay stage 244 to create stage output 245. Multiplexer output 254 is gated reference signal 203 after it has been passed through delay stage 242, delay stage 244, delay stage 246, delay stage 248 and in some cases delay stage 250 depending upon the assertion of selector input as discussed above in relation to FIG. 2a. As shown, up signal 274 and down signal 273 are originally asserted at a logic '0'. Upon the next positive transition of stage output 245, the output of flip-flop 271a transitions to a logic '1'. Then, upon the next positive transition of gated reference clock 203, up signal 274 transitions to a logic '1', and upon the next positive transition of multiplexer output 254, down signal 273 transitions to a logic '1'. Where up signal 274 transitions before down signal 273, increment/decrement signal 215 is asserted as a logic '0'. In contrast, where up signal 274 transitions after down signal 273, increment/decrement signal 215 is asserted as a logic '1'. In this way, a signal indicating whether the value in

unified selector register 230 may be incremented or decremented based on a comparison of a phase shifted version of a reference clock with the reference clock. It should be noted that up/down and increment generator circuit 270 is merely exemplary, and that one of ordinary skill in the art will recognize other up/down circuits that may be used in relation to various embodiments of the invention.

Turning to FIG. 3, a slave delay stage 360 along with an interface register 330 is shown in accordance with various embodiments of the invention. Slave delay stage 360 may be used in place of any or all of slave delay stages 162, 164 discussed above in relation to FIG. 1a. Interface register 330 is used to register program number output 292 discussed above in relation to FIG. 2a. Interface register 330 is a group of D type flip-flops 332 that registers program number output 292 whenever a clock 327 is asserted. In particular, the least significant bit of program number output 292 corresponds to program_number[0] 321, the next bit of program number output 292 corresponds to program_number[1] 323, and the most significant bit of program number output 292 corresponds to program_number[X] 325. The outputs of flip-flops 332 are collectively referred to as delay element enable signals. As shown, slave delay stage 360 includes a number of delay elements 361 that can be configured as a chain of delay elements including one delay element up to the total number of delay elements depending upon the value maintained in interface register 330. Slave delay stage 360 receives an input signal 364 and provides an output signal 365. As an example, where delay stage 360 is used in place of slave delay stage 162, input signal 364 corresponds to strobe 0x and output signal 365 corresponds to strobe 0.

Each delay element 361 includes a delay buffer 363 that may be, but is not limited to, an inverting buffer, a logic gate, or a non-inverting buffer. Based on the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuits that may be used to cause a signal delay. In addition, each delay element 361 includes a multiplexer 362 that is controlled by an input from interface register 330 and is used to control whether the particular delay element is included in an overall delay chain implemented by delay stage 360. In particular, when the value provided from interface register 330 is a logic '1', the particular delay element is not selected. In contrast, when the value provided from selector register 330 is a logic '0', the particular delay element is selected. As each delay element 361 drives a subsequent delay element 361 (e.g., the output of delay element 361d, drives the

output of delay element 361c), the value provided from selector register 330 includes a series of logic '1's followed by a series of logic '0's, with the transition between logic '0's and logic '1's being positioned such that it corresponds to the overall delay line length implemented in delay stage 360.

Again, it should be noted that X-bit output 232 may be encoded. In such cases, an decoder may be implemented to decode program number output 292 before it is registered by interface register 330. In any event, interface circuitry capable of translating program number output 292 into the number of delay elements 361 to be utilized in slave delay stage 361 may be implemented in accordance with different embodiments of the invention. Further, it should be noted that a different delay element configuration and associated interface register may be utilized as will be appreciated by one of ordinary skill in the art based on the disclosure provided herein.

Turning to FIG. 4, a flow diagram 400 depicts a method for signal synchronization in accordance with one or more embodiments of the invention. Flow diagram 400 includes a master flow 405 and a slave flow 425. In some cases, master flow 405 and slave flow 425 operate simultaneously with little or no interaction. In other cases, as suggested by a dashed line 460, portions of slave flow 425 are only operated when certain conditions of master flow 405 are identified. In yet other cases where circuitry used for the master portion is reused in the slave portion, master flow 405 and slave flow 425 do not operate at the same time.

Following master flow 405, a master portion of a delay lock loop circuit is operated (block 410). Operation of the delay lock loop circuit includes comparing a reference signal with a delayed derivative of the reference signal. The delayed derivative of the reference signal is created by applying the reference signal to one or more delay stages that each includes a programmable number of delay elements. Where the delayed derivative of the reference signal is in phase with the reference signal, the two signals are considered locked (block 415). Where the two signals are not locked (block 415), the programmable number of delay elements utilized in the one or more delay stages is modified either up or down in an effort to achieve the lock condition (block 420). Thus, the master portion of the delay lock loop circuit operates to establish a program number that represents the number of delay elements that are used in the one or more delay stages to phase align the delayed derivative of the reference signal with the reference signal.

The program number established in master flow 405 is received by slave flow 42(block 430). The program number is multiplied by a determined multiplicand (block 435), and the product of the multiplication is provided to one or more slave delay stages to select the number of delay elements included in the slave delay stages that are utilized (block 440). The slave delay stages are then operated to delay input signals by an amount corresponding to the product of the multiplication (block 445). It is then determined whether the program number has been updated (block 450). Where the program number has not been changed (block 450), operation of the slave delay stages continues without change (block 445). Alternatively, where the program number has been modified (block 450), the processes of blocks 430-445 are repeated. Again, it should be noted that the multiplication process increases resolution error, but this is less important for operation at lower frequencies. Where higher frequency operation is called for, the multiplication process is not performed.

Those skilled in the art will appreciate that many other embodiments and variations are also possible within the scope of the claimed invention. Embodiments having different combinations of one or more of the features or steps described in the context of example embodiments having all or just some of such features or steps are also intended to be covered hereby.

TI-63572WO

CLAIMS

What is claimed is:

1. A method for reduced area delay signal timing, the method comprising:

providing a delay lock loop circuit, wherein the delay lock loop circuit includes a plurality of selectable delay elements;

operating the delay lock loop circuit in a first mode, wherein a program number is established in relation to a reference frequency, and wherein the program number corresponds to a number of the plurality of selectable delay elements used to establish a first delay time at the reference frequency;

multiplying the program number by a multiplicand; and

operating the delay lock loop circuit in a second mode, wherein an input signal is applied to the delay lock loop circuit, wherein a derivative of the input signal is provided as an output that is delayed by a second delay time corresponding to the multiplied program number, and wherein the second delay time is approximately the first delay time multiplied by the multiplicand.

2. The method of Claim 1, wherein the multiplicand is 2^n, and wherein n is a non-zero integer.

3. The method of Claim 2, wherein multiplying the program number by the multiplicand is accomplished by a process selected from a group consisting of: applying the multiplicand and the program number to a multiplier circuit, left shifting the program number, right shifting the program number, left aligning the program number, right aligning the program number, and replicating delay element enable signals.

4. The method of Claim 3, wherein the multiplicand is the integer two, and wherein multiplying the program number by the multiplicand includes at least one of a) aligning the program number to the left by one bit; b) replicating each delay element enable signal.

5. The method of any of Claims 1-4, wherein the first mode is a master mode, wherein the second mode is a slave mode, and wherein the master mode and the slave mode operate at the same time.

6. The method of any of Claims 1-4, wherein the delay lock loop circuit is implemented in relation to a DDR memory, and wherein the reference frequency is obtained by using a 2x clock implemented as part of the DDR memory interface.

7. The method of any of Claims 1-4, wherein the plurality of selectable delay elements is a first plurality of selectable delay elements incorporated in a first delay stage; wherein the delay lock loop circuit includes a second plurality of selectable delay elements incorporated in a second delay stage; wherein in the master mode a reference clock operating at the reference frequency is applied to the first delay stage and an output of the first delay stage is applied to the second delay stage; wherein the input signal is a first input signal; and wherein operating the delay lock loop circuit in the second mode includes:

applying the first input signal to the first delay stage programmed with the program number multiplied by the multiplicand, wherein the first delay stage provides a first delay output; and

applying a second input signal to the second delay stage programmed with the program number multiplied by the multiplicand, wherein the second delay stage provides a second delay output.

8. A delay lock loop circuit, the delay lock loop circuit comprising:

a first delay stage, wherein the first delay stage includes a first plurality of selectable delay elements, wherein the first delay stage is operable to receive an input clock and to provide a stage clock, and wherein the stage clock is a delayed derivative of the input clock;

a register, wherein the register maintains a program number, and wherein the program number determines a number of the plurality of first plurality of selectable delay elements used in the first delay stage;

a feedback loop, wherein the feedback loop is operable to establish the program number corresponding to a desired delay time;

a multiplication circuit, wherein the multiplication circuit multiplies the program number by a multiplicand;

a second delay stage, wherein the second delay stage includes a second plurality of selectable delay elements, wherein the second delay stage receives an input signal, wherein a selected number of the second plurality of selectable delay elements are

used to delay the input signal to derive an output signal, and wherein the output signal is delayed the desired delay time multiplied by the multiplicand.

9. The system of Claim 8, wherein the system further comprises a DDR memory with a DDR memory interface, wherein the DDR memory interface includes a 2x clock, and wherein the 2x clock is applied as the input clock.

10. The system of Claim 8 or 9, wherein the input signal is a first input signal, wherein the output signal is a first output signal, and wherein the system further comprises:

a third delay stage, wherein the third delay stage includes a third plurality of selectable delay elements, wherein the third delay stage receives a second input signal, wherein a selected number of the third plurality of selectable delay elements are used to delay the second input signal to derive a second output signal, and wherein the second output signal is delayed the desired delay time multiplied by the multiplicand.

11. The system of Claim 8 or 9, wherein the delay lock loop circuit includes a master portion and a slave portion, wherein a portion of the master portion is used to implement the first delay stage, and wherein the portion of the master mode is reused to implement the slave portion.

12. The system of Claim 8 or 9, wherein the delay lock loop circuit is implemented in relation to a DDR memory interface, wherein the DDR memory interface includes a 1x clock and a 2x clock, wherein the reference clock is the 2x clock, and wherein the 1x clock is applied to the slave stage.

13. A method for signal synchronization, the method comprising:

providing at least a first delay stage and a second delay stage, wherein the first delay stage includes a first selectable plurality of delay elements, and wherein the second delay stage includes a second plurality of delay elements;

applying a reference clock to the first delay stage, wherein an output of the first delay stage is a first derivative of the reference clock;

applying the first derivative of the reference clock to the second delay stage, wherein an output of the second delay stage is a second derivative of the reference clock, and wherein the second derivative of the reference clock is a phase shift delayed from the reference clock;

repeatedly selecting a number of the first plurality of delay elements and the second plurality of delay elements until the phase shift is at a desirable amount;

multiplying the number of the first plurality of delay elements and the second plurality of delay elements by a multiplicand; and

applying the product of the multiplication to a slave stage, wherein the product of the multiplication determines a number of utilized delay elements in the slave stage.

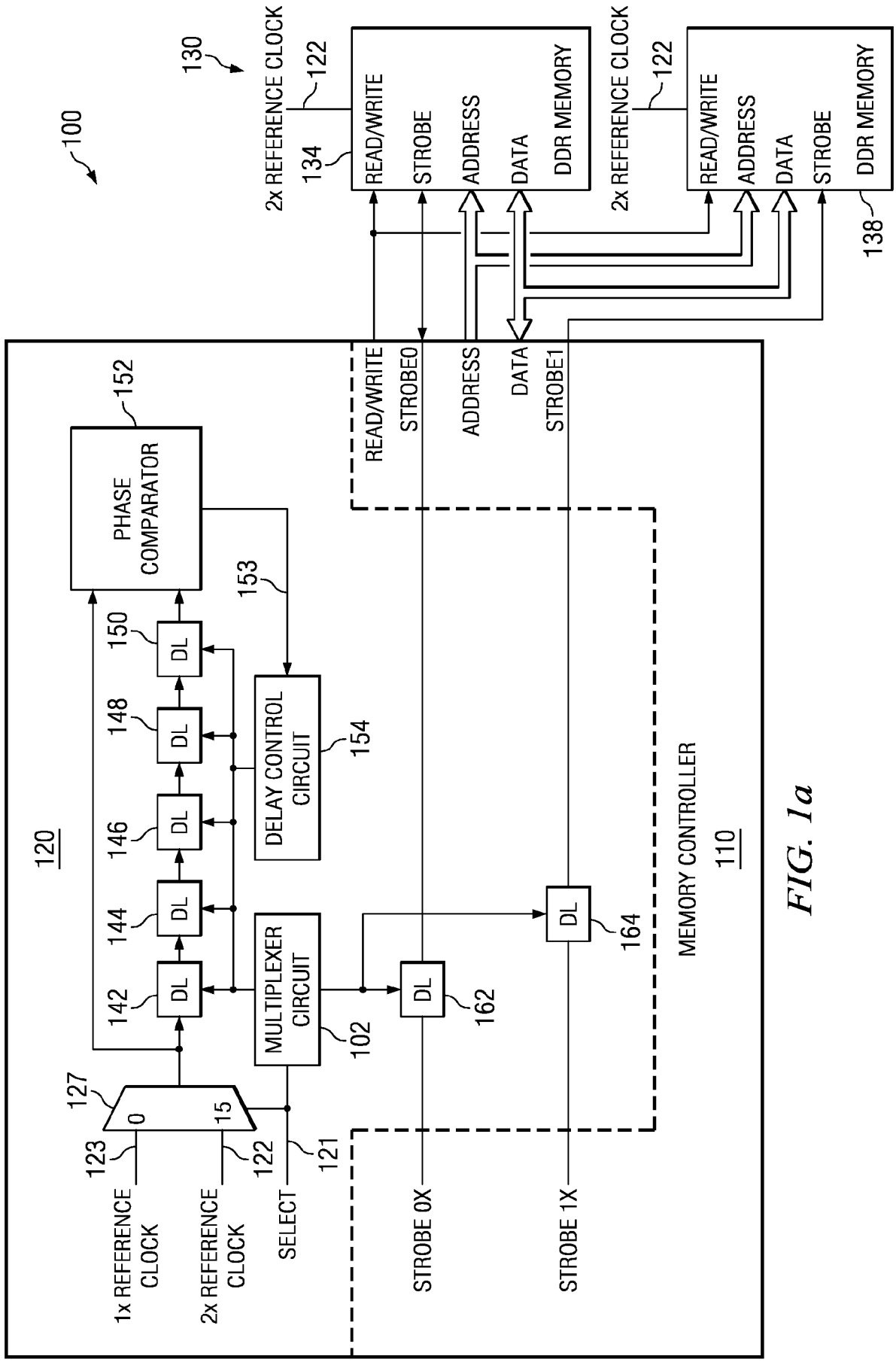

100
130
2x REFERENCE CLOCK
122
134
READ/WRITE
STROBE
ADDRESS
DATA
DDR MEMORY
138
120
PHASE COMPARATOR
152
153
150
148
146
144
142
DL
DELAY CONTROL CIRCUIT
154
MULTIPLEXER CIRCUIT
102
127
0
15
123
122
121
1x REFERENCE CLOCK
2x REFERENCE CLOCK
SELECT
STROBE 0X
STROBE 1X
162
164
READ/WRITE
STROBE0
ADDRESS
DATA
STROBE1
MEMORY CONTROLLER
110

FIG. 1a

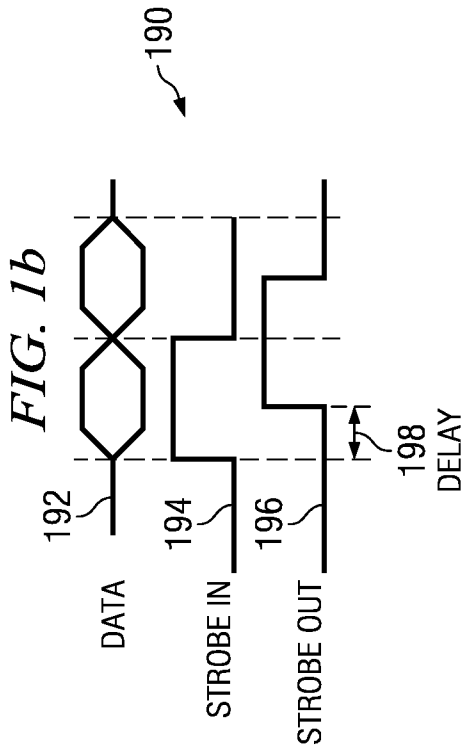

190
192
194
196
198
DELAY
DATA
STROBE IN
STROBE OUT

FIG. 1b

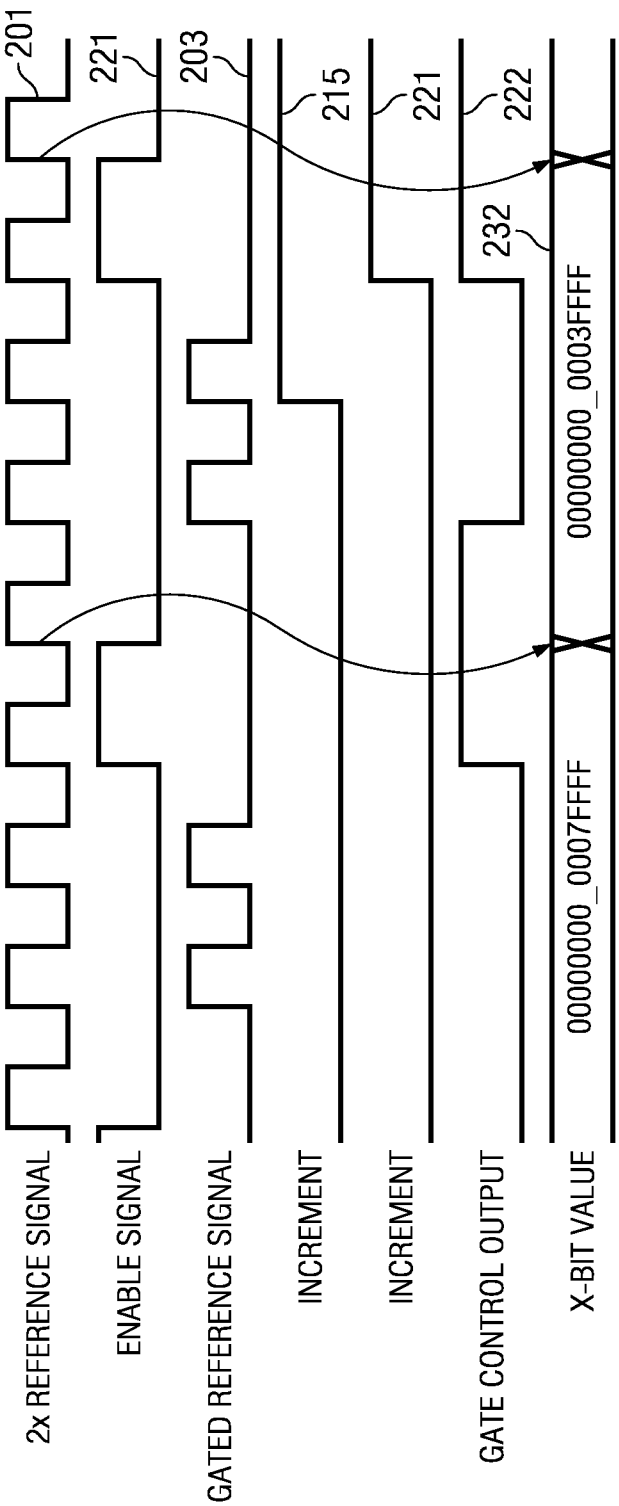

201
221
203
215
221
222
232
2x REFERENCE SIGNAL
ENABLE SIGNAL
GATED REFERENCE SIGNAL
INCREMENT
INCREMENT
GATE CONTROL OUTPUT
X-BIT VALUE
00000000_0007FFFF
00000000_0003FFFF

FIG. 2b

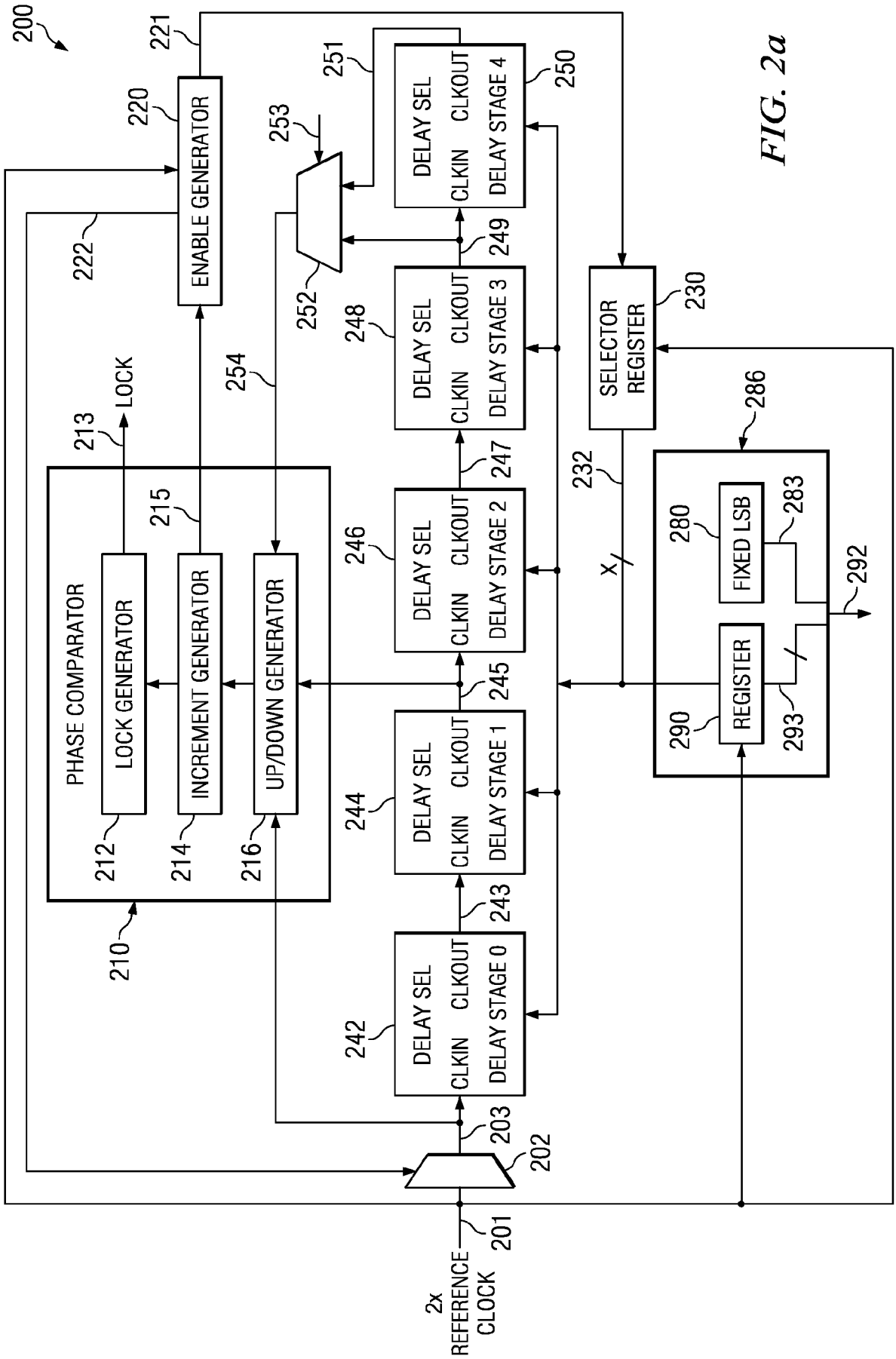

200
221
220
ENABLE GENERATOR
222
253
251
DELAY SEL
CLKIN CLKOUT
DELAY STAGE 4
250
252
249
248
DELAY SEL
CLKIN CLKOUT
DELAY STAGE 3
254
213
LOCK
215
247
246
DELAY SEL
CLKIN CLKOUT
DELAY STAGE 2
PHASE COMPARATOR
LOCK GENERATOR
INCREMENT GENERATOR
UP/DOWN GENERATOR
212
214
216
210
245
244
DELAY SEL
CLKIN CLKOUT
DELAY STAGE 1
243
242
DELAY SEL
CLKIN CLKOUT
DELAY STAGE 0
203
202
201
2x
REFERENCE
CLOCK
SELECTOR
REGISTER
230
232
X
286
280
FIXED LSB
283
292
290
REGISTER
293

FIG. 2a

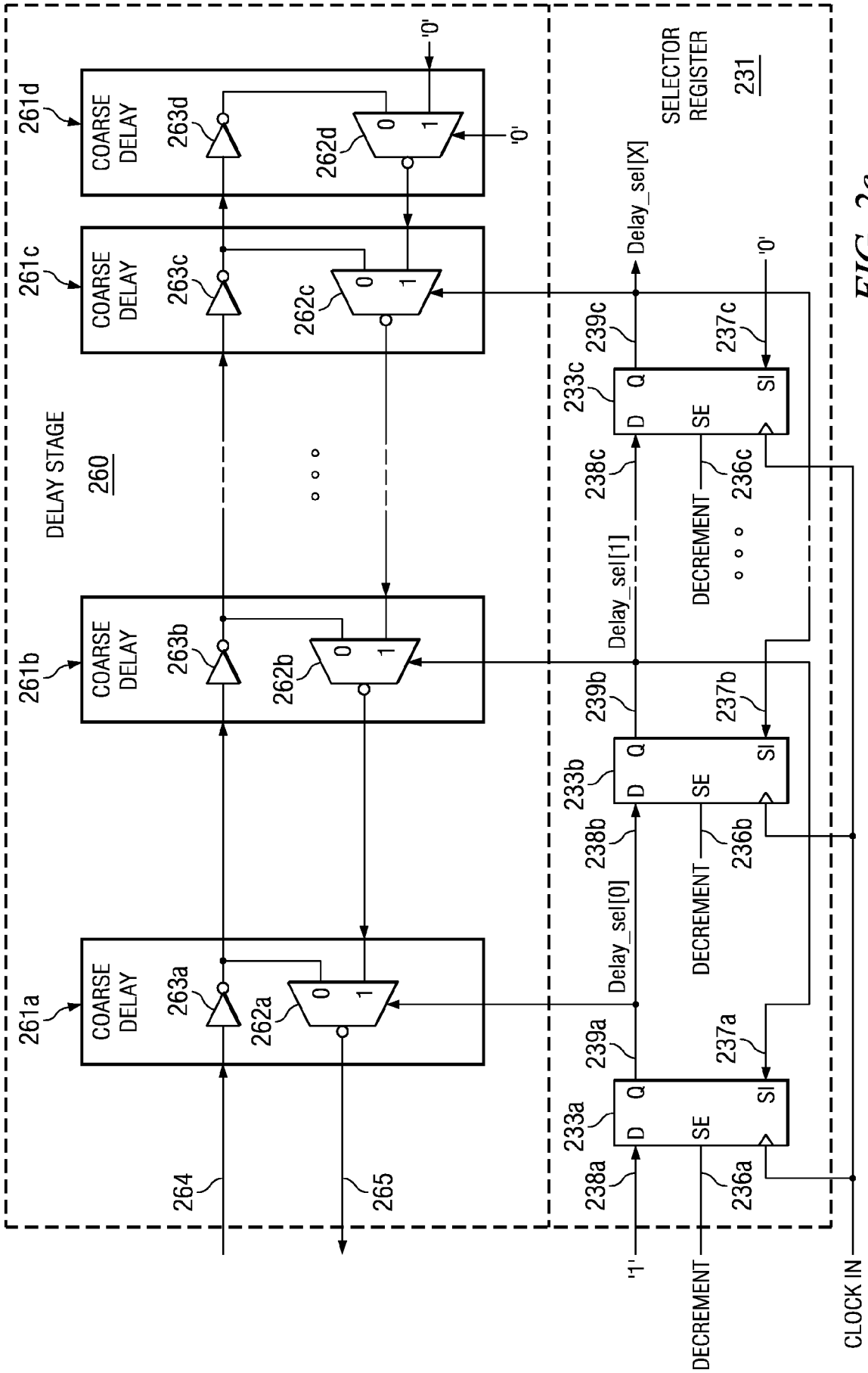

DELAY STAGE
260
SELECTOR REGISTER
231
COARSE DELAY
261a
261b
261c
261d
263a
263b
263c
263d
262a
262b
262c
262d
'0'
'1'
Delay_sel[X]
Delay_sel[1]
Delay_sel[0]
DECREMENT
CLOCK IN
264
265
233a
233b
233c
236a
236b
236c
237a
237b
237c
238a
238b
238c
239a
239b
239c
D
Q
SE
SI

FIG. 2c

FIG. 2d

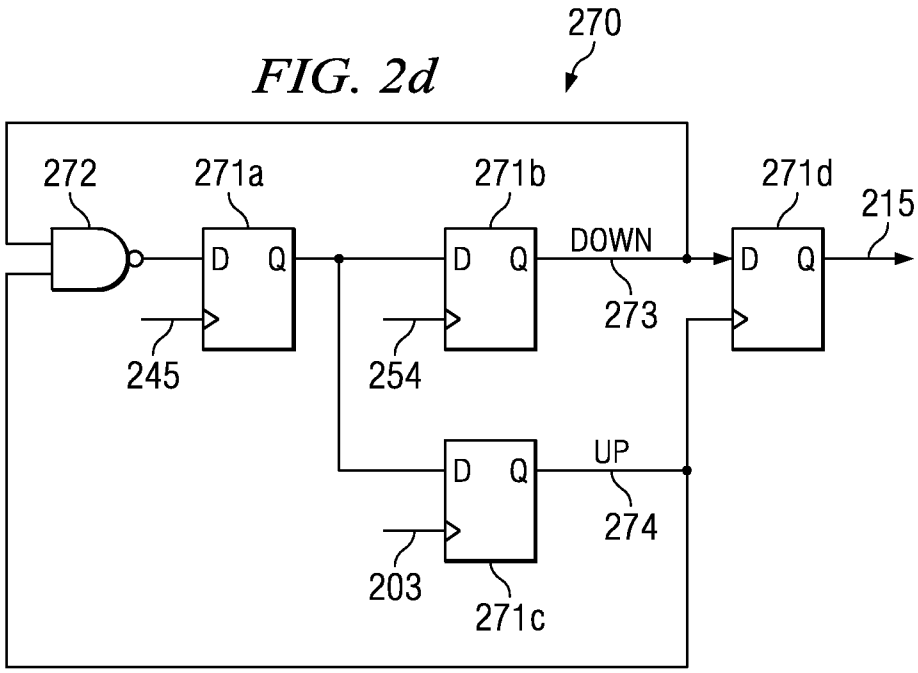
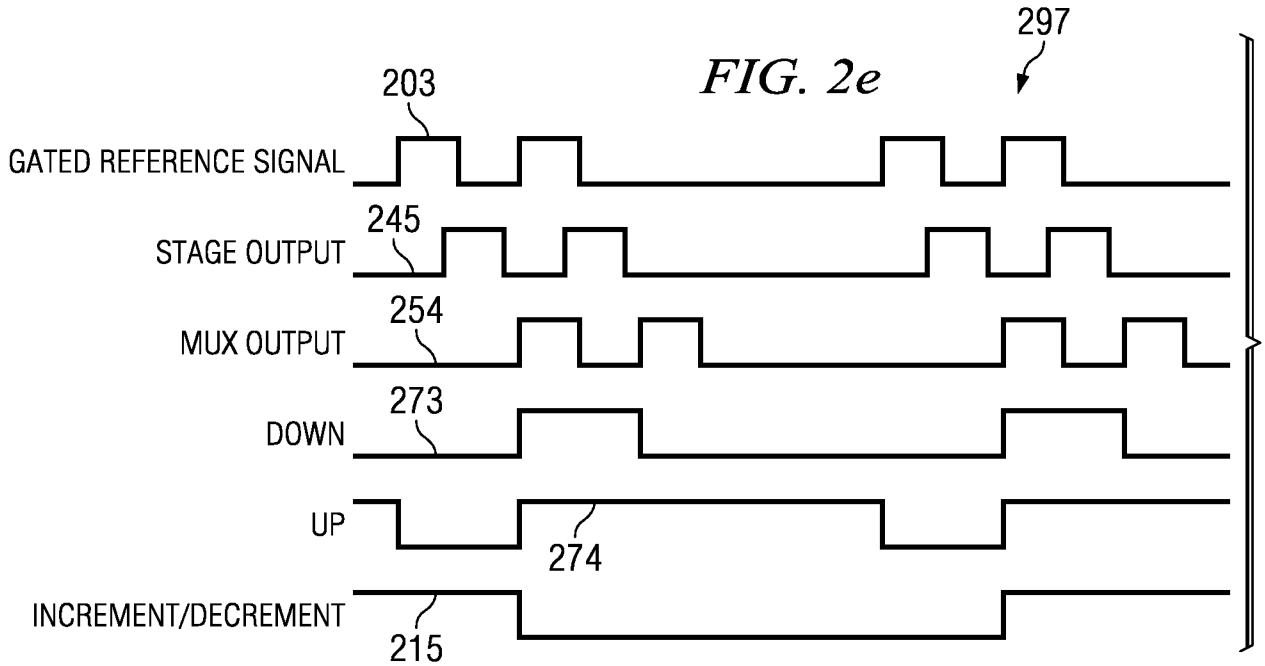

270
272
271a
271b
271d
215
D Q
DOWN
273
245
254
UP
274
203
271c

FIG. 2e


297
203
GATED REFERENCE SIGNAL
245
STAGE OUTPUT
254
MUX OUTPUT
273
DOWN
UP
274
INCREMENT/DECREMENT
215

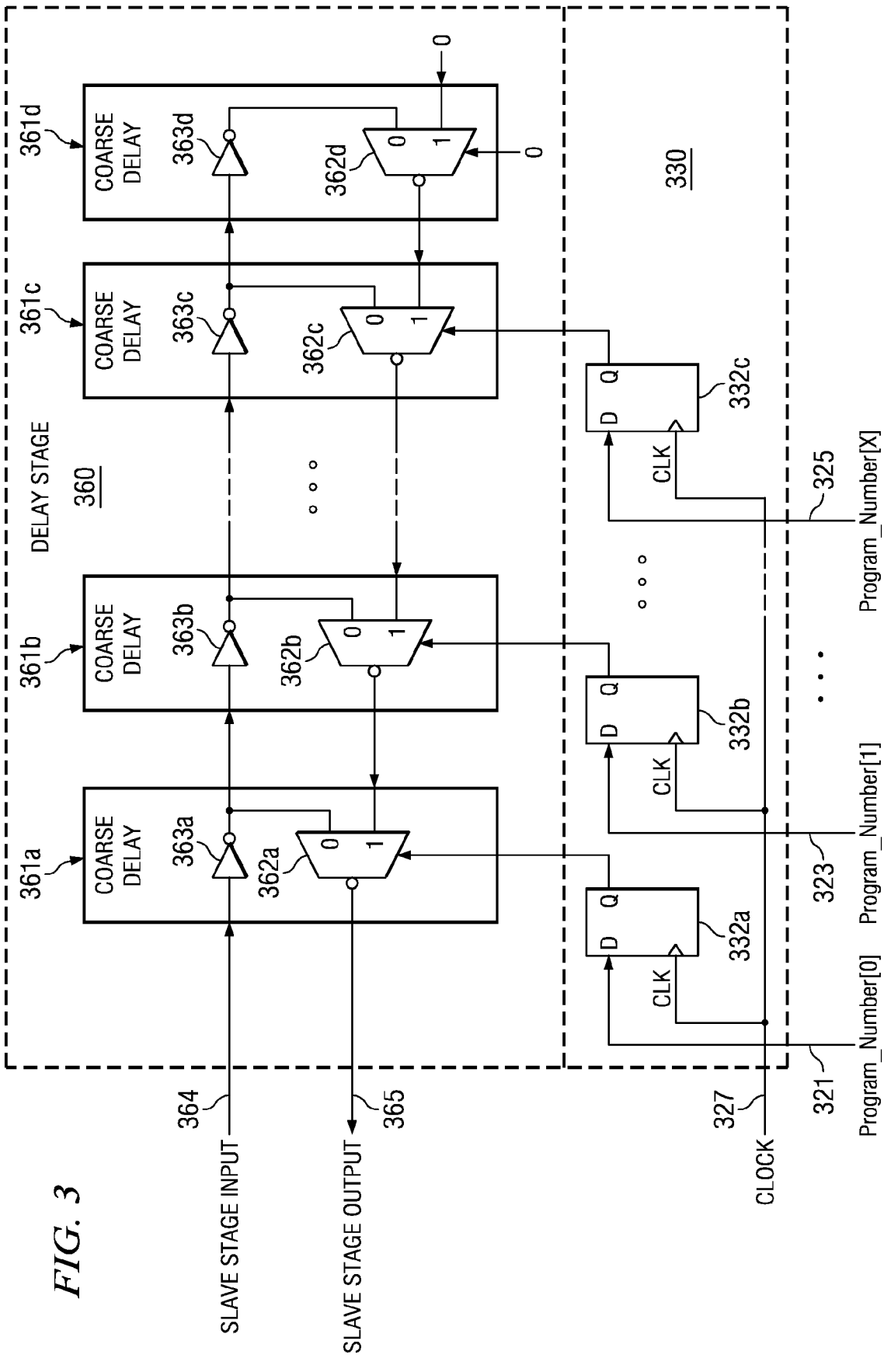
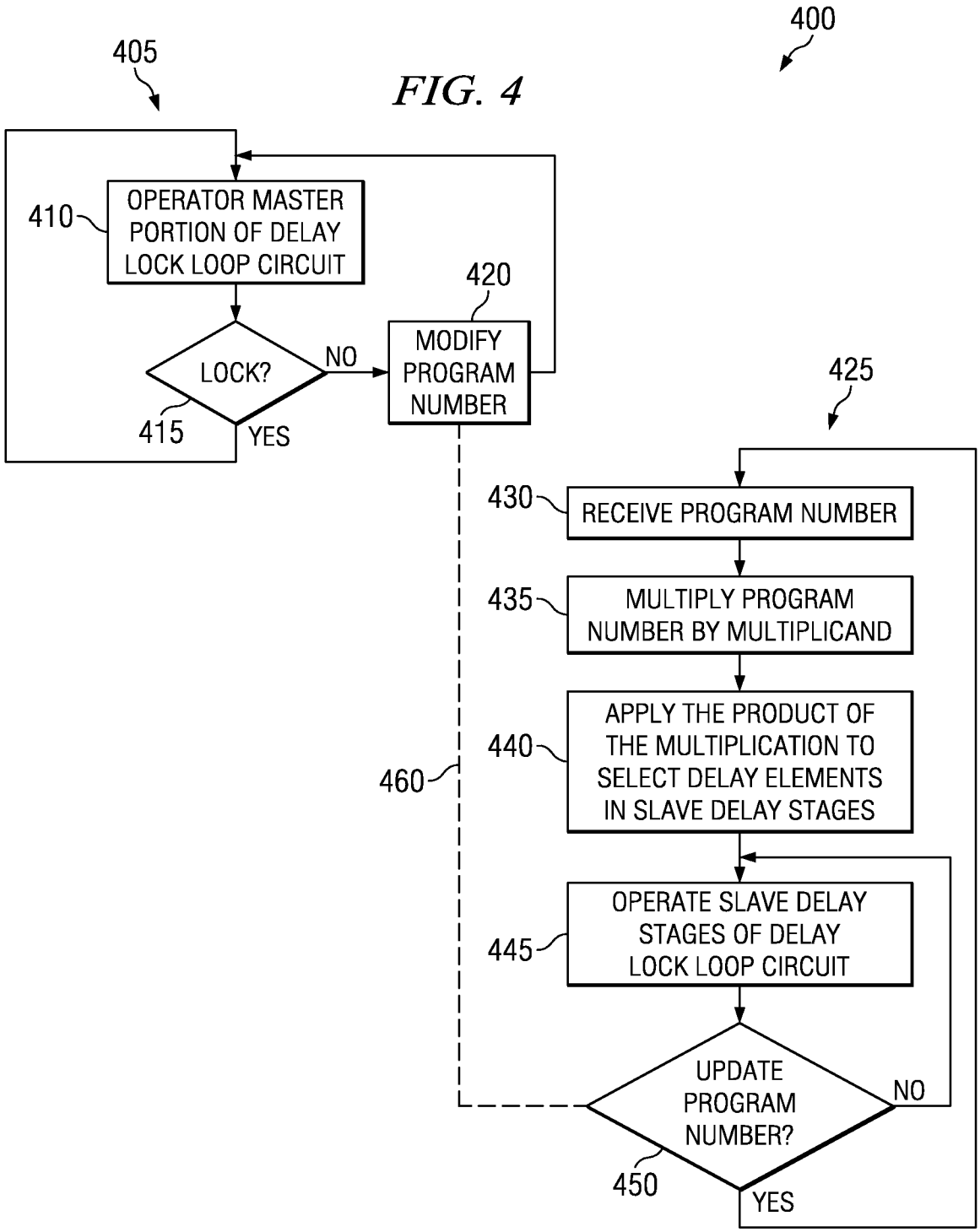

DELAY STAGE
360
330
361a
361b
361c
361d
COARSE DELAY
363a
363b
363c
363d
362a
362b
362c
362d
0
1
0
0
332a
332b
332c
D Q
CLK
323
325
Program_Number[0]
Program_Number[1]
Program_Number[X]
321
327
CLOCK
364
365
SLAVE STAGE INPUT
SLAVE STAGE OUTPUT

FIG. 3

FIG. 4


400
405
410
OPERATOR MASTER PORTION OF DELAY LOCK LOOP CIRCUIT
420
LOCK?
NO
MODIFY PROGRAM NUMBER
415
YES
425
430
RECEIVE PROGRAM NUMBER
435
MULTIPLY PROGRAM NUMBER BY MULTIPLICAND
440
APPLY THE PRODUCT OF THE MULTIPLICATION TO SELECT DELAY ELEMENTS IN SLAVE DELAY STAGES
460
445
OPERATE SLAVE DELAY STAGES OF DELAY LOCK LOOP CIRCUIT
UPDATE PROGRAM NUMBER?
NO
450
YES

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/072032

A. CLASSIFICATION OF SUBJECT MATTER

H03L 7/081(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 8 :H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Utility models and applications for Utility models since 1975
Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKIPASS(KIPO internal, Keyword: " delay, lock, loop, selectable, memory, controller, hold, time, strobe and the similar terms")

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7234069 B1(Johnson) 19 June 2007 See abstract; Figs 16, 17; column 12, line 61-column 15, line 16	1-13
A	US 7126399 B1(Lee) 24 October 2006 See abstract; Figs 5, 6; column 4, line 66-column 8, line 8	1-13
A	US 6946872 B1(Pan et al.) 20 September 2005 See abstract; Fig 2; column 3, line 40-column 4, line 12	1-13
A	US 6940768 B2(Dahlberg et al.) 6 September 2005 See abstract; Figs 1, 2; column 3, line 52-column 4, line 47	1-13

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 OCTOBER 2008 (09.10.2008)	**09 OCTOBER 2008 (09.10.2008)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea	KIM, Ki Wan
Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-5682

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2008/072032

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7234069 B1	19.06.2007	NONE	
US 7126399 B1	24.10.2006	NONE	
US 6946872 B1	20.09.2005	US 7167023 B1	23.01.2007
US 6940768 B2	06.09.2005	US 2005-0105349 A1	19.05.2005