

(57) Abstract: The present application provides a level shifter in integrated circuit with a reduced N-well spacing requirement.

Title

A LEVEL SHIFTER

Field

5 The present application relates to level shifters.

Background of The Invention

A level shifter in digital electronics, also called a logic-level shifter, is a circuit used to translate signals from one logic level or voltage domain to
10 another, allowing compatibility between different circuits having different voltage requirements, such as TTL and CMOS. Level shifters, also known as voltage translators, are devices that resolve mixed voltage incompatibility between different parts of a system that operate in multiple voltage domains.

A prior art implementation of a level shifter is shown in Figure 1, which
15 converts an input signal *In* in a first voltage domain (switching between *Vss* and *Vdd*) to an output signal *Out* in a second voltage domain (switching between *Vdda* and *Vssa*). The level shifter shown is a uni-directional level shifter in that changes in state of the signal *In* are presented to the output *Out*, but the reverse does not apply.

20 The supply voltage of the first voltage domain, *Vdd* might, for example, be 1.8V while the supply voltage for the second voltage domain *Vdda* might be 3.3V. Typically, the references *Vss* and *Vssa* are commonly connected as a ground *gnd*.

The level shifter 1 comprises a first transistor 2 and a second transistor 4
25 arranged together as an inverter 22. The first transistor is a PMOS transistor having its source connected to *Vdd* and its drain connected to an output node from the inverter and to the drain of the second transistor. The source of the second transistor, which is a NMOS transistor, is connected to the reference voltage *Vss* of the first voltage domain. The input to the level shifter is provided
30 as an input to the inverter at the commonly connected gates of the first and second transistors. The output of the inverter is provided to the gate of a third

transistor 6 which is part of a cross coupled circuit 24, which acts as a buffer in which a level shifting occurs.

Thus whilst the output of the inverter is in the first voltage domain, the output from the cross coupled circuit is in the second voltage domain and the transistors of the cross coupled circuit are connected to the second voltage domain. Thus the source of the third transistor is tied to the reference voltage V_{ssa} of the second voltage domain. The cross coupled circuit further comprises a fourth transistor 8, fifth transistor 10 and sixth transistor 12. The drain of the third transistor 6 is connected to a first intermediate node which is also connected to the drain of the fourth transistor 8. The source of the fourth transistor is connected to the supply voltage V_{dda} of the second voltage domain. The input signal In is provided to the gate of the fifth transistor 10. The source of the fifth transistor is connected to the reference voltage V_{ssa} . The drain of the fifth transistor is connected to a second intermediate node which is also connected to the drain of the sixth transistor 12. The source of the sixth transistor is connected to V_{dda} . The gate of the fourth transistor is connected to the second intermediate node with the gate of the sixth transistor connected to the first intermediate node. The output from the cross coupled circuit is taken from the second intermediate node and provided to commonly connected gates of a seventh transistor 14 and an eighth transistor 16, which are configured as an inverter circuit 26. The source of the eighth transistor is connected to V_{dda} . The drains of the seventh and eighth transistors are commonly connected to an output node. The source of the seventh transistor 14 is switchably connected through a ninth transistor 18 to V_{ssa} . The output node is switchably connected by a tenth transistor 20 to V_{dda} . The gates of the ninth and tenth transistors are connected to a signal En .

The operation of the level shifter will now be explained with signal En set at V_{dda} (the purpose of the signal En will be explained below). With En set high (i.e. at V_{dda}), this ensures the ninth transistor is on and the tenth transistor is off. Then if "in" is high the fifth transistor is turned on and the third transistor is off. The fifth transistor being on means the gate of the fourth transistor is low ensuring that it is on. This means the gate of the sixth transistor is high.

Therefore, the fifth transistor drain is low turning on the eighth transistor and pulling the “out” node high to $Vdda$. In the same way if In is low, the signal Out is pulled low. In the high or low states there is no dc current flow from either Vdd or $Vdda$ supplies.

5 The purpose of the En signal is to ensure a defined output state at node “out” and no dc current draw when say the vdd supply is down and the $Vdda$ supply is up. For example, if vdd is down then the gates of the third transistor and the fifth transistor are both low. This means the voltages at the drains of the third transistor and the fifth transistor are poorly defined so any following
 10 inverter can be poorly defined in terms of input voltage and consume a lot of current. The signal En comes from a circuit (not shown) that is configured to ensure it is high when Vdd is low and $Vdda$ is high. This means that the ninth transistor is off and the inverter comprising the eighth transistor and the seventh transistor does not consume DC current. The tenth transistor also pulls the “out”
 15 node high in this condition ensuring that any following logic gates do not consume unwanted current.

As will be familiar to those skilled in the art, the nature of NMOS and PMOS transistors is illustrated in Figure 2, with the structure 40a of a NMOS device 40b is shown and the structure 42a of a PMOS device 42b is shown.

20 The NMOS device is provided in a p substrate. There are four connections to the NMOS device corresponding to the gate G, drain D, source S and body B.

The drain and body connection of the first transistor (a PMOS transistor) is connected to the supply voltage of the first voltage domain. The drain and body connections of the remaining PMOS transistors 8, 12, 16, 20 are connected to
 25 the supply voltage of the second voltage domain $Vdda$. Similarly, the source and body connection of the second transistor (a NMOS transistor) is connected to the reference voltage of the first voltage domain. The body and source connections of NMOS transistors 6, 10, 18 are connected to the reference voltage of the second voltage domain $Vssa$. NMOS transistor 14 is slightly
 30 different in that body is connected to the reference voltage of the second voltage domain with the source switchably connected to the reference voltage of the second domain by the ninth transistor 18.

The voltage rating of the transistors are selected to match their operating domain, thus the voltage rating of the first and second transistors are selected to match the first voltage domain, thus if the first voltage domain is 1.8 volts then the first and second transistors are selected to correspond and have an
5 operating voltage to match closely, for example 2V. Similarly, the operating voltages of the remaining transistors operate in the second voltage domain and have operating voltages rated to match. Thus if the second voltage domain is 3V then the transistors may be rated at 3V or above.

The present application provides an alternative design of level shifter
10 which has a reduced footprint in an integrated circuit.

Summary

The present application provides a level shifter in an integrated circuit comprising a substrate. The integrated circuit has a first level shifting circuit for
15 translating a first input signal in a first voltage domain, the first voltage domain defined by a first supply voltage and a first reference voltage, to a first output signal in a second voltage domain, the second voltage domain defined by a second supply voltage and a second reference voltage. The first level shifting circuit suitably comprises:

20 a first inverter comprising a first transistor and a second transistor, the first and second transistors being configured to invert the input signal to provide an inverted input signal,

a cross coupled circuit responsive to the inverted input signal to provide a buffered signal of the inverted input signal, and

25 a second inverter for inverting the buffered signal to provide an output signal from the level shifting circuit,

wherein the first transistor is formed using a well in the substrate and wherein the well of first transistor is connected to the supply voltage of the second voltage domain.

30 The first transistor may be rated for the second voltage domain. The second transistor may be rated for the second voltage domain.

The source of the first transistor may be connected to the supply voltage of the first voltage domain. The gates of the first and second transistors may be commonly connected. The drains of the first and second transistors are commonly connected and the inverted input signal is provided from the drains of the first and second transistors. The integrated circuit may further comprising a state defining circuit configured to set the output from the level shifter in a defined state when the supply voltage of the first voltage domain is absent.

Brief Description of The Drawings

The present application will now be described with reference to the accompanying drawings in which:

Figure 1 is an example of a prior art level shifter;

Figure 2 illustrates the structure of NMOS and PMOS transistors in a P type substrate;

Figure 3 is a level shifter according to a first aspect of the present application;

Figure 4 is an integrated circuit employing the level shifter of Figure 3; and

Figure 5 is an integrated circuit employing a level shifter of the type shown in Figure 3 in combination with a level shifter of the type shown in Figure 1.

Detailed Description of The Drawings

The present application is directed at reducing the footprint of a level shifter and provides an alternative design to that of Figure 1.

This design will now be explained with reference to the embodiment of Figure 3 which, as with the example of Figure 1, converts an input signal *In* in a first voltage domain defined between *Vss* and *Vdd* to an output signal *Out* in a second voltage domain defined between *Vssa* and *Vdda*. *Vss* is not shown as it is commonly connected, for example as a ground, with *Vssa*. Thus as input signal switches between *Vss* and *Vdd*, the level switcher causes the output to switch between *Vssa* and *Vdda*. As before, the supply voltage of the first voltage domain, *Vdd* might, for example, be 1.8V while the supply voltage for the second voltage domain *Vdda* might be 3.3V.

The level shifter 101 comprises a first transistor 102 and a second transistor 104 arranged together as a first inverter 122. The first transistor 102 is a PMOS transistor having its source connected to the reference voltage of the first voltage domain *Vdd*. The drain of the first transistor is connected to an output node 130 of the first inverter. *In* contrast to the first transistor in figure 1, the body of the first transistor 102 is connected to the supply voltage of the second domain *Vdda*. Otherwise stated, the body of the first transistor is biased at the supply voltage of the second domain.

The second transistor 104 is an NMOS transistor. The drain of the second transistor is connected to the output node 130 of the first inverter. The source of the second transistor 104 is connected to the reference voltage *Vssa* of the second voltage domain.

The gates of the first and second transistors are commonly connected to an input node 132 of the level shifter. The input to the level shifter *In* is provided to the input node 132. The output node 130 of the inverter is connected to the gate of a third transistor 106 which is part of a cross coupled circuit 124, in which a level shifting occurs. The cross coupled circuit may also be considered a latching circuit as it latches the changes presenting at *In*.

Thus whilst the first and second transistors of the first inverter are connected to the first voltage domain and the output of the inverter is in the first

voltage domain, the cross coupled circuit output operates in the second voltage domain.

The source of the third transistor 106 is tied to the reference voltage V_{ssa} of the second voltage domain. The drain of the third transistor is connected to a
5 first intermediate node 134.

The cross coupled circuit further comprises a fourth transistor 108, fifth transistor 110 and sixth transistor 112. The fourth transistor is a PMOS transistor. The drain of the fourth transistor is connected to the first intermediate node 134. The source of the fourth transistor is connected to the supply voltage
10 V_{dda} of the second voltage domain. Similarly, the body of the fourth transistor is connected to V_{dda} . The gate of the fourth transistor is connected to a second intermediate node 136 of the cross coupled circuit 124.

The fifth transistor 110 is a NMOS transistor. The source of the fifth transistor is connected to V_{ssa} . The body of the fifth transistor is also connected
15 to V_{ssa} . The drain of the fifth transistor is connected to the second intermediate node 136. The gate of the fifth transistor is connected to the input node 132.

The sixth transistor 112 is a PMOS transistor. The drain of the sixth transistor is connected to the second intermediate node 136. The source of the sixth transistor is connected to V_{dda} . Similarly, the body of the sixth transistor is
20 connected to V_{dda} . The gate of the sixth transistor is connected to the first intermediate node 134.

The output from the cross coupled circuit is taken from the second intermediate node 136 and provided as the input to a second inverter 126. The second inverter 126 comprises a seventh transistor 114 and an eighth transistor
25 116.

The seventh transistor 114 is a NMOS transistor. The source of the seventh transistor is connected to V_{ssa} . The body of the seventh transistor is also connected to V_{ssa} . The drain of the seventh transistor is connected to an output node 138 of the level shifter from which the signal *Out* is provided. The
30 gate of the seventh transistor is connected to the second intermediate node 136.

The eighth transistor 116 is a PMOS transistor. The source of the eighth transistor is connected to V_{dda} . Similarly, the body of the eighth transistor is connected to V_{dda} . The gate of the eighth transistor is connected to the second intermediate node 136. The drain of the eighth transistor is connected to the output node 138.

A ninth transistor 118 is provided to safeguard for non-normal working conditions. The ninth transistor 118 is a NMOS transistor. The source of the ninth transistor is connected to V_{ssa} . The body of the ninth transistor is also connected to V_{ssa} . The drain of the ninth transistor is connected to the second intermediate node 136. The gate of the ninth transistor is connected to a signal poc , the purpose of which will be explained below.

The operation of the level shifter in Figure 3 is broadly similar to that of Figure 1 and will now be explained.

The operation of the level shifter will now be explained with signal poc set low, i.e. at V_{ssa} (the purpose of poc will be explained below). With poc low, the the ninth transistor is off.

If In is high the first transistor 102 is off and the second transistor 104 is on so that the output from the first inverter 122 presented at node 130 is low. With the node 130 low, the third transistor 106 is off.

Similarly, with In high the fifth transistor is on and so the second intermediate node 136 is connected to V_{ssa} through the fifth transistor.

This in turn causes the fourth transistor to turn on meaning that the first intermediate node 134 is high. With the first intermediate node 134 high, the sixth transistor is turned off. Accordingly, the output from the cross coupled circuit 124 at the second intermediate node 136 is ensured to be low.

With the second intermediate node low, the seventh transistor is turned off and the eighth transistor is turned on. Accordingly the output node is connected through the eighth transistor to V_{dda} and so the output from the level shifter is high in the second voltage domain. Thus with In being a high in the first voltage domain, the output Out is high in the second voltage domain.

Similarly, the opposite situation is the case namely In being a low in the first voltage domain, the output Out is low in the second voltage domain.

Specifically, if In is low the first transistor 102 is on and the second transistor 104 is off so that the output from the first inverter 122 presented at node 130 is high. With the node 130 high, the third transistor 106 is on. This means that the voltage at the first intermediate node is low and thus the sixth transistor 112 is on.

Similarly, with In low the fifth transistor 110 is off. Thus the second intermediate node 136 is connected to $Vdda$ through the sixth transistor 112, i.e. the second intermediate node 136 is high.

This in turn ensures that the fourth transistor is turned off ensuring that the first intermediate node 134 is low. With the second intermediate node high, the seventh transistor is turned on and the eighth transistor is turned off. Accordingly the output node is connected through the seventh transistor to $Vssa$ and so the output from the level shifter is low in the second voltage domain. Thus with In being a low in the first voltage domain, the output Out is low in the second voltage domain.

As with the signal En signal in figure 1, the purpose of the poc signal in combination with the ninth transistor 118 is to ensure a defined output state at the output of the cross coupled circuit and no DC current draw when say the Vdd supply is down (not present) and the $Vdda$ supply is up (present). For example, if Vdd is down then the gates of the third transistor and the fifth transistor are both low. The result of this is that the voltage at nodes 134, 136 float at a level based on leakage effects. This is since the first and second intermediate nodes are both being pulled low which in turn is forcing the respective fourth and sixth transistors to be turning on and thus pulling up the first and second intermediate nodes. This has the clear effect that the voltage at the second intermediate node can be poorly defined (at least in terms of input voltage) and the cross coupled circuit can consume a lot of current.

The signal poc comes from a circuit (not shown) that is configured to ensure it is high when Vdd is low and $Vdda$ is high. Under such conditions, with poc high, this means that the ninth transistor 118 is on. As a result, the voltage presented at the second intermediate node is pulled low (i.e. connected through the ninth transistor to $Vssa$). Thus the ninth transistor in combination with the

circuit providing the poc signal combine to act as a state defining circuit which sets the output from the level shifter in a defined state when the supply voltage of the first voltage domain is absent.

With the gate of the fourth transistor low and gate of the sixth transistor high, this causes the seventh transistor to be off and the eighth transistor to be on – resulting with the output node 138 going high. At the same time, the third and fifth transistors are off since V_{dd} is low. Overall there is again no dc current flow and the output of the level shifter is well defined.

A significant difference with the prior art is that the body 140 of the first transistor 102 is connected to the supply voltage V_{dda} of the second voltage domain rather than the conventional approach of Figure 1 of connecting it to the supply voltage V_{dd} of the first domain. This approach is on the face of it entirely counter intuitive. However by connecting the body 140 of the first transistor 102, the nwell of the first transistor is connected to V_{dda} . By having, the nwell of the first transistor at the same potential to that of the remaining PMOS transistors of the level shifter, it eliminates the requirement to have nwell to nwell spacing between the nwell of the first transistor and the nwells of the fourth, sixth and eighth transistors. It also relieves the necessity of having spacing between the nwell and deep n wells as illustrated in Figure 2.

For example, in the exemplary situation where the first voltage domain was 1.8V and the second voltage domain was 3V a nwell to nwell spacing of typically 5um might be needed where deep nwell is used. In the case of an integrated circuit which is purely a level shifter 101 of the type shown in Figure 3, such as the example shown in Figure 4, this may appear a small difference as the scale of the level shifter to the overall size of the integrated circuit package is very small.

However, where the integrated circuit has a significant number of level shifters in combination with other circuits on the integrated circuit, the real estate occupied on the integrated circuit by level shifters becomes quite costly. In this context, an integrated circuit may have hundreds of level shifters.

The nature of the space saved was calculated with reference to an example layout of a level shifter of the type shown in Figure 1, which occupied

space having dimensions of approximately 30.7 μm x 11.9 μm when using a 180nm process.

In contrast, an exemplary layout of the level shifter of Figure 3 using the same 180nm process resulted in an occupied space of 7.7 μm x 7.6 μm . As a
5 result, the space occupied by a cell on an integrated containing a level shifter of the present application is approximately only 16% of that of the prior art example of Figure 1 representing over a six fold reduction in space.

Some of the reduction arises from the *poc* implementation due to a more compact layout, but a significant saving is due to the elimination of the nwell to
10 nwell spacing.

One of the consequences of the design is that the first and second transistors may be selected to be voltage rated for operating in the second voltage domain. Thus in the case where the second voltage domain is 3V, the first transistor may be designed as a 3V devices. The reason why this is
15 advisable is that given that the input node 132 can be at ground while the V_{dda} nwell of the first transistor may be at 3.3V nominally, there are some potential reliability concerns. At the same time, the second transistor is selected to match the first transistor and so is suitably also a 3V device.

Although, the level shifter of Figure 3 results in a significant space saving
20 on an integrated circuit, there is a cost. One downside of connecting the nwell of first transistor to the supply voltage of the second voltage domain V_{dda} is that the threshold voltage of the first transistor becomes higher due to body effect. This increase in threshold voltage can affect the speed of the input inverter in the level shifter and correspondingly the speed of the level shifter. However, for
25 most applications, the input to level shifters is DC or very slow moving. For situations that require speed the arrangement of Figure 1 may be used.

Thus, an integrated circuit 300, may result, as shown in the example of Figure 5, where there is a first type of level shifter 302 and a second type of level shifter 304. In this case, the first level shifter may be a design
30 corresponding to that of Figure 3 in which the nwell of the PMOS transistor in the first inverter is connected to the supply voltage of the second voltage domain. In contrast, the second level shifter 304, may be a design (as for

example) shown in Figure 1 where the nwell of the PMOS transistor in the first inverter is connected to the supply voltage of the first voltage domain.

Although, the use of the *poc* signal requires an additional circuit, e.g. circuit 202 in Figure 4, to sense for the absence of *Vdd* in the presence of *Vdda*,
5 such a circuit occupies a reasonably small space and it may be employed for multiple level shifters.

It will be appreciated that the *En* and arrangement of the ninth and tenth transistors of Figure 1 may be used in place of the *poc* signal and ninth transistor in Figure 3. This approach will still provide the space saving from the
10 avoidance of the requirement for nwell to nwell spacing.

Similarly, the use of the ninth transistor and *poc* signal of Figure 3 may be employed in the arrangement of Figure 1 without the nwell space saving of Figure 3.

The present application is directed to modern processes where a P-
15 substrate is typically used, which means that PMOS devices can have their own NWELLS or share an NWELL with the same voltage applied. This is in contrast to older N-substrate processes where there are no additional isolated wells and the PMOS devices sit in N-substrate. As a result with these older N-substrates, there is no choice about where the PMOS back gate can be connected. At the
20 same time, in these older processes, the same oxide thickness PMOS device would have been used everywhere.

Additionally, modern processes typically used thick oxide MOSFETs to stand off high voltages in analog regions while using thin oxide devices in logic regions to optimize power, speed, and area in logic regions. The thin oxide
25 devices usually have their own NWELL connected to the lower VCC supply for reliability reasons. This issue did not exist in the older processes where one type of thick oxide device was typically used.

In addition, in some modern processes isolated PWELL in DNWELL is used to isolate NMOS devices from the P-substrate region to improve noise
30 rejection in circuits.

As a result, in previous designs, typically the PMOS device of the input inverter would be a thin oxide device with its source connected to its back gate.

When this is done there is a layout requirement in terms of nwell to nwell spacing of the different nwell s with different voltage supplies.

The present application recognizes the spacing of nwells required. The present application reduces the area required by using the same nwell for both
5 types of PMOS devices. Although the saving for an individual device may be small, in a circuit for example where hundreds of level shifters are used the area saving is very significant.

As a result of the common nwell connection presented, the speed of the input inverter may be reduced so this type of level shifter is less suitable for use
10 in high speed applications. However, typically over 95% of the level shifter applications are DC level shifters, where bits are being set statically e.g. trim bits. With these inverters, the speed of the inverter is largely irrelevant. Accordingly, a significant space saving is possible for these inverters in a circuit using the arrangement presented in this application.

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Claims

1. An integrated circuit comprising a substrate and having a first level shifting circuit for translating a first input signal in a first voltage domain, the first voltage domain defined by a first supply voltage and a first reference voltage, to
5 a first output signal in a second voltage domain, the second voltage domain defined by a second supply voltage and a second reference voltage, the first level shifting circuit comprising:
a first inverter comprising a first transistor and a second transistor, the first and second transistors being configured to invert the input signal to provide an
10 inverted input signal,
a cross coupled circuit responsive to the inverted input signal to provide a buffered signal of the inverted input signal, and
a second inverter for inverting the buffered signal to provide an output signal from the level shifting circuit,
15 wherein the first transistor is formed using a well in the substrate and wherein the well of first transistor is connected to the supply voltage of the second voltage domain.
2. An integrated circuit according to claim 1, wherein the first transistor is
20 rated for the second voltage domain.
3. An integrated circuit according to claim 2, wherein the second transistor is rated for the second voltage domain.
- 25 4. An integrated circuit according to claim 1, wherein the first transistor has a drain, source and gate and the second transistor has a drain source and gate.
5. An integrated circuit according to claim 4, wherein the source of the first
30 transistor is connected to the supply voltage of the first voltage domain.

6. An integrated circuit according to claim 4, wherein the respective gates of the first and second transistors are commonly connected.
7. An integrated circuit according to claim 4, wherein the drains of the first
5 and second transistors are commonly connected and the inverted input signal is provided from the drains of the first and second transistors.
8. An integrated circuit according to claim 1, further comprising a state
10 defining circuit configured to set the output from the level shifter in a defined state when the supply voltage of the first voltage domain is absent.
9. An integrated circuit according to any preceding claim, wherein the substrate is a P type substrate.

15

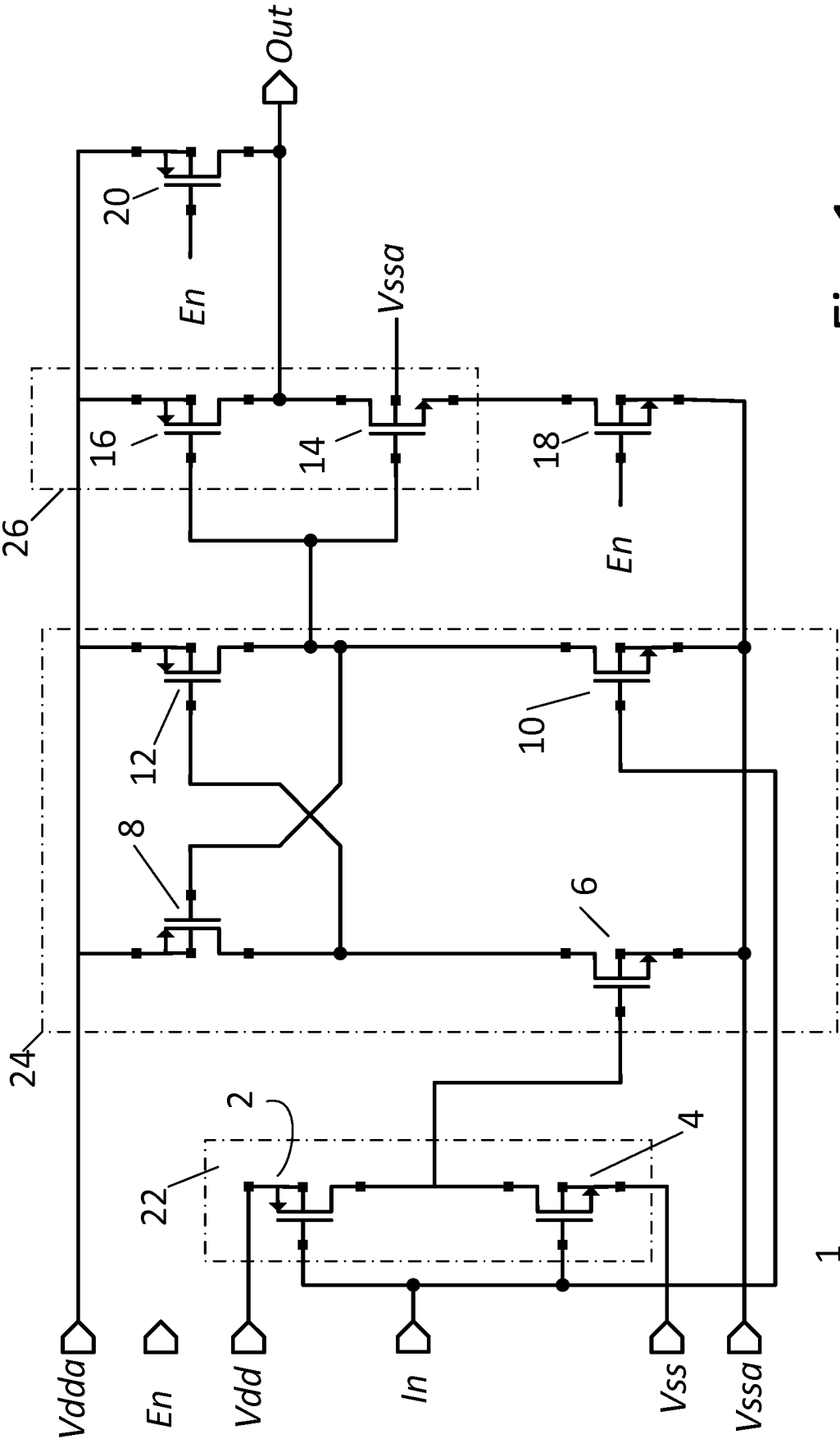
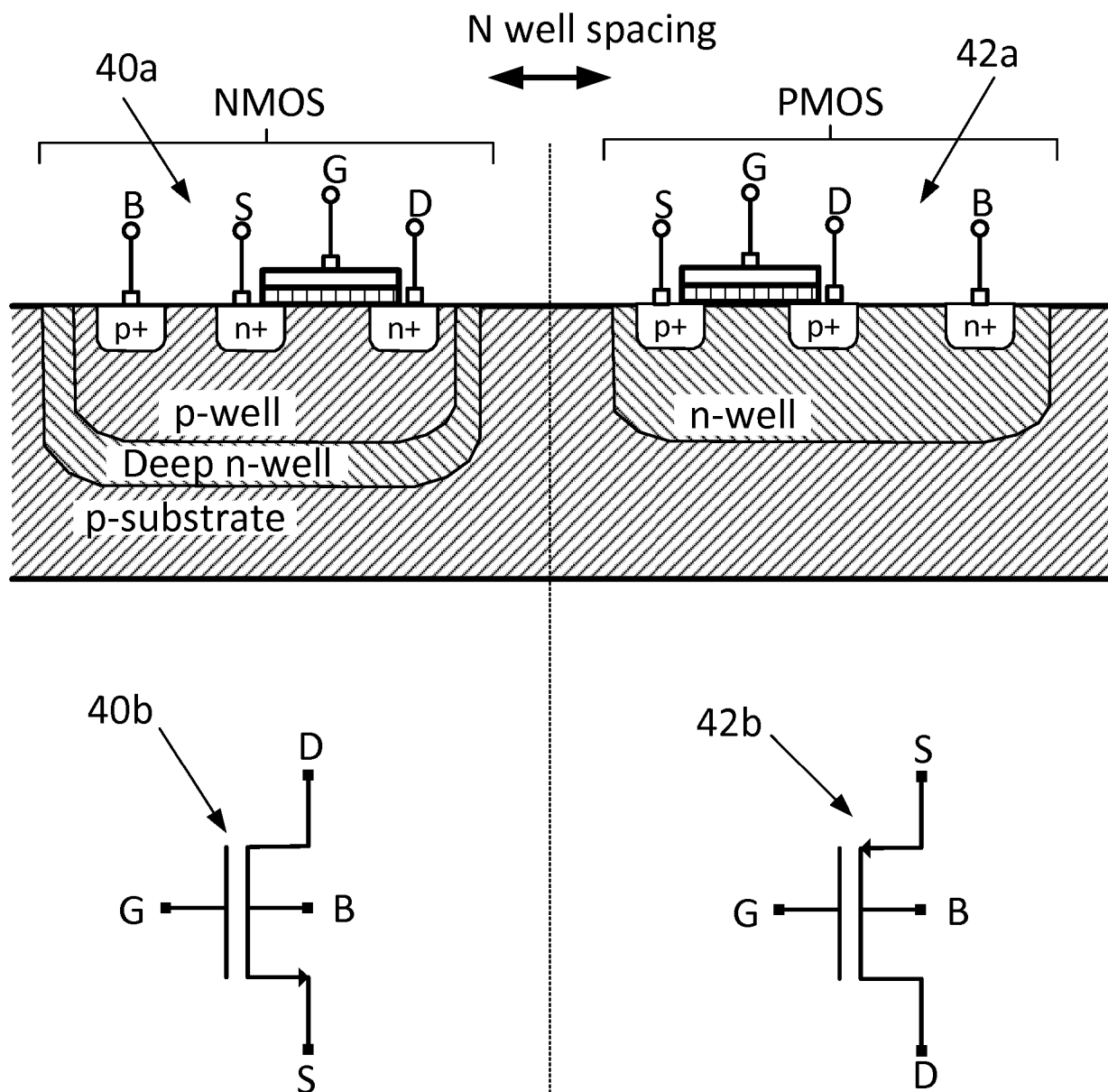


Fig. 1

PRIOR ART



PRIOR ART

Fig. 2

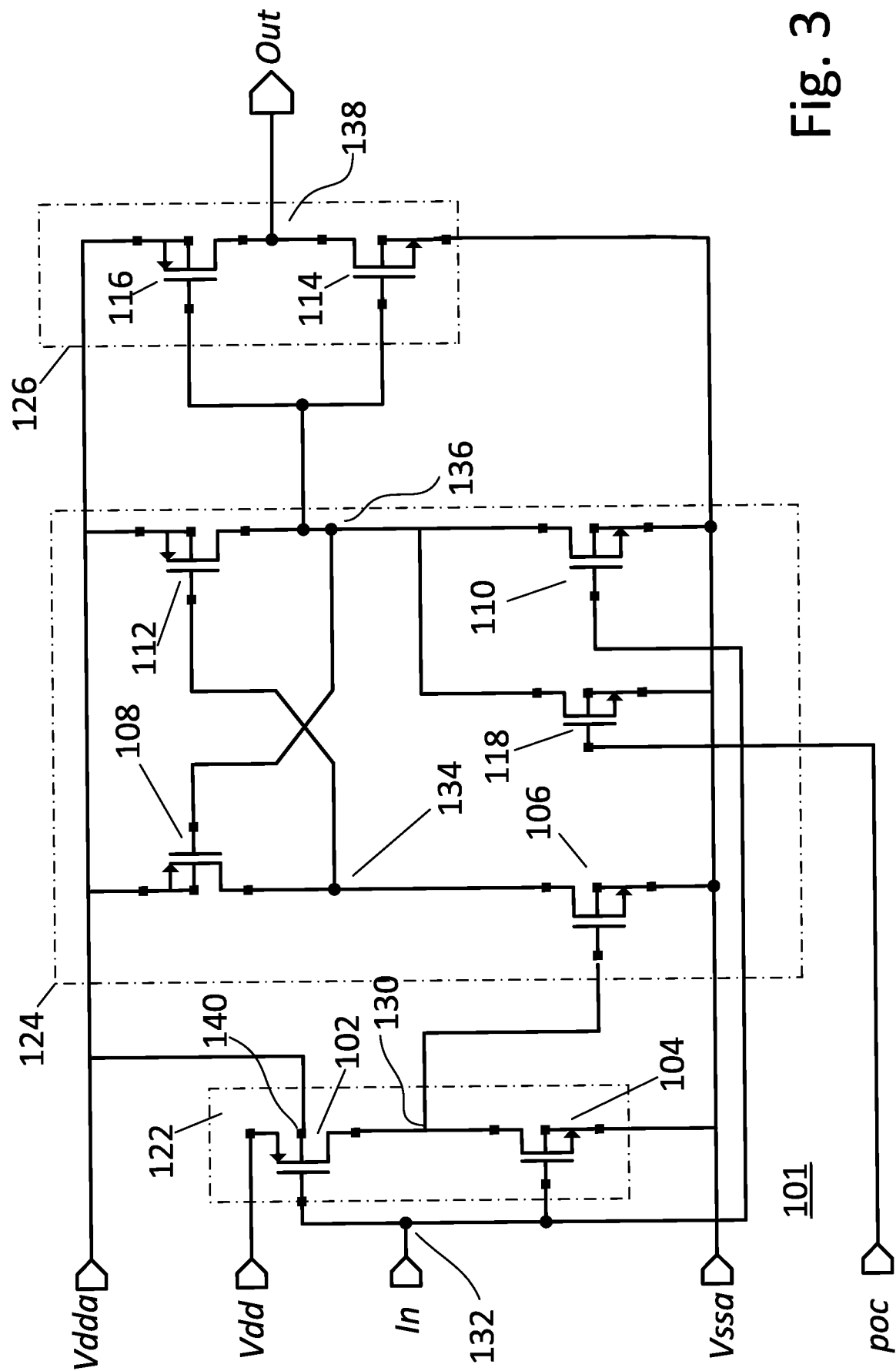


Fig. 3

200

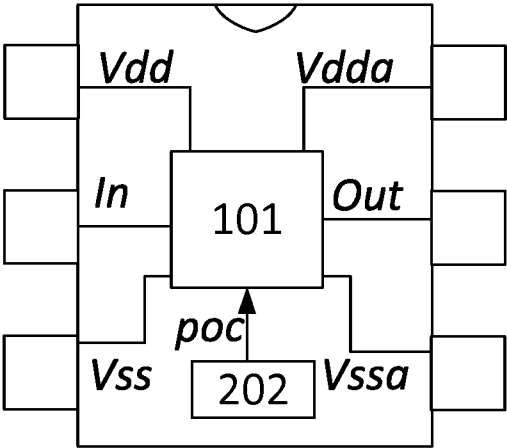


Fig. 4

300

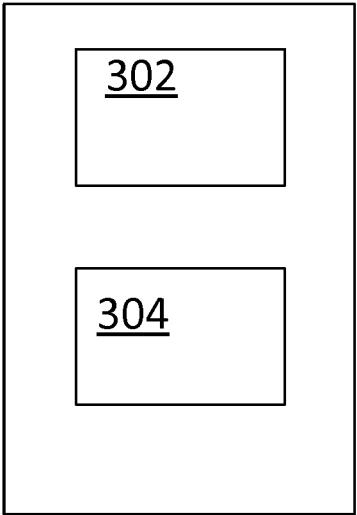


Fig. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/067993

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03K3/356 H03K19/00 H01L21/8238
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/143418 A1 (LU LEE-CHUNG [TW] ET AL) 19 June 2008 (2008-06-19)	1-7
Y	abstract; figure 2 paragraphs [0002], [0004], [0005], [0013], [0017], [0-19]	8,9
Y	----- US 2010/219800 A1 (FUKUOKA KAZUKI [JP] ET AL) 2 September 2010 (2010-09-02)	8,9
A	abstract; figures 1,4,6,20 paragraphs [0169], [0172]	1,4-7
A	----- US 3 916 430 A (HEUNER ROBERT CHARLES ET AL) 28 October 1975 (1975-10-28) abstract; figures 1,3 column 1, line 15 - column 2, line 29 column 4, line 1 - line 30 ----- -/-	1,2,4-7



Further documents are listed in the continuation of Box C.



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Date of the actual completion of the international search

24 September 2019

Date of mailing of the international search report

09/10/2019

Name and mailing address of the ISA/

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Authorized officer

Mesic, Maté

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/067993

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7 205 820 B1 (YEUNG SALLY [CA] ET AL) 17 April 2007 (2007-04-17) abstract; figures 3,6a,6b -----	1,4-8
A	US 2005/285623 A1 (JAHAN MIRZA M [US] ET AL) 29 December 2005 (2005-12-29) abstract; figures 1,6 -----	1,4-8

INTERNATIONAL SEARCH REPORT

Information on patent family members

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