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(54) Title: USING ZEOLITES TO IMPROVE THE MECHANICAL STRENGTH OF LOW-K INTERLAYER DIELECTRICS

(57) Abstract: A method for impregnating the pores of a zeolite low-k dielectric layer with a polymer, and forming an interconnect structure therein, thus mechanically strengthening the dielectric layer and preventing metal deposits within the pores.

USING ZEOLITES TO IMPROVE THE MECHANICAL STRENGTH OF LOW-K INTERLAYER DIELECTRICS

5 BACKGROUND

[001] Silica films, such as SiO₂, are used in the microelectronics industry as dielectrics. A dielectric is described by its dielectric constant, more commonly known as the k-value of the dielectric. Dielectrics are used to isolate metal lines or layers from one another. Using a dielectric with a low dielectric constant helps to
10 lessen crosstalk, the undesired capacitive or inductive interaction of one part of the circuit to another. As device density on integrated circuits increases, the metal lines become smaller, and the distance between metal layers decreases. As device geometries decrease, crosstalk effects become significant. Crosstalk effects can be reduced by lowering the k-value of the dielectric. Current technology uses
15 dielectrics with a k-value between 2.5 and 4.0.

[002] Silica has a dielectric constant of about 4.0, which is too high to be useful for next generation integrated circuits. Since air has a dielectric constant of 1.0, one way to lower the dielectric constant of silica is to incorporate voids or pores into the silica. There are several drawbacks to using this approach in an
20 integrated circuit manufacturing process. First, porous dielectrics are generally not mechanically stable enough to support subsequent polishing operations. Additionally, the porous dielectric may allow transport of metal through the dielectric layer.

25 [003] BRIEF DESCRIPTION OF THE DRAWINGS

[004] A better understanding of the present invention can be obtained from the following detailed description in conjunction with the following drawings, in which:

[005] **Figure 1** is an illustration of a graph showing the mechanical strength of low-k dielectric materials as a function of dielectric constant.

[006] **Figure 2** is an illustration of hexagonal, lamellar, and cubic mesoporous materials.

5 [007] **Figure 3** is an illustration of a cross section of a damascene opening in a porous zeolite.

[008] **Figures 4A - 4B** are flow diagrams illustrating processes according to embodiments of the present invention.

10 [009] **Figures 5A - 5G** are illustrations of cross sections of a zeolite dielectric layer according to embodiments of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0010] The terms chip, integrated circuit, monolithic device, semiconductor
15 device, and microelectronic device, are often used interchangeably in this field. The present invention is applicable to all of the above as they are generally understood in the field.

[0011] The terms contact and via both refer to structures for electrical connection of conductors from different interconnect levels. These terms are sometimes used
20 in the art to describe both an opening in an insulator in which the structure will be completed, and the completed structure itself. For purposes of this disclosure, contact and via refer to the completed structure.

[0012] The expression low dielectric constant material refers to materials having a lower dielectric constant than silicon dioxide, which has a dielectric constant of 4.
25 For example, organic polymers, amorphous fluorinated carbons, nanofoams,

silicon based insulators containing organic polymers, carbon doped oxides of silicon and fluorine doped oxides of silicon have lower dielectric constants than silicon dioxide.

[0013] The letter k is often used to refer to dielectric constant. Similarly, the terms
5 high-k and low-k are used in this field to refer to high dielectric constant and low dielectric constant respectively, where high means greater than the dielectric constant of silicon dioxide, and low means lower than the dielectric constant of silicon dioxide.

[0014] The parasitic capacitance seen by an interconnect line is a function of the
10 distance to another conductor and the dielectric constant of the material between the conductors. However, increasing the spacing between interconnect lines increases the physical size, and thus the cost, of an integrated circuit. Therefore, in order to manufacture integrated circuits with low parasitic capacitance between interconnect lines, it is desirable to electrically isolate the conductors from each
15 other with an insulator having a low dielectric constant.

[0015] One way to reduce the adverse effects of parasitic capacitance is to use low-k materials as insulators in advanced microelectronics. To achieve low dielectric constants, one can introduce porosity into the dielectric film. While increasing the porosity of a dielectric lowers the k-value of the film, it also lowers the mechanical
20 strength of the film. Figure 1 is a graph (100) which illustrates the modulus of a film as a function of k-value for three low-k dielectric films: carbon-doped oxide (CDO), silicon dioxide (SiO₂), and fluorinated silicon oxide (SiOF). As the porosity of the dielectric increases, the k-value decreases, and the modulus or

mechanical strength of the film decreases as well, thus making it more difficult to integrate these porous dielectrics into the semiconductor manufacturing process.

[0016] Because of their ordered nature, zeolites have significantly higher strengths than porous silicon oxide based materials such as porous SiO₂, SiOF, and CDO. A

5 zeolite is characterized by a high degree of ordered porosity, a high mechanical strength, and a low k-value. Figure 2 illustrates images of porous zeolite structures 200 and their corresponding transmission electron micrographs 202.

Hexagonal 210, 212 and lamellar 220, 222 structures are closed systems that do not allow transport of materials through the surface of the film. Cubic structures 230,

10 232 have channels running through the entire film that allow transport to and from the surface.

[0017] The inherent porosity and permeability of zeolite dielectric layers poses significant integration challenges when using these porous dielectrics in the semiconductor manufacturing process. Chemical uptake may occur during etch

15 or clean, significantly increasing the dielectric constant. Porosity may compromise the integrity of the metal barrier layer, leading to poor gap fill and interline leakage. Finally, permeability and ion-exchange properties can result in trapping of mobile ions, catalysts of undesirable reactions during barrier atomic layer deposition (ALD).

20 [0018] Figure 3 illustrates a cross sectional view of a porous zeolite low-k dielectric layer in a semiconductor interconnect structure. A porous zeolite layer (302) containing pores (304) is formed on an etch stop layer (306) and an underlying semiconductor substrate (300). The substrate is typically a wafer upon

which other semiconductor manufacturing operations have been performed to form various electrical components, including, but not limited to transistors and conductive interconnections. The etch stop layer may comprise silicon nitride, silicon carbide, or another material.

5 [0019] Damascene or dual damascene openings (308), which may include trench (308A) and/or via (308B) openings are formed in the porous zeolite layer.

Trenches (308A) are formed in the zeolite layer (302), while via openings (308B) are formed through both the zeolite layer (302) and etch stop layer (306). A metal barrier layer (310) is formed over the damascene openings. The metal barrier
10 layer may be formed by chemical vapor deposition (CVD) or by atomic layer deposition (ALD).

[0020] When the metal barrier layer is deposited over the porous zeolite layer, metal deposits may be formed inside of the pores (312). This may lead to electrical shorts and/or a low breakdown voltage for the dielectric.

15 [0021] By impregnating the pores of the zeolite layer with a second low-k dielectric, the internal pores of the zeolite may be sealed, yet the zeolite layer will retain its desirable mechanical and low-k properties.

[0022] Figure 4A is a flow diagram illustrating a process in accordance with one embodiment of the present invention. First, as illustrated in block 402, a porous
20 zeolite low-k dielectric layer is formed on a substrate. The zeolite may be synthesized either *in situ* on the wafer via spin-coating and subsequent calcination, or *a priori* as a nanoparticle suspension followed by calcination.

[0023] Next, as shown in block 404, the zeolite is impregnated with another low-k material. The low-k material may be a spin-on or plasma-deposited monomer or polymer, or may be another low-k material which is able to penetrate the pores of the zeolite. Alternately, the low-k material may be a polymer which is dissolved
5 in another material, or may be a polymer which is part of a mixture with another material. Impregnation of the zeolite by the low-k material may be either complete or partial.

[0024] Once the pores of the zeolite have been partially or completely filled with a polymer or other low-k material, a damascene or dual damascene opening may be
10 formed in the zeolite layer, as shown by block 406.

[0025] Next, as shown in block 408, a barrier layer metal may be formed over the damascene opening and the zeolite layer. In one embodiment, the barrier layer metal may be comprised of copper or an alloy of copper.

[0026] After the barrier layer metal has been formed, the damascene opening may
15 be filled with a metal, such as, but not limited to copper or a copper alloy as shown in block 410. Thus, a damascene or dual damascene interconnect structure is formed.

[0027] After the dual damascene structures are formed, excess copper and barrier layer material may be removed, typically by a chemical mechanical polishing
20 (CMP) process, as illustrated in block 412. Although dual damascene structures are described, damascene or other interconnect structures may be formed within the zeolite dielectric layer as well.

[0028] Figure 4B is a flow diagram illustrating a process in accordance with another embodiment of the present invention. In this embodiment, the zeolite layer may be formed using a zeolite nanoparticle/low-k precursor suspension applied directly to the wafer, as illustrated by block 452. Next, the suspension
5 may be treated to form a polymer impregnated zeolite layer, as shown in block 454. In one embodiment, calcination may be used to treat the suspension.

Calcination of the suspension will allow the low-k precursor to polymerize within the pores of the zeolite. Using this method, the zeolite nanoparticles can be prepared with a significantly lower k-value ($k < 2.0$) than fully dense silica ($k =$
10 3.9).

[0029] After the suspension has been treated to form a zeolite layer having polymer-impregnated pores, subsequent processing may occur, including formation of a damascene or dual damascene opening in the zeolite layer (block 456), formation of a barrier metal layer over the damascene opening and the
15 zeolite layer (block 458), filling the damascene opening with a metal (block 460), and polishing the top surface of the metal (block 462). Each of these processes is described in greater detail above, in conjunction with Fig. 4A.

[0030] Figures 5A through 5G illustrate cross-sectional views of a zeolite dielectric layer formed in accordance with embodiments of the process set forth in Figure 4
20 and described above.

[0031] Figure 5A illustrates a porous zeolite layer (504) having pores (505) formed on a substrate (502). The porous zeolite layer (504) is exposed to a low-k polymer precursor (506). The zeolite layer (504) may be impregnated with the

precursor (506) using vapor, liquid, or supercritical fluid exposure. One appropriate precursor which may be used is divinyl siloxane-benzocyclobutene (DVS-BCB), which forms a low-k siloxane-organic hybrid polymer upon polymerization. Another group of precursors which may be used are the CDO
5 related precursors, which form a low-k silicon dioxide-based dielectric. In one embodiment, the polymer precursor may be dissolved in another material, or may be part of a mixture with another material.

[0032] Polymerization of the precursor (506) may be initiated via thermal, plasma, or other means to facilitate polymerization during or subsequent to the
10 impregnation process. In one embodiment, polymerization may be initiated by applying heat to the zeolite layer and the polymer precursor. In another embodiment, polymerization may be initiated by exposing the zeolite layer and the polymer precursor to a plasma.

[0033] In another embodiment, illustrated in Figure 5B, the pores (505) of porous
15 zeolite (504) may be directly impregnated with a long-chain, non-crosslinked polymer (507), such as paralyene, poly(arylene ether)s (such as FLARE™ from Honeywell), polyphenylene derivatives (such as a non-crosslinked version of SiLK™ from Dow Chemical), or another thermally robust, low-k dielectric material. Impregnation may be performed in either liquid or supercritical
20 solution, to enhance diffusion of the polymer into the zeolite structure. In one embodiment, the polymer may be dissolved in another material, or may be part of a mixture with another material.

[0034] In another embodiment, the zeolite may be impregnated by using a hybrid method in which a macromonomer, such as oligomeric polyphenylene, is introduced into the zeolite matrix and then subsequently reacted to form a crosslinked network. The ability to modify the chemical properties of the zeolite host over a wide range by using specific additives makes it possible to tailor the zeolite to specific applications.

[0035] Figure 5C illustrates the zeolite layer (508) on a substrate (502) after the pores have been partially or fully impregnated with a polymer or other low-k material (510). Because the pores of the zeolite have been filled with a low-k polymer, the zeolite is more mechanically robust. The polymer-filled zeolite layer may act as mechanical reinforcement for the interlayer dielectric (ILD) stack during subsequent process operations. Also, because the k-value of both the zeolite and the polymer is low, the k-value of the resulting stack will be low.

[0036] Figure 5D illustrates the polymer-filled zeolite layer (508) after a damascene opening (512) has been formed. The damascene opening (512) may include a via region (512B) and a trench region (512A), and may be formed by photolithography and etch operations. Because the pores of the zeolite are sealed by the polymer (510), chemical uptake, ion exchange, and catalysis are prevented during the photolithography, etch, and subsequent operations.

[0037] Next, as shown in Figure 5E, a metal barrier layer (514) is formed over the damascene openings. The metal barrier layer may be formed by chemical vapor deposition (CVD) or by atomic layer deposition (ALD). Because the pores of the zeolite (508) are filled by a polymer (510), the barrier metal may not penetrate the

zeolite layer. Thus, metal deposits may not form in the pores, and the resulting zeolite ILD layer may be more electrically robust.

[0038] Figure 5F illustrates the structure of Figure 5E after the damascene opening (512) is filled with a metal (516). In one embodiment, the metal is copper or a copper alloy. The metal (516) forms copper interconnects, creating damascene or dual damascene interconnect structures.

[0039] After the damascene or dual damascene structures are formed, excess copper and barrier layer material is removed, typically by a chemical mechanical polishing (CMP) process. The resulting structure is illustrated in Figure 5G.

Damascene or dual damascene structures (520) are formed within a zeolite layer having polymer filled pores. The polymer-filled zeolite (508) may act as a mechanical reinforcement for the inter-layer dielectric (ILD) stack during the CMP process and subsequent manufacturing operations.

[0040] Thus, as described above, a porous zeolite ILD may be impregnated with a second low-k dielectric, such as a polymer, so as to seal the internal pores of the zeolite. The resulting structure may have a greater mechanical strength than a porous zeolite, because the pores have been filled with a polymer. Additionally, the k-value of the resulting structure may remain low because both the zeolite and polymer are low-k materials.

[0041] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth herein. The

specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.

IN THE CLAIMS

We claim:

- 5 1. A method comprising:
forming a zeolite layer on a substrate, wherein the zeolite layer contains
pores;
impregnating the pores of the zeolite layer with a polymer to form a polymer
impregnated zeolite layer;
10 forming an opening in the polymer impregnated zeolite layer; and
forming a barrier layer over the damascene opening and the polymer
impregnated zeolite layer.
2. The method of claim 1, wherein impregnating the pores of the zeolite layer
15 with a polymer comprises exposing the zeolite layer to a polymer precursor and
subsequently initiating polymerization.
3. The method of claim 2, wherein the polymer precursor is selected from a
group consisting of divinyl siloxane-benzocyclobutene (DVS-BCB), and carbon
20 doped oxide (CDO).
4. The method of claim 2, wherein the polymer precursor is in vapor form.
5. The method of claim 2, wherein the polymer precursor is in liquid form.
25
6. The method of claim 2, wherein the polymer precursor is in supercritical
fluid form.

7. The method of claim 2, wherein the polymer precursor is dissolved in another material.

8. The method of claim 2, wherein the polymer precursor is part of a mixture
5 with another material.

9. The method of claim 2, wherein initiating polymerization comprises heating the zeolite layer and the polymer precursor.

10 10. The method of claim 2, wherein initiating polymerization comprises exposing the zeolite layer and the polymer precursor to a plasma.

11. The method of claim 1, wherein impregnating the pores of the zeolite layer with a polymer comprises exposing the zeolite layer to the polymer.

15

12. The method of claim 11, wherein the polymer is a liquid.

13. The method of claim 11, wherein the polymer is a supercritical solution.

20 14. The method of claim 11, wherein the polymer is dissolved in another material.

15. The method of claim 11, wherein the polymer is part of a mixture with another material.

25

16. The method of claim 11, wherein the polymer comprises a long-chain, non-crosslinked polymer.

17. The method of claim 16, wherein the polymer is selected from a group consisting of paralyene, poly(arylene ether)s, and polyphenylene derivatives.

18. The method of claim 1, wherein the barrier layer comprises a layer of metal.

5

19. The method of claim 1, further comprising filling the opening with a metal layer.

20. The method of claim 19, further comprising polishing the metal layer

10

21. The method of claim 19, wherein the metal layer comprises a copper alloy.

22. A method comprising:

applying a zeolite-nano particle precursor suspension to a substrate;

15

treating the suspension to form a polymer impregnated zeolite layer;

forming an opening in the polymer impregnated zeolite layer; and

forming a barrier layer over the opening and the polymer impregnated zeolite layer.

20

23. The method of claim 22, wherein treating the suspension to form a polymer impregnated zeolite layer comprises calcining the suspension.

24. The method of claim 22, wherein the barrier layer comprises a layer of metal.

25

25. The method of claim 22, further comprising filling the opening with a metal layer.

26. The method of claim 25, further comprising polishing the metal layer

27. The method of claim 25, wherein the metal layer comprises a copper alloy.

28. An interconnect structure comprising:

5 a via and a trench defined by a polymer impregnated zeolite dielectric layer,
which is disposed above an underlying layer;

a barrier layer disposed on the surface of the polymer impregnated zeolite
dielectric; and

a conductive material disposed in the via opening and in the trench.

10

29. The interconnect structure of claim 28, wherein the barrier layer is a metal
layer.

30. The interconnect structure of claim 28, wherein the conductive material

15 comprises a copper alloy.

31. The interconnect structure of claim 28, wherein the underlying layer is a
semiconductor substrate.

20 32. The interconnect structure of claim 31, further comprising an etch stop layer
formed over the conductive material.

33. The interconnect structure of claim 32, wherein the etch stop layer comprises
a silicon carbide layer.

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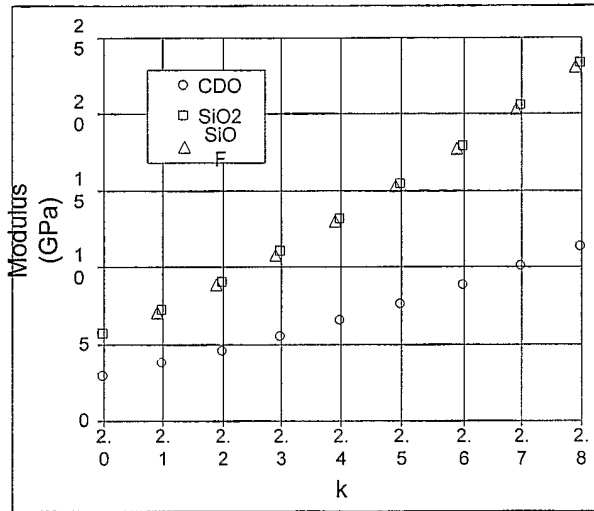


FIG. 1

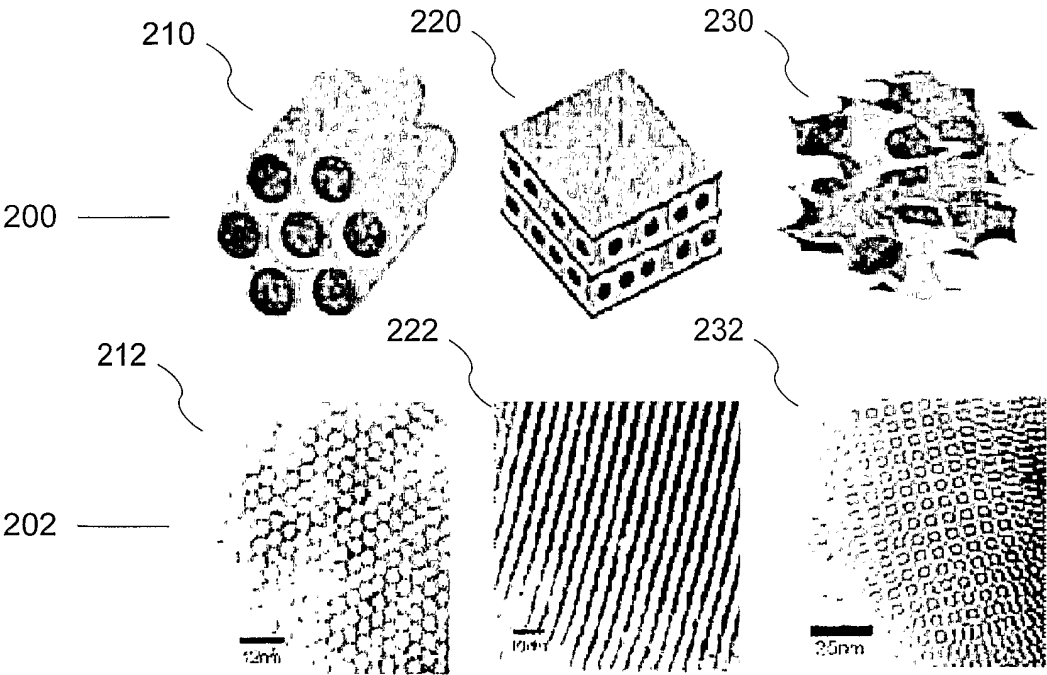


FIG. 2
(Prior Art)

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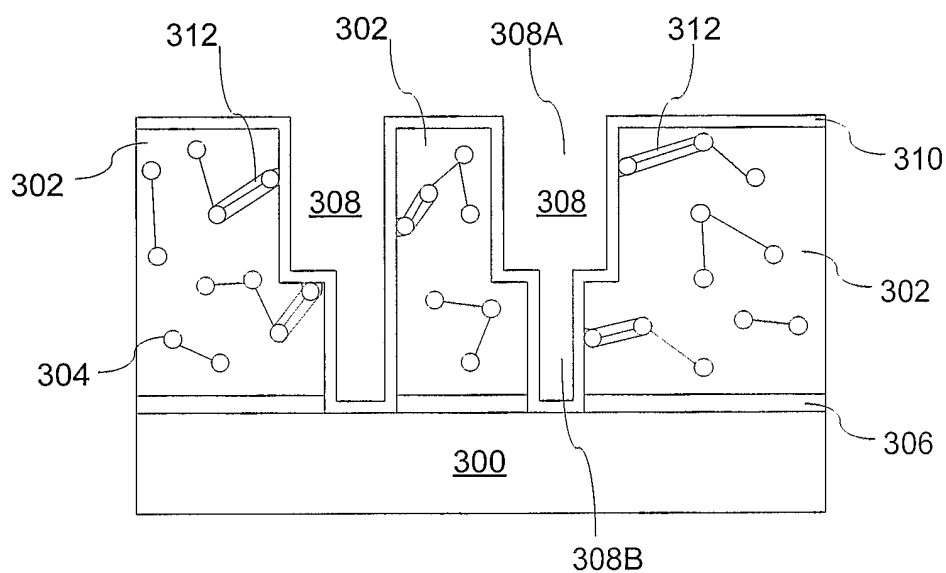


FIG. 3

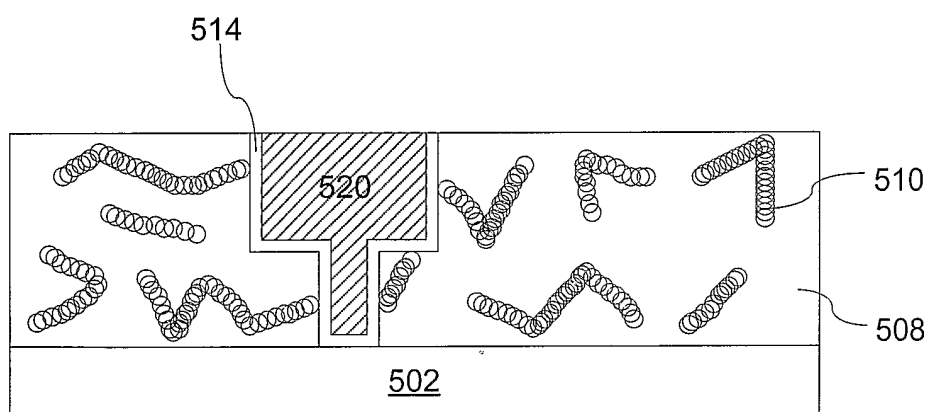


FIG. 5G

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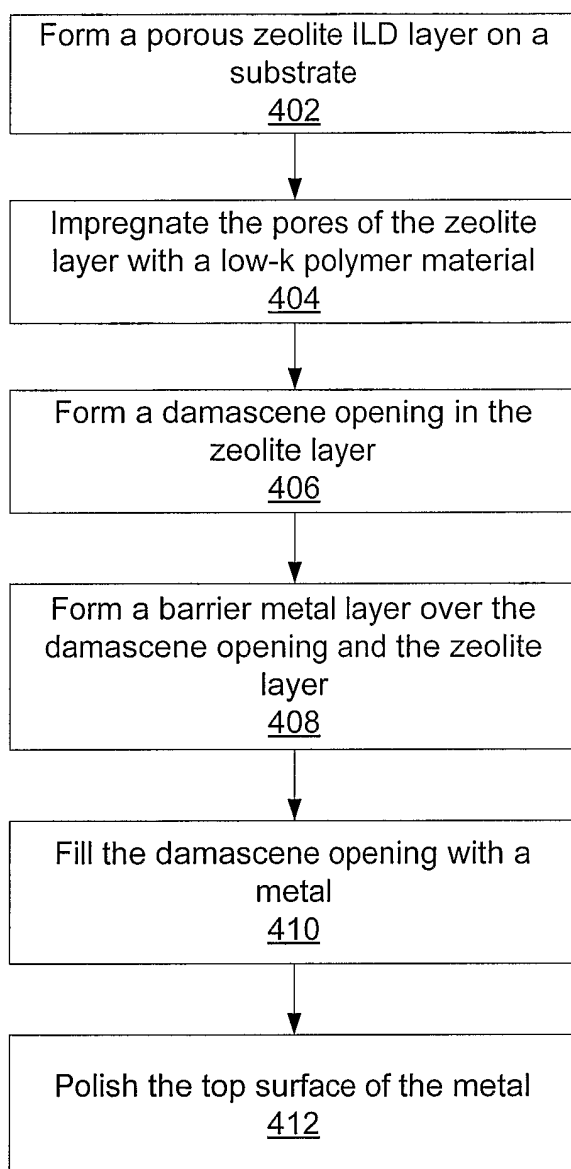


FIG. 4A

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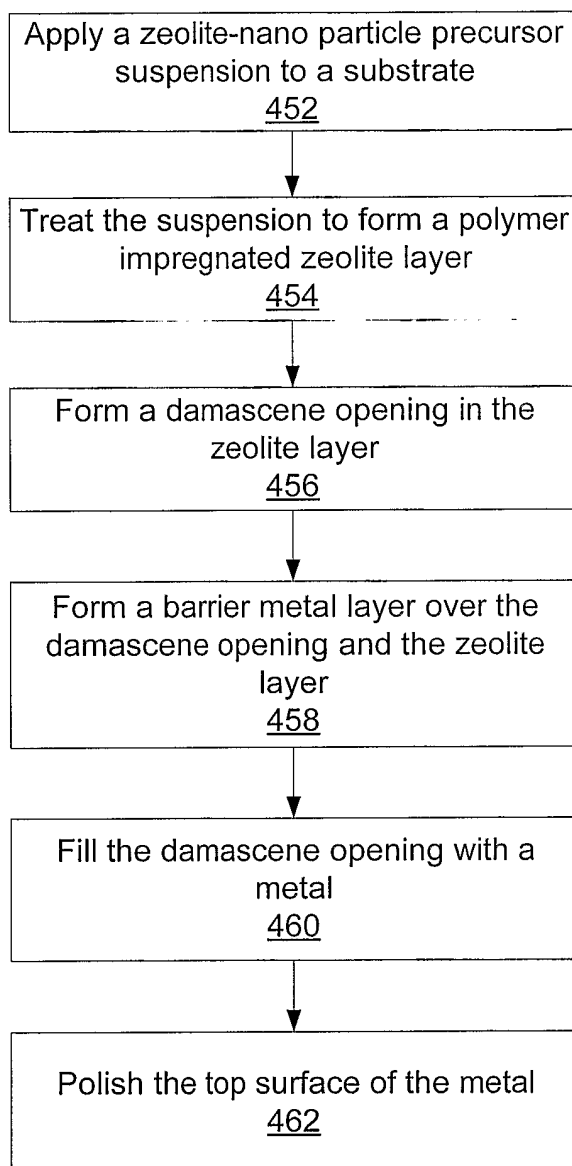


FIG. 4B

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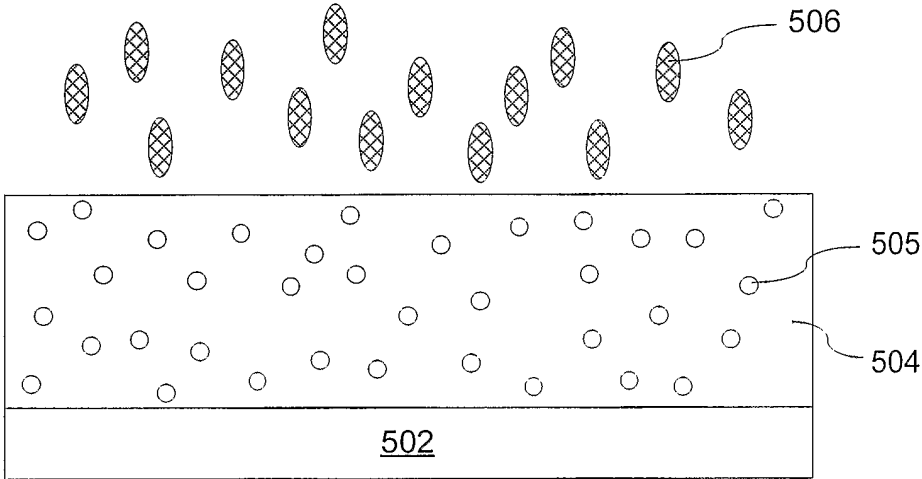


FIG. 5A

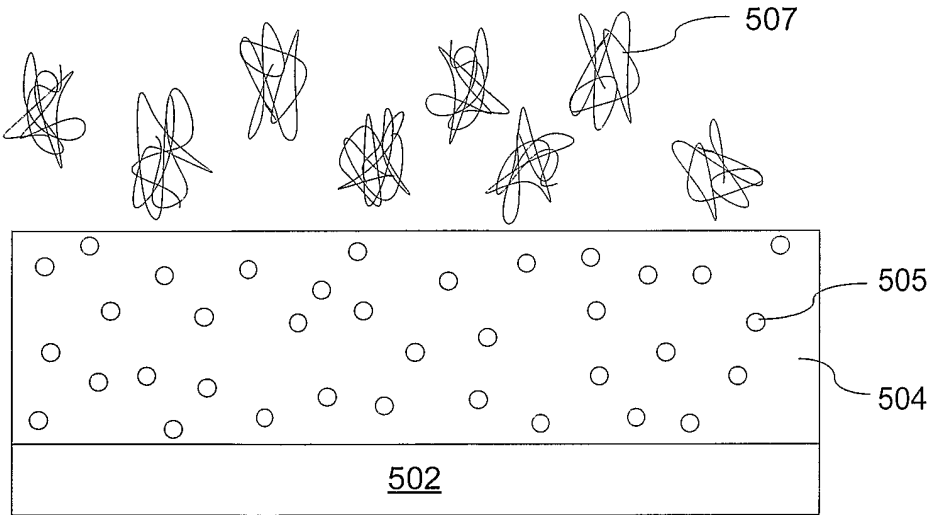


FIG. 5B

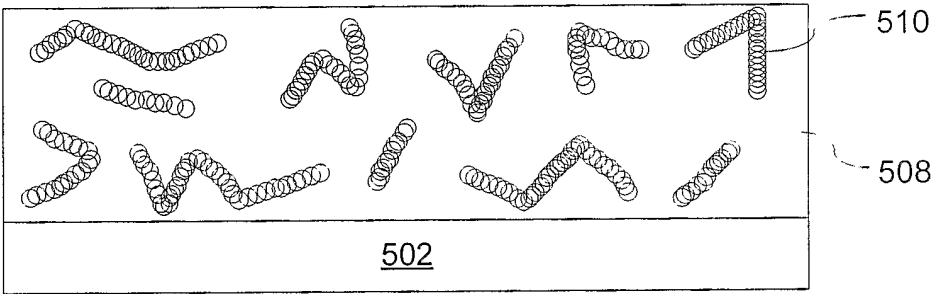


FIG. 5C

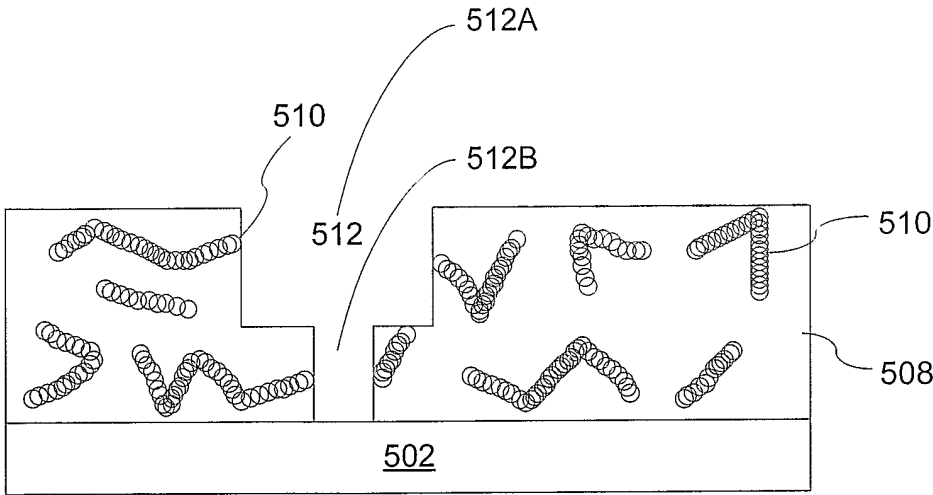


FIG. 5D

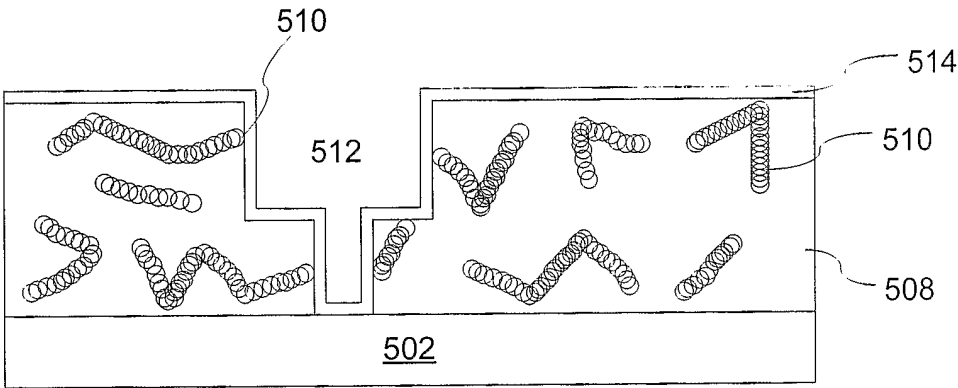


FIG. 5E

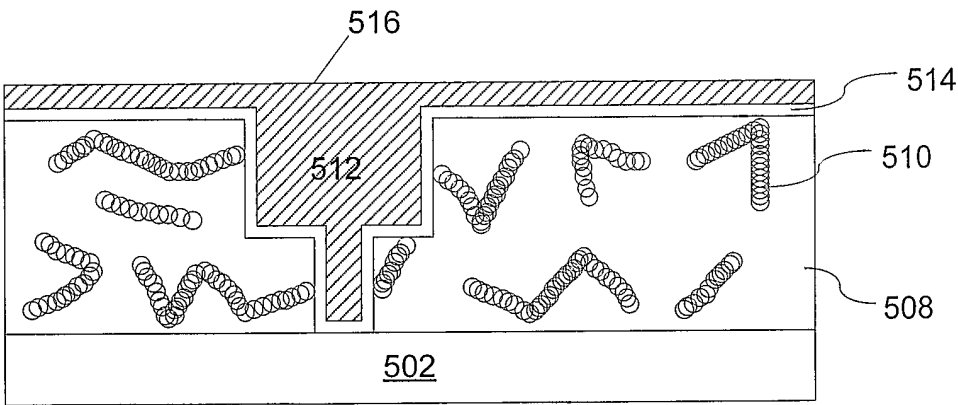


FIG. 5F