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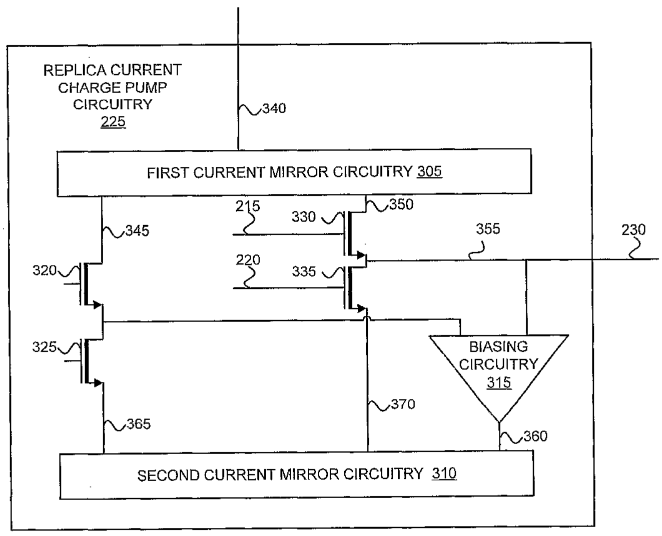
(54) Title: PHASE-LOCKED LOOP CIRCUITRY USING CHARGE PUMPS WITH CURRENT MIRROR CIRCUITRY



(57) Abstract: A system and method for performing phase-locked loop is disclosed. The system includes phase frequency detector circuitry, charge pump circuitry (225) having first current mirror circuitry (305) and second current mirror circuitry (310), loop filter circuitry, and voltage controlled oscillator circuitry. The phase frequency detector circuitry generates an up signal and a down signal based on the phase difference of an input signal and a feedback signal. The first and second current miroir circuitries (305, 310) replicate a refrence current (340). A biasing circuitry (315) is configured to generate a voltage for the first current miroir circuitry (310) based on a voltage bias to the second current mirror circuitry (310) based on a voltage for the first current mirror circuitry and the voltage of the circuitries to accurately replicate the reference current (340) at low power thereby providing current pulses of equal magnitude at low currents.

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PHASE-LOCKED LOOP CIRCUITRY USING CHARGE PUMPS WITH CURRENT MIRROR CIRCUITRY

RELATED APPLICATIONS

This application is a continuation of U.S. Application No. (unknown), filed October 31, 2005, which claims the benefit of U.S. Provisional Application No. 60/635,849, filed on December 13, 2004. The entire teachings of the above applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Technical Field

[0002] The present invention relates generally to phase-locked loop circuitry and more particularly to phase-locked loop circuitry using charge pumps with current mirror circuitry.

2. Description of Related Art

[0003] A phase-locked loop (PLL) is an electronic circuit with a voltage- or current-driven oscillator that is adjusted to match in phase (and thus lock on) the frequency of an input signal. In addition, PLLs are used to generate a signal, modulate or demodulate a signal, reconstitute a signal with less noise, and multiply or divide a frequency. PLLs are frequently used in wireless communications, particularly where signals are carried using amplitude modulation (AM), frequency modulation (FM) and phase modulation (PM). PLLs are more commonly used for digital data transmission, but can also be designed for analog information. Examples of applications for PLLs include frequency synthesizers for digitally-tuned radio receivers and transmitters, recovery of small signals that otherwise would be lost in noise lock-in amplifier, recovery of clock timing information from a data stream such as from a disk drive, clock multipliers, and dual-tone multi-frequency (DTMF) decoders, modems, and other tone decoders, for remote control and telecommunications.

[0004] FIG. 1 illustrates phase-locked loop (PLL) circuitry 100, according to the prior art. Phase-frequency detector (PFD) circuitry 110 generates an "up" signal 115 and a "down" signal 120 by comparing the phase difference of an input signal 105 to a feedback signal 160. The PFD circuitry 110 outputs the up signal 115 and the down signal 120 depending on whether or not the phase of the feedback signal 160 lags (needs to speed up) or leads (needs to slow down) when compared to the input signal 105. Charge pump circuitry 125 generates current pulses in a charge pump output signal 130 (e.g., to charge capacitors in loop filter circuitry 135) based on the up signal 115 and the down signal 120. The charge pump circuitry 125 generates the current pulses with a minimum pulse width. For example, when the input signal 105 and the feedback signal 160 have equal phase, the current pulses of the charge pump output signal 130 have equal width. With unequal phase, one of the current pulses of the charge pump output signal 130 is lengthened to correct the phase.

[0005] The loop filter circuitry 135 filters the charge pump output signal 130 and generates a filtered control signal 140. Voltage controlled oscillator (VCO) circuitry 145 generates an output signal 150 whose frequency is determined by the voltage of the filtered control signal 140. The PLL circuitry 100 loops the output signal 150 back to the PDF circuitry 110 as the feedback signal 160. Optionally, frequency divider circuitry 155 is placed in the feedback path of the loop to generate the feedback signal 160 and to allow the output signal 150 to be a multiple of the input signal 105.

[0006] One problem that arises with the PLL circuitry 100 is that the magnitude of the current pulses that charge the loop filter circuitry 135 (e.g., current pulses of the charge pump output signal 130) is dependent on a variety of voltage sources. Some examples upon which the current pulses depend are power supply voltages and the voltage of the filtered control signal 140. Also, if circuitry in the PLL circuitry 100 is terminated to voltages not equidistant from the voltage of the filtered control signal 140, the current pulses for the charge pump output signal 130 may not have equal magnitude. Having unequal magnitude in the current pulses, either from voltage variations or termination mismatch, results in static phase offsets in the output of the PLLs.

[0007] The magnitude of the independent current pulses may also be adjusted to set the desired loop bandwidth. The loop bandwidth is the measure of the ability of the PLL circuitry 100 to lock onto the input signal 105 and to handle jitter. A high loop bandwidth provides a fast lock time and tracks jitter on the input signal 105, passing the jitter through to the output signal 150. A low loop bandwidth filters out the jitter of the input signal 105, but increases the lock time of the PLL circuitry 100. Typically, for a given capacitor in the loop filter 140, a smaller current for the charge pump output signal 130 produces a lower loop bandwidth and a larger current for the charge pump output signal 130 produces a higher loop bandwidth.

[0008] When determining the ideal loop bandwidth, noise performance is an important consideration. In most PLLs, the two primary noise sources that exist are noise from the VCO circuitry 145 (VCO noise) and reference noise. Each source of noise has conflicting loop bandwidth requirements to minimize the effects of the noise. VCO noise is due to thermal and shot noise in the VCO circuitry 145 and affects the output signal 150. VCO noise is usually dominant and is reduced by increasing the loop bandwidth (i.e., increasing the current output from the charge pump circuitry 125) which allows the PLL circuitry 100 to track low frequency noise (i.e., noise below the loop bandwidth) and compensate for the effect of the low frequency noise on the output signal 150. Typically, VCO noise drops off rapidly at higher frequencies, so the noise remaining above the loop bandwidth generally has little effect on the output signal 150.

[0009] Reference noise has multiple contributors such as jitter on the input signal 105, thermal noise in the charge pump circuitry 125, and supply noise associated with the voltage of the filtered control signal 140. In integer PLLs with a clean input signal 105 (i.e., no jitter), increasing the loop bandwidth reduces the effect of the thermal noise in the charge pump circuitry 125, which reduces reference noise. However, if the input signal 105 is noisy, a high loop bandwidth allows more of the reference noise to pass through to the output signal 150. Similarly, in certain types of PLLs, known as a delta-sigma PLLs, the value of the feedback divider circuitry 155 may be varied dynamically, which produces noise similar to reference noise on a noisy input signal 105. The reference noise can dominate the VCO noise and therefore the minimum possible loop bandwidth is desired rather than increasing the loop bandwidth.

[0010] Two exemplary ways to minimize the loop bandwidth are to increase the size of capacitors used in the loop filter circuitry 135 and to decrease the magnitude of the current of the charge pump output signal 130. Because area is a major concern in many designs and large capacitors increase the area requirements, decreasing the magnitude of the current is usually chosen. To achieve loop bandwidths on the order of 100 kHz using integrated capacitors of a reasonable size, currents with magnitudes ranging down to 10s of nanoamps may be necessary. Reducing the magnitude of the current may reduce noise (e.g., reference noise), however, many other challenges arise when attempting to generate very low currents, especially in deep submicron technologies.

[0011] In particular, with nanoampere currents, such as those used in the delta-sigma PLLs, current mismatch due to the Early effect (i.e., reduction of the width of the base in bipolar transistor due to the widening of the base-collector junction with increasing base-collector voltage) can be significant depending on the value of the voltage for the filtered control signal. Moreover, the magnitude of device leakage in deep submicron technologies is often significantly larger than the actual signals being generated. Any mismatch between the currents in the up signal 115 and the down signal 120 caused by the device leakage results in the static phase offset between the input signal 105 and the output signal 160. Additionally, the mismatch generally requires one of the up signal 115 and the down signal 120 to be "on" for more than the minimum required time which allows more noise to be injected into the loop.

SUMMARY OF THE INVENTION

[0012] The invention addresses the above problems by providing a system and method for performing phase-locked loop. The system includes phase frequency detector circuitry, charge pump circuitry having a first current mirror circuitry and a second current mirror circuitry, loop filter circuitry, and voltage controlled oscillator circuitry. The phase frequency detector circuitry generates an up signal and a down signal based on the phase difference of an input signal and a feedback signal. The charge pump circuitry includes the first current mirror circuitry and the second mirror circuitry and generates a charge pump output signal based on the up and down signals. The loop filter circuitry generates a filtered control signal based on the charge pump output signal. The voltage controlled oscillator circuitry generates the feedback signal with a repeating waveform based on the filtered control signal. Advantageously, the system and method provide accurate current pulses to reduce static phase offset and provide a good resolution for tracking the input signal in the feedback signal. Another advantage is that the system and method provide good resolution for tracking the input signal at low power in submicron technologies.

[0013] To provide the accurate current pulses, the second current mirror circuitry of the charge pump circuitry may mirror a reference current of the first current mirror circuitry. Additionally, the charge pump circuitry may generate current pulses of substantially equal magnitude. Further, the system may include biasing circuitry that generates a voltage bias in the second current mirror circuitry. The biasing circuitry may comprise an operational amplifier. The biasing circuitry may generate the voltage bias based on a voltage for the first current mirror circuitry and a voltage for the charge pump output signal. Generating the voltage bias can provide current pulses of substantially equal magnitude at low currents.

[0014] In some embodiments, one of the first current mirror circuitry and the second current mirror circuitry further comprises current mirror output circuitry having a plurality of current outputs of differing magnitude. The plurality of current outputs may provide one or more loop bandwidths. Programmable loop bandwidth circuitry may select one of the plurality of current outputs to determine the loop bandwidth. Further, leakage compensation circuitry may reduce off-state leakage from the current mirror output circuitry to the charge pump output signal. The leakage compensation circuitry may also include a third current mirror circuitry configured to receive the off-state leakage and transfer the off-state leakage to the current mirror output circuitry.

[0015] In further embodiments, current pulse circuitry generates up current pulses and down current pulses in the charge pump output signal from the first current mirror circuitry and the second current mirror circuitry, respectively. Pulse leakage isolation circuitry may reduce off-state leakage from the pulse circuitry to the charge pump output signal. In one aspect, reducing the off-state leakage comprises producing a first voltage across the pulse circuitry substantially equal to a second voltage for the charge pump output signal. Additionally, charge compensation circuitry may reduce charge transfer from the pulse circuitry to the charge pump output signal.

[0016] In some embodiments, power-on circuitry generates a turn-on voltage for the filtered control signal. Power-on leakage isolation circuitry may reduce off-state leakage from the power-on circuitry to the filtered control signal. Advantageously, the power-on circuitry is large enough to start the system with little or no leakage during normal operation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. 1 illustrates phase-locked loop circuitry according to the prior art;

[0018] FIG. 2 illustrates phase-locked loop circuitry with current replica charge pump circuitry in an exemplary implementation of the invention;

[0019] FIG. 3 illustrates the current replica charge pump circuitry in an exemplary implementation of the invention;

[0020] FIG. 4 illustrates a programmable current mirror digital to analog converter (PCMDAC) in an exemplary implementation of the invention;

[0021] FIG. 5 illustrates a leakage compensated PCMDAC in an exemplary implementation of the invention;

[0022] FIG. 6 illustrates power-on leakage isolation circuitry in an exemplary implementation of the invention;

[0023] FIG. 7 illustrates current pulse leakage isolation circuitry in an exemplary implementation of the invention; and

[0024] FIG. 8 illustrates charge compensated current pulse leakage isolation circuitry in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0025] The embodiments discussed herein are illustrative of one example of the present invention. As these embodiments of the present invention are described with reference to illustrations, various modifications or adaptations of the methods and/or specific structures described may become apparent to those skilled in the art. All such modifications, adaptations, or variations that rely upon the teachings of the present invention, and through which these teachings have advanced the art, are considered to be within the scope of the present invention. Hence, these descriptions and drawings should not be considered in a limiting sense, as it is understood that the present invention is in no way limited to only the embodiments illustrated.

[0026] A circuit implementation of the principles disclosed may be implemented using PMOS transistors alone, NMOS transistors alone, parallel combinations of PMOS and NMOS transistors, or other types of transistors. In some embodiments, the parallel combinations may be preferred to result in improved charge compensation. Additionally, current mirror circuitry may have multiple possible transistor implementations.

[0027] FIG. 2 illustrates phase-locked loop (PLL) circuitry 200 with replica current charge pump circuitry 225 in an exemplary implementation of the invention. The PLL circuitry 200 includes phase-frequency detector (PFD) circuitry 210, the replica current charge pump circuitry 225, loop filter circuitry 235, voltage controlled oscillator (VCO) circuitry 245, and frequency divider circuitry 255. The PFD circuitry 210 receives an input signal 205 and a feedback signal 260 and generates an "up" signal 215 and a "down" signal 220. The replica current charge pump circuitry 225 receives the up signal

215 and the down signal 220 and generates a charge pump output signal 230. The loop filter circuitry 235 receives the charge pump output signal 230 and generates a filtered control signal 240. The VCO circuitry 245 receives the filtered control signal 240 and generates an output signal 250. The frequency divider circuitry 255 receives the output signal 250 and generates the feedback signal 260.

[0028] The PFD circuitry 210 comprises any device, component, or circuitry configured to generate the up signal 215 and the down signal 220 based on the phase difference of the input signal 205 and the feedback signal 260. The replica current charge pump circuitry 225 comprises any device, component, or circuitry configured to replicate a reference current in first current mirror circuitry and second current mirror circuitry and generate the charge pump output signal 230 based on the up signal 215 and the down signal 220. One example of the replica current charge pump circuitry 225 is described below in FIG. 3.

[0029] The loop filter circuitry 235 comprises any device, component, or circuitry configured to filter the charge pump output signal 230 and generate a filtered control signal 240. The VCO circuitry 245 comprises any device, component, or circuitry configured to generate the output signal 250 with a repeating waveform based on the voltage of the filtered control signal 240. The frequency divider circuitry 255 comprises any device, component, or circuitry configured to multiply and/or divide the frequency of the output signal 250 and generate the feedback signal 260.

[0030] FIG. 3 illustrates the replica current charge pump circuitry 225 in an exemplary implementation of the invention. The replica current charge pump circuitry 225 includes first current mirror circuitry 305, second current mirror circuitry 310, biasing circuitry 315, a replica switch 320, a replica switch 325, an up signal switch 330, and a down signal switch 335.

[0031] The first current mirror circuitry 305 receives a reference current 340 and has a first output 345 linked to the replica switch 320. The first current mirror circuitry 305 also has a second output 350 linked to the up signal switch 330. The second current mirror circuitry 310 is linked to the biasing circuitry 315 via an input 360 and has a first output 365 linked to the replica switch 325. The second current mirror circuitry 310 also has a second output 370 linked to the down signal switch 335. The replica switch 320 is linked to the replica switch 325. The up signal switch 330 is linked to the down signal switch 335. The biasing circuitry 315 is further linked to the connection between the replica switches 320 and 325, and to the line 355. The gates of the replica switches 320 and 325 are enabled (i.e., the switch is always closed). The up signal 215 (FIG. 2) is linked to the gate of the up signal switch 330. The down signal 220 (FIG. 2) is linked to the gate of the down signal switch 335. The up signal switch 330 and the down signal switch generate the charge pump output signal 230 (FIG. 2) on line 355.

[0032] The first current mirror circuitry 305 comprises any device, component, or circuitry configured to replicate a reference current on one or more current mirror outputs. For example, the first current mirror circuitry 305 replicates the reference current 340 on the output 345 and the output 350. The second current mirror circuitry 310 comprises any device, component, or circuitry configured to replicate a reference current on one or more current mirror outputs. For example, the second current mirror 310 replicates the current received from the biasing circuitry 315 on the output 365 and the output 370. The biasing circuitry 315 comprises any device, component, or circuitry configured to generate a voltage bias in current mirror circuitry. One example of the biasing circuitry 315 is an operational amplifier.

[0033] During operation, the biasing circuitry 315 forces the first output 365 and the second output 370 of the second current mirror circuitry 310 to the same voltage of the charge pump output signal 230 on the line 355. The voltage bias produced by the biasing circuitry 315 results also in the first current mirror circuitry 305 having an identical and/or similar voltage bias condition as the charge pump output signal 230 on the line 355. Since there is negligible loading on the up signal switch 330 and the down signal switch 335, all the current from the reference current 340 flows through the second current mirror circuitry 310. The second output 370, if enabled by the down signal switch 335, will have an identical current as the second output 350 of the first current mirror circuitry 305 for any given voltage.

[0034] Therefore, the replica current charge pump circuitry 225 provides equal magnitude current pulses for the charge pump output signal 230 when enabled by the up signal 215 and the down signal 220. The voltage bias provided by the biasing circuitry 315 removes the effect of the voltage of the charge pump output signal 230 on the accuracy of the first current mirror circuitry 305 and the second current mirror circuitry 310 to generate the current pulses. The voltage bias provided by the biasing circuitry 315 further allows the first current mirror circuitry 305 and the second current mirror circuitry 310 to accurately replicate the reference current 340 at low power thereby providing the current pulses of equal magnitude at low currents. Accurately producing current pulses of equal magnitude prevents noise from propagating from the replica current charge pump circuitry 225 to the loop filter 235, and eventually to the

VCO 245 where the noise causes offsets in the output signal 250. Additionally, replicating the current pulses with equal magnitude reduces mismatch. Furthermore, any mismatch between currents pulses for the up signal 215 and the down signal 220 is now determined by the basic mismatch between the first current mirror circuitry 305 and the second current mirror circuitry 310 under essentially identical voltage bias conditions.

[0035] In some embodiments, a large current in the charge pump output signal 230 is required relative to the magnitude of the reference current 340. For example, large divider values in the feedback divider circuitry 255 (FIG. 2) require a relatively large current. One or more currents of differing magnitude, including a relatively large current, may be provided from the reference current 340 through a programmable current mirror digital to analog converter coupled to one of the first current mirror circuitry 305 and the second current mirror circuitry 310.

[0036] FIG. 4 illustrates a programmable current mirror digital to analog converter (PCMDAC) 400 in an exemplary implementation of the invention. The PCMDAC 400 includes an input switch 410, converter outputs 420, 430, and 440, and converter selectors 450, 460, and 470. A reference current 480 is linked to the input switch 410. The reference current 480 further is linked to the gate of the input switch 410. The input switch 410 is linked to the converter outputs 420, 430, and 440. The reference current 480 is also linked to the gates of the converter outputs 420, 430, and 440. The converter output 420 is linked to the converter selector 450. The converter output 430 is linked to the converter selector 460. The converter output 440 is linked to the converter selector 470. Each of the converter selectors 460, 470, and 480 are linked to form a converter output signal 490.

[0037] The converter outputs 420, 430, and 440 comprise any device, component, or circuitry configured to provide currents of differing magnitude from the reference current 480. In one example, the PCMDAC 400 receives the reference current 480 from current mirror circuitry (e.g., via the second output 350 of the first current mirror circuitry 305). The digital input to the converter selectors 460, 470 and 480 is a binary value M where M = [magnitude of converter output 430 x 2^0] + [magnitude of converter output 440 x 2^1] + [magnitude of converter output 450 x 2^2]. The converter outputs 420, 430, and 440 are binary weighted multiples of the reference current 480 in series with the converter selectors 450, 460, and 470, respectively. Therefore, the converter output signal 490 is a multiple of M times the reference current 480. This principle may be extended to large numbers of bits with the accuracy of the PCMDAC 400 limited by the matching of the individual converter outputs and converter selectors which have similar bias conditions.

[0038] The input switch 410 in the PCMDAC 400 may be a single unit (N=1), such that the converter output signal 490 equals M times the reference current 480. The input switch 410 may provide a larger unit such that the converter output signal 490 equals M/N times the reference current 490. In some embodiments, generating arbitrary functions are possible for the converter output signal 490 where the converter outputs 420, 430, and 440 are not binary weighted.

[0039] Used in the replica current charge pump circuitry 225 (FIG. 2), the reference current 480 may be derived from a current bias reference generation circuit (e.g., via the reference current 340 of FIG. 3). The first current mirror circuitry 305 (FIG. 3) coupled to or configured as the PCMDAC 400 is used to generate a current for the converter output signal 490, which determines the loop bandwidth of the PLL circuitry 200. The converter output signal 490 is used as the reference current for the second current mirror 310. The second current mirror circuitry 310 also may be coupled to or configured as a PCMDAC and may be programmed to generate a larger magnitude current, for example, for larger feedback divider ratios as discussed below.

[0040] In alternative embodiments of the PLL circuitry 200 having more than one VCO (with different voltages for the filtered control signal 240), a third PCMDAC 400 may be used. The converter output 490 of the third PCMDAC 400 is controlled by the logical values selecting the VCO in use. As a result, the third PCMDAC 400 provides a constant loop bandwidth, regardless of the individual loop parameters (e.g., voltage of the filtered control signal 230). The concatenation of several PCMDACs further enables the construction of programmable PLL circuitry where the loop bandwidth is thus independently programmable. The programmable PLL circuitry facilitates usage in other circuits where a constant loop bandwidth is desirable.

[0041] Moreover, in the programmable PLL circuitry, a wide range of loop bandwidth settings are desirable in combination with a wide range of settings for the feedback divider circuitry 255 (FIG. 2) where a large range of currents may be required to be provided by the replica current charge pump circuitry 225. When implementing multiple PCMDACs to provide the large range of currents in the replica current charge pump circuitry 225, noise typically accumulates with each additional PCMDAC. The magnitude of the noise typically decreases with increasing current. Therefore, the largest possible currents may be used within the constraints of current mirror headroom and power budget.

[0042] To minimize noise and mismatch effects, the PCMDAC 400 is preferably dimensioned with the largest transistor drive voltages allowed by the minimum operational supply voltage desired. The largest transistor drive voltage therefore results in a low voltage on the input switch 410 when large output currents are programmed. The PCMDAC 400 may also work with currents down to the nanoampere range for other loop bandwidth, VCO voltage settings, and frequency divider settings. In some embodiments, the converter selectors 450, 460, and 470 provide a very low resistance to allow sufficient voltage headroom for the wide range of currents.

[0043] In deep submicron technologies, however, low on-resistance corresponds to high leakage in the off-state. The leakage through the converter selectors 450, 460, and 470 for the converter outputs 420, 430, and 440 having a higher magnitude current may exceed the desired output signal for the converter output signal 490 (e.g., for a 7 bit DAC, the leakage may be 1-2 orders of magnitude larger than the signal). The leakage may also increase with each additional bit (and therefore each higher magnitude converter output) in the PCMDAC 400.

[0044] FIG. 5 illustrates a leakage compensated PCMDAC 500 in an exemplary implementation of the invention. The leakage compensated PCMDAC 500 includes the PCMDAC 400 (FIG. 4), current mirror circuitry 505, converter outputs 510, 515, and 520, off-state switches 525, 530, and 535, and converter selectors 540, 545, and 555. The converter outputs 510, 515, and 520 are linked to the input switch 410 in the PCMDAC 400. The reference current 480 is linked to the gate of the converter outputs 510, 515, and 520.

[0045] The converter output 510 is linked by the off-state switch 525 to the converter selector 540. The converter output 515 is linked by the off-state switch 530 to the converter selector 545. The converter output 520 is linked by the off-state switch 535 to the converter selector 550. The converter selectors 540, 545, and 550 are linked to the current mirror circuitry 510 via line 555. The current mirror circuitry 510 is linked to the PCMDAC 400 at the converter output 490.

[0046] Leakage currents in the PCMDAC 400 are replicated in the leakage compensated PCMDAC 500 which is nearly identical to the PCMDAC 400. In the leakage compensated PCMDAC 500, however, the converter outputs 510, 515, and 520 are always off or disabled. The off-state switches 525, 530, and 535 (i.e., which may be "low-leakage" switches) are placed in series with each converter output 510, 515, and 520. The converter selectors 540, 545, and 550 are only enabled when the corresponding converter selectors 450, 460, and 470, respectively in the PCMDAC 400 are disabled. For example, when converter output 420 is disabled by the converter selector 450, the converter selector 540 is enabled. Every inactive branch (converter output) in the PCMDAC 400 corresponds to an active branch in the leakage compensated PCMDAC 500 and identical leakage currents flow through both.

[0047] In some embodiments, high on-resistance in the converter selectors 540, 545, and 550 is acceptable because the currents through the converter selectors 540, 545, and 550 are so small (only leakage) that the voltage drop across the converter selectors 540, 545, and 550 is negligible even with a relatively high resistance. Additionally, the current mirror circuitry 505, used to mirror the leakage compensation current, is able to operate with low supply voltages. The leakage current can be mirrored and then fed back into the PCMDAC 400 leaving only the intended signal on the converter output 490. One advantage of the leakage compensated PCMDAC 500 is that the topology allows the use of short (low on-resistance) switch devices, enabling efficient layout and a smaller silicon area than would otherwise be possible.

[0048] In another aspect of reducing leakage in the replica current charge pump 225 (FIG. 2), when the PLL circuitry 200 (FIG. 2) is powered on, the filtered control voltage 240 is often at ground. At the ground voltage, the VCO 245 may fail to oscillate. The power-on ground voltage may potentially prevent the PLL circuitry 200 from ever reaching a locked state.

[0049] FIG. 6 illustrates power-on leakage isolation circuitry 600 in an exemplary implementation of the invention. The power-on leakage isolation circuitry 600 includes a first switch 610, a second switch 620, and biasing circuitry 630. The gates of the first switch 610 and the second switch 620 are controlled via line 640. The first switch 610 receives a turn-on voltage via line 650 and is further linked to the second switch 620. The second switch 620 outputs the turn-on voltage to the loop filter 235 (FIG. 2) via the line 660. The biasing circuitry 630 is linked to the output of the second switch 620 (the line 660) and to the connection between the first switch 610 and the second switch 620.

[0050] The biasing circuitry 630 comprises any device, component, or circuitry configured as a voltage follower to reduce the potential another device, component, or circuitry. For example, the biasing circuitry 630 reduces the potential across the second switch 620. One example of the biasing circuitry 630 is an operational amplifier. During startup, both the first switch 610 and the second switch 620 are enabled (e.g., closed). Once the voltage of the filtered control signal 240 reaches a level where the VCO 245 begins running, both the first switch 610 and the second switch 620 may be turned off (e.g., opened). Because the potential across the switch 620 is zero, no leakage current will flow through the second switch 620 to the loop filter 235 via the line 660.

[0051] In some embodiments, the biasing circuitry 630 may not need to be turned off because the current through the second switch 620 dominates. In other embodiments, the biasing circuitry 630 only needs to be strong enough to supply the leakage through the second switch 620, which is off for normal operation. An alternative to using the biasing circuitry 630 with a weak buffer is to turn off the biasing circuitry 630 when the first switch 610 and the second switch 620 are closed.

[0052]. FIG. 7 illustrates current pulse leakage isolation circuitry 700 in an exemplary implementation of the invention. The current pulse leakage isolation circuitry 700 includes biasing circuitry 710, an up signal switch 720, an inverted up signal switch 730, a down signal switch 740, and an inverted down signal switch 750. The up signal switches 720 and 730 are linked to a power source (e.g., the second output 350 of the first current mirror circuitry 305 of FIG. 3) via the line 350. The up signal switch 720 is linked to the down signal switch 740. The inverted up signal switch 730 is linked to the inverted down signal switch 750. The down signal switches 740 and 750 are linked to a power drain (e.g., the second output 370 of the second current mirror 310 of FIG. 3) via line 370. The biasing circuitry 710 is linked to the connection between the up signal switch 720 and the down signal switch 740 and is further linked to the connection between the inverted up signal switch 730 and the inverted down signal switch 750. The up signal switch 720 and the down signal switch 740 generate the charge pump output signal 230

(FIG. 2) via line 760 based on the up signal 215 (FIG. 2) and the down signal 220 (FIG. 2).

[0053] The largest current and voltage levels, for the PLL circuitry 200 operating with small supply voltages, determine the size of the up and down signal switches 720, 730, 740, and 750. However, with small output currents, the leakage through the up and down signal switches 720, 730, 740, and 750 may result in a leakage current flowing through the up and down signal switches 720, 730, 740, and 750 to the charge pump output signal 230 (and into the loop filter 235). To reduce the leakage current, the biasing circuitry 710 generates a voltage bias equal or close to the voltage of the filtered control signal 240 (e.g., the voltage across the loop filter circuitry 235). When the up and down signal switches 720, 730, 740, and 750 are off, the leakage currents are diverted to the biasing circuitry 710. The biasing circuitry 710 ensures that the voltage across the up and down signal switches 720, 730, 740, and 750 is small. The small voltage reduces the leakage currents from the up and down switches 720, 730, 740, and 750 to the charge pump output signal 230.

[0054] FIG. 8 illustrates charge compensated current pulse leakage isolation circuitry 800 in an exemplary implementation of the invention. The charge compensated current pulse leakage isolation circuitry 800 includes the current pulse leakage isolation circuitry 700 and an additional inverted up signal switch 810 and inverted down signal switch 820. The inverted up signal switch 810 is linked to the up signal switch 720 and the inverted down signal switch 830. The inverted down signal switch 830 is further linked to the down signal switch 740. The gate-source and gate-drain of the inverted up signal switch 810 is linked via line 830. The gate-source and gate-drain of the inverted down signal switch 830 is linked via line 840.

[0055] During operation of the current pulse leakage isolation circuitry 700 (FIG. 7), when the up and down signal switches 720, 730, 740, and 750 are switched, the gate-source and gate-drain capacitance for the up and down signal switches 720, 730, 740, and 750 may result in a small amount of charge being transferred from the control signals (e.g., the up signal 215 and the down signal 220) for the up and down signal switches 720, 730, 740, and 750 to the charge pump output signal 230 on the line 780. The charge compensated current pulse leakage isolation circuitry 800 reduces charge transfer by shorting the gate-drain and gate-source of the inverted up and down signal switches 810 and 820 placed nearest to the charge pump output signal 230 on the line 760. In some embodiments, the inverted up and down signal switches 810 and 820 have sizes adjusted to compensate charge transfer at the operational voltage of the VCO 245 (FIG. 2).

[0056] The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

CLAIMS

What is claimed is:

1. A system for performing phase-locked loop, the system comprising:

phase frequency detector circuitry configured to generate an up signal and a down signal based on the phase difference of an input signal and a feedback signal;

charge pump circuitry including a first current mirror circuitry and a second current mirror circuitry, the charge pump circuitry configured to generate a charge pump output signal based on the up and down signals;

loop filter circuitry configured to generate a filtered control signal based on the charge pump output signal; and

voltage controlled oscillator circuitry configured to generate the feedback signal with a repeating waveform based on the filtered control signal.

2. The system for performing phase-locked loop of claim 1 wherein the second current mirror circuitry is configured to mirror a reference current of the first current mirror circuitry.

3. The system for performing phase-locked loop of claim 1 wherein the charge pump output signal comprises current pulses of substantially equal magnitude.

4. The system for performing phase-locked loop of claim 1, further comprising biasing circuitry configured to generate a voltage bias in the second current mirror circuitry.

5. The system for performing phase-locked loop of claim 4 wherein the biasing circuitry is configured to generate the voltage bias based on a voltage for the first current mirror circuitry and a voltage for the charge pump output signal.

6. The system for performing phase-locked loop of claim 1 wherein one of the first current mirror circuitry and the second current mirror circuitry further comprises output circuitry having a plurality of current outputs of differing magnitude.

7. The system for performing phase-locked loop of claim 6 wherein the plurality of current outputs provide one or more loop bandwidths.

8. The system for performing phase-locked loop of claim 6, further comprising programmable loop bandwidth circuitry configured to select one of the plurality of current outputs.

9. The system for performing phase-locked loop of claim 1, further comprising leakage compensation circuitry configured to reduce off-state leakage to the charge pump output signal.

10. The system for performing phase-locked loop of claim 1, further comprising charge compensation circuitry configured to reduce charge transfer to the charge pump circuitry.

11. The system for performing phase-locked loop of claim 1, further comprising power-on circuitry configured to generate a turn-on voltage for the filtered control signal.

12. A method for performing phase-locked loop, the method comprising:

generating an up signal and a down signal based on the phase difference of an input signal and a feedback signal;

generating a charge pump output signal based on the up and down signals in charge pump circuitry including first current mirror circuitry and second current mirror circuitry;

generating a filtered control signal based on the charge pump output signal; and

generating the feedback signal with a repeating waveform based on the filtered control signal.

13. The method for performing phase-locked loop of claim 12, further comprising mirroring in the second current mirror circuitry a reference current of the first current mirror circuitry.

14. The method for performing phase-locked loop of claim 12 wherein the charge pump output signal comprises current pulses of substantially equal magnitude.

15. The method for performing phase-locked loop of claim 12, further comprising generating a voltage bias in the second current mirror circuitry.

16. The method for performing phase-locked loop of claim 15 wherein generating the voltage bias is based on a voltage for the first current mirror circuitry and a voltage for the charge pump output signal.

17. The method for performing phase-locked loop of claim 12 further comprising generating a plurality of current outputs of differing magnitude.

18. The method for performing phase-locked loop of claim 17, further comprising providing one or more loop bandwidths based on the plurality of current outputs.

19. The method for performing phase-locked loop of claim 17, further comprising selecting one of the plurality of current outputs.

20. The method for performing phase-locked loop of claim 12, further comprising reducing off-state leakage to the charge pump output signal.

21. The method for performing phase-locked loop of claim 20 wherein reducing the off-state leakage comprises producing a first voltage substantially equal to a second voltage for the charge pump output signal.

22. The method for performing phase-locked loop of claim 12, further comprising reducing charge transfer to the charge pump output signal.

23. The method for performing phase-locked loop of claim 12, further comprising generating a turn-on voltage in the filtered control signal.

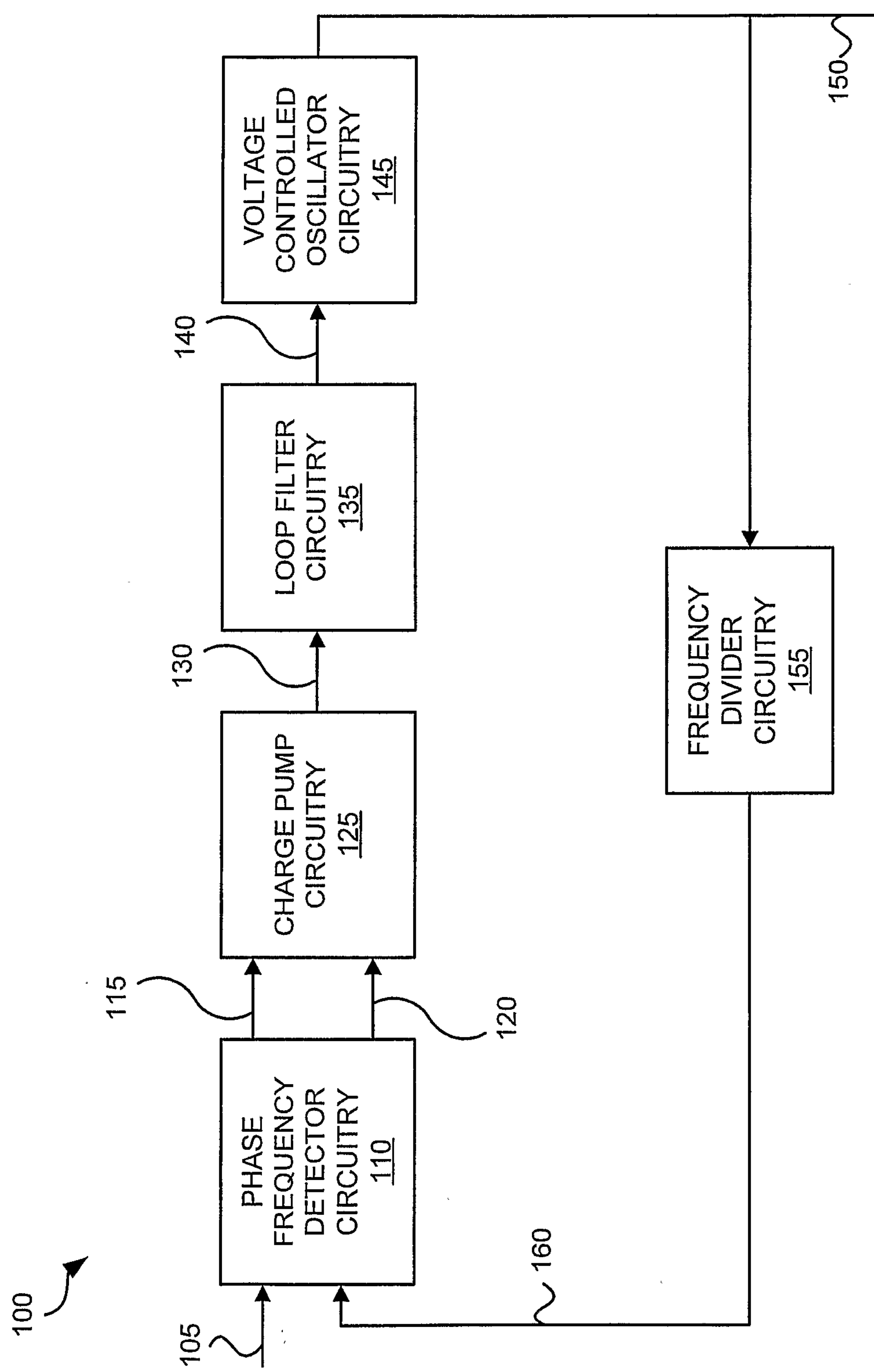


FIG. 1
PRIOR ART

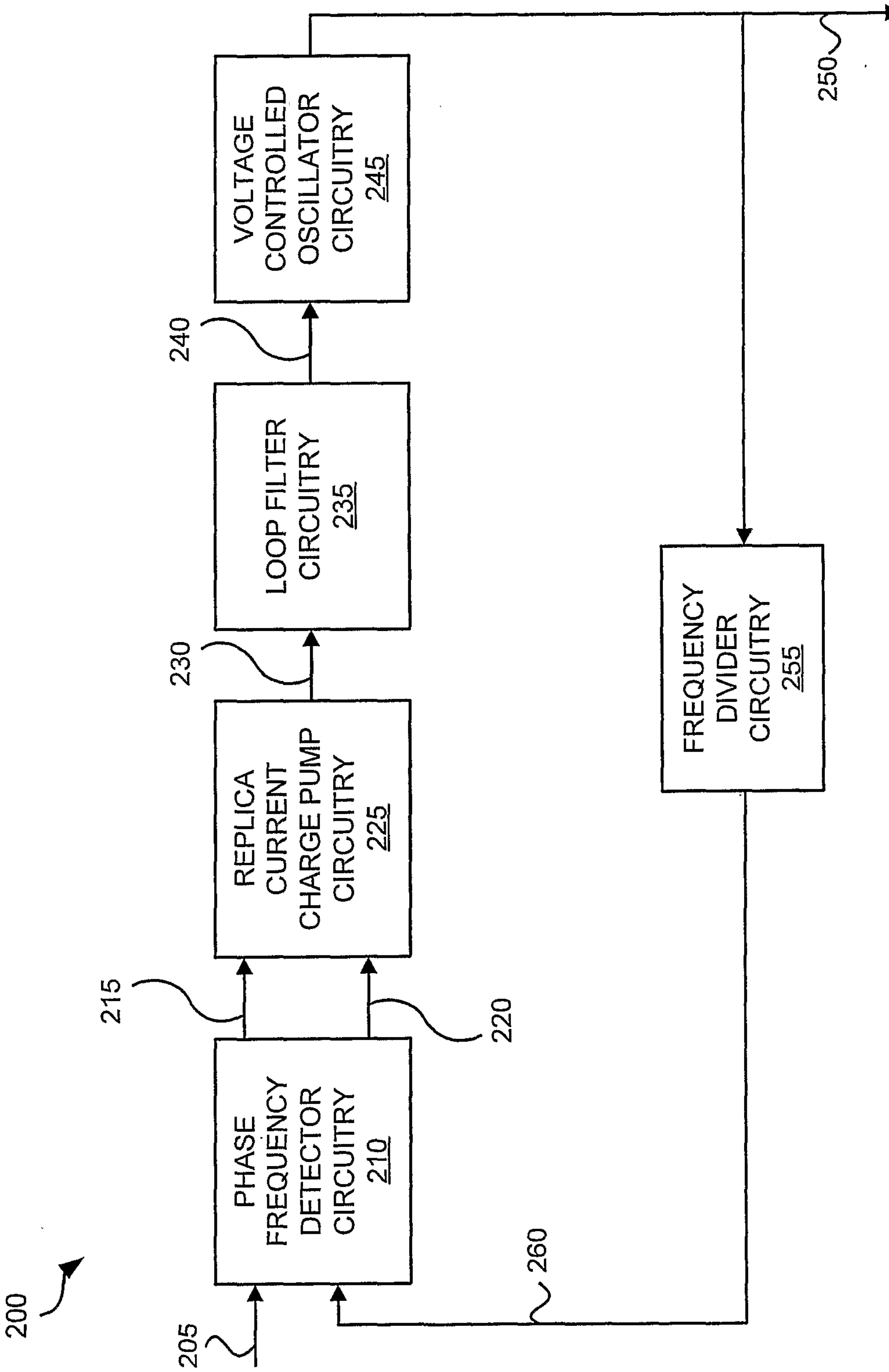

200
205
PHASE FREQUENCY DETECTOR CIRCUITRY 210
215
220
REPLICA CURRENT CHARGE PUMP CIRCUITRY 225
230
LOOP FILTER CIRCUITRY 235
240
VOLTAGE CONTROLLED OSCILLATOR CIRCUITRY 245
250
FREQUENCY DIVIDER CIRCUITRY 255
260

FIG. 2

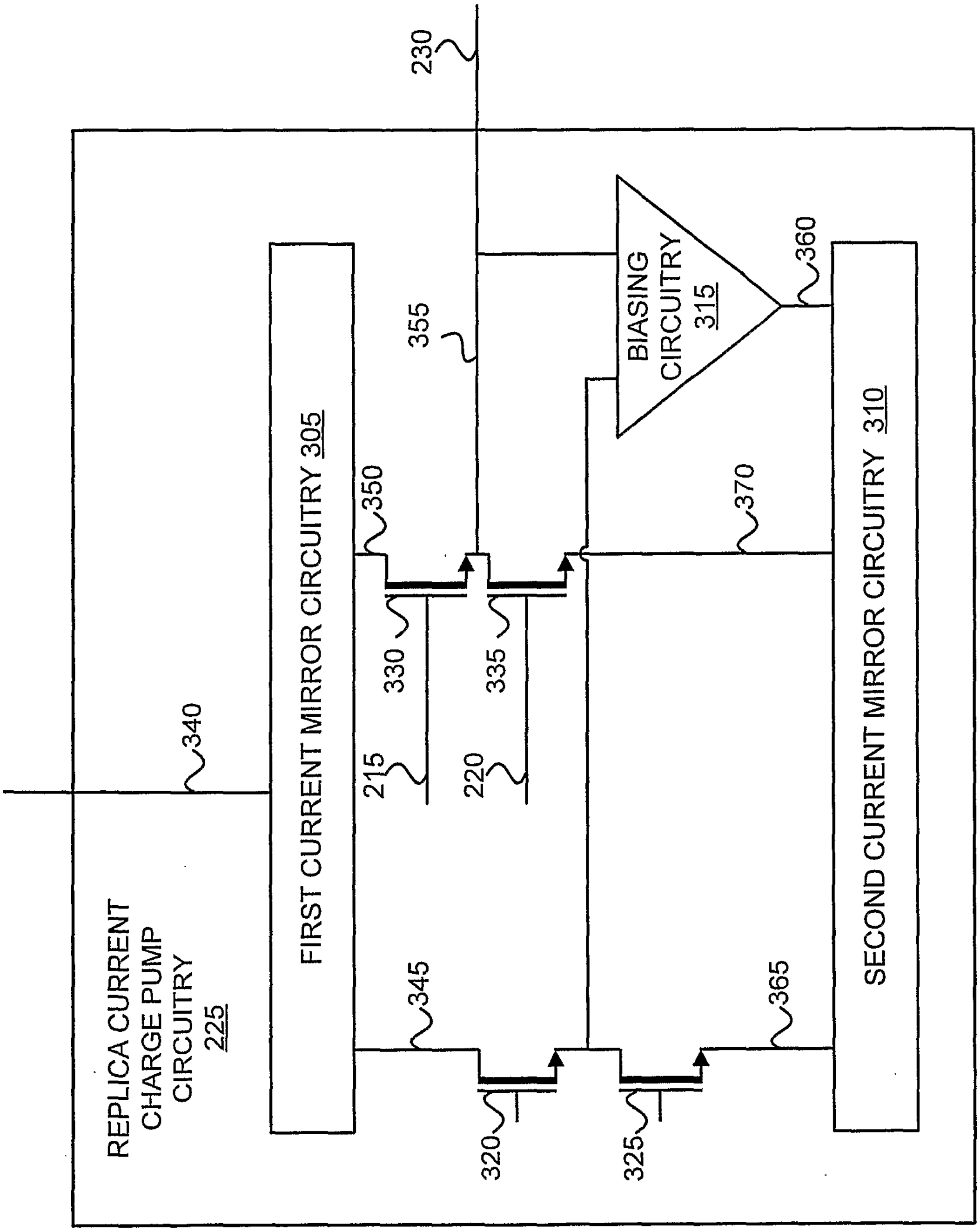

REPLICA CURRENT CHARGE PUMP CIRCUITRY 225
FIRST CURRENT MIRROR CIRCUITRY 305
SECOND CURRENT MIRROR CIRCUITRY 310
BIASING CIRCUITRY 315
230
355
360
350
370
330
335
340
215
220
345
365
320
325

FIG. 3

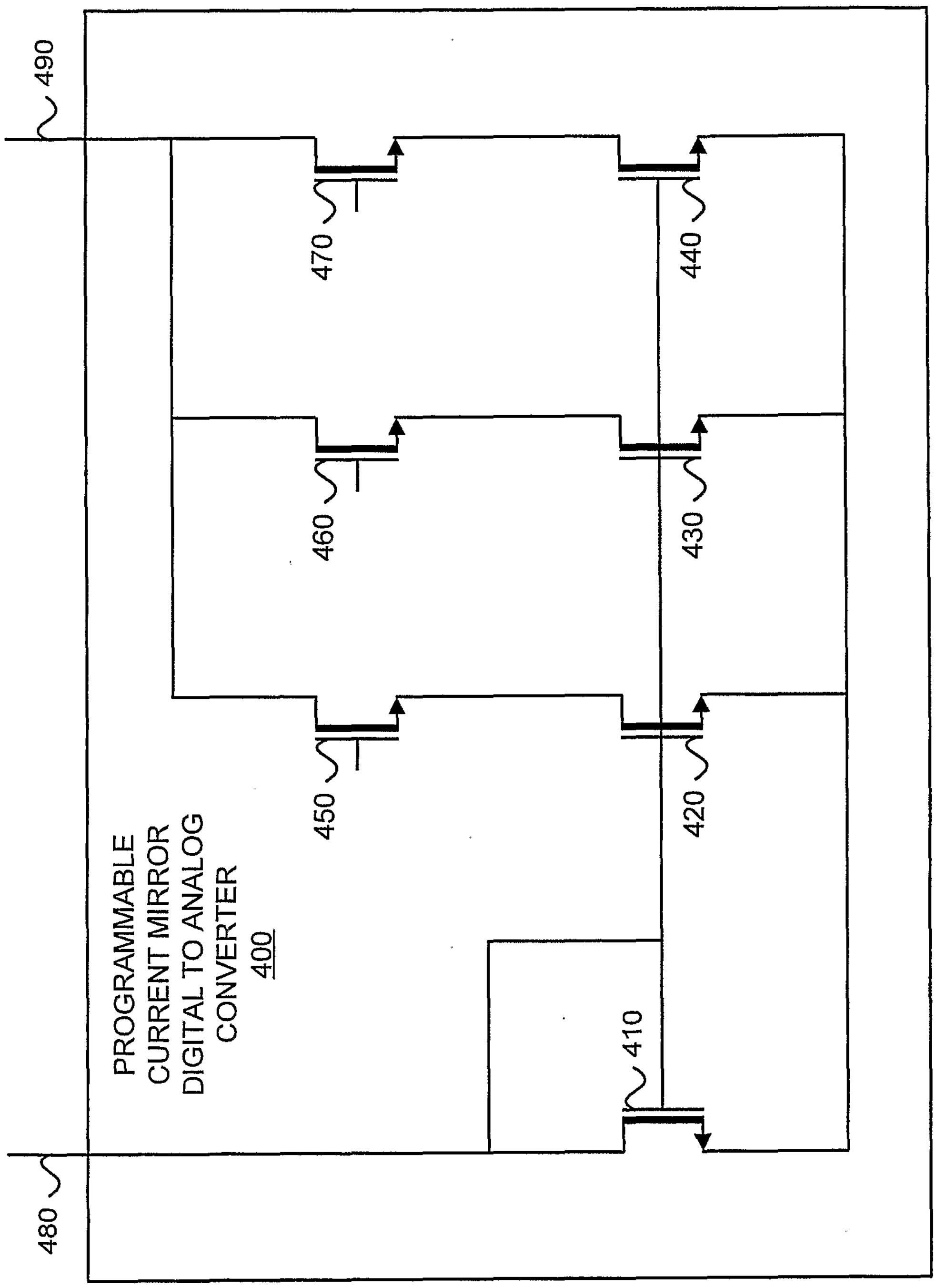

490
470
440
460
430
450
420
PROGRAMMABLE
CURRENT MIRROR
DIGITAL TO ANALOG
CONVERTER
400
410
480

FIG. 4

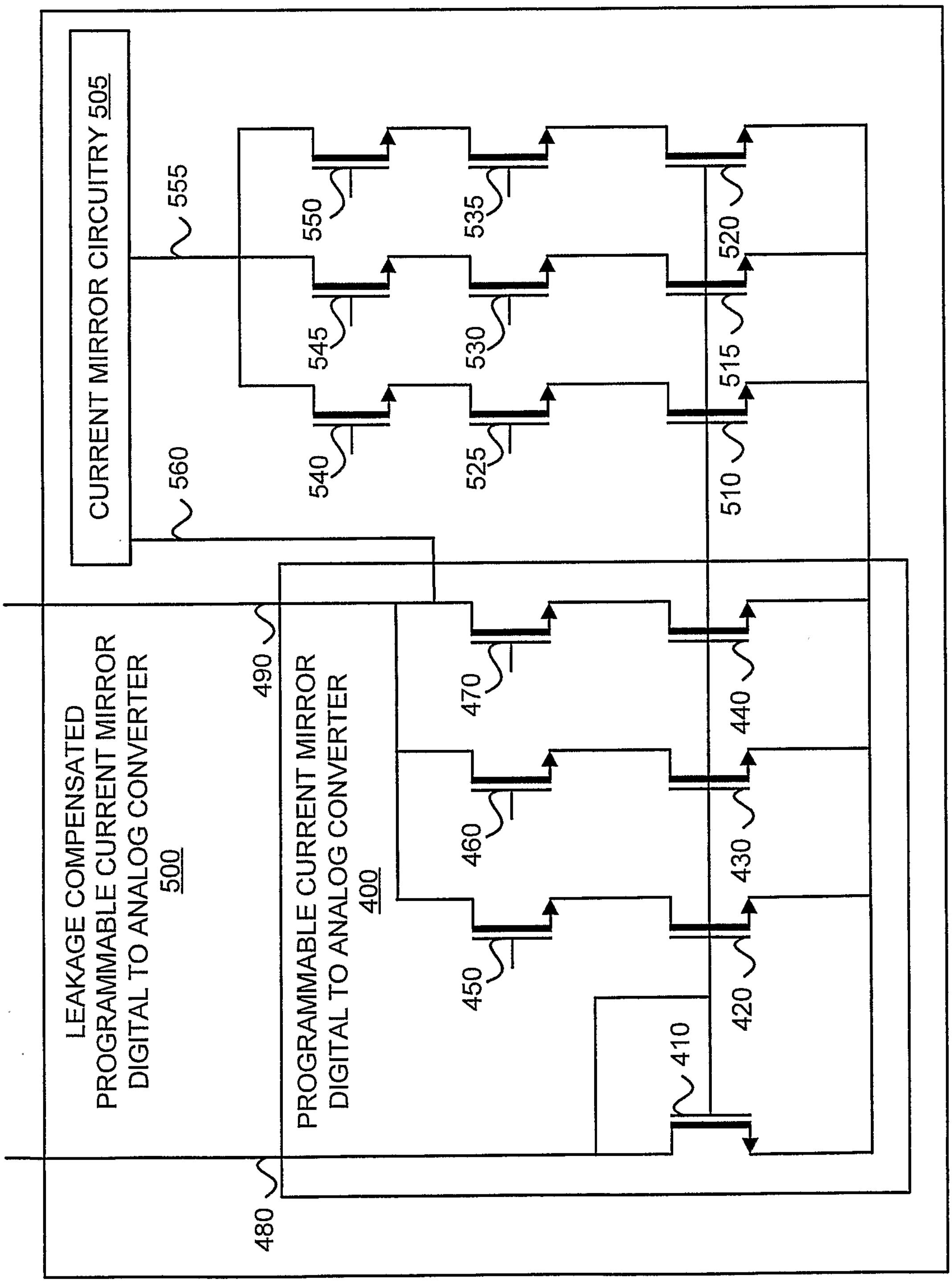

CURRENT MIRROR CIRCUITRY 505
LEAKAGE COMPENSATED PROGRAMMABLE CURRENT MIRROR DIGITAL TO ANALOG CONVERTER 500
PROGRAMMABLE CURRENT MIRROR DIGITAL TO ANALOG CONVERTER 400
555
560
550
545
540
535
530
525
520
515
510
490
480
470
460
450
440
430
420
410

FIG. 5

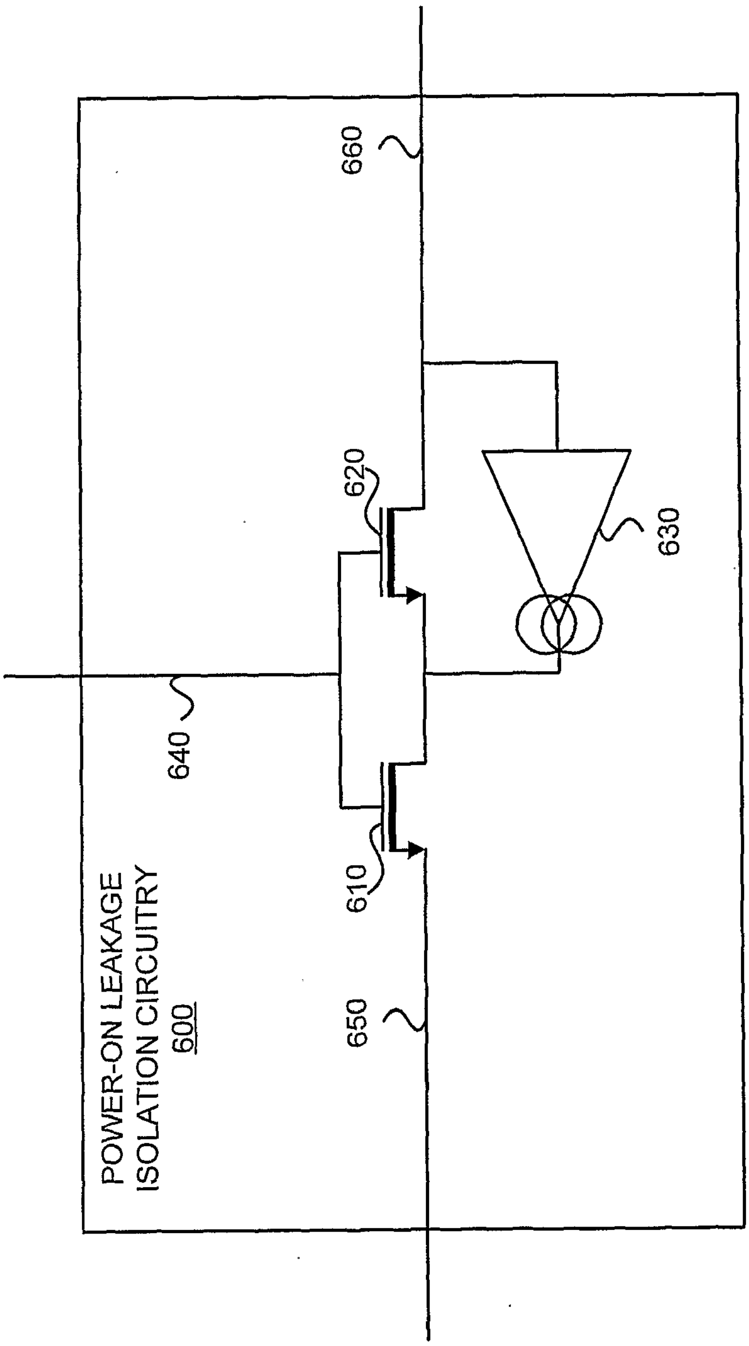

POWER-ON LEAKAGE
ISOLATION CIRCUITRY
600
610
620
630
640
650
660

FIG. 6

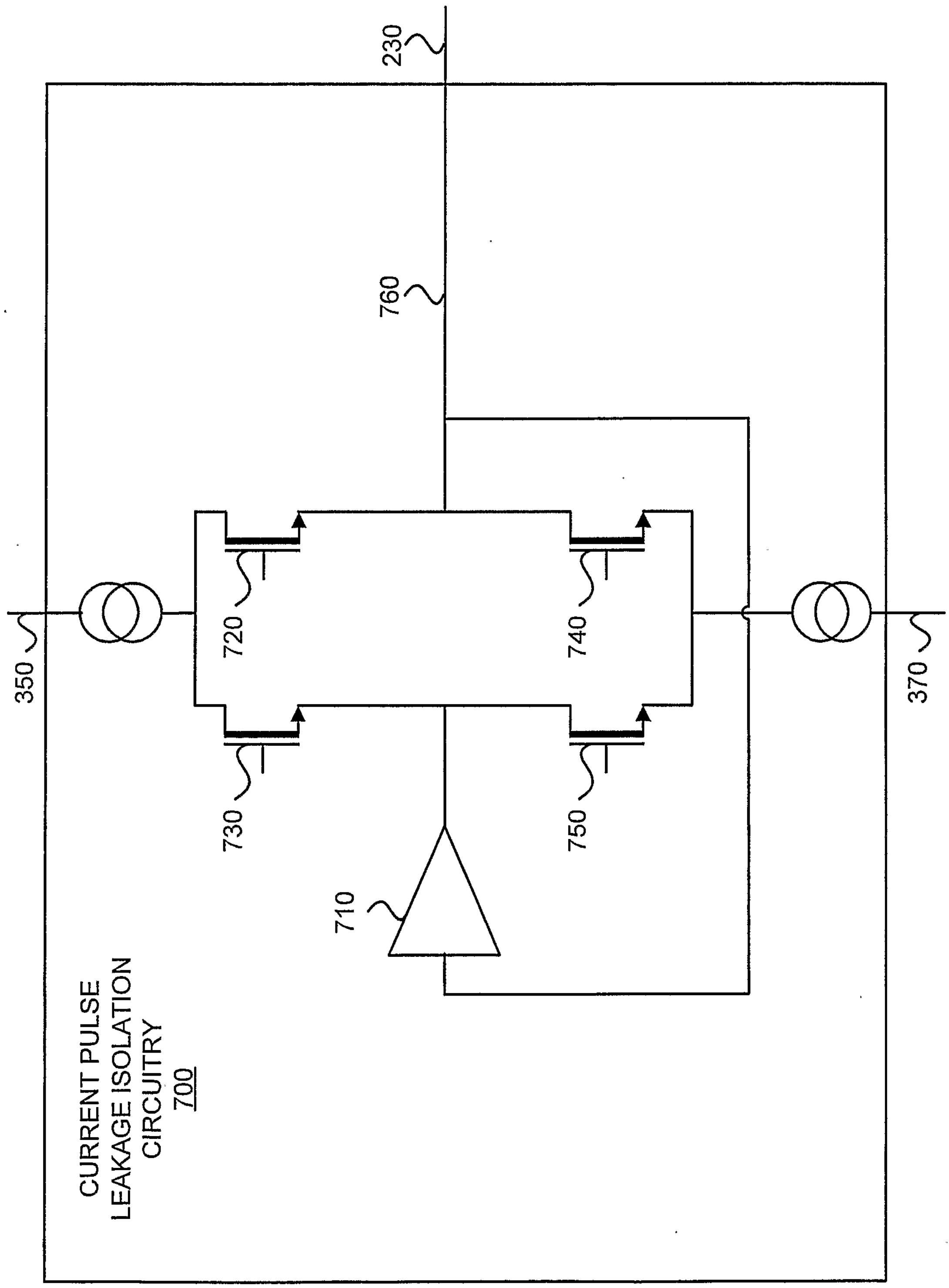
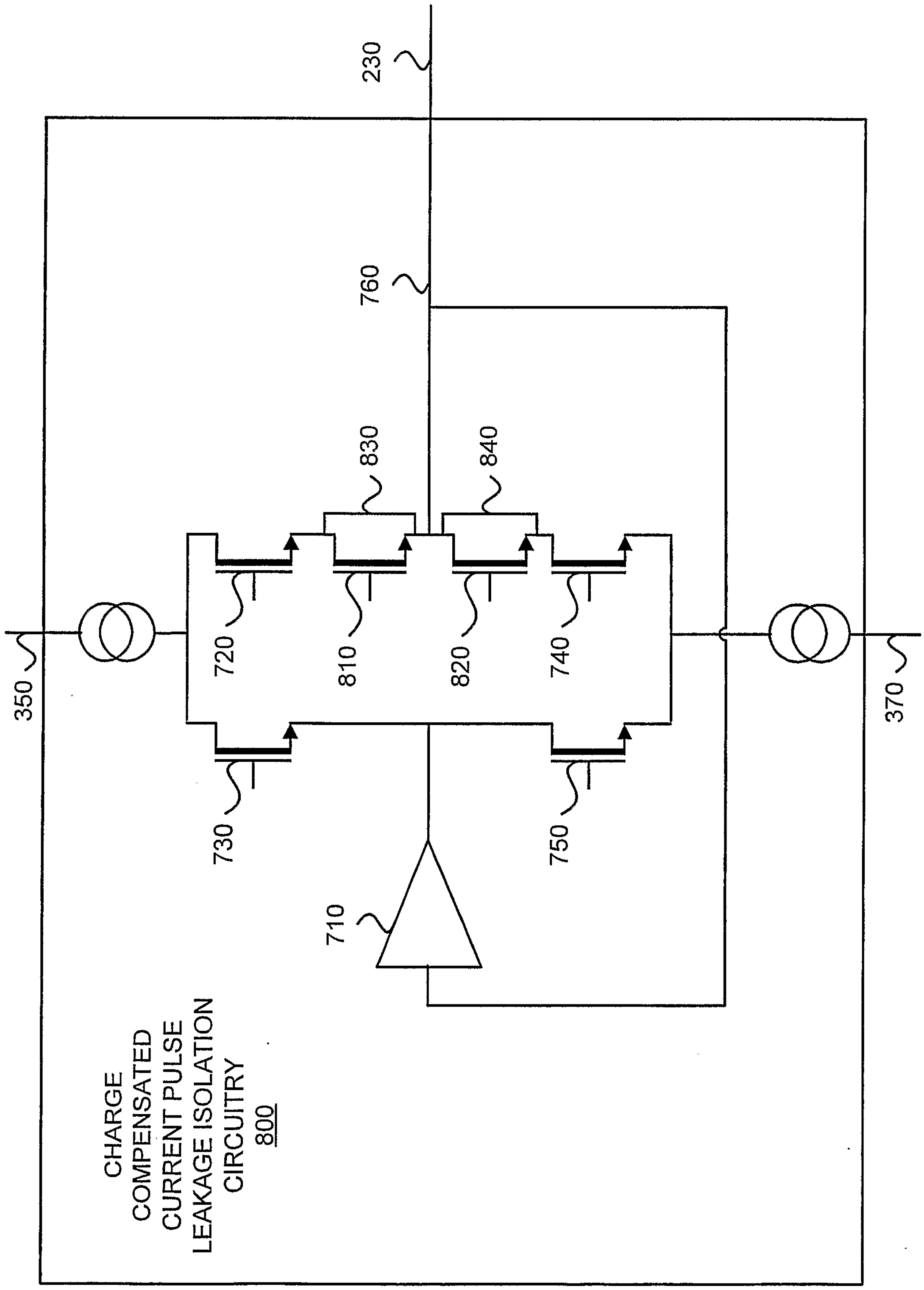

230
760
350
720
740
370
730
750
710
CURRENT PULSE LEAKAGE ISOLATION CIRCUITRY 700

FIG. 7



230
760
830
840
350
720
810
820
740
370
730
750
710
CHARGE
COMPENSATED
CURRENT PULSE
LEAKAGE ISOLATION
CIRCUITRY
800

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/045427

A. CLASSIFICATION OF SUBJECT MATTER
H03L7/089

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SAMAVATI H ET AL: "A fully-integrated 5GHz CMOS wireless-LAN receiver" SOLID-STATE CIRCUITS CONFERENCE, 2001. DIGEST OF TECHNICAL PAPERS. ISSCC. 2001 IEEE INTERNATIONAL FEB. 5-7, 2001, PISCATAWAY, NJ, USA,IEEE, 5 February 2001 (2001-02-05), page 208, 209, 248, XP010536240 ISBN: 0-7803-6608-5 page 208, column 1, line 45 - column 2, line 17 figures 13.7.1,13.7.2	1-5,9, 10, 12-16, 20-22
Y		11,23

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 March 2006	12/04/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Balbinot, H

Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 124 755 A (PARKER ET AL) 26 September 2000 (2000-09-26)	1-5,9, 10, 12-16, 20-22
	column 1, line 16 - line 39 column 4, line 49 - column 6, line 43 figures 1,5	
Y		11,23
X	US 2004/085106 A1 (JEONG MINSU) 6 May 2004 (2004-05-06) paragraph [0001] - paragraph [0004] paragraph [0015] - paragraph [0018] paragraph [0032] - paragraph [0051] paragraph [0093] - paragraph [0111] figures 1,3,8	1-5,10, 12-16,22
Y		11,23
X	EP 0 405 523 A (SONY CORPORATION) 2 January 1991 (1991-01-02)	1-3,6-8, 12-14, 17-19
	column 7, line 38 - column 11, line 43; figures 1,7	
Y		11,23
X	EP 0 755 120 A (NEC CORPORATION) 22 January 1997 (1997-01-22)	1-3,6-8, 12-14, 17-19
	page 3, line 34 - line 42 page 4, line 43 - page 5, line 15 figures 1,8	
Y		11,23
Y	EP 1 292 032 A (MITSUBISHI DENKI KABUSHIKI KAISHA) 12 March 2003 (2003-03-12) paragraph [0088] - paragraph [0090]	11,23

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2005/045427

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			WO	9917450 A1	08-04-1999
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EP 0405523	A	02-01-1991	CA	2019778 A1	27-12-1990
			DE	69016850 D1	23-03-1995
			DE	69016850 T2	14-09-1995
			JP	2879763 B2	05-04-1999
			JP	3030517 A	08-02-1991
			US	5068626 A	26-11-1991
			US	5153530 A	06-10-1992
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			US	6812754 B1	02-11-2004