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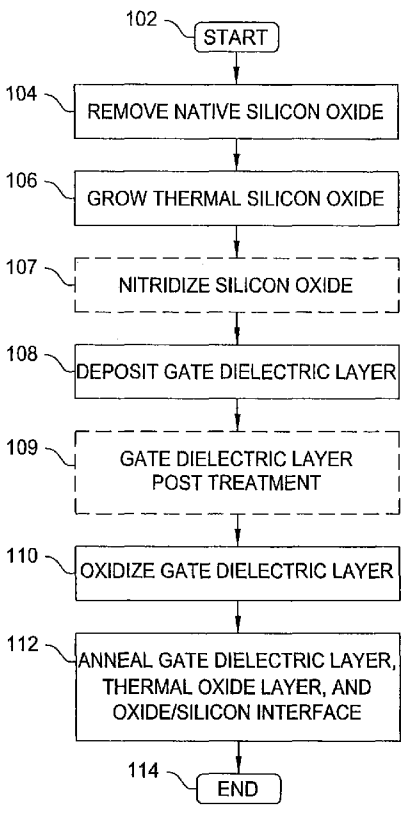

(57) Abstract: A method for fabricating a gate dielectric of a field effect transistor is provided. In one embodiment, the method includes removing a native oxide layer, forming an oxide layer, forming a gate dielectric layer over the oxide layer, forming an oxide layer over the gate dielectric layer, and annealing the layers and underlying thermal oxide/silicon interface. Optionally, the oxide layer may be nitridized prior to forming the gate dielectric layer. In one embodiment, the oxide layer on the substrate is formed by depositing the oxide layer, and the oxide layer on the gate dielectric layer is formed by oxidizing at least a portion of the gate dielectric layer using an oxygen-containing plasma. In another embodiment, the oxide layer on the gate dielectric layer is formed by forming a thermal oxide layer, i.e., depositing the oxide layer on the gate dielectric layer.

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METHOD FOR FABRICATING A GATE DIELECTRIC OF A FIELD EFFECT TRANSISTOR

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the present invention generally relate to methods for fabricating devices on semiconductor substrates. More specifically, the present invention relates to a method for fabricating field effect transistors and, in particular, gate dielectrics of the field effect transistors.

Description of the Related Art

[0002] Integrated circuits may include more than one million micro-electronic field effect transistors (*e.g.*, complementary metal-oxide-semiconductor (CMOS) field effect transistors) that are formed on a substrate and cooperate to perform various functions within the circuit. A CMOS transistor comprises a gate structure disposed over a channel region formed between source and drain regions of the transistor. The gate structure generally comprises a gate electrode and a gate dielectric. The gate electrode is disposed over the gate dielectric and, in operation, is used to control a flow of charge carriers (*i.e.*, electric current) in the channel region beneath the gate dielectric.

[0003] The gate dielectric is typically formed from silicon nitride (Si_3N_4) or silicon oxynitride (SiON). To increase the speed of the transistor, a thickness of the gate dielectric in advanced integrated circuits is selected in a range of about 20-30 Angstroms or less. However, fabrication of gate structures having such ultra-thin gate dielectrics represents a challenging task. One specific problem is that present manufacturing techniques cause high leakage currents through the gate dielectric and decrease mobility of the charge carriers in the channel region due to diffusion of large amounts of nitrogen (N_2) into the silicon / gate dielectric interface of the transistors. In addition, interaction of nitrogen with poly silicon of the gate electrode shifts V_{FB}/V_t, wherein V_{FB} is the flat-band voltage and V_t is the threshold voltage.

[0004] Therefore, there is a need in the art for an improved method for fabricating a gate dielectric of a field effect transistor.

SUMMARY OF THE INVENTION

[0005] Embodiments of the present invention generally relates to a method for fabricating a gate dielectric of a field effect transistor. The invention may be utilized in integrated circuit devices, such as microprocessors, application specific integrated circuits (ASICs), electronic memory devices, and the like.

[0006] In one embodiment, the method includes steps of removing a native oxide layer from a silicon substrate, forming a first oxide layer on the substrate, forming a gate dielectric layer (*e.g.,* silicon nitride (Si_3N_4), hafnium oxide (HfO_2), hafnium silicate ($HfSi_xO_y$, where x and y are integers), and the like) over the first oxide layer, forming a second oxide layer over the gate dielectric layer, and annealing the formed layers and interface between the first oxide layer and the substrate. Optionally, the first oxide layer on the substrate may be nitridized prior to forming the gate dielectric layer. Optionally, the gate dielectric layer may be nitridized prior to forming the second oxide layer on the gate dielectric layer. In one embodiment, at least portions of the method may be performed using processing reactors of an integrated semiconductor substrate processing system (*i.e.,* a cluster tool). In one embodiment, the oxide layer on the substrate is formed by depositing the first oxide layer, and the oxide layer on the gate dielectric layer is formed by oxidizing the gate dielectric layer. In another embodiment, the oxide layer on the substrate is formed by depositing the oxide layer, and the oxide layer on the gate dielectric layer is formed by depositing the second oxide layer on the gate dielectric layer.

[0007] In another embodiment, a method for fabricating a gate dielectric of a field effect transistor upon a substrate, includes the steps of removing a native oxide layer from the substrate and placing the substrate in a nitrogen purged or vacuum environment, forming a first thermal oxide layer on the silicon substrate, forming a gate dielectric layer on the first thermal oxide layer, forming a second oxide layer on the gate dielectric layer, and thermally annealing the substrate having the first thermal oxide layer and the oxidized gate dielectric layer formed thereon. In one

embodiment, the oxide layer on the substrate is formed by depositing the first oxide layer, and the oxide layer on the gate dielectric layer is formed by oxidizing at least a portion of the gate dielectric layer using an oxygen-containing plasma. In another embodiment, the oxide layer on the substrate is formed by depositing the first oxide layer, and the oxide layer on the gate dielectric layer is formed by forming a thermal oxide layer, *i.e.*, depositing the second oxide layer on the gate dielectric layer.

[0008] In another aspect of the invention, an integrated semiconductor substrate processing system is disclosed for fabricating a gate dielectric of a field effect transistor. In one embodiment, the system includes at least one first reactor configured for forming a thermal oxide layer on a silicon substrate, at least one second reactor configured for depositing a gate dielectric layer on the thermal oxide layer, at least one third reactor configured for oxidizing the gate dielectric layer, at least one load-lock chamber, at least one substrate transfer chamber coupled to each of the reactors and load lock chambers, and a controller administering and monitoring operation of the processing system.

[0009] In another aspect of the invention, an integrated semiconductor substrate processing system is disclosed for fabricating a gate dielectric of a field effect transistor. In one embodiment, the system includes a reactor configured for forming a thermal oxide layer on a silicon substrate, the reactor being configured for depositing a gate dielectric layer on the thermal oxide layer and being configured for forming a thermal oxide layer on the gate dielectric layer; a decoupled plasma source; one or more load lock chambers; at least one substrate transfer chamber coupled to the reactor and the load lock chambers; and a controller for administering and monitoring operation of the processing system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The teachings of the present invention will become apparent by considering the following detailed description in conjunction with the accompanying drawings, in which:

[0011] FIG. 1 depicts a flow diagram illustrating a method for fabricating a gate dielectric of a field effect transistor in accordance with one embodiment of the present invention;

[0012] FIGS. 2A-2E, together, depict a series of schematic, cross-sectional views of a substrate where the gate structure is fabricated in accordance with the method of FIG. 1; and

[0013] FIG. 3 depicts a schematic diagram of an exemplary integrated semiconductor substrate processing system of the kind that may be used to practice portions of the invention.

[0014] FIG. 4 depicts a schematic diagram of an exemplary integrated semiconductor substrate processing chamber of the kind that may be used to practice portions of the invention.

[0015] Where possible, identical reference numerals are used herein to designate identical elements that are common to the figures. The images in the drawings are simplified for illustrative purposes and are not depicted to scale.

[0016] The appended drawings illustrate exemplary embodiments of the invention and, as such, should not be considered as limiting the scope of the invention, which may admit to other equally effective embodiments.

DETAILED DESCRIPTION

[0017] The present invention is a method for fabricating a gate dielectric of field effect transistors having ultra-thin gate dielectrics (*e.g.,* less than about 20 - 30 Angstroms). The invention may be used in fabrication of integrated semiconductor devices and circuits.

[0018] FIG. 1 is a flow diagram illustrating a method 100 for fabricating a gate dielectric of a field effect transistor in accordance with one embodiment of the present invention. The method 100 includes processing steps performed upon a substrate during fabrication of the gate structure of an exemplary CMOS field effect transistor. In some embodiments, these processing steps are performed in the

depicted order. In alternate embodiments, at least two of these steps may be performed contemporaneously or in a different order. Sub-steps and auxiliary procedures (*e.g.*, substrate transfers between processing reactors, process control steps, and the like) are well known in the art and, as such, herein are omitted.

[0019] At least portions of the method 100 may be performed using processing reactors of an integrated semiconductor substrate processing system (*i.e.*, a cluster tool). One such processing system is the CENTURA® integrated processing system, available from Applied Materials, Inc. of Santa Clara, California. A general description of a suitable processing system 300 and a suitable CVD chamber 400 is discussed below with reference to FIG. 3 and Fig. 4, respectively.

[0020] FIGS. 2A-2E, together, depict a series of schematic, cross-sectional views of a substrate upon which a gate structure is fabricated using the method of FIG. 1. The cross-sectional views in FIGS. 2A-2E relate to individual processing steps performed to fabricate the gate dielectric. The images in FIGS. 2A-2E are not depicted to scale and are simplified for illustrative purposes. To best understand the invention, the reader should refer simultaneously to FIGS. 1 and 2A-2E.

[0021] The method 100 starts at step 102 and proceeds to step 104.

[0022] At step 104, a silicon (Si) substrate 200 is provided (*e.g.*, 200 mm wafer, 300 mm wafer, and the like) and exposed to a solution for removing a native oxide (S_iO_2) layer 204 from a surface of the substrate (FIG. 2A). Illustratively, the method 100 may be utilized to form a gate structure (not shown) of a transistor. The gate structure is generally disposed, for example, in region 220 above channel region 226 and source and drain regions 222 and 224 (depicted with broken lines) of the transistor. For graphical clarity, regions 220-226 are shown only in FIG. 2A.

[0023] In one embodiment, the layer 204 is removed using a solution comprising hydrogen fluoride (HF) and deionized (DI) water (*i.e.*, a hydrofluoric acid solution). In one embodiment, the solution has between about 0.1 and 10% by weight of HF and a temperature of about 20 - 30 degrees Celsius (°C). In another embodiment, the solution has about 0.5% of HF and a temperature of about 25°C. Step 104 can

use a wet dip of the substrate 200 into the solution, followed by a rinse in de-ionized water, and may be performed in either a single wafer or batch baths, including ultrasonically enhanced baths. Alternatively, step 104 may be performed using a single substrate wet cleaning reactor of the integrated processing system 300. In another embodiment, the layer 204 may be removed using an RCA clean method. Upon completion of step 102, the substrate 200 is placed in a vacuum load lock or nitrogen (N_2) purged environment.

[0024] At step 106, a thermal oxide (S_iO_2) layer 206 is grown on the substrate 200 (FIG. 2B). Generally, the layer 206 may have a thickness between about 2 - 40 Angstroms, preferably between about 2 - 10 Angstroms. In one embodiment, the layer 206 has a thickness between about 6 - 10 Angstroms. Step 106 can be performed using, *e.g.*, a RADIANCE® rapid thermal processing (RTP) reactor, a decoupled plasma oxidation (DPO) reactor, or a plasma enhanced chemical vapor deposition (PECVD) reactor of the integrated processing system 300. The RADIANCE® reactor is available from Applied Materials, Inc., of Santa Clara, California.

[0025] In one embodiment, step 106 may be performed using an RTP reactor to grow the layer 206 by providing oxygen (O_2) at about 0.5 - 10 slm, while maintaining a substrate temperature of about 750 - 850°C, and a pressure in the reaction chamber of about 0.1 - 50 Torr. The duration of the process may be between about 5 - 30 seconds. In one embodiment, O_2 is provided at about 2 slm, while maintaining a temperature of about 800°C and a pressure of about 2 Torr.

[0026] In another embodiment, the layer 206 may be grown in an RTP reactor by providing nitrous oxide (N_2O) at a rate of about 1 - 10 slm and hydrogen (H_2) at a rate of about 10 - 500 sccm (*i.e.,* a N_2O:H_2 flow ratio ranging from about 2:1 - 1000:1) while maintaining a substrate temperature of about 700 - 850°C. Further, step 106 maintains a pressure in the reaction chamber at about 0.5 - 20 Torr. The duration of the process may be between about 5 - 60 seconds. One specific process recipe provides N_2O at a rate of about 4.9 slm and H_2 at a rate of about 50 sccm (*i.e.,* a N_2O:H_2 flaw ratio of about 98:1) at a temperature of about 800°C.

[0027] In another embodiment, step 106 may be performed using a process chamber suitable for producing a low-energy plasma, such as a DPO chamber. The low energy of the plasma helps to control the reaction at the surface of the substrate and/or layer. For example, the plasma may be produced using a quasi-remote plasma source, an inductive plasma source, and/or an RLSA source, among other plasma sources. In alternate embodiments, sources of CW and/or pulsed microwave power, such as magnetron or RLSA microwave sources, may be used to form the layer 206.

[0028] In one embodiment, the layer 206 may be grown in a DPO reactor by exposing the substrate 200 to a plasma containing at least one of oxygen (O_2), nitric oxide (NO), nitrous oxide (N_2O), and the like. In addition, the plasma may optionally contain nitrogen (N_2) and/or an optional inert gas (*e.g.,* argon (Ar), helium (He), and the like).

[0029] In one embodiment, the layer 206 may be formed using a DPO reactor by providing oxygen (O_2) at about 10 - 2000 sccm, a substrate pedestal temperature of about 20 - 500°C, and a pressure in the reaction chamber between about 5 - 1000 m Torr. The radio-frequency (RF) plasma is energized, *e.g.*, at 13.56 MHz, using either a continuous wave (CW) or pulsed plasma power source of up to about 3-5 kW. During pulsing, the peak RF power may be in a range of about 10 - 3000 W, the frequency may be in a range of about 2 - 100 kHz, and the duty cycle may be in a range of about 2 - 50%. This process may be performed for about 1 - 180 sec. In one embodiment, O_2 is provided at about 200 sccm, and about 500 W of peak RF power is pulsed at about 10 kHz with a duty cycle of about 5% applied to an inductive plasma source, at a temperature of about 25°C and a pressure of about 40 - 80 mTorr, for about 15 - 60 sec.

[0030] In a further embodiment, a thermal silicon oxide layer 206 may be deposited using a PE-CVD chamber as described with respect to FIG. 4. Oxygen (O_2), nitric oxide (NO), nitrous oxide (N_2O), or the like is injected via an upper gas injector 435, whereas silane (SiH_4) is injected via a lower gas injector. Other silicon source disclosed in embodiments described herein may alternatively be used. The gases

injected via upper gas injector 435 may be excited by an inductively coupled plasma. The oxygen is excited by a radio-frequency (RF) plasma at for example 13.56 MHz. The plasma source may be either operated in pulsed mode or in a CW mode. In the event pulsed RF plasma is applied, the peak power may be in the range of 10 to 3000 watts. In the event a CW mode plasma is applied, the peak power may be in the range of 10W to 1000W.

[0031] The layer 206 may be grown by providing oxygen at about 10-2000 sccm, a pedestal temperature of about 20°C to 500°C and a pressure in the chamber between 1 and 50 mTorr.

[0032] At optional step 107, the oxide layer 206 may be nitridized. The layer 206 may be nitridized, for example, in a plasma process or in a thermal process. Illustratively, step 107 forms a sub-layer 207 of nitridized material in an upper portion of the layer 206 (FIG. 2C). A thickness of the nitridized sub-layer 207 is typically formed in a range from about 0.5 – 5 Angstroms, preferably about 1 - 3 Angstroms.

[0033] In one embodiment, the layer 206 is exposed to a nitrogen-containing plasma. In one embodiment, the plasma contains nitrogen (N_2), and may optionally contain one or more optional inert gases (*e.g.,* argon (Ar), helium (He), and the like). Step 107 can be performed using, *e.g.,* a decoupled plasma nitridation (DPN) plasma reactor of the integrated processing system 300.

[0034] In one embodiment, the sub-layer 207 may be formed using a DPN reactor by providing nitrogen (N_2) at about 10 - 2000 sccm, a substrate pedestal temperature of about 20 - 500°C, and a pressure in the reaction chamber between about 5 - 1000 mTorr. The radio-frequency (RF) plasma is energized, *e.g.,* at 13.56 MHz, using either a continuous wave (CW) or pulsed plasma power source of up to about 3-5 kW. During pulsing, peak RF power, frequency and a duty cycle are typically selected in the ranges from about 10 - 3000 W, about 2 - 100 kHz, and about 2 - 50%, respectively. This process may be performed for about 1 -180 sec. In one embodiment, N_2 is provided at about 200 sccm, and about 1000 W of peak RF power is pulsed at about 10kHz with a duty cycle of about 5% applied to an inductive plasma source, at a temperature of about 25°C and a pressure of about 40

- 80 mTorr, for about 15 - 60 sec. The plasma may be produced using a quasi-remote plasma source, an inductive plasma source, and a radial line slotted antenna (RLSA) source, among other plasma sources. In alternate embodiments, sources of CW and/or pulsed microwave power may be used to form the sub-layer 207.

[0035] At optional step 107, the thermal oxide layer 206 can also be thermally nitrided by exposing it to an ammonia (NH_3) gas, or a mixture of NH_3 and N_2, or one or more inert gas such as helium, argon, and the like at high temperature in an RTP reactor to form the sub-layer 207 of nitridized material.

[0036] In one embodiment, the sub-layer 207 may be formed using an RTP reactor by providing ammonia (NH_3) gas at 5 to 1000 sccm while maintaining a substrate temperature of 700°C - 1000°C and a pressure in the reactor chamber of about 0.1 - 10Torr. The duration of the process may be between about 5 - 120 seconds. In one embodiment, NH_3 is provided at 100 sccm while maintaining a temperature of about 800°C and a pressure of 0.3 Torr for a time of 15 seconds. Optionally, batch furnaces may be used to form the sub-layer 207.

[0037] At step 108, a gate dielectric layer 208 is deposited over the thermal oxide layer 206 (FIG. 2D). The layer 208 may be formed from silicon nitride (Si_3N_4) to a thickness of about 2 - 20 Angstroms or a high-k material, such as hafnium oxide (Hf02), hafnium silicate (such as Hf_xSi_yO), where x and y are integers), and the like, or a combination thereof, to a thickness of about 10 - 60 Angstroms. Step 108 can be performed using, *e.g.,* a chemical vapor deposition (CVD) reactor or an atomic layer deposition (ALD) reactor of the integrated processing system 300, such as a CVD reactor or an ALD reactor. One suitable CVD reactor is an XGen CVD reactor, available from Applied Materials, Inc.

[0038] In one embodiment, using a CVD reactor, the gate dielectric layer 208 may comprise silicon nitride (Si_3N_4) and may be formed by providing ammonia (NH_3) at about 100 -1000 sccm, silane (SiH_4) at about 1 - 100 sccm (*i.e.,* a NH_3:SiH_4 flow ratio ranging from 1:1 to 1000:1), and nitrogen (N_2) at about 10 - 1000 sccm, while maintaining a substrate pedestal temperature of about 400 - 750°C, and a pressure In the reaction chamber of between about 0.1 -50 Torr. This process may be

performed for about 30 - 180 sec. In one embodiment, NH3 is provided at about 500 sccm, SiH4 at about 10 sccm (*i.e.*:, a NH_3: SiH_4 flow ratio of about 50:1), and N_2 at about 25 sccm, while maintaining a temperature of about 600°C and pressure of about 5 Torr in the chamber. Other silicon source gas or chemical can be used in place of silane (SiH_4) such as disilane (Si_2H_6), dichlorosilane (DCS), trichlorosilane (TCS), tetrachlorosilane (TCS) or hexachlorodisilane (HCD).

[0039] In another embodiment, the gate dielectric layer 208 may comprise hafnium oxide or hafnium silicate and may be deposited using a CVD or an ALO process. The hafnium oxide or hafnium silicate gate dielectric layer 208 may be formed using metal-organic or inorganic precursors of hafnium and silicon with an oxidizer comprising at least one of ozone, water, or remote plasma oxygen radicals.

[0040] In one embodiment, the dielectric layer formed of silicon nitride (Si_3N_4) is deposited in a PE-CVD chamber as described with respect to FIG. 4. Ammonia (NH_3) and/or nitrogen (N_2) is injected via an upper gas injector, whereas silane (SiH_4) is injected via a lower gas injector. According to one embodiment, NH_3 is injected at about 100-1000 sccm and silane is injected at about 1-100 sccm, *i.e.*, at a flow rate ratio ranging from 1:1 to 1000:1. Additionally, N_2 may be injected at a flow rate of 10-1000 sccm. The pedestal is maintained at a temperature of about 400°C to about 750°C and a pressure in the reactor chamber is about 1 mTorr to 50 mTorr, typically about 1 mTorr to 20 mTorr. Other silicon source disclosed in embodiments described herein may alternatively be used.

[0041] NH_3 and/or N_2 are excited by the inductively coupled plasma. The ammonia and/or nitrogen are excited by a radio-frequency (RF) plasma at for example 13.56 MHz. The plasma source may be either operated in pulsed mode or in a CW mode. In the event pulsed RF plasma is applied, the peak power may be in the range of 10 to 3000 watts. In the event a CW mode plasma is applied, the peak power may be in the range of 10W to 1000W.

[0042] At step 110, the gate dielectric layer 208 is oxidized by exposure to an oxygen-containing plasma. Illustratively, step 110 forms a sub-layer 210 of oxidized material in an upper portion of the layer 208 (FIG. 2E). A thickness of the oxidized

sub-layer 210 is typically selected in a range from about 0.2 - 10 Angstroms, preferably about 0.5 - 5 Angstroms.

[0043] In one embodiment, the plasma contains at least one of oxygen (O_2), nitric oxide (NO), nitrous oxide (N_2O), and the like, as well as may contain optional nitrogen (N_2) and/or an optional inert gas (*e.g.,* argon (Ar), helium (He), and the like). Step 110 may be performed using a process chamber suitable for producing a low-energy plasma. The low energy of the plasma helps to control the reaction at the surface of the substrate and/or layer. For example, the plasma may be produced using a quasi-remote plasma source, an inductive plasma source, and/or an RLSA source, among other plasma sources. In alternate embodiments, sources of CW and/or pulsed microwave power, such as magnetron or RLSA microwave sources, may be used to form the sub-layer 210. In one embodiment, step 110 may be performed using, *e.g.,* the DPN plasma reactor of the integrated processing system 300.

[0044] The sub-layer 210 may be formed by providing oxygen (O_2) at about 10 - 2000 sccm. The oxygen may optionally be mixed with N_2 and/or He and/or Ar. The substrate pedestal temperature is maintained at about 20 - 500°C, and the pressure in the reaction chamber may be between about 5 - 1000 mTorr. The radio frequency (RF) plasma is energized, *e.g.,* at about 13.56 MHz, using either a continuous wave (CW) or pulsed plasma power source of up to about 3-5 kW. During pulsing, peak RF power, frequency and a duty cycle are typically selected in the ranges from about 10 - 3000 W, about 2 - 100 kHz, and about 2 - 50%, respectively. The oxidation process may be performed for about 1 - 180 seconds. In one embodiment, O_2 is provided at about 200 sccm, with about 1000 W of peak RF power pulsed at about 10 kHz with a duty cycle of about 5% applied to an inductive plasma source, at a temperature of about 25°C and a pressure of about 40 mTorr for about 30 seconds.

[0045] In one embodiment, additionally or alternatively to oxidizing the gate dielectric layer, a silicon oxide layer is grown on the silicon nitride dielectric layer 208. A thermal silicon oxide layer is deposited using a PE-CVD chamber as described with

respect to FIG. 4. Oxygen (O_2), nitric oxide (NO), nitrous oxide (N_2O), or the like is excited by an inductively coupled plasma, the gas being injected from an upper gas injection, while a silicon source (*e.g.* silane) is provided by a lower gas inject. Other silicon source disclosed in embodiments described herein may alternatively be used. The plasma source may either be operated in pulsed mode or a CW mode. The silicon oxide layer on top of the silicon nitride layer is deposited with a thickness in the range of 2-20 Angstrom and may be grown by providing oxygen at about 10-2000 sccm, a pedestal temperature of about 20°C to 500 °C and a pressure in the chamber between 1 and 50 mTorr. The oxygen is excited by a radio-frequency (RF) plasma at for example 13.56 MHz. In the event pulsed RF plasma is applied, the peak power may be in the range of 10 to 3000 watts. In the event a CW mode plasma is applied, the peak power may be in the range of 10W to 1000W.

[0046] According to the embodiments related to steps 106, 108, and 110 being conducted in a PE-CVD chamber, as for example disclosed in FIG. 4, the stack of SiO_2, Si_3N_4, and SiO_2 may be deposited in the same chamber. The steps of depositing the layers in the stack may optionally be conducted with plasma assistance. The plasma enhanced process allows lower substrate temperatures.

[0047] The chamber arrangement including the evacuation unit for low pressures, the plasma source 410, and the lower chamber body 420 allows for growth of thin layers such that the gate dielectric stack formed of SiO_2, Si_3N_4, and SiO_2 may be thermally deposited.

[0048] At step 112, the gate dielectric layer 208 and oxide/silicon interface between the layer 206 and substrate 200 are annealed. Step 112 improves the leakage current reduction of the layers 206 and 210 and increases the mobility of charge carriers in the channel region 226 (shown in FIG. 2A), as well as improves reliability of the oxide/silicon interface. Step 112 can be performed using a suitable thermal annealing chamber, such as an RTP (*e.g.*, a RADIANCE® or RTP XE+) reactor of the integrated processing system 300, or either a single substrate or batch furnace.

[0049] In one embodiment, the annealing process of step 112 may performed by providing at least one of oxygen (O_2) at about 2 - 5000 sccm and nitric oxide (NO) at about 100 - 5000 sccm, either gas optionally mixed with nitrogen (N_2), while maintaining a substrate surface temperature of about 800 - 1100°C, and a pressure in the reaction chamber of about 0.1 - 50 Torr. The process may be performed for about 5 - 180 seconds. In one embodiment, O_2 is provided at about 500 sccm while maintaining the chamber at a temperature of about 1000°C and a pressure of about 0.1 Torr, for a duration of about 15 seconds. In another embodiment, NO is provided at about 500 sccm, while maintaining the chamber at a temperature of about 1000°C and a pressure of about 0.5 Torr, for duration of about 15 seconds.

[0050] Upon completion of step 112, at step 114, method 100 ends. In the manufacture of integrated circuits, the method 100 advantageously forms ultra-thin gate dielectrics representing high resistivity paths for leakage currents and facilitates high mobility of charge carriers in the channel regions of the field effect transistors.

[0051] FIG. 3 depicts a schematic diagram of the exemplary CENTURA® integrated semiconductor substrate processing system (*e.g.,* cluster tool) 300 of the kind that may be used to practice portions of the method 100 of FIG. 1. The particular embodiment of the system 300 is illustrative only and should not be used to limit the scope of the invention. It is contemplated that the method 100 may be practiced using other semiconductor substrate processing systems and/or processing reactors.

[0052] The integrated processing system 300 generally includes vacuum load-lock chambers 322, a vacuum-tight plenum 328 having a robot 330 supplied with a substrate receptacle 334, process modules 310, 312, 314, 316, and 318 coupled to the plenum 328, an input/output module 302, an optional metrology module 326, and a system controller 340. The load-lock chambers 322 are used as docking stations for substrate cassettes and protect the plenum 328 from atmospheric contaminants. The robot 330 transfers the substrates between the load lock chambers and process modules. The depicted embodiment of the robot 330 is exemplary and should not limit the scope of the invention. The input/output module 302 comprises at least one

front opening unified pod (FOUP) 306 (two FOUPs 306 are depicted) facilitating an exchange of the substrate cassettes between a factory interface 324, the metrology module 326, and the load-lock chambers 322.

[0053] The system controller 340 generally comprises a central processing unit (CPU) 342, a memory 344, and support circuits 346 and is coupled to and controls modules and apparatus of the integrated processing system 300, as well as enables data collection and feedback from the respective modules to optimize performance of the system 300. In operation, the controller 340 uses a direct control of modules and apparatus of the system 300 or, alternatively, administers computers (or controllers) associated with these modules and apparatuses.

[0054] At least one of the processing modules 310, 312, 314, 316, and 318 may be an RTP reactor (*e.g.*, a RADIANCE® reactor), a PECVD reactor, a CVD reactor (*e.g.,* an XGen reactor), an ALD reactor, a DPN reactor, and/or other reactor suitable for performing the processes described above on reference to FIG. 1. One example of a possible configuration of the system 300 for performing processes in accordance with the present invention includes two load-lock· chambers 322, two RTP modules 310 and 312, an ALD module 314, a CVD module 316, a DPN module 318, a metrology module 326 comprising a measuring tool 304 and robots 308 and 320, and the input/output module 302 comprising two FOUPs 306. It is contemplated that other configurations of the system 300 may also be utilized to practice the invention described herein.

[0055] FIG. 4 depicts a schematic diagram of exemplary PE-CVD chamber 400. A decoupled plasma nitridation (DPN) plasma source 410 is provided above processing region 402 of lower chamber body 420. Chamber walls 422 surround the processing region 402. Substrate 401 is located on pedestal 424. Pedestal 424 has a stem 450 including connections for a dual zone heater of the pedestal. Details related to a dual zone heater pedestal are described in more detail in U.S. Patent No. 6,646,235, filed October 19, 2001, which is herein incorporated by reference in its entirety.

[0056] The coil 412 spirals around the vertical axis of the upper wall of the dome of the plasma source. The coil 412 is positioned over electrode plate 18 and conforms to the dome shape. One end of the coil 412 is connected to an RF source 462, and an opposing end of the coil is connected to ground. According to one embodiment, an RF match circuit 464 may be provided between the RF source 462 and the coil 412.

[0057] The RF source 462 may be operated to provide RF current to the coil 412 at a frequency of for example 13.56 MHz. A power of 0 to 3000 watts may be applied. The RF field couples with the nitrogen gas or oxygen gas injected into the gas inject 435. Gas inject 435 may inject N_2, NH_3, or the like. Further, gas inject 435 may inject oxygen (O_2), nitric oxide (NO), or nitrous oxide (N_2O) in the case oxides are grown. RF source 462 may either be operated in a pulsed mode or in a CW mode.

[0058] The gas injected by gas inject 435 and ionized by the RF plasma and the deposition gas injected by deposition gas inject 430 reacts in the processing region 402 and/or on the heated wafer surface for thermal deposition of a layer on the substrate.

[0059] Turbo pump 440 is connected to the chamber body 420 via valve 442 and via gas exhaust 443. In one embodiment valve 442 may be a throttle valve. Turbo pump 440 can reduce the pressure in the chamber to a level appropriate for the desired growth conditions on the substrate 401. The pressure in the processing region is, according to one embodiment, controlled to be below about 30 mTorr, typically from about 1 mTorr and about 20 mTorr.

[0060] The above described embodiment allows for example for growth of silicon with excited nitrogen (N_2), ammonia (NH_3), oxygen (O_2), nitric oxide (NO), or nitrous oxide (N_2O). Nitrogen and/or NH_3 are used to deposit a silicon nitride layer. O_2, NO, and/or N_2O are used to deposit a silicon oxide layer. The gases introduced from the upper gas inject 435 can be excited with a pulsed RF inductive source before mixing with the silicon source. Thereby, plasma enhanced CVD can be conducted at a lower wafer temperature.

[0061] Further details of a chamber that may be included in chamber 400 to form further embodiments are described in more detail in U.S. Patent No. 6,831,021, filed June 12, 2003, which is herein incorporated by reference in its entirety.

[0062] The invention may be practiced using other processes where parameters may be adjusted to achieve acceptable characteristics by those skilled in the art by utilizing the teachings disclosed herein without departing from the spirit of the invention. Although the forgoing discussion referred to fabrication of a field effect transistor, fabrication of the other devices and structures used in integrated circuits can also benefit from the invention.

[0063] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims:

1. A method for fabricating a gate dielectric of a field effect transistor, comprising:

(a) providing a silicon substrate;

(b) removing a native oxide layer from the silicon substrate;

(c) forming a first oxide layer on the silicon substrate;

(d) forming a gate dielectric layer on the first oxide layer;

(e) forming a second oxide layer on the gate dielectric layer; and

(f) annealing the gate dielectric layer, the first oxide layer, and an interface between the first oxide layer and the silicon substrate.

2. The method of claim 1, further comprising:

maintaining the silicon substrate in a single chamber from step (c) through step (e).

3. The method of claim 1, wherein step (c) further comprises:

depositing the first oxide layer to a thickness between about 2 -10 Angstroms.

4. The method of claim 1, wherein step (c) further comprises:

exposing the first oxide layer to a plasma comprising at least one of oxygen, nitric oxide, or nitrous oxide generated by a decoupled plasma source.

5. The method of claim 1, wherein step (c) further comprises:

nitridizing the first oxide layer.

6. The method of claim 5, wherein the step of nitridizing further comprises:

creating a sub-layer of nitridized material in the first oxide layer, the sub-layer having a thickness between about 0.5 - 3 Angstroms.

7. The method of claim 5, wherein nitridizing the first oxide layer comprises:

exposing the first oxide layer to nitrogen-containing plasma.

8. The method of claim 1, wherein step (d) further comprises:

forming the gate dielectric layer from at least one of silicon nitride, hafnium oxide, and hafnium silicate.

9. The method of claim 8, wherein step (d) further comprises:

forming the gate dielectric layer from at least one of hafnium oxide or hafnium silicate to a thickness of about 10 - 60 Angstroms.

10. The method of claim 8, further comprising:

forming the gate dielectric layer from silicon nitride to a thickness of about 2 - 10 Angstroms.

11. The method of claim 1, wherein step (d) further comprises:

forming the gate dielectric layer in a plasma enhanced process.

12. The method of claim 1, wherein the second oxide layer has a thickness between about 2 – 10 Angstroms.

13. The method of claim 1, wherein step (e) further comprises:

forming a plasma using a low energy plasma source.

14. The method of claim 1, wherein step (f) further comprises:

thermally annealing the substrate in a rapid thermal processing chamber or a furnace.

15. A method for fabricating a gate dielectric of a field effect transistor upon a substrate, comprising:

(a) removing a native oxide layer from the substrate and placing the substrate in a nitrogen purged or vacuum environment;

(b) forming a first thermal oxide layer on the substrate;

(c) forming a gate dielectric layer on the first thermal oxide layer;

(d) forming a second thermal oxide layer on the gate dielectric layer; and

(e) thermally annealing the substrate having the first thermal oxide layer and the oxidized gate dielectric layer formed thereon.

16. The method of claim 15, further comprising:

nitridizing the first thermal oxide layer prior to step (c).

17. The method of claim 15, further comprising:

nitridizing the gate dielectric layer prior to step (d).

18. An integrated semiconductor substrate processing system for fabricating a gate dielectric of a field effect transistor, comprising:

a reactor configured for forming a thermal oxide layer on a silicon substrate, the reactor being configured for depositing a gate dielectric layer on the thermal oxide layer and being configured for forming a thermal oxide layer on the gate dielectric layer;

a decoupled plasma source ;

one or more load lock chambers;

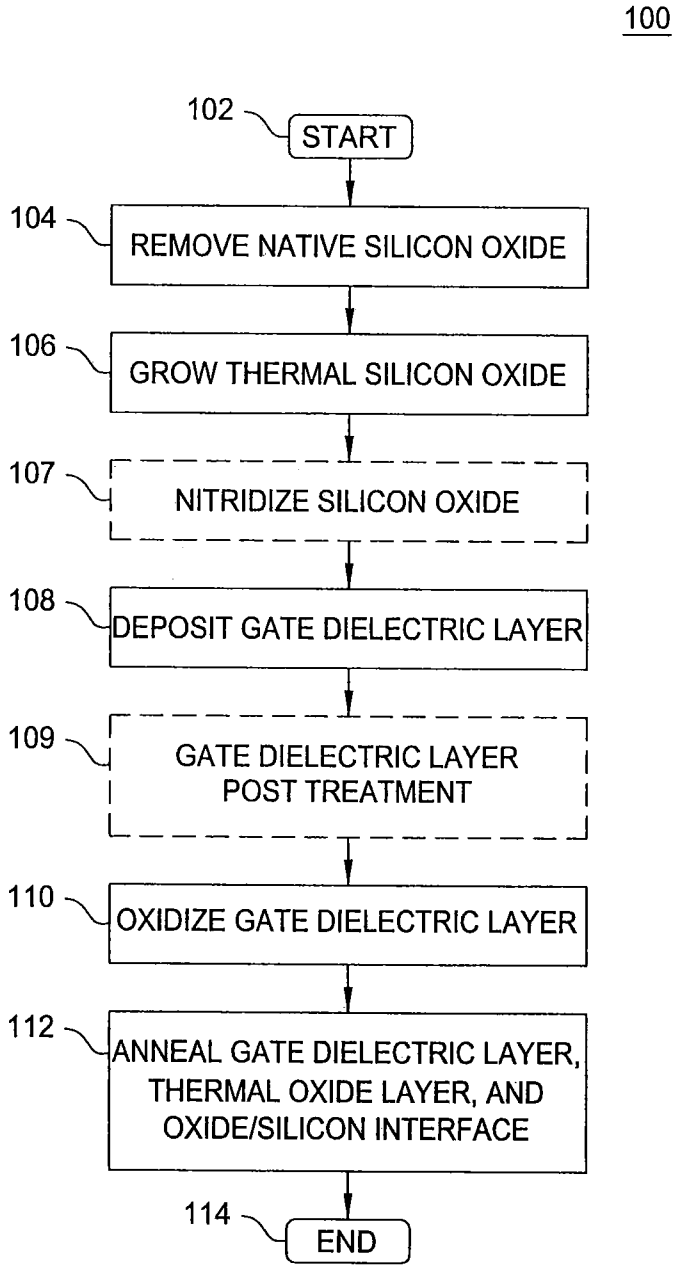
at least one substrate transfer chamber coupled to the reactor and the load lock chambers; and

a controller for administering and monitoring operation of the processing system.

19. The integrated semiconductor substrate processing system of claim 18, further comprising:

an upper gas inject and a lower gas inject.

20. The integrated semiconductor substrate processing system of claim 19, wherein the lower gas inject is provided below the decoupled plasma source and the upper gas inject is provided above the decoupled plasma source.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102
START
104
REMOVE NATIVE SILICON OXIDE
106
GROW THERMAL SILICON OXIDE
107
NITRIDIZE SILICON OXIDE
108
DEPOSIT GATE DIELECTRIC LAYER
109
GATE DIELECTRIC LAYER POST TREATMENT
110
OXIDIZE GATE DIELECTRIC LAYER
112
ANNEAL GATE DIELECTRIC LAYER, THERMAL OXIDE LAYER, AND OXIDE/SILICON INTERFACE
114
END

FIG. 1

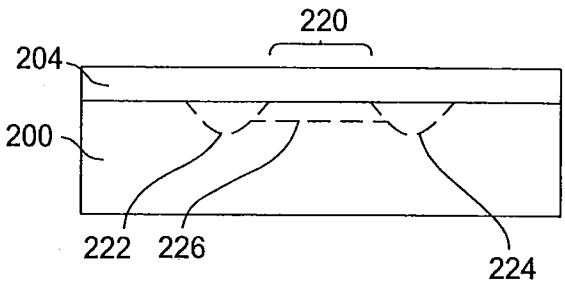


FIG. 2A

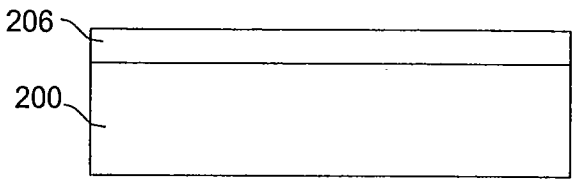


FIG. 2B

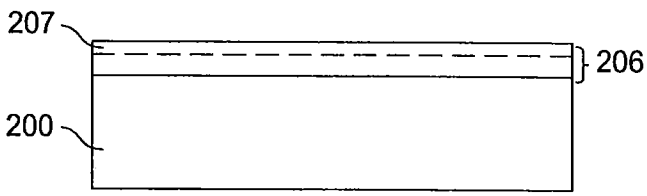


FIG. 2C

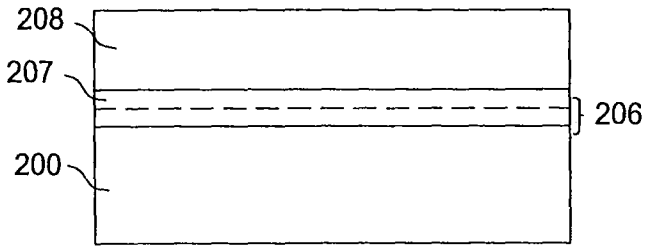


FIG. 2D

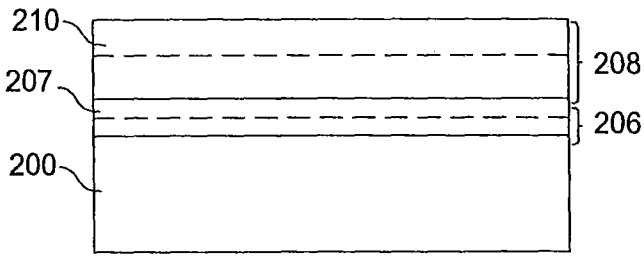
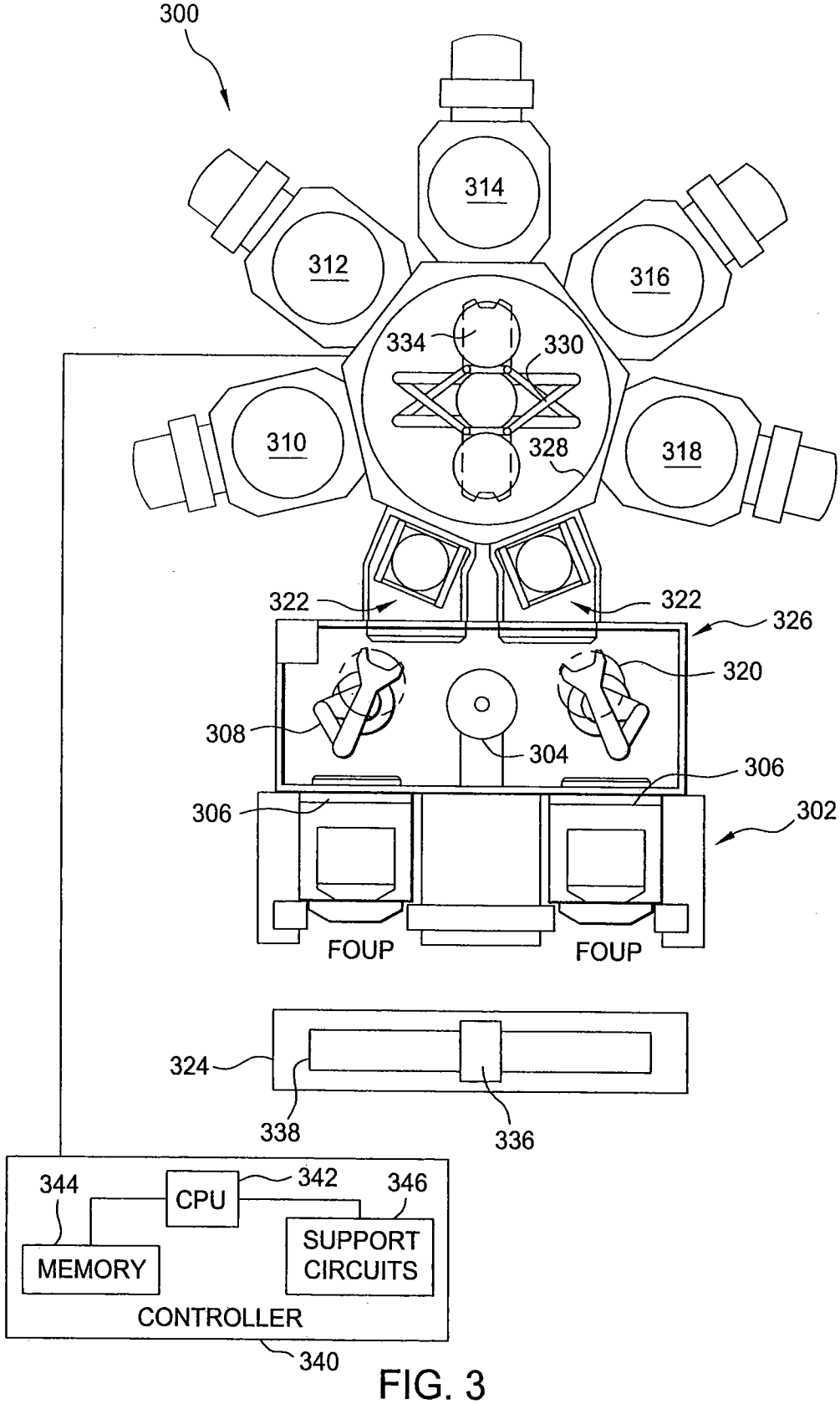


FIG. 2E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FOUP
FOUP
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SUPPORT CIRCUITS
MEMORY
CONTROLLER
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FIG. 3

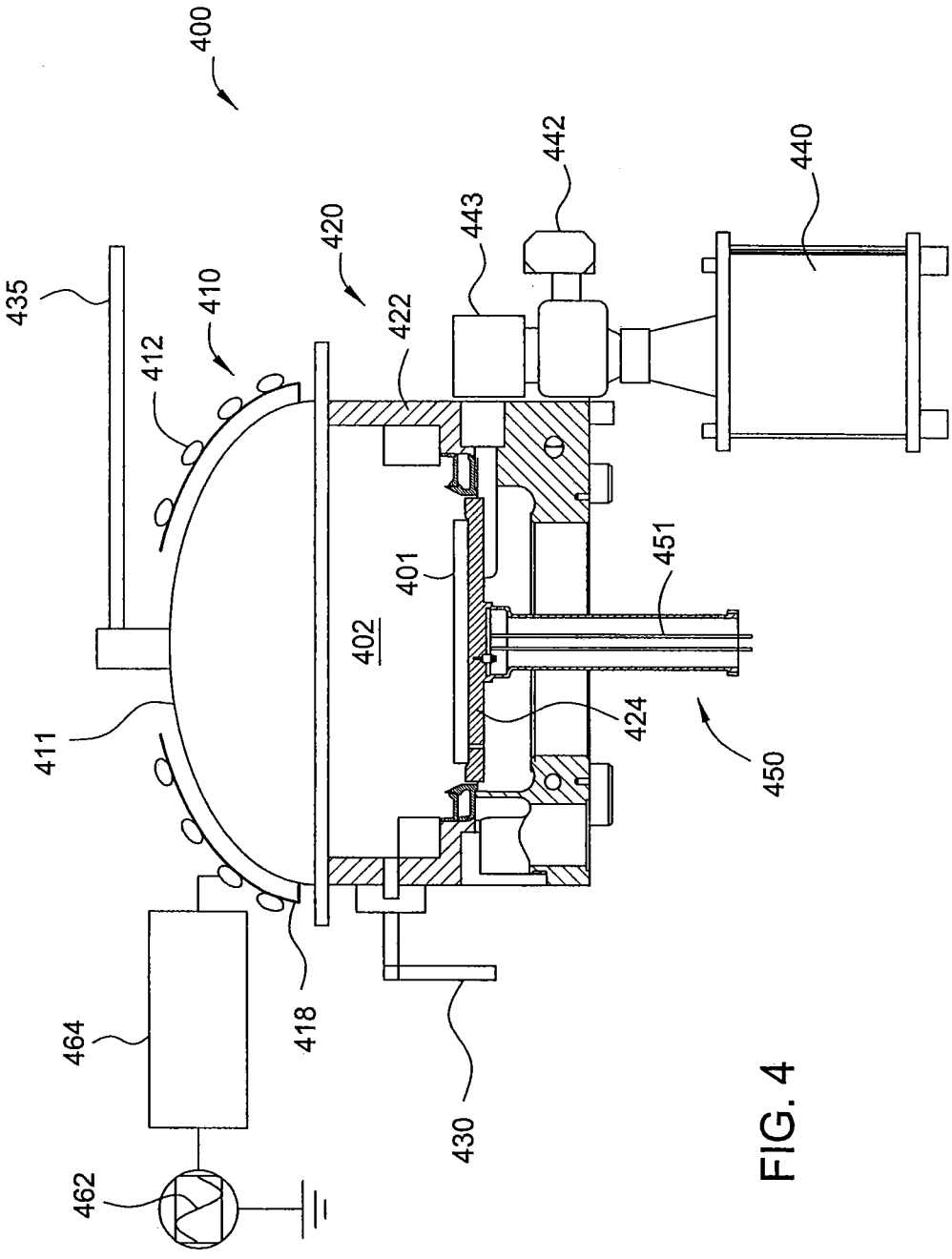
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FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/68056

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/8234; H01L 21/336 (2007.01)
USPC - 438/197; 438/287
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC (8) - H01L 21/8234; H01L 21/336 (2007.01)
USPC - 438/197; 438/287

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 438

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PUBWEST (PGPB,USPT,USOC,EPAB,JPAB) Terms - nitriding dielectric hafnium HfO reactor
Google - Method for Fabricating a Gate Dielectric of a Field Effect Transistor; Gate Dielectric Field Effect Transistor nitrided; oxide layer on the gate dielectric; load lock chambers

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,991,989 B2 (LEE et al.) 31 January 2006 (31.01.2006), col 2, ln 50-68; col 3, ln 1-5	1, 3, 5, 8-9, 11 --- 2, 4, 6-7, 10, 12-17
X	US 2005/0136604 A1 (AL-BAYATI et al.) 23 June 2005 (23.06.2005), paragraphs 146, 151, 319, 319, 337, FIG. 2	18-20
Y	US 6,818,517 B1 (MAES) 16 November 2004 (16.11.2004), col 1, ln 35-39; col 2, ln 53-54; col 3, ln 26-30; col 3, ln 36-66; col 5, ln 26-30; col 5, ln 35-37; col 6, ln 20-21; col 7, ln 9-15; col 7, ln 25-26; col 7, ln 38-43	2, 4, 6-7, 10, 12-13, 15-17
Y	US 6,821,868 B2 (CHENG et al.) 23 November 2004 (23.11.2004), col 3, ln 1-4	14

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 Sep 2007 (18.09.2007)	17 OCT 2007

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774