(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 December 2003 (18.12.2003)

PCT

(10) International Publication Number
WO 03/105206 A1

(51) International Patent Classification[7]: H01L 21/285

(21) International Application Number: PCT/US03/18140

(22) International Filing Date: 10 June 2003 (10.06.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/387,867 10 June 2002 (10.06.2002) US

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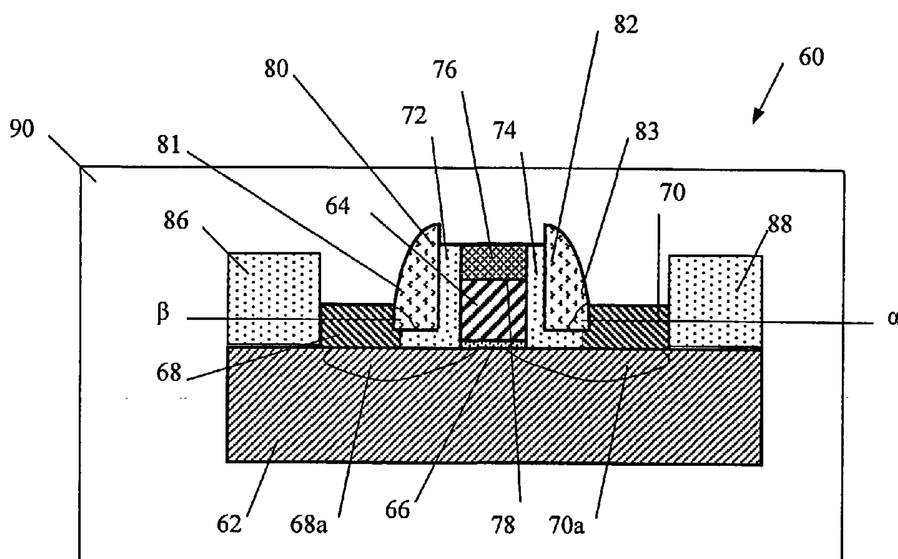
(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

[Continued on next page]

(54) Title: GROWING SOURCE AND DRAIN ELEMENTS BY SELECIVE EPITAXY



(57) Abstract: Methods for fabricating facetless semiconductor structures using commercially available chemical vapor deposition systems are disclosed herein. A key aspect of the invention includes selectively depositing an epitaxial layer of at least one semiconductor material on the semiconductor substrate while *in situ* doping the epitaxial layer to suppress facet formation. Suppression of faceting during selective epitaxial growth by in situ doping of the epitaxial layer at a predetermined level rather than by manipulating spacer composition and geometry alleviates the stringent requirements on the device design and increases tolerance to variability during the spacer fabrication.

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GROWING SOURCE AND DRAIN ELEMENTS BY SELECTIVE EPITAXY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to and the benefit of U.S. Provisional Application Serial No. 60/387,867 filed June 10, 2002, the entire disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates generally to semiconductor fabrication methods and, more specifically, to methods for fabricating semiconductor devices having substantially facetless raised source and drain elements.

BACKGROUND

[0003] In order to improve performance and packing density of modern microelectronic devices, it is often desirable to reduce channel lengths of metal-oxide-semiconductor-field-effect transistors ("MOSFETs") during device design. As the MOSFET channel length decreases, however, short channel effects and parasitic resistance become of increasing concern. To minimize short channel effects in bulk silicon devices, for example, the source/drain doping junction depths are decreased during scaling. But shallower junctions require the use of thinner silicides to minimize leakage current from the silicon/silicide interface to the junction depletion region, which, at the same time, may increase parasitic contact resistances. As another example, to improve performance of a silicon-on-insulator ("SOI") device by reducing short channel effects, its silicon region should preferably be less than about 20 nm thick. Conventional silicide formation processes, however, may consume substantially the entire silicon layer of such thickness, which may, in turn, result in undesirably large leakage currents and parasitic contact resistance because the silicide/silicon interface area is small.

[0004] The increasing operating speeds and computing power of microelectronic devices have recently given rise to the need for an increase in the complexity and functionality of the semiconductor substrates that are used as the starting substrate in these microelectronic devices. Such "virtual substrates" based on silicon and germanium provide a platform for new

generations of VLSI devices that exhibit enhanced performance when compared to devices fabricated on bulk Si substrates. Specifically, new technological advances enable formation of heterostructures using silicon- germanium alloys (hereinafter referred to as "SiGe" or "$Si_{1-x}Ge_x$") to further increase performance of the semiconductor devices by changing the atomic structure of Si to increase electron mobility. These substrates are called strained Si substrates.

[0005] A strained Si substrate is generally formed by a first epitaxial growth of a relaxed SiGe layer on bulk Si, and then a second epitaxial growth of a thin (less than about 500 Å) Si layer on the relaxed SiGe layer. Because the lattice constant of relaxed SiGe heterostructure is different from Si, the thin Si layer becomes "strained," resulting in enhanced mobilities (and hence improved device speeds) over bulk Si. The percentage of Ge in SiGe, and the method of deposition can have a dramatic effect on the characteristics of the strained Si layer. U.S. Patent No. 5,442,205, "Semiconductor Heterostructure Devices with Strained Semiconductor Layers," incorporated herein by reference, demonstrates one such method of producing a strained Si device structure.

[0006] A method of epitaxially growing a relaxed SiGe layer on bulk Si is discussed in international application WO 01/22482, "Method of Producing Relaxed Silicon Germanium Layers," incorporated herein by reference. The method includes providing a monocrystalline Si substrate, and then epitaxially growing a graded $Si_{1-x}Ge_x$ layer with increasing Ge concentration at a gradient of less than 25% Ge per micron to a final composition in the range of $0.1 < x < 1$, using a source gas of $Ge_xH_yCl_z$ for the Ge component, on the Si substrate at a temperature in excess of 850 °C, and then epitaxially growing a semiconductor material on the graded layer.

[0007] Another method of epitaxially growing a relaxed SiGe layer on bulk Si is discussed in a paper entitled, "Low Energy plasma enhanced chemical vapor deposition," by M. Kummer et. al. (Mat. Sci. & Eng. B89, 2002, pp. 288-95), incorporated herein by reference, in which a method of low-energy plasma-enhanced chemical vapor deposition (LEPECVD) is shown, which allows the formation of a SiGe layer on bulk Si at high growth rates (0.6 micron per minute) and low temperatures (500-750 °C).

[0008] To grow a high-quality, thin, epitaxial strained Si layer on a graded SiGe layer, the SiGe layer is, preferably, planarized to reduce the surface roughness in the final strained Si substrate. Current methods of chemical mechanical polishing (CMP) are typically used to improve the planarity of surfaces in semiconductor fabrication processes. U.S. Patent No. 6,107,653, "Controlling Threading Dislocations in Ge on Si Using Graded GeSi Layers and

Planarization," incorporated herein by reference, describes how planarization can be used to improve the quality of SiGe graded layers.

[0009] Although the resulting biaxial tensile or compressive strain alters the carrier mobilities in the layers of the "virtual substrate" enabling the fabrication of high-speed and/or low-power devices, short channel effects and parasitic resistance remain of concern for strained-Si-based devices as well.

[0010] Raised source/drain structures have been proposed as a technique for forming high-quality contacts to improve performance of bulk silicon, silicon-on-insulator (SOI), and strained silicon devices. Raised source/drains are generally fabricated by raising the level of the source and drain regions by selective semiconductor, e.g., silicon, deposition. The extra silicon increases the process margin for the silicide process and extends the latitude for contact junction design. To maintain a similar crystalline structure, the extra silicon is "grown" by silicon epitaxy.

[0011] For example, in bulk and strained Si devices, raised source/drain contacts have been proposed as a means of forming shallow dopant junctions to minimize contact resistances and short channel effects. In SOI devices, the raised source and drain regions provide sacrificial silicon useful for silicide consumption to form low resistance contacts on thin Si films.

[0012] Typically, source and drain regions are formed by selective epitaxial silicon growth after formation of a sidewall dielectric spacer of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), or a combination of both materials. In this process, silicon is epitaxially grown on exposed windows in a dielectric mask while nucleation of polysilicon on the masking material is suppressed during the incubation time by, for example, etching of spurious nuclei on the dielectric material by hydrogen chloride, the mediation of saturation by formation of a number of intermediate chlorine-containing silicon precursors, and passivation of surface defect sites which serve as heterogeneous nucleation centers. Also, selectivity is facilitated by growing for a period of time that is generally shorter than the incubation period needed for polysilicon nucleation on the dielectric mask.

[0013] The dielectric spacer electrically isolates a gate made of, for example, polysilicon, from the source and drain regions. After the selective epitaxial growth step, a heavy low-energy implant forms a doped region, and is followed by a silicidation process for, e.g., low resistance complementary metal-oxide-semiconductor (CMOS) contacts.

[0014] During selective epitaxial growth, however, decreased thickness of the epitaxial layer typically occurs at interfaces between the epitaxial layer and the dielectric spacer or field oxide, where facets form by growth of low-energy crystal planes that minimize the energetically less favorable epitaxial Si/dielectric material interface. Because the raised source/drain regions grow thinner near the dielectric spacer edge, faceting leads to non-planar device layers. This phenomenon raises processing concerns in bulk Si, SOI, and strained Si devices by complicating implementation of selective epitaxial growth in device applications. Specifically, thinner faceted regions cause localized deeper dopant penetration during ion implantation, which increases short channel effects and leakage currents. Also, thinner faceted regions typically result in deeper silicide penetration and greater Si consumption during silicidation. Thus, faceting may result in poor doping profile control and poor silicide depth control, leading to degraded device characteristics and more complex device designs.

[0015] For example, referring to FIG. 1, a cross-sectional transmission electron microscope (XTEM) image illustrates undoped Si layers 10 grown adjacent to reactive ion etched <110>-oriented SiO_2 sidewalls 12. The SiGe layers 14 were included as markers to track facet development and evolution. The selective Si epitaxy has noticeable (311)-oriented facets 15 and (110)-oriented facets 17 next to SiO_2 sidewalls. Such faceting would be detrimental during implant and silicidation of source and drain regions. Referring to FIG. 2, a silicided source region 20 is formed by selective epitaxial growth on a thin film SOI substrate 22 according to any method known in the art. Such faceted growth leads to deep penetration of a silicide 24 to a buried SiO_2 layer 26. This penetration may dramatically increase the contact resistance because the silicide/silicon channel interfacial area is reduced, which leads to poor device characteristics. The electrical contact to the device channel is made through the area adjacent to the spacer 28, which is only the width of the Si channel. Furthermore, the contact quality may degrade because of incomplete silicide formation if the thickness of consumed Si is insufficient.

[0016] Similarly, in strained-Si-based devices, thinner faceted raised source and drain regions may cause the silicide to penetrate into a relaxed silicon-germanium (SiGe) layer underneath a strained Si layer. This may result in formation of a poor quality silicide because of the rejection of Ge during alloying of the SiGe layer with the silicide metal. This rejection may create high-resistivity regions that compromise the contact quality.

[0017] Facetless selective epitaxial growth is, therefore, desirable for fully realizing the performance advantages of the raised source/drain scheme for fabrication of low-resistance

contacts and shallow junctions in advanced devices that have wide ranging application to Si, SOI, and strained Si technologies.

[0018] Recently, facetless epitaxy has received much attention in the design of raised source/drain contacts for CMOS applications. For example, selective growth in inverse patterns, i.e. using SiO_2 pillars with a Si field as opposed to Si windows in a SiO_2 field, has been proposed. Another approach involves fabrication of facetless raised source/drain structures by selective epitaxial growth in commercially available low-pressure and atmospheric-pressure chemical vapor deposition systems by carefully controlling the geometry of the multilayer spacer structure and sidewall spacer profile. For example, it has been suggested that undercutting the liner oxide and silicon growth under the silicon nitride spacer recesses the silicon-liner oxide interaction away from the source/drain region. This gives extra thickness in the source/drain region before the increase in silicon-dielectric interface energy causes the epitaxial layer to facet.

[0019] In yet another approach, discussed in a thesis entitled "Selective SiGe Nanostructures" by Tom Langdo (Ph.D. Thesis, MIT, 2001)("Langdo thesis"), incorporated herein by reference, facetless growth was demonstrated by *in situ* n-type doping of a silicon layer being deposited by selective epitaxy adjacent to a sidewall of a reactive ion etched SiO_2 spacer in a ultra-high vacuum chemical vapor deposition (UHVCVD) system. It was demonstrated that a combination of moderate n-type doping and relatively vertical SiO_2 sidewalls results in facet-free epitaxy along <110>-oriented SiO_2 sidewalls. Referring to FIG. 3, an XTEM image illustrates growth of $1x10^{18}/cm^3$ n-type doped Si with $Si_{0.9}Ge_{0.1}$ marker layers on <110>-oriented SiO_2 sidewalls. As shown in FIG. 3, all $Si_{0.9}Ge_{0.1}$ marker layers follow (100) planes, and thus, facet formation is suppressed during the growth. SiO_2 was chosen as the sidewall material instead of more commonly used Si_3N_4 because selective growth generally cannot be achieved with either SiH_4 or SiH_2Cl_2 source gases, common Si precursors, on Si_3N_4 spacers without the addition of hydrogen chloride. Because of the deleterious effects of chloride on a UHVCVD system, however, addition of hydrogen chloride to the source gases is impractical.

[0020] Obstacles hinder the commercialization of this UHVCVD growth approach. First, UHVCVD is generally not feasible for large-scale commercial applications. Second, UHVCVD selective growth is not possible with Si_3N_4 dielectric materials. Finally, the UHVCVD process described above is generally not compatible with multi-layered commercial spacer structures that include, e.g., Si_3N_4 materials.

[0021] Thus, there remains a need in the art for a process of fabricating semiconductor devices having facetless raised source/drain structures that is compatible with existing semiconductor manufacturing processes, systems, and materials and that also possesses improved process tolerances.

5 *SUMMARY OF THE INVENTION*

[0022] It is an object of the present invention to provide a process for fabricating facetless semiconductor structures that overcomes the limitations of known processes. Specifically, it is an object of the invention to provide a process for fabricating semiconductor devices having facetless raised source/drain structures that complements existing epitaxial processes and does
10 not require stringent control of the geometry of the dielectric regions. It is also desirable that such process be less expensive in comparison to the manufacturing processes known in the art and not limited to a particular dielectric or semiconductor material.

[0023] Accordingly, methods for fabricating facetless semiconductor structures using commercially available chemical vapor deposition systems are disclosed herein. A key aspect of
15 the invention includes selectively depositing an epitaxial layer of at least one semiconductor material on the semiconductor substrate while *in situ* doping the epitaxial layer to suppress facet formation. Suppression of facet formation during selective epitaxial growth by *in situ* doping of the epitaxial layer at a predetermined level rather than by manipulating spacer composition and geometry alleviates the stringent requirements on the device design. For example, in various
20 embodiments of the fabrication methods according to the invention, it is not necessary to precisely control the liner oxide undercut beneath the silicon nitride spacer prior to epitaxial growth to minimize faceting, thus making the process more robust and compatible with very thin spacer dimensions. Accordingly, *in situ* doping during epitaxial growth to suppress faceting increases tolerance to variability during the spacer fabrication, providing an improved robust
25 process suitable for volume manufacturing.

[0024] Throughout the following description, the term "facet" is used to refer generally to a slanted low-energy crystal plane formed in a semiconductor material at its interface with a dielectric material. Further, the term "epitaxy" is used to refer generally to methods for growing thin layers of single crystal materials on a single crystal substrate whereby crystallographic
30 structure of the substrate is reproduced in the deposited material. Also, the term "MOS" is used to refer generally to semiconductor devices that include a conductive gate spaced at least by an

insulating layer from a semiconducting channel layer. Conversely, the terms "MOSFET" or "MOS transistor" refer to a field-effect transistor having a conductive gate spaced at least by an insulating layer from a semiconducting channel layer. The terms "SiGe" and "$Si_{1-x}Ge_x$" are used interchangeably to refer to silicon-germanium alloys. The term "silicide" is here used to refer to
5 a reaction product of a metal, silicon, and optionally other components, such as germanium. The term "silicide" is also used, less formally, to refer to the reaction product of a metal with an elemental semiconductor, a compound semiconductor or an alloy semiconductor. The term "doping" is used to refer generally to the process of adding impurities to a semiconductor material to achieve desired properties.

10 **[0025]** In general, in one aspect, the invention is directed to a method of fabricating a semiconductor structure including the steps of providing a chamber and providing a semiconductor substrate in the chamber. The semiconductor substrate has a surface including a first portion and a second portion proximal to the first portion. The method of the invention also includes forming a dielectric region on the first portion of the substrate and selectively
15 depositing an epitaxial layer of at least one semiconductor material on the second portion of the substrate while in situ doping the epitaxial layer. The *in situ* doping occurs at a first predetermined level to substantially suppress facet formation thereby forming a substantially facetless semiconductor region. The pressure in the chamber during selective deposition of the epitaxial layer is greater than about 5 Torr.

20 **[0026]** In one embodiment of the invention, the epitaxial layer is deposited in a chemical vapor deposition system, such as, for example, a reduced-pressure chemical vapor deposition system, atmospheric-pressure chemical vapor deposition system, or plasma-enhanced chemical vapor deposition system.

[0027] In another embodiment of the invention, the step of selectively depositing an epitaxial
25 layer includes introducing a source gas into the chamber. The source gas may include at least one precursor gas and a carrier gas, such as, for example hydrogen. According to one feature of this embodiment, the at least one precursor gas includes a silicon precursor gas, such as, for example, silane, disilane, trisilane, or dichlorosilane. According to another feature of this embodiment, the at least one precursor gas includes a germanium precursor gas, such as, for
30 example, germane, digermane, germanium tetrachloride, or germanium dichloride. According to yet another feature of this embodiment, in addition to the at least one precursor gas and a carrier

gas, the source gas also includes an etchant for suppressing nucleation of the at least one semiconductor material over the dielectric region during deposition. The etchant may include hydrogen chloride or chlorine.

[0028] In yet another embodiment of the invention, the epitaxial layer is doped by adding a dopant to the epitaxial layer during deposition of the epitaxial layer. Examples of suitable dopants are phosphorus, arsenic, antimony, and boron. The dopant may be added to the epitaxial layer by introducing a dopant gas, such as phosphine, arsine, stibine, and diborane, into the chamber. According to one feature of this embodiment, the first predetermined level of doping ranges from about 10^{17} to about 10^{19} cm^{-3}

[0029] The epitaxial layer may include at least one of silicon and germanium. Also, the dielectric region may include at least one of silicon oxide and silicon nitride. Optionally, the dielectric region may have a two-layered spacer structure including a silicon oxide layer and a silicon nitride layer disposed thereon.

[0030] In some embodiments of the invention, the semiconductor substrate includes silicon. In other embodiments, the semiconductor substrate may include a silicon wafer; an insulating layer disposed thereon; and a strained semiconductor layer, for example, silicon or germanium, disposed on the insulating layer. Alternatively, the semiconductor substrate may include a silicon wafer; a compositionally uniform relaxed $Si_{1-x}Ge_x$ layer deposited thereon; and a strained silicon layer deposited on the relaxed $Si_{1-x}Ge_x$ layer. In this embodiment, the semiconductor substrate may also include a compositionally graded $Si_{1-x}Ge_x$ layer disposed between the compositionally uniform relaxed $Si_{1-x}Ge_x$ layer and the silicon wafer, or an insulating layer disposed between the compositionally uniform relaxed $Si_{1-x}Ge_x$ layer and the silicon wafer.

[0031] In still another embodiment of the invention, the temperature in the chamber during selective deposition of the epitaxial layer ranges from about 300 °C to about 900 °C, for example, from about 500 °C to about 700 °C. Also, the epitaxial layer may be deposited at a rate greater than about 1 nm/min.

[0032] In one embodiment of the invention, the method includes the steps of fabricating an n-channel MOSFET in a first portion of the semiconductor region; and fabricating a p-channel MOSFET in a second portion of the semiconductor region. According to one feature of this embodiment, the method includes counter-doping the first portion or the second portion at a

second predetermined level. Optionally, the first predetermined level of doping does not exceed the second predetermined level of doping.

[0033] In some embodiments, the method of the invention also includes forming a metal silicide layer over the semiconductor region. The surface of the semiconductor substrate may have a substantially (100) crystallographic orientation. Also, the dielectric region may include a sidewall having an angle relative to the semiconductor substrate that ranges from about 60° to about 90°. The sidewall may be substantially aligned with either the <110> crystallographic plane or the <100> crystallographic plane of the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

FIG. 1 depicts an XTEM image illustrating faceted selective epitaxial growth of alternating Si and SiGe layers proximate a sidewall of a SiO_2 spacer according to methods known in the art

FIG. 2 depicts a cross-sectional schematic view of a semiconductor device having a faceted raised source region according to methods known in the art;

FIG. 3 depicts an XTEM image illustrating facetless selective epitaxial growth according to one method known in the art;

FIG. 4 depicts a cross-sectional view of a semiconductor substrate suitable for use with various embodiments of the invention;

FIG. 5 depicts a cross-sectional view of a semiconductor device having selectively grown and *in situ* doped facetless Si source/drain epitaxial layers according to the invention; and

FIG. 6 depicts a cross-sectional view of the device of FIG. 5 after silicidation of the source/drain epitaxial layers.

DETAILED DESCRIPTION

[0035] In various embodiments of the invention, facetless semiconductor structures, for example, raised source and drain elements of a MOSFET, are fabricated by selective epitaxial growth proximate commonly used spacer structures, such as those including Si_3N_4, SiO_2, or both,

using commercially available chemical vapor deposition systems. Facet formation in the epitaxial layer is suppressed by doping the epitaxial layer at a predetermined level *in situ* during epitaxial growth, which increases tolerance to variability during the spacer fabrication process.

[0036] Referring to FIG. 4, a substrate 40 suitable for use with the invention, comprises a semiconductor, such as silicon or silicon deposited over an insulator, such as, for example, SiO_2. In one embodiment, several layers collectively indicated as 42 are formed on the substrate 40. The layers 42 may be grown, for example, in a CVD system, including a reduced-pressure chemical vapor deposition system (LPCVD), atmospheric-pressure chemical vapor deposition system (APCVD), and plasma-enhanced chemical vapor deposition system (PECVD). In this embodiment, the layers 42 and the substrate 40 may be referred to together as a "semiconductor substrate 44."

[0037] The layers 42 include a graded layer 46 disposed over the substrate 40. The graded layer 46 may include SiGe with a grading rate of, for example, 10% Ge/µm of thickness, with a thickness T1 of, for example, 2 - 9 µm, and grown, for example, at 600 - 1100 °C. A relaxed layer 48 is disposed over the graded layer 46. The relaxed layer 48 may include, for example, $Si_{1-x}Ge_x$ with a uniform composition containing, for example, 20 - 90% Ge, (i.e., $0.2 \leq x \leq 0.9$) having a thickness T2 ranging from, e.g., about 0.2 µm to about 2 µm. In an alternative embodiment, the relaxed layer 48 may be formed directly on the substrate 40, without the graded layer 46.

[0038] A tensilely strained layer 50 is disposed over relaxed layer 48, sharing an interface therewith. In one embodiment, the tensilely strained layer 50 is formed of silicon. In other embodiments, the tensilely strained layer 50 may be formed of SiGe, or at least one of a group II, a group III, a group V, and a group VI element. The tensilely strained layer 50 may have a starting thickness T3 ranging, for example, from about 50 angstroms to about 300 angstroms (Å).

[0039] In some embodiments, a compressively strained layer (not shown) may be disposed between the relaxed layer 48 and the tensilely strained layer 50. In an embodiment, the compressively strained layer includes $Si_{1-y}Ge_y$ with a Ge content (y) higher than the Ge content (x) of the relaxed $Si_{1-x}Ge_x$ layer 48. The compressively strained layer may contain, for example 40 - 100% Ge and have a thickness ranging, e.g., from about 10 angstroms to about 200 angstroms (Å).

[0040] Referring to FIG. 5, in one embodiment, a semiconductor device, such as, for example, a transistor 60 having facetless raised source/drain regions is fabricated in a chamber 90 of a chemical vapor deposition system, such as, for example, LPCVD, APCVD, or PECVD system. The transistor 60 is formed on a semiconductor substrate 62 including, for example, silicon, silicon-on-insulator, or strained silicon, as described in detail above. The surface of the semiconductor substrate may have a substantially (100) crystallographic orientation.

[0041] In a particular variation of this embodiment of the invention, prior to MOSFET fabrication, the substrate 62 is cleaned using, for example, a dilute RCA process known in the art, in order to remove organic contaminants, particles, and any ionic or heavy metal contaminants from the substrate surface. Alternatively, or in addition to the RCA cleaning, the surface of the substrate may be passivated with hydrogen using a dilute hydrofluoric acid treatment. In yet another variation, a sacrificial SiO_2 layer may be grown on the substrate thermally or by an oxygen plasma and then completely removed by hydrofluoric acid. In still another variation, a non-selective dry-etch process can be used. The clean surface must be achieved while minimizing substrate consumption to ensure compatibility with thin film materials heterostructures and SOI wafers. For example, after hydrogen passivation with a dilute HF treatment a suitable bake could include heating the substrate for 5 minutes at 800°C.

[0042] The transistor 60 includes a gate electrode 64, made of, for example, polycrystalline silicon, and a gate insulator 66 made of, for example, SiO_2 or a high-k material, patterned using, for example, reactive ion etching ("RIE") whereby SiO_2 gate insulator is defined by selective reactive ion etching using, e.g. CHF_3 / O_2 gas mixture with subsequent post-RIE cleaning to remove the growth-inhibiting fluoropolymer layer, as described in the above-referenced Langdo thesis.

[0043] Isolation regions 86, 88, made of, e.g., SiO_2, are introduced to isolate transistor 60 from other devices. Isolation regions 86,88 can be, for example, shallow trench isolation regions produced early in the transistor fabrication process by methods known in the art.

[0044] The transistor 60 also includes a source region 68 and a drain region 70 defined in the substrate 60 proximate the gate electrode 64. In a particular embodiment, the transistor 60 is an n-type MOSFET with the source and drain regions formed by n-type doping via, e.g. implantation of arsenic ions, as will be described in detail below. Shallow extension regions 68a, 70a of the source region 68 and the drain region 70, respectively, are formed by, e.g., ion

implantation after the gate electrode 64 and the gate insulator 66 are defined. The shallow extension regions 68a, 70a preferably extend to and, in one variation of this embodiment, slightly below the gate insulator 66. The depth of the extension regions 68a, 70a may range from about 5 nm to about 50 nm. A first liner 72 and a second liner 74 are deposited proximate the gate electrode 64 and the gate insulator 66. In a particular embodiment, the thickness of the liners 72, 74 is approximately 250 angstroms. The liners 72, 74 may be formed of, e.g., a low temperature oxide (LTO). During the formation of liners 72, 74, a hard mask 76 is formed on a top surface 78 of the gate electrode 64. Hard mask 76 is formed of, e.g., LTO.

[0045] Subsequently, spacers 80, 82 are formed proximate liners 72, 74 to electrically isolate the gate and source/drain regions during the device operation. The spacers 80, 82 are formed of a dielectric such as, for example, Si_3N_4, by chemical vapor deposition followed by an etchback step, such as reactive ion etch. Alternatively, spacers can be formed from SiO_2. In one embodiment, the height of the spacers 80, 82 roughly approximates or exceeds the height of the gate electrode 64 and ranges from about 80 nm to about 250 nm. The widths of the spacers 80, 82 range from about 30 nm to about 100 nm. Spacer sidewalls 81, 83 proximate to the source/drain regions 68, 70 may have at least partially concave profile. Sidewalls 81, 83 intersect the surface of the substrate 62 at angles α, β that range from about 60° to about 90°. In a particular embodiment, the angles α, β substantially, but not necessarily precisely, equal 90°. Furthermore, in various embodiments of the fabrication methods according to the invention, it is not necessary to precisely control the liner oxide undercut beneath the silicon nitride spacer prior to epitaxial growth to minimize faceting, . The spacers 80, 82 may be fabricated so that the sidewalls 81, 83 are substantially aligned with a particular crystallographic plane of the semiconductor substrate 62, such as, for example, the <100> or <110> crystallographic plane.

[0046] The raised source/drain regions 68, 70 are formed by selective epitaxial growth coupled with ion implantation after formation of sidewall spacers 80, 82, as described below. The height of the source/drain regions 68, 70 may range from about 10 nm to about 100 nm.

[0047] Referring to Figure 6, a contact material 100 is subsequently formed on raised source and drain regions 68, 70. In a particular embodiment, the contact material 100 is a metal compound that is thermally stable and has low electrical resistivity at the silicon/refractory metal interface, such as a metal silicide including, for example, cobalt, titanium, tungsten, molybdenum, platinum, nickel, or tantalum. Preferably, the contact material 90 is formed by a

self-aligned silicide process, in which the contacts are formed only in the areas where the deposited metal is in direct contact with the source/drain regions 68, 70. Because of the facet-free formation, the metal uniformly penetrates the raised source 68 and drain 70 regions thereby maintaining the advantages of the raised source and drain approach.

5 **[0048]** In various embodiments of the invention, the raised source/drain elements 68, 70 include, for example, Si, Ge, or SiGe alloys, and are formed by selective epitaxial growth in a CVD system, such as LPCVD, APCVD, or PECVD reactor. Suitable CVD systems commonly used for volume epitaxy in manufacturing applications include, for example, EPI CENTURA™ single-wafer multi-chamber systems available from Applied Materials of Santa Clara, CA, or 10 EPSILON® single-wafer epitaxial reactors available from ASM International based in Bilthoven, The Netherlands.

[0049] In the CVD process, selective epitaxial growth typically includes introducing a source gas into the chamber. The source gas may include at least one precursor gas and a carrier gas, such as, for example hydrogen. In those embodiments of the invention where the raised regions 15 68, 70 are formed from Si, silicon precursor gases such as, for example, silane, disilane, trisilane, or dichlorosilane (DCS) are used. Conversely, in those embodiments of the invention where the raised regions 68, 70 are formed from Ge, germanium precursor gases, such as, for example, germane (GeH_4), digermane, germanium tetrachloride, or germanium dichloride are used. Finally, in the embodiments where the raised regions 68, 70 are formed from SiGe alloy, a 20 combination of silicon and germanium precursor gases in various proportions is used. In a particular embodiment of the invention for selective deposition of $Si_{0.80}Ge_{0.20}$ layers, 100 standard cubic centimeters (sccm) of DCS, 25 sccm 10% GeH_4/H_2, and 150 sccm of HCl in a hydrogen carrier gas at a growth temperature of 750°C and pressure of 20 Torr may be used. In another embodiment of the invention for selective deposition of Si layers, 100 sccm of DCS and 25 100 sccm of HCl in a hydrogen carrier gas at a growth temperature of 850°C and pressure of 10 Torr may be used.

[0050] The LPCVD, APCVD, or PECVD system chamber is heated, such as, for example, by RF-heating. The growth temperature in the chamber ranges from about 300°C to about 900°C depending on the composition of the raised regions 68, 70. Specifically, if the source gas 30 predominantly contains silicon precursor, the temperature preferably ranges from about 500 to about 900°C, and if the source gas predominantly contains germanium precursor, the

temperature ranges from about 300°C to about 700°C. The chamber pressure during formation of raised regions 68, 70 is greater than about 5 Torr and the growth rate is greater than 1 nanometer/minute (nm/min).

[0051] Referring again to FIG. 5, during selective epitaxial growth, the material composing raised regions 68, 70 forms only on the semiconductor substrate, such as the silicon substrate 62. The top surface 78 of gate electrode 64 is protected from epitaxial growth by the hard mask 76. Alternatively, hard mask 76 is absent from top surface 78 of gate electrode 64, and epitaxial growth additionally occurs on top surface 78. Epitaxy parameters are chosen such that substantially no epitaxial layer is formed on sidewall spacers 80, 82, and, as described below, substantially no facets are formed at the interface between raised regions 68, 70 and spacers 80, 82.

[0052] Selective growth of epitaxial layers substantially only on silicon or other semiconductors, and not on dielectrics such as silicon nitride or silicon dioxide, is facilitated by the introduction of an etchant, such as, for example, hydrogen chloride or chlorine, to the source gas mixture. Specifically, epitaxial layers are grown on exposed windows in a dielectric mask while nucleation of polysilicon on the masking material is suppressed during the incubation time by, for example, etching of spurious nuclei on the dielectric material, the mediation of saturation by formation of a number of intermediate chlorine-containing silicon precursors, and passivation of surface defect sites which serve as heterogeneous nucleation centers. Also, selectivity is facilitated by growing for a period of time that is generally shorter than the incubation period needed for polysilicon nucleation on the dielectric mask.

[0053] In various embodiments of the invention, the epitaxial layers of the source/drain regions 68, 70 are doped in situ by adding a dopant during deposition of the epitaxial layer to suppress facet formation at the interface with the spacers 80, 82. Examples of suitable dopants are n-type dopant such as phosphorus, arsenic, and antimony, or p-type dopant, such as boron. The dopant may be added to the epitaxial layer by introducing a dopant gas, such as phosphine, arsine, stibine, and diborane, into the chamber. The dopant gas is diluted in a carrier gas of the source gas mixture to, for example, approximately 1% concentration.

[0054] In a particular embodiment, facetless selective epitaxial growth according to the invention is compatible with CMOS fabrication. CMOS fabrication entails formation of a n-channel MOSFET ("NMOS") in a first portion of the semiconductor region; and a p-channel

MOSFET ("PMOS") in a second portion of the semiconductor region so that both MOSFETs are disposed on the same substrate. Accordingly, in this embodiment, *in situ* doping that is used during the epitaxial growth to suppress facet formation is sufficiently low so that it will not interfere with introduction of additional dopants of opposite type ("counterdoping") that is
5 necessary in order to manufacture both n-channel and p-channel MOSFETs on the same substrate. This counterdoping may be performed with suitable masking in place for either NMOS (if the *in situ* doping to suppress faceting was p-type) or PMOS (if the *in situ* doping to suppress faceting was n-type), thus allowing CMOS fabrication. Accordingly, in this embodiment of the invention, a level of *in situ* doping that is used during the epitaxial growth to
10 suppress facet formation does not exceed the level of counterdoping (for example, ion implantation) that is necessary for CMOS fabrication. For example, in one variation of this embodiment, the level of *in situ* doping ranges from about 10^{17} to about 10^{19} cm^{-3}, which does not interfere with a typical doping level used during CMOS fabrication that usually exceeds about 10^{20} cm^{-3}.

15 **[0055]** Other embodiments incorporating the concepts disclosed herein may be used without departing from the spirit and scope of the invention. The described embodiments are to be considered in all respects as only illustrative and not restrictive. Therefore, it is intended that the scope of the invention be only limited by the following claims.

CLAIMS

1 1. A method of fabricating a semiconductor structure, the method comprising:
2 providing a chamber;
3 providing a semiconductor substrate in the chamber, the semiconductor substrate
4 having a surface including a first portion and a second portion proximal to the first
5 portion;
6 forming a dielectric region on the first portion of the substrate; and
7 selectively depositing an epitaxial layer of at least one semiconductor material on
8 the second portion of the substrate while in situ doping the epitaxial layer at a first
9 predetermined level to substantially suppress facet formation thereby forming a
10 substantially facetless semiconductor region, wherein the pressure in the chamber during
11 selective deposition of the epitaxial layer is greater than about 5 Torr.

1 2. The method of claim 1 wherein the epitaxial layer is deposited in a chemical vapor
2 deposition system.

1 3. The method of claim 2 wherein the chemical vapor deposition system is selected from the
2 group consisting of: a reduced-pressure chemical vapor deposition system, atmospheric-
3 pressure chemical vapor deposition system, and plasma-enhanced chemical vapor
4 deposition system.

1 4. The method of claim 1 wherein the step of selectively depositing an epitaxial layer
2 comprises introducing a source gas into the chamber.

1 5. The method of claim 4 wherein the source gas comprises at least one precursor gas and a
2 carrier gas.

1 6. The method of claim 5 wherein the carrier gas comprises hydrogen.

1 7. The method of claim 5 wherein the at least one precursor gas comprises a silicon
2 precursor gas.

1 8. The method of claim 7 wherein the silicon precursor gas is selected from the group
2 consisting of: silane, disilane, trisilane, and dichlorosilane.

1 9. The method of claim 5 wherein the at least one precursor gas comprises a germanium
2 precursor gas.

1 10. The method of claim 9 wherein the germanium precursor gas is selected from the group
2 consisting of: germane, digermane, germanium tetrachloride, or germanium dichloride.

1 11. The method of claim 5 wherein the source gas further comprises an etchant for
2 suppressing nucleation of the at least one semiconductor material over the dielectric
3 region during deposition.

1 12. The method of claim 11 wherein the etchant comprises hydrogen chloride or chlorine.

1 13. The method of claim 1 wherein the epitaxial layer is doped by adding a dopant to the
2 epitaxial layer during deposition of the epitaxial layer, the dopant selected from the group
3 consisting of: phosphorus, arsenic, antimony, and boron

1 14. The method of claim 13 wherein the dopant is added to the epitaxial layer by introducing
2 a dopant gas into the chamber, the dopant gas selected from the group consisting of:
3 phosphine, arsine, stibine, and diborane.

1 15. The method of claim 13 wherein the first predetermined level of doping ranges from
2 about 10^{17} to about 10^{19} cm^{-3}

1 16. The method of claim 1 wherein the epitaxial layer comprises at least one of silicon and
2 germanium.

1 17. The method of claim 1 wherein the dielectric region comprises at least one of silicon
2 oxide and silicon nitride.

1 18. The method of claim 17 wherein the dielectric region comprises a two-layered spacer
2 structure comprising a silicon oxide layer and a silicon nitride layer disposed thereon.

1 19. The method of claim 1 wherein the semiconductor substrate comprises silicon.

1 20. The method of claim 1 wherein the semiconductor substrate comprises
2 a silicon wafer;
3 an insulating layer disposed thereon; and
4 a strained semiconductor layer disposed on the insulating layer.

1 21. The method of claim 20 wherein the strained semiconductor layer comprises silicon or
2 germanium.

1 22. The method of claim 1 wherein the semiconductor substrate comprises
2 a silicon wafer;
3 a compositionally uniform relaxed $Si_{1-x}Ge_x$ layer deposited thereon; and
4 a strained silicon layer deposited on the relaxed $Si_{1-x}Ge_x$ layer

1 23. The method of claim 22 wherein the semiconductor substrate further comprises a
2 compositionally graded $Si_{1-x}Ge_x$ layer disposed between the compositionally uniform
3 relaxed $Si_{1-x}Ge_x$ layer and the silicon wafer.

1 24. The method of claim 22 wherein the semiconductor substrate further comprises an
2 insulating layer disposed between the compositionally uniform relaxed $Si_{1-x}Ge_x$ layer
3 and the silicon wafer.

1 25. The method of claim 1 wherein the temperature in the chamber during selective
2 deposition of the epitaxial layer ranges from about 300 °C to about 900 °C.

1 26. The method of claim 25 wherein the temperature in the chamber during selective
2 deposition of the epitaxial layer further ranges from about 500 °C to about 700 °C.

1 27. The method of claim 1 wherein the epitaxial layer is deposited at a rate greater than about
2 1 nm/min.

1 28. The method of claim 1 further comprising:
2 fabricating a n-channel MOSFET in a first portion of the semiconductor region;
3 and
4 fabricating a p-channel MOSFET in a second portion of the semiconductor
5 region.

1 29. The method of claim 28 comprising counter-doping the first portion or the second portion
2 at a second predetermined level.

1 30. The method of claim 29 wherein the first predetermined level of doping does not exceed
2 the second predetermined level of doping.

1 31. The method of claim 1 further comprising forming a metal silicide layer over the
2 semiconductor region.

1 32. The method of claim 1 wherein the surface of the semiconductor substrate has a
2 substantially (100) crystallographic orientation.

1 33. The method of claim 1 wherein the dielectric region comprises a sidewall having an
2 angle relative to the semiconductor substrate, the angle ranging from about 60° to about
3 90°.

1 34. The method of claim 32 wherein the sidewall is substantially aligned with the <110>
2 crystallographic plane of the semiconductor substrate

1 35. The method of claim 32 wherein the sidewall is substantially aligned with the <100>
2 crystallographic plane of the semiconductor substrate.

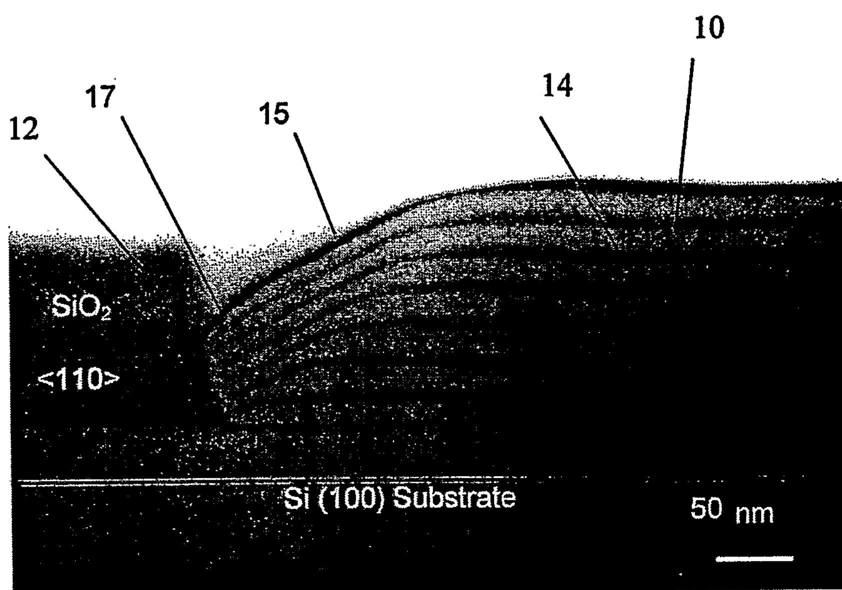

FIG. 1

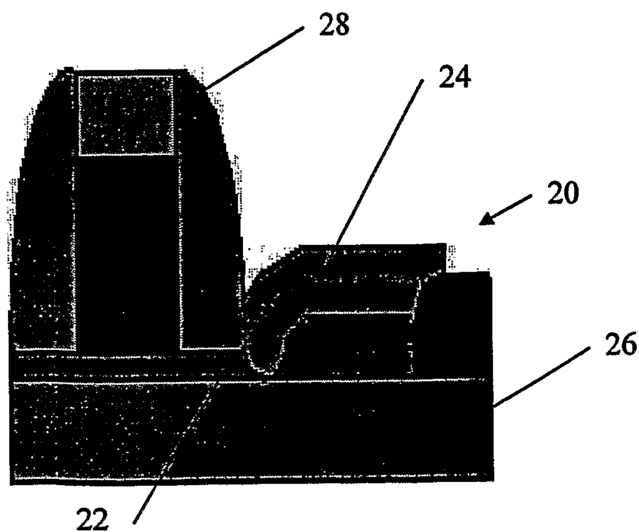

FIG. 2

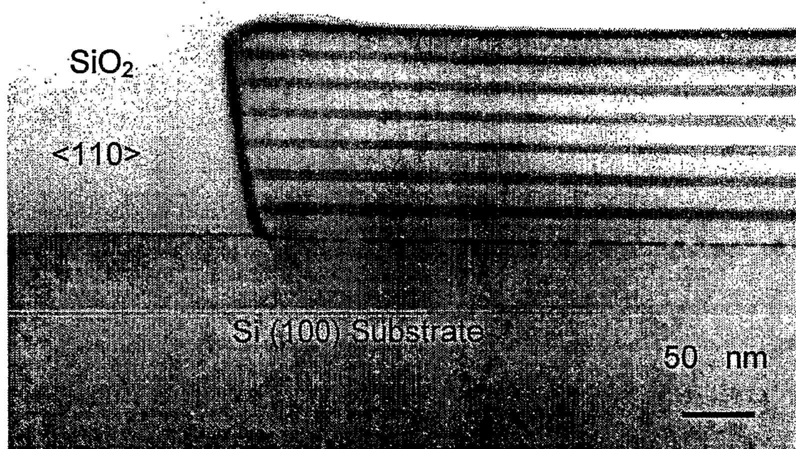

FIG. 3

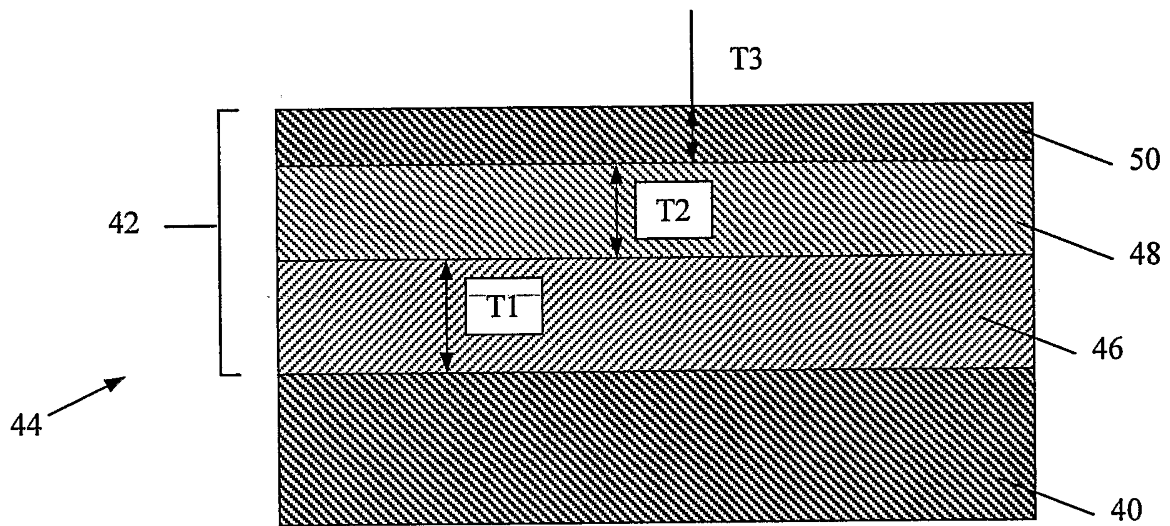

FIG. 4

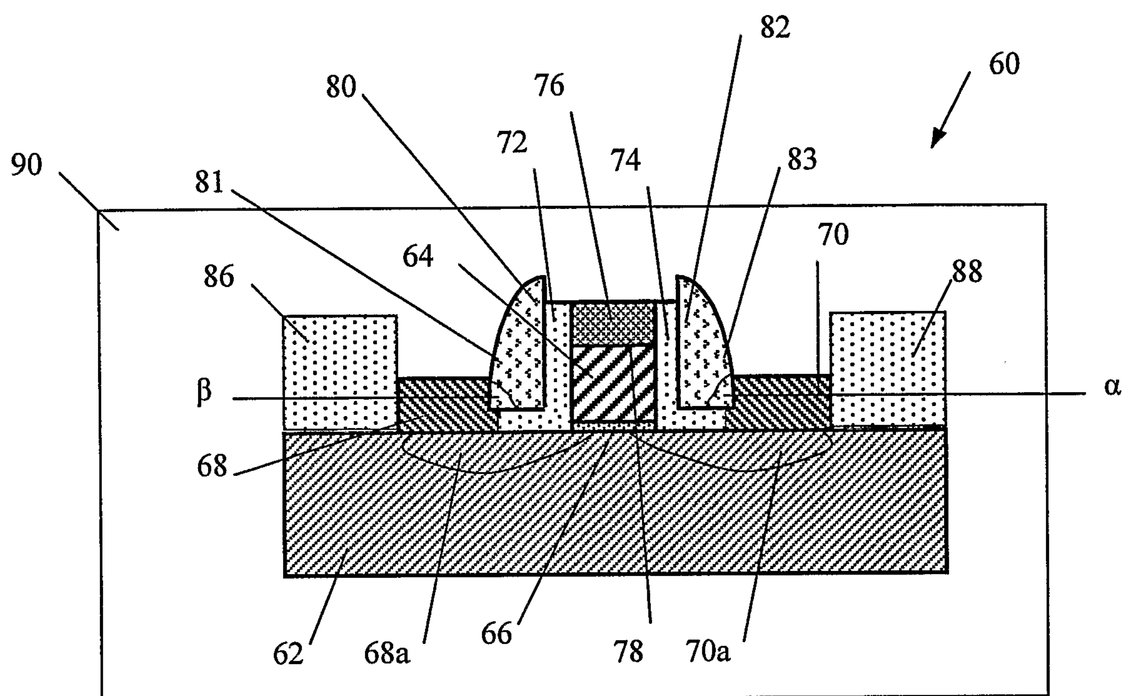

FIG. 5

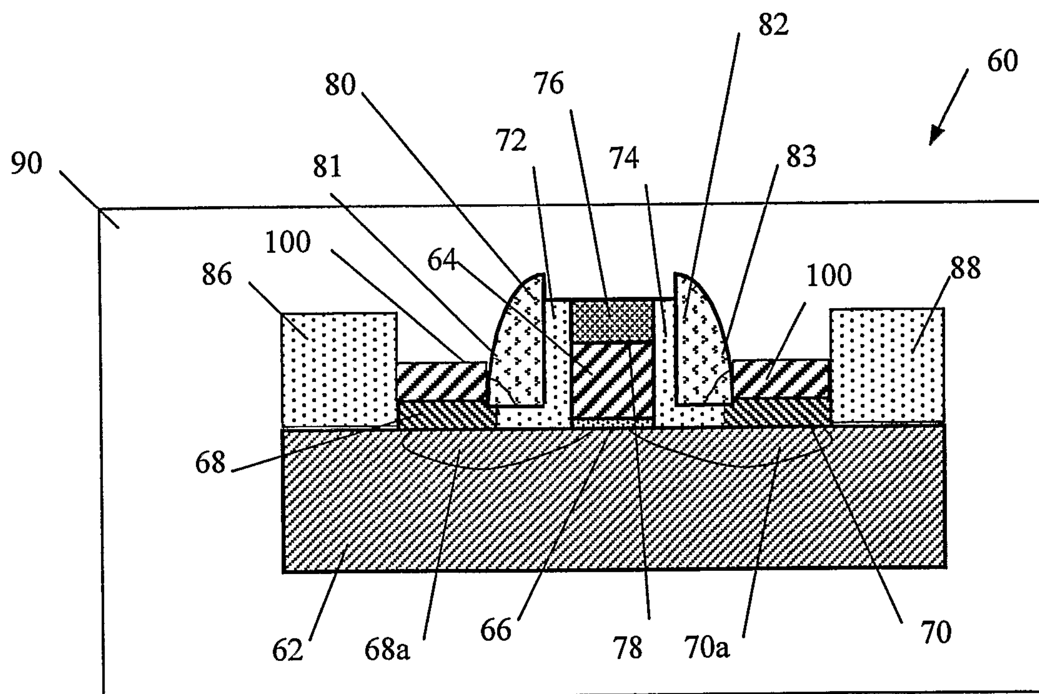

FIG. 6

INTERNATIONAL SEARCH REPORT

PCT/US 03/18140

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/285

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001/045604 A1 (WASHIO KATSUYOSHI ET AL) 29 November 2001 (2001-11-29) paragraphs '0081!-'0107!	1-19
A	US 6 214 679 B1 (CHAU ROBERT S ET AL) 10 April 2001 (2001-04-10) the whole document	
A	US 6 235 575 B1 (KASAI NAOKI ET AL) 22 May 2001 (2001-05-22) column 6, line 4-52	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 October 2003	05/11/2003

Name and mailing address of the ISA
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INTERNATIONAL SEARCH REPORT

International Application No. PCT/US 03 18140

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: 20-35

D1: US2001/0045604 A1, see especially paragraphs 81 to 100, shows in Fig. 4(b) and corresponding text almost no facet formation when growing SiGe at a pressure of 50 kPa on a silicon substrate with silicon nitride as dielectric on second portions thereof. The used gases, e.g. silane as source gas, phosphine as doping gas, hydrogen as carrier gas etc. correspond to those used in the present application, rendering D1 relevant to claims 1 to 19.

D1 therefore destroys a common inventive concept linking the claims dependent on claim 1. However, inviting for payment of additional search fees was considered inappropriate since according to paragraph 18 of the present application, facetless growth in commercially available atmospheric pressure chemical vapor deposition (= APCVD) systems is state of the art. Thus, the disadvantages cited in paragraph 20 of the application, namley deposition based on UHVCVD, no longer exist because APCVD has already been used for facetless deposition. Accordingly, claim 1 did not define the invention properly with respect to the prior art known to the Applicant.

The invention being not properly defined in claim 1, a meaningful complete search becomes impossible, so asking for additional search fees was considered innappropriate.

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

PCT/US 03/18140

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. [ ] Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. [X] Claims Nos.: 20-35
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. [ ] Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. [ ] As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. [ ] As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. [ ] No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

[ ] The additional search fees were accompanied by the applicant's protest.

[ ] No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

PCT/US 03/18140

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
US 2001045604	A1	29-11-2001	JP	2001338988	A	07-12-2001
			TW	502443	B	11-09-2002
US 6214679	B1	10-04-2001	NONE			
US 6235575	B1	22-05-2001	JP	3219051	B2	15-10-2001
			JP	11330233	A	30-11-1999