(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 August 2016 (18.08.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/128609 A1

(51) International Patent Classification:
H03K 19/0175 (2006.01)

(21) International Application Number:
PCT/FI2016/050030

(22) International Filing Date:
21 January 2016 (21.01.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15154247.9 9 February 2015 (09.02.2015) EP

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

WO 2016/128609 A1

(54) Title: AN APPARATUS AND METHODS FOR SENSING

(57) Abstract: An apparatus and method wherein the apparatus comprises;a sensor arrangement comprising a plurality of sensor cells wherein a sensor cell comprises a transistor and a sensor coupled to the transistor;first selection circuitry configured to sequence a subset of sensor cells to which a gate input signal is provided, wherein the gate input signal is provided to the gate of the transistors within the sensor cells; second selection circuitry configured to sequence a subset of sensor cells from which an output signal is received;sensing signal circuitry configured to provide a sensing signal, wherein the sensors are provided between the sensing signal circuitry and the second selection circuitry such that the output signal provides an indication of the impedance of the sensors.

TITLE

An Apparatus and Methods for Sensing

TECHNOLOGICAL FIELD

Examples of the disclosure relate to an apparatus and method of providing an apparatus for sensing. In particular, they relate to an apparatus and method of providing an apparatus which may comprise a plurality of sensors.

BACKGROUND

Sensors which enable attributes such as user inputs and environmental parameters to be sensed are known. Such sensors may comprise a material which produces a measurable change in electrical properties in response to the attributes. It may be useful to arrange such sensors into an array comprising a plurality of sensor elements. This may enable a single apparatus to detect a plurality of different attributes. In some examples this may enable a single apparatus to detect the same attribute or attributes in a a plurality of locations and/or at a plurality of different times.

It is useful to be able to read signals from the array of sensors to obtain information indicative of the attribute or attributes which have been sensed and/or information about the distribution of the attribute over the area covered by the array.

BRIEF SUMMARY

According to various, but not necessarily all, examples of the disclosure there may be provided an apparatus comprising; a sensor arrangement comprising a plurality of sensor cells wherein a sensor cell comprises a transistor and a sensor coupled to the transistor; first selection circuitry configured to sequence a subset of sensor cells to which a gate input signal is provided, wherein the gate input signal is provided to the gate of the transistors within the sensor cells; second selection

circuitry configured to sequence a subset of sensor cells from which an output signal is received; sensing signal circuitry configured to provide a sensing signal, wherein the sensors are provided between the sensing signal circuitry and the second selection circuitry such that the output signal provides an indication of the impedance of the sensors.

In some examples the second selection circuitry may comprise an analogue multiplexer configured to receive a complex output signal from the sensor cells.

In some examples the second selection circuitry may comprise the plurality of sensor cells are arranged in a plurality of rows and columns. The columns may be orthogonal to the rows. In some examples the first selection circuitry may be configured to sequence through a series of different rows and the second selection circuitry may be configured to sequence through a series of different columns. In other examples the first selection circuitry may be configured to sequence through a series of different columns and the second selection circuitry may be configured to sequence through a series of different rows.

In some examples the sensor may be connected in series with the transistor within the sensor cell. In other examples the sensor may be connected in parallel with the transistor within the sensor cell.

In some examples the transistor may comprise a thin film transistor.

In some examples the data input signal may comprise an alternating current signal.

In some examples the sensor may comprise a material which changes impedance in dependence on a sensed attribute.

In some examples the sensor may comprise a material which changes resistance in response to the sensed attribute.

In some examples the sensor may comprise a material which changes permittivity in response to the sensed attribute.

In some examples the apparatus may further comprise at least one transmitter configured to transmit information obtained from the output signal.

According to various, but not necessarily all, examples of the disclosure there may be provided a communication device comprising an apparatus as described above.

According to various, but not necessarily all, examples of the disclosure there may be provided a method comprising; providing a sensor arrangement comprising a plurality of sensor cells wherein a sensor cell comprises a transistor and a sensor coupled to the transistor; providing first selection circuitry configured to sequence a subset of sensor cells to which a gate input signal is provided, wherein the gate input signal is provided to the gate of the transistors within the sensor cells; providing second selection circuitry configured to sequence a subset of sensor cells from which an output signal is received; providing sensing signal circuitry configured to provide a sensing signal, wherein the sensors are provided between the sensing signal circuitry and the second selection circuitry such that the output signal provides an indication of the impedance of the sensors.

In some examples the second selection circuitry may comprise an analogue multiplexer configured to receive a complex output signal from the sensor cells.

In some examples the plurality of sensor cells may be arranged in a plurality of rows and columns. In some examples the columns may be orthogonal to the rows. In some examples the first selection circuitry may be configured to sequence through a series of different rows and the second selection circuitry may be configured to sequence through a series of different columns. In other examples the first selection circuitry may be configured to sequence through a series of different columns and the second selection circuitry may be configured to sequence through a series of different rows.

In some examples the sensor may be connected in series with the transistor within the sensor cell. In other examples the sensor may be connected in parallel with the transistor within the sensor cell.

In some examples the transistor may comprise a thin film transistor.

In some examples the data input signal may comprise an alternating current signal.

In some examples the sensor may comprise a material which changes impedance in dependence on a sensed attribute.

In some examples the sensor may comprise a material which changes resistance in response to the sensed attribute.

In some examples the sensor may comprise a material which changes permittivity in response to the sensed attribute.

In some examples the method may further comprise providing at least one transmitter configured to transmit information obtained from the output signal.

According to various, but not necessarily all, examples of the disclosure there may be provided examples as claimed in the appended claims.

BRIEF DESCRIPTION

For a better understanding of various examples that are useful for understanding the brief description, reference will now be made by way of example only to the accompanying drawings in which:

Fig. 1 illustrates an apparatus;

Fig. 2 illustrates another apparatus comprising read out electronics and a transmitter;

Fig. 3 schematically illustrates a sensor arrangement;

Fig. 4 schematically illustrates another sensor arrangement;

Fig. 5 illustrates a method;

Fig. 6 illustrates a plot of sensor sensitivity sampled with a first frequency; and

Fig. 7 illustrates another plot of sensor sensitivity sampled with a second frequency.

DETAILED DESCRIPTION

The Figures illustrate an apparatus 1 comprising; a sensor arrangement 3 comprising a plurality of sensor cells 35 wherein a sensor cell 35 comprises a transistor 31 and a sensor 33 coupled to the transistor 31; first selection circuitry 5 configured to sequence a subset of sensor cells 35 to which a gate input signal 6 is provided, wherein the gate input signal 6 is provided to the gate of the transistors 31 within the sensor cells 35; second selection circuitry 9 configured to sequence a subset of sensor cells 35 from which an output signal 8 is received; sensing signal circuitry 7 configured to provide a sensing signal 4, wherein the sensors 33 are provided between the sensing signal circuitry 7 and the second selection circuitry 9 such that the output signal 8 provides an indication of the impedance of the sensors 33.

Examples of the disclosure provide the technical effect of enabling the transistors 31 within the sensor arrangement 3 to be used as switches. This enables each of the sensor cells 35 to be addressed individually to enable the impedance of each sensor 33 to be measured separately. As only one transistor 31 is provided in each sensor cell 35 this ensures that the resistance within the sensor arrangement 3 is low enough to enable accurate measurements from the sensors 33.

The apparatus 1 may be for sensing. The apparatus 1 may be for sensing a plurality of different attributes.

Fig. 1 schematically illustrates an example apparatus 1 which may be provided in some examples of the disclosure. The apparatus 1 comprises a sensor arrangement 3, first selection circuitry 5, second selection circuitry 9 and sensing signal circuitry 7.

The sensor arrangement 3 may comprise a plurality of sensor cells 35. A sensor cell 35 may comprise a transistor 31 and a sensor 33 coupled to the transistor 31. In some of the examples each of the plurality of sensor cells 35 within the apparatus 1 may comprise a transistor 31 and a sensor 33 coupled to the transistor 31. In some examples only one transistor 31 may be provided within each sensor cell 35. The sensors 33 may be arranged within the sensor arrangement 3 so that they are positioned between the sensing signal circuitry 7 and the second selection circuitry 9. The sensors 33 may be arranged within the sensor arrangement 3 so that the output signal 8 provides a measurement of the electrical properties, such as impedance, of the sensors 33.

Examples of sensor arrangements 3 which may be used in implementations of the disclosure are illustrated in Figs. 3 and 4. It is to be appreciated that other sensor arrangements 3 could be used in other examples.

The first selection circuitry 5 may comprise means for providing a gate input signal 6 to a selected subset of sensor cells 35 within the sensor arrangement 3. In some examples the first selection circuitry 5 may be configured to sequence the subset of sensor cells 35 to which the gate input signal 6 is provided. The gate input signal 6 may be sequentially provided to the gates of the transistors 31 within each of the sensor cells 35.

The second selection circuitry 9 may comprise means for sequencing a subset of sensor cells 35 from which an output signal 8 is received. In some examples the second selection circuitry 9 may comprise a multiplexer. In some examples the second selection circuitry 9 may comprise an analogue multiplexer. The output signal 8 may comprise a complex signal which may comprise both real and imaginary components. In some examples the second selection circuitry 9 may be coupled directly to the sensor arrangement 3 so that there is no processing or sampling of the output signal 8 before it is provided to the second selection circuitry 9.

The sensing signal circuitry 7 may comprise means for providing a sensing signal 4. The sensing signal 4 may by an AC (alternating current) signal. In such examples the frequency of the sensing signal 4 may be selected to optimise sensitivity of the sensors 33 within the sensor arrangement 3.

The apparatus 3 may be configured so that the output signal 8 obtained by the second selection circuitry 9 can be used to obtain information from each of the sensors 33 within the sensor arrangement 3. By controlling the first selection circuitry 5 and the second selection circuitry 9 each sensor cell 35 within the sensor arrangement 3 may be addressed individually. This may enable a measurement of the electrical properties, such as impedance, of each of the sensors 33 to be obtained. As the electrical properties of the sensors 33 are dependent on the sensed attributes these measurements provide information about the sensed attribute.

In some examples the output signal 8 which is obtained by the second selection circuitry 9 may be provided to analyzing circuitry 21 to enable information about the sensed attributes to be obtained.

Fig. 2 schematically illustrates another example apparatus 1. The example apparatus 1 of Fig. 2 is configured to process the output signal 8 and then enable the processed signal to be transmitted to another device.

The example apparatus 1 of Fig. 2 also comprises a sensor arrangement 3, first selection circuitry 5 and second selection circuitry 9. The sensor arrangement 3, first selection circuitry 5 and second selection circuitry 9 may be as described above in relation to Fig. 1. The example apparatus of Fig. 2 also comprises analyzing circuitry 21, controlling circuitry 23, one or more transmitters 25, a power source 27 and a filter 29.

The analyzing circuitry 21 may comprise any means which may be configured to analyse a signal 22 provided by the second selection circuitry 9. The analyzing circuitry 21 may be configured to analyse the signal 22 provided by the second

selection circuitry 9 to determine the current impedance of the different sensor cells 35 within the sensor arrangement 3.

In the example apparatus of Fig. 2 the analyzing circuitry 21 is configured to act as sensing signal circuitry 7 and provide the input signal 4 to the sensor arrangement 3. The analyzing circuitry 21 may comprise a frequency generator which may be configured to provide the input signal 4 to the sensor arrangement 3.

The input signal 4 is then provided to the sensors 33 within the sensor arrangement 3 so that the output signal 8 provides an indication of the impedance of the sensors 33. The output signal 8 is obtained by second selection circuitry 9. In the example of Fig. 2 there are no intervening components between the sensor arrangement 3 and the second selection circuitry 9. The signal which is provided by the second selection circuitry 9 to the analyzing circuitry 21 may be a complex signal which comprises both real components and imaginary components.

The signal 22 may comprise information relating to the impedance of a plurality of the sensors 33 within the sensor arrangement 3. In some examples an anti-aliasing filter 29 may be provided between the second selection circuitry 9 and the analyzing circuitry 21.

The analyzing circuitry 21 may be configured to sample the signal 22. In some examples the analyzing circuitry 21 may comprise an analogue to digital converter which may be configured to sample the signal 22. The sampled signal may then be analyzed to provide a data indicative of the real and imaginary components of the signal 22. For instance a discrete Fourier transform may be performed on the sampled signal. This data may be used to calculate the magnitude and/or phase of the impedance of each of the sensors 33 within the sensor arrangement 3.

The analyzing circuitry 21 may comprise any suitable circuitry. In some examples the analyzing circuitry 21 may comprise a vector network analyzer impedance converter or any other suitable circuitry.

The data which is obtained by the analyzing circuitry 21 may be provided to controlling circuitry 23 in a data signal 24. The controlling circuitry 23 may comprise means for controlling the apparatus 1. The controlling circuitry 23 may be configured to control the first selection circuitry 5 to control the sequencing of the gate input signal 6. The controlling circuitry 23 may also be configured to control the second selection circuitry 9. The controlling circuitry 23 may be configured to control the first selection circuitry 5 to control the sequencing of the subsets of the sensor cells 35 from which the output signal 8 is received. The controlling circuitry 23 may be configured to synchronize the first selection circuitry 5 and the second selection circuitry 9 to synchronize the sequencing of the subsets of the sensor cells 35 so that each sensor cell 35 can be measured separately.

The controlling circuitry 23 may also be configured to process the data signal 24 which is received from the analyzing circuitry 21. The received data signal 24 comprises data indicative of the measured impedances. The controlling circuitry 23 may be configured to use the received data signal 24 to determine the current impedance for different sensor cells 35 within the sensor arrangement 3. This may enable information about different sensed attributes to be obtained.

In the example of Fig. 2 the apparatus 1 also comprises one or more transmitters 25. The one or more transmitters 25 may comprise any means which enables the apparatus 1 to establish a communication connection with another device. The transmitter 25 may enable the apparatus 1 to exchange information with the another device. In some examples the another device could be another user device, such as a mobile phone or tablet computer, a server or any other suitable device.

The communication connection which is established by the transmitter 25 may comprise a wireless connection. In some examples the wireless communication connection may comprise a connection such as near field communication (NFC), Bluetooth, wireless local area network (wireless LAN), Bluetooth low energy (BTLE) or any other suitable connection. In some examples the connection may comprise a connection dedicated to the sensor so that only information associated with the sensor is transmitted using the connection.

In some examples the apparatus 1 may also comprise one or more receivers which may enable the apparatus 1 to receive information from other devices.

The one or more transmitters 25 may enable information which has been obtained from the sensor arrangement 3 to be transmitted to another device. This may enable information obtained by the sensors 33 in the sensor arrangement 3 to be transmitted to other devices.

The example apparatus 1 of Fig. 2 also comprises a power source 27. The power source may comprise any means which may be configured to provide power to the sensor arrangement 3. In some examples the power source 27 may comprise a battery or any other suitable means.

In the example of Fig. 2 the power source 27 is arranged to provide voltages between the range of +2.7V and -20V. It is to be appreciated that other ranges may be provided in other examples of the disclosure. In some examples the voltage range may depend on the gate voltage requirements of the transistors 31 within the sensor arrangement 3.

The apparatus of Figs. 1 and 2 may be provided within a communication device. The communication device could be a handheld or wearable device which may be configured to be positioned close to the body of a user. In such examples the apparatus 1 may enable information about the parameters of the environment and/or status of a user to be collected and transmitted to another device.

Fig. 3 illustrates a sensor arrangement 3 which may be used in some examples of the disclosure. The example sensor arrangement 3 of Fig. 3 may be provided within apparatus 1 such as the apparatus of Figs. 1 and 2. In the example sensor arrangement 3 of Fig. 3 the sensors 33 are connected in series with the transistors 31.

The sensor arrangement 3 may be coupled to first selection circuitry 5 and second selection circuitry 9. The first selection circuitry 5 and the second selection circuitry 9 may be as described above in relation to Figs. 1 to 2. An input signal 4 may be provided by sensing signal circuitry 7. The second selection circuitry 9 may comprise a multiplexer as described above.

The sensor arrangement 3 comprises a plurality of sensor cells 35. In the example of Fig. 3 sixteen sensor cells 35 are provided in a four by four array. It is to be appreciated that any number and/or arrangement of sensor cells 35 may be provided in other examples of the disclosure.

In the example of Fig. 3 the sensor arrangement 3 comprises a distributed network of sensor cells 35 arranged as an array. The array comprises a plurality of rows and a plurality of columns. In the example illustrated in Fig. 3, the array is a regular array comprising regularly spaced parallel rows and regularly spaced parallel columns. In the illustrated example, the array is orthogonal in that the rows are orthogonal to the columns. It is to be appreciated that in some examples the array might not be regular and/or might not be orthogonal.

In the example of Fig. 3 each of the sensor cells 35 comprises a transistor 31 coupled to a sensor 33. Only one transistor 31 is provided in each of the sensor cells 35. In the example of Fig. 3 the sensor 33 is connected in series to the transistor 31. In the example of Fig. 3 there are no intervening components between the transistor 31 and the sensor 33.

The transistors 31 are arranged within the sensor arrangement 3 so that they are positioned between the sensing signal circuitry 7 and the second selection circuitry 9. The transistors 31 are arranged to act as switches for the sensors 33. The transistors 31 are arranged so that the source input signal is received from the sensing signal circuitry 7 and the drain signal is provided to the second selection circuitry 9. The gate input signal 6 is received from the first selection circuitry 5. The first selection circuitry 5 is arranged so that, by providing a gate input signal 6

to different subsets of sensor cells 35 at different times the different sensor cells 35 can be made active at different times.

The transistors 31 may comprise any suitable transistors 31. In some examples the transistors 31 may comprise thin film transistors or other similar transistors. In some examples the transistors 31 may comprise organic or inorganic thin film transistors. The transistors 31 may be formed using any suitable technique. For example the transistors 31 may be printed or deposited onto a substrate. Printed methods such as roll-to-roll printing, sheet to sheet printing, silk screen printing, or other printed electronics methods can be used depending on the materials used within the transistor 31.

The sensors 33 may comprise any means which may produce a measurable change in an electrical property in response to a sensed attribute. In the illustrated examples the sensors 33 are configured to produce a change in impedance. In the example of Fig. 3 the impedance of the sensor 33 is represented as a capacitance in parallel with a resistance which gives a time varying complex impedance.

The detected attribute which is sensed by the sensors 33 could be a user input such as a user touching the apparatus 1 or bending or deforming the apparatus 1. In some examples the detected attribute could comprise an environmental parameter, such as temperature, radiation the presence of chemicals or any other suitable attribute. The materials which are used within the sensors 33 may be selected in dependence of the attribute which is to be sensed.

In some examples the sensor 33 may comprise graphene oxide. This may enable the sensor 33 to detect attributes such as humidity, temperature or other suitable environmental parameters.

In some examples sensors 33 comprising graphene may be used to detect attributes such as UV(ultraviolet) and IR (infra red) radiation, chemicals such as antigens or other contaminants. In some examples graphene may be used to detect contaminants within water. This may enable the sensors 33 to be used in water

purification systems or for ensuring water quality for food production and preparation or for any other suitable use.

In some examples sensors 33 comprising zinc oxide may be used to detect humidity or other environmental parameters such as gases or other chemicals. The zinc oxide may be provided in nanostructures or any other suitable form.

In some examples the sensors 33 may comprise materials which have capacitive transduction mechanism such as polysiloxane and methacrylic polymers, polyimide, poly(vinyl pyrrolidone), poly(vinyl alcohol), ceramic materials or any other suitable material. If the material has a capacitive transduction mechanism then the environmental parameter or other attributes may change the permittivity of the material. Such materials may be used to detect attributes such as temperature, infrared radiation, contaminants such as gases or any other suitable parameters.

In some examples the sensor 33 may comprise materials which may be configured to detect changes in shape or strain applied to the apparatus 1. This may enable the sensor arrangement 3 to be used to detect user inputs such as a user bending or otherwise deforming the apparatus. In some examples the sensors 33 may comprise carbon structures such as carbon nanotubes which may have an impedance which changes when the sensor 33 is deformed. In some examples the sensors 33 may comprise a piezoelectric material such as PZT (lead zirconate titanate), Zinc Oxide or any other suitable material.

The sensors 33 are provided between the sensing signal circuitry 7 and the second selection circuitry 9 so that the output signal 8 provides a measurement of the impedance of the sensors 33.

The apparatus 1 may be configured so that each of the sensor cells 35 in the sensor arrangement 3 may be separately measured. The first selection circuitry 5 may be configured to direct the gate input signal 6 to a particular subset of sensor cells 35. The first selection circuitry 5 may be configured to direct the gate input signal 6 to a

particular row of sensor cells 35. The gate input signal is provided to the gate of the transistors 31 to enable the transistors 31 to act as switches.

The second selection circuitry 9 may be configured to direct the output signal 8 from a particular subset of sensor cells 35. The second selection circuitry 9 may be configured to direct the output signal 8 from a particular column of sensor cells 35.

The first selection circuitry 5 and the second selection circuitry 7 may be synchronised so that they simultaneously direct the gate input signal 6 to and direct the output signal 8 from, the same active sensor cell 35. In some examples the synchronization of the first selection circuitry 5 and the second selection circuitry 7 may be controlled by controlling circuitry 23.

The first selection circuitry 5 may be configured to sequence the row to which the gate input signal 6 is provided through a series of different rows. Each row may be made active once in a given time period. The second selection circuitry 9 may be configured to sequence the column from which the output signal 8 is received through a series of different columns. Each column may be made active once in the given time period.

In some examples the gate input signal 6 and the output signal 8 may have regular time sequences where each cell is addressed as frequently and for the same amount of time as all the other cells. In other examples the signals may have an irregular time sequence so that some cells are addressed more frequently than others and/or for a longer period of time.

It is to be appreciated that although it is described that gate input signal 6 is provided to rows and the output signal 8 is taken from columns, this may be reversed. For instance in other examples the gate input signal 6 may be provided to columns and the output signal 8 may be taken from rows. Depending upon context, the terms “row” and “column” may therefore be interchanged.

Fig. 4 illustrates another sensor arrangement 3 which may be used in some examples of the disclosure. The example sensor arrangement 3 of Fig. 4 may be provided within apparatus 1 such as the apparatus of Figs. 1 and 2. In the example sensor arrangement 3 of Fig. 4 the sensor arrangement 35 comprises a plurality of sensor cells 35 each comprising a transistor 31 and a sensor 33. The transistors 31 and the sensors 33 may be as described previously. The sensor arrangement 3 of Fig. 4 differs from the sensor arrangement 3 of Fig. 3 in that, in Fig. 4, the sensors 33 are connected in parallel with the transistors 31 rather than in series.

In the example of Fig. 4 the first selection circuitry 5 is configured to enable the gate input signal 6 to be provided to different columns of the sensor arrangement 3 and the second selection circuitry 9 is configured to enable the output signal 8 to be taken from different rows. It is to be appreciated that the operation of the first selection circuitry 5 and the second selection circuitry 9 may be as described previously. It is also to be appreciated that other examples the gate input signal 6 may be provided to rows and the output signal 8 may be taken from columns.

Fig. 5 illustrates a method. The method may be used to provide apparatus such as the apparatus described above with reference to Figs. 1 to 4.

The method comprises, providing, at block 51 a sensor arrangement 3 comprising a plurality of sensor cells 35 wherein a sensor cell 35 comprises a transistor 31 and a sensor 33 coupled to the transistor 31. At block 53 the method comprises providing first selection circuitry 5 configured to sequence a subset of sensor cells 35 to which a gate input signal 6 is provided, wherein the gate input signal 6 is provided to the gate of the transistors 31 within the sensor cells 35.

The method also comprises providing, at block 55, second selection circuitry 9 configured to sequence a subset of sensor cells 35 from which an output signal is received and providing at block 57, sensing signal circuitry 7 configured to provide a sensing signal 4, wherein the sensors 33 are provided between the sensing signal circuitry 7 and the second selection circuitry 9 such that the output signal provides an indication of the impedance of the sensors 33.

Fig. 6 illustrates a plot of sensor sensitivity for an example device where the data is sampled with a first frequency. Sensor sensitivity is plotted on the y axis and impedance Z is plotted on the x axis. Sensor sensitivity (figure of merit) is given by $\frac{d|Z_{meas}|}{dR_{pDUT}} \cdot \frac{R_{pDUT}}{|Z_{meas}|}$. The data plotted in Fig. 6 was obtained using 5kHz sampling frequency.

The plot of Fig. 6 shows that sensitivity of the sensor cell 35 is good enough for reliable measurement when the impedance of the sensor 33 is in the range 20kΩ to 200kΩ. The impedance of the transistor 31 should be significantly smaller than the resistance of the device under test (sensor 33). For high sensor 33 impedances the resistance of the device under test is larger than the impedances of the channel of the transistor 31 which are arranged as switches.

Fig. 7 illustrates another plot of sensor sensitivity where the data was sampled with a second frequency. In this plot the sampling frequency was 100Hz. The use of the lower frequency increases the sensitivity of the sensor so that the detection range is widened to between 30kΩ to 30MΩ.

It is to be appreciated that the sampling frequency which is used in examples of the disclosure may depend upon the sensors 33 and transistors 31 which are used.

Examples of the disclosure provide for a sensor arrangement 3 which only comprises a single transistor 31 in each of the sensor cells 35. This reduces the number of connections needed to address each sensor cell individually. The reduced number of connection lines needed may enable arrays comprising a large number of sensor cells 35 to be provided. For instance in some examples the array may comprise more than 100 sensors cells 35 in each column and/or row.

Having only a single transistor 31 in each of the sensor cells 35 may also reduce the resistance of each sensor cell and may enable a wider measurement range for the sensor 33. In the example of Fig. 3 the resistance in series with the sensor 33

may be low enough to enable accurate measurements from the sensors 33. In the example of Fig. 4 the resistance in parallel with the sensor 33 may be low enough to enable accurate measurements from the sensors 33.

The sensor arrangement 3 may be formed by printing and may provide a small and compact sensing device. The sensing device may be integrated into wearable electronics or into portable electronic devices such as mobile telephones. This may enable the sensor arrangement 3 to be used to be used to monitor the environment of the user. For instance it could be used to monitor a user's exposure to harmful or potentially harmful parameters such as heat, radiation such as UV radiation or IR radiation, contaminants which could be harmful to a user or any other suitable parameters.

In some examples the information which is obtained by the sensor arrangement could be provided to other devices via one or more transmitters. This may enable the other device to monitor the conditions to which the apparatus has been exposed and may enable a warning, or other action, to be enabled if the exposure exceeds a given threshold.

In some examples the sensor arrangement 3 could be configured to detect user inputs such as a user bending or otherwise deforming the apparatus 1. This may enable the same components to be used to detect environmental parameters and also user inputs.

The controlling circuitry 23 previously described may be implemented using instructions that enable hardware functionality, for example, by using executable computer program instructions in a general-purpose or special-purpose processing circuitry that may be stored on a computer readable storage medium (disk, memory etc) to be executed by such processing circuitry.

Processing circuitry may be configured to read from and write to memory circuitry. The processing circuitry may also comprise an output interface via which data

and/or commands are output by the processing circuitry and an input interface via which data and/or commands are input to the processing circuitry.

The memory circuitry may be configured to store a computer program comprising computer program instructions that control the operation of the apparatus 1 when loaded into the processing circuitry. The computer program instructions provide the logic and routines that enable the apparatus to perform the methods described. The processing circuitry by reading the memory circuitry is able to load and execute the computer program.

The apparatus 1 therefore comprises: processing circuitry and memory circuitry including computer program code, the at least one memory and the computer program code configured to, with the processing circuitry, cause the analysing circuitry 21 to perform as described.

The computer program may arrive at the apparatus 1 via any suitable delivery mechanism. The delivery mechanism may be, for example, a non-transitory computer-readable storage medium, a computer program product, a memory device, a record medium such as a compact disc read-only memory (CD-ROM) or digital versatile disc (DVD), an article of manufacture that tangibly embodies the computer program. The delivery mechanism may be a signal configured to reliably transfer the computer program. The apparatus 1 may propagate or transmit the computer program as a computer data signal.

In some examples the memory circuitry may be implemented as a single component it may be implemented as one or more separate components some or all of which may be integrated/removable and/or may provide permanent/semi-permanent/ dynamic/cached storage.

References to “computer-readable storage medium”, “computer program product”, “tangibly embodied computer program” etc. or a “controller”, “computer”, “processor” etc. should be understood to encompass not only computers having different architectures such as single/multi- processor architectures and sequential (Von

Neumann)/parallel architectures but also specialized circuits such as field-programmable gate arrays (FPGA), application specific circuits (ASIC), signal processing devices and other processing circuitry. References to computer program, instructions, code etc. should be understood to encompass software for a programmable processor or firmware such as, for example, the programmable content of a hardware device whether instructions for a processor, or configuration settings for a fixed-function device, gate array or programmable logic device etc.

As used in this application, the term "circuitry" refers to all of the following:
(a) hardware-only circuit implementations (such as implementations in only analog and/or digital circuitry) and
(b) combinations of circuits and software (and/or firmware), such as (as applicable): (i) a combination of processor(s) or (ii) portions of processor(s)/software (including digital signal processor(s)), software, and memory(ies) that work together to cause an apparatus, such as a mobile phone or server, to perform various functions) and
(c) circuits, such as a microprocessor(s) or a portion of a microprocessor(s), that require software or firmware for operation, even if the software or firmware is not physically present.

This definition of "circuitry" applies to all uses of this term in this application, including in any claims. As a further example, as used in this application, the term "circuitry" would also cover an implementation of merely a processor (or multiple processors) or portion of a processor and its (or their) accompanying software and/or firmware. The term "circuitry" would also cover, for example and if applicable to the particular claim element, a baseband integrated circuit or applications processor integrated circuit for a mobile phone or a similar integrated circuit in server, a cellular network device, or other network device."

The blocks illustrated in the Fig. 5 do not necessarily imply that there is a required or preferred order for the blocks and the order and arrangement of the block may be varied. Furthermore, it may be possible for some blocks to be omitted.

The term “comprise” is used in this document with an inclusive not an exclusive meaning. That is any reference to X comprising Y indicates that X may comprise only one Y or may comprise more than one Y. If it is intended to use “comprise” with an exclusive meaning then it will be made clear in the context by referring to “comprising only one..” or by using “consisting”.

In this brief description, reference has been made to various examples. The description of features or functions in relation to an example indicates that those features or functions are present in that example. The use of the term “example” or “for example” or “may” in the text denotes, whether explicitly stated or not, that such features or functions are present in at least the described example, whether described as an example or not, and that they can be, but are not necessarily, present in some of or all other examples. Thus “example”, “for example” or “may” refers to a particular instance in a class of examples. A property of the instance can be a property of only that instance or a property of the class or a property of a sub-class of the class that includes some but not all of the instances in the class. It is therefore implicitly disclosed that a features described with reference to one example but not with reference to another example, can where possible be used in that other example but does not necessarily have to be used in that other example.

Although examples of the disclosure have been described in the preceding paragraphs with reference to various examples, it should be appreciated that modifications to the examples given can be made without departing from the scope of the invention as claimed.

Features described in the preceding description may be used in combinations other than the combinations explicitly described.

Although functions have been described with reference to certain features, those functions may be performable by other features whether described or not.

Although features have been described with reference to certain embodiments, those features may also be present in other embodiments whether described or not.

Whilst endeavoring in the foregoing specification to draw attention to those features of the invention believed to be of particular importance it should be understood that the Applicant claims protection in respect of any patentable feature or combination of features hereinbefore referred to and/or shown in the drawings whether or not particular emphasis has been placed thereon.

I/we claim:

CLAIMS

1. An apparatus comprising;

a sensor arrangement comprising a plurality of sensor cells wherein a sensor cell comprises a transistor and a sensor coupled to the transistor;

first selection circuitry configured to sequence a subset of sensor cells to which a gate input signal is provided, wherein the gate input signal is provided to the gate of the transistors within the sensor cells;

second selection circuitry configured to sequence a subset of sensor cells from which an output signal is received;

sensing signal circuitry configured to provide a sensing signal, wherein the sensors are provided between the sensing signal circuitry and the second selection circuitry such that the output signal provides an indication of the impedance of the sensors.

2. An apparatus as claimed in any preceding claim wherein the second selection circuitry comprises an analogue multiplexer configured to receive a complex output signal from the sensor cells.

3. An apparatus as claimed in any preceding claim wherein the plurality of sensor cells are arranged in a plurality of rows and columns and the columns are orthogonal to the rows.

4. An apparatus as claimed in claim 3 wherein the first selection circuitry is configured to sequence through a series of different rows and the second selection circuitry is configured to sequence through a series of different columns.

5. An apparatus as claimed in claim 3 wherein the first selection circuitry is configured to sequence through a series of different columns and the second selection circuitry is configured to sequence through a series of different rows.

6. An apparatus as claimed in any preceding claim wherein the sensor is connected in series with the transistor within the sensor cell.

7. An apparatus as claimed in any of claims 1 to 5 wherein the sensor is connected in parallel with the transistor within the sensor cell.

8. An apparatus as claimed in any preceding claim wherein the transistor comprises a thin film transistor.

9. An apparatus as claimed in any preceding claim wherein the sensing signal comprises an alternating current signal.

10. An apparatus as claimed in any preceding claim wherein the sensor comprises a material which changes impedance in dependence on a sensed attribute.

11. An apparatus as claimed in any preceding claim wherein the sensor comprises a material which changes resistance in response to the sensed attribute.

12. An apparatus as claimed in any preceding claim wherein the sensor comprises a material which changes permittivity in response to the sensed attribute.

13. An apparatus as claimed in any preceding claim further comprising at least one transmitter configured to transmit information obtained from the output signal.

14. A communication device comprising an apparatus as claimed in any of claims 1 to 13.

15. A method comprising;

providing a sensor arrangement comprising a plurality of sensor cells wherein a sensor cell comprises a transistor and a sensor coupled to the transistor;

providing first selection circuitry configured to sequence a subset of sensor cells to which a gate input signal is provided, wherein the gate input signal is provided to the gate of the transistors within the sensor cells;

providing second selection circuitry configured to sequence a subset of sensor cells from which an output signal is received;

providing sensing signal circuitry configured to provide a sensing signal, wherein the sensors are provided between the sensing signal circuitry and the second selection circuitry such that the output signal provides an indication of the impedance of the sensors.

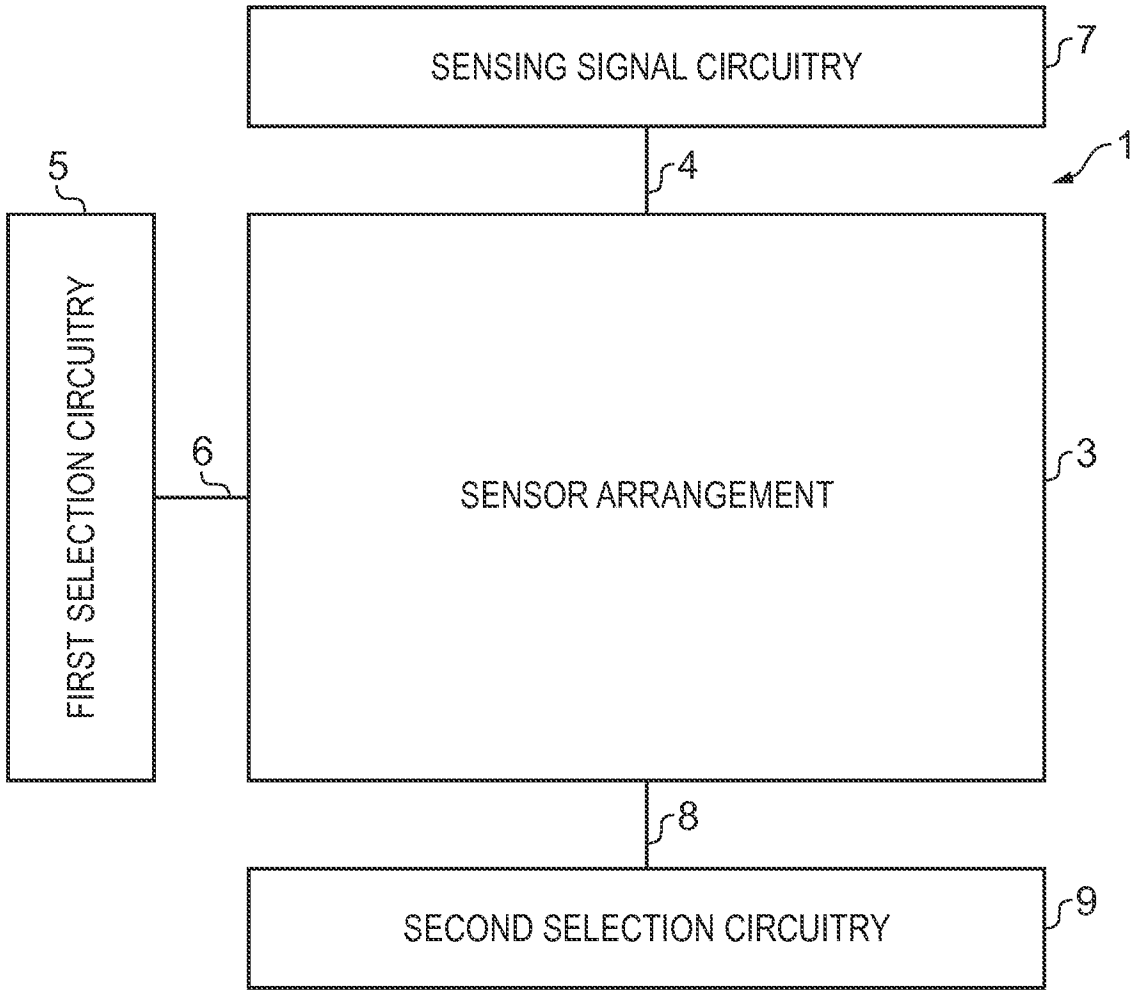
SENSING SIGNAL CIRCUITRY
7
1
4
5
FIRST SELECTION CIRCUITRY
6
SENSOR ARRANGEMENT
3
8
SECOND SELECTION CIRCUITRY
9

FIG. 1

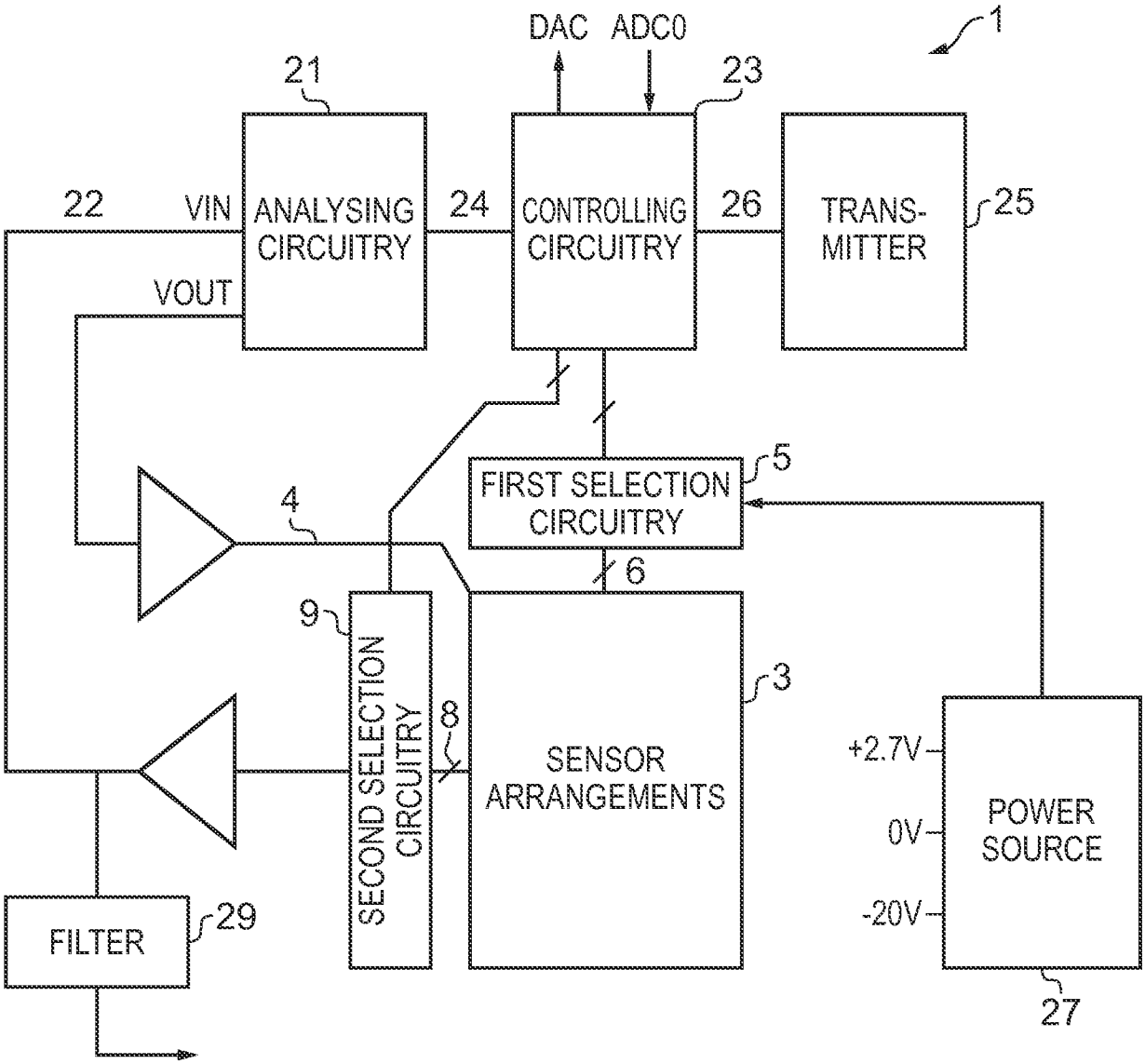
DAC
ADC0
1
21
23
22
VIN
ANALYSING CIRCUITRY
24
CONTROLLING CIRCUITRY
26
TRANS-MITTER
25
VOUT
FIRST SELECTION CIRCUITRY
5
4
6
9
SECOND SELECTION CIRCUITRY
8
SENSOR ARRANGEMENTS
3
+2.7V
0V
-20V
POWER SOURCE
27
FILTER
29

FIG. 2

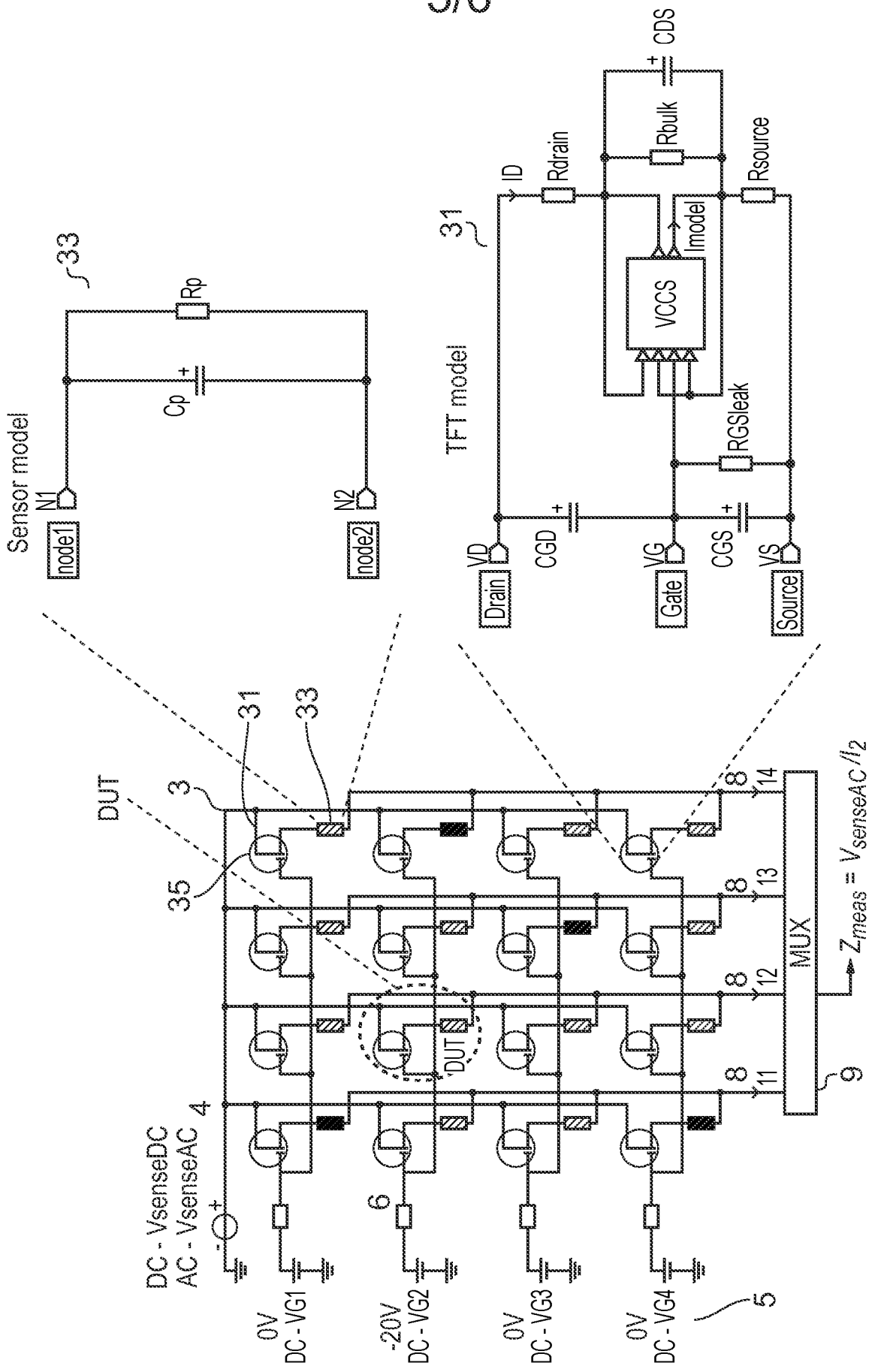
Sensor model
N1
node1
33
Rp
Cp
N2
node2
TFT model
31
ID
Rdrain
CDS
Rbulk
Rsource
Imodel
VCCS
RGSleak
VD
Drain
CGD
VG
Gate
CGS
VS
Source
DUT
3
31
33
35
4
DC - VsenseDC
AC - VsenseAC
6
DUT
0V
DC - VG1
-20V
DC - VG2
0V
DC - VG3
0V
DC - VG4
5
8
14
13
12
11
MUX
9
$Z_{meas} = V_{senseAC}/I_2$

FIG. 3

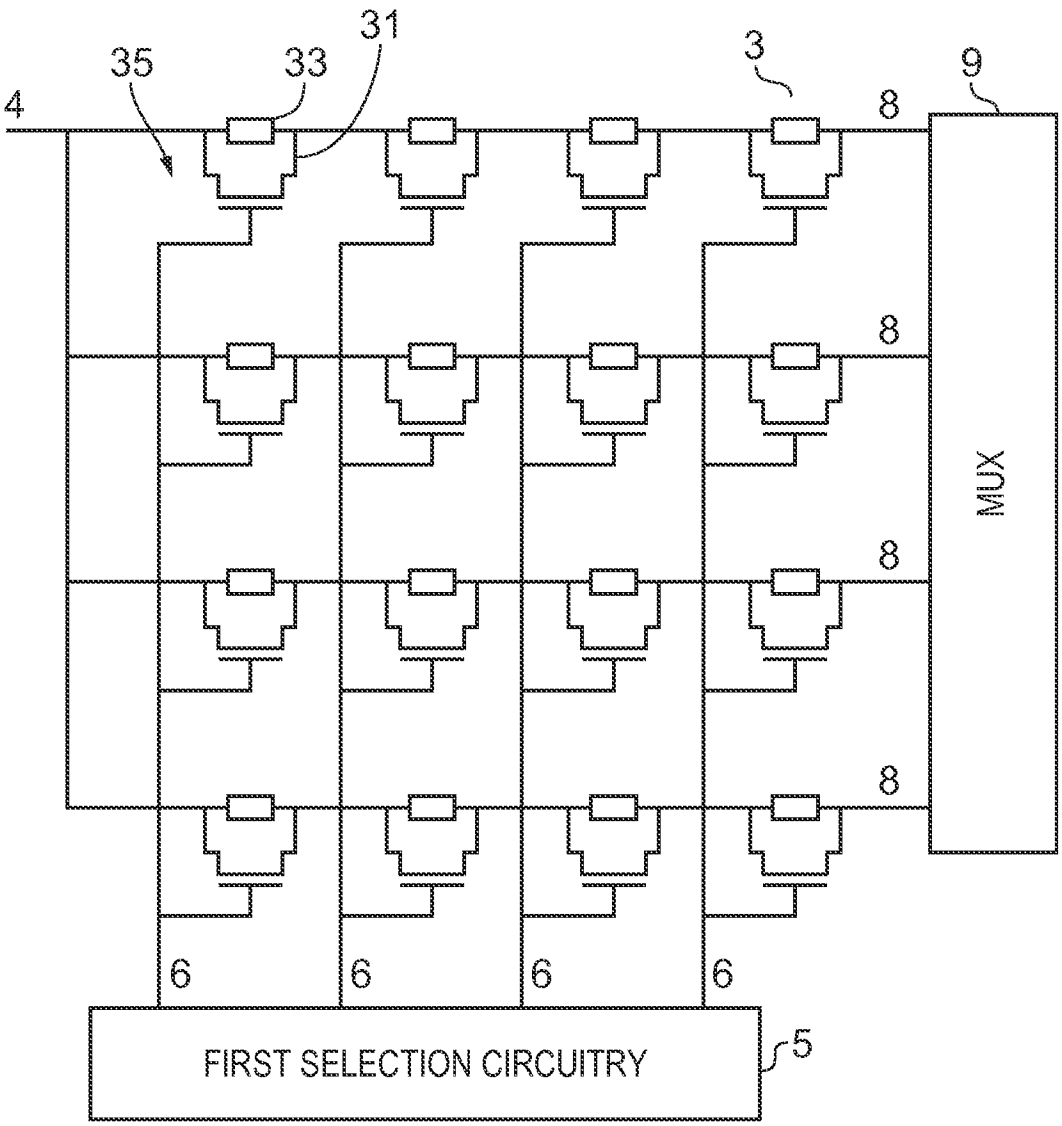

FIG. 4

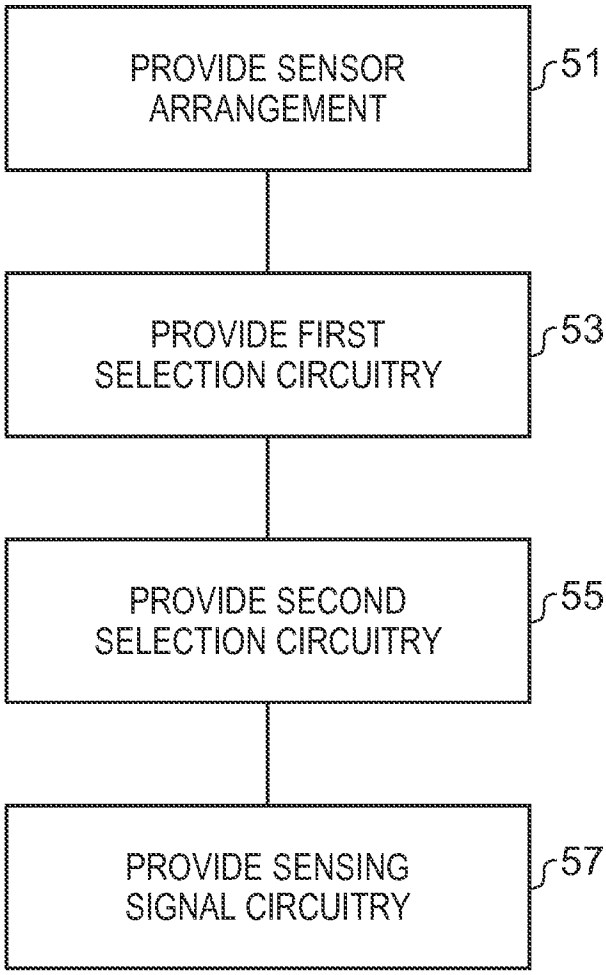
PROVIDE SENSOR ARRANGEMENT
51
PROVIDE FIRST SELECTION CIRCUITRY
53
PROVIDE SECOND SELECTION CIRCUITRY
55
PROVIDE SENSING SIGNAL CIRCUITRY
57

FIG. 5

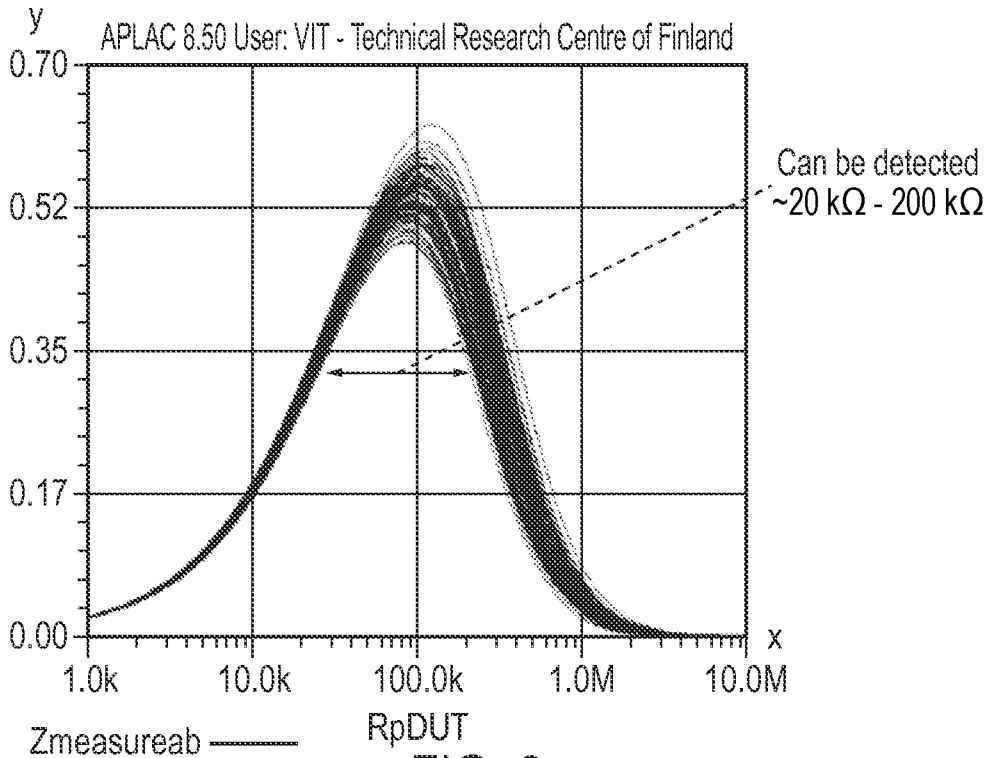
y
APLAC 8.50 User: VIT - Technical Research Centre of Finland
0.70
0.52
0.35
0.17
0.00
Can be detected
~20 kΩ - 200 kΩ
x
1.0k
10.0k
100.0k
1.0M
10.0M
RpDUT
Zmeasureab

FIG. 6

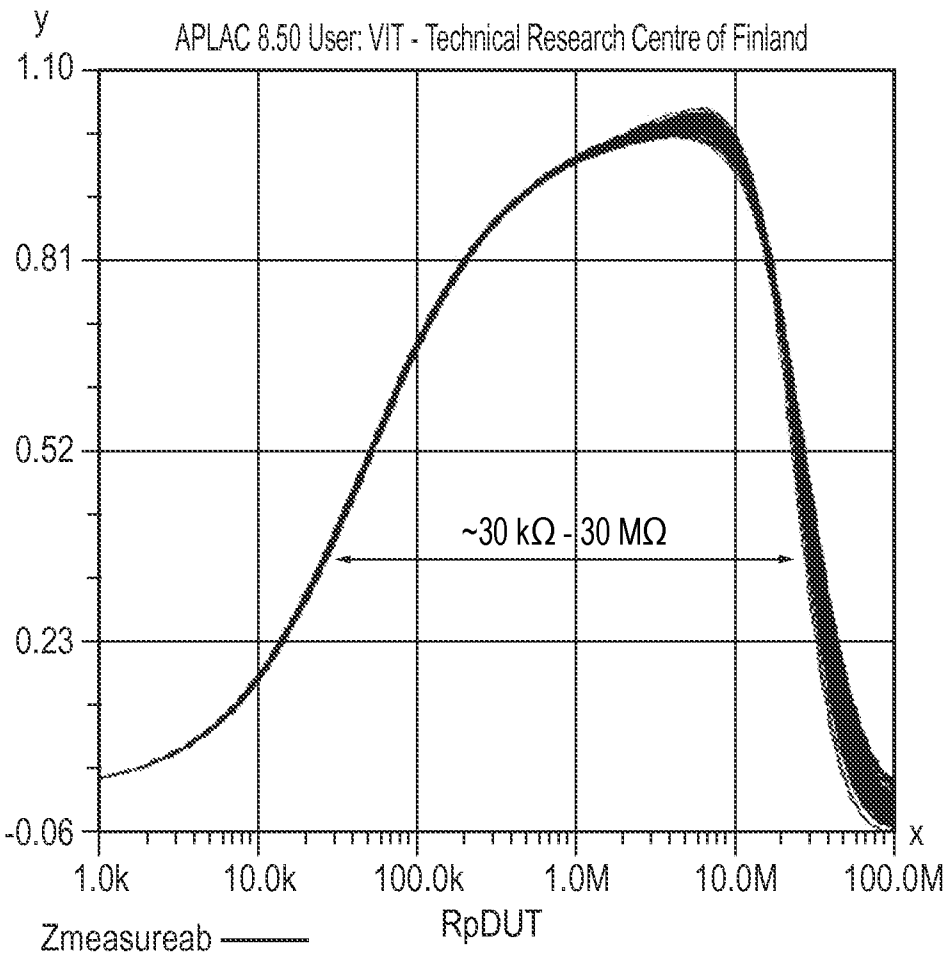
y
APLAC 8.50 User: VIT - Technical Research Centre of Finland
1.10
0.81
0.52
0.23
-0.06
~30 kΩ - 30 MΩ
x
1.0k
10.0k
100.0k
1.0M
10.0M
100.0M
RpDUT
Zmeasureab

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/FI2016/050030

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K19/0175
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/002120 A1 (YOSHIKAWA REI [JP] ET AL) 7 January 2010 (2010-01-07) paragraph [0122] - paragraph [0126]; figures 1,2,5	1-15
X	US 2010/315540 A1 (HOSHINO KOZO [JP]) 16 December 2010 (2010-12-16) paragraph [0127] - paragraph [0180]; figures 1,2	1-15
X	JP S64 16902 A (AGENCY IND SCIENCE TECHN) 20 January 1989 (1989-01-20) figure 3	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 April 2016	26/04/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Riccio, Ettore

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/FI2016/050030

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