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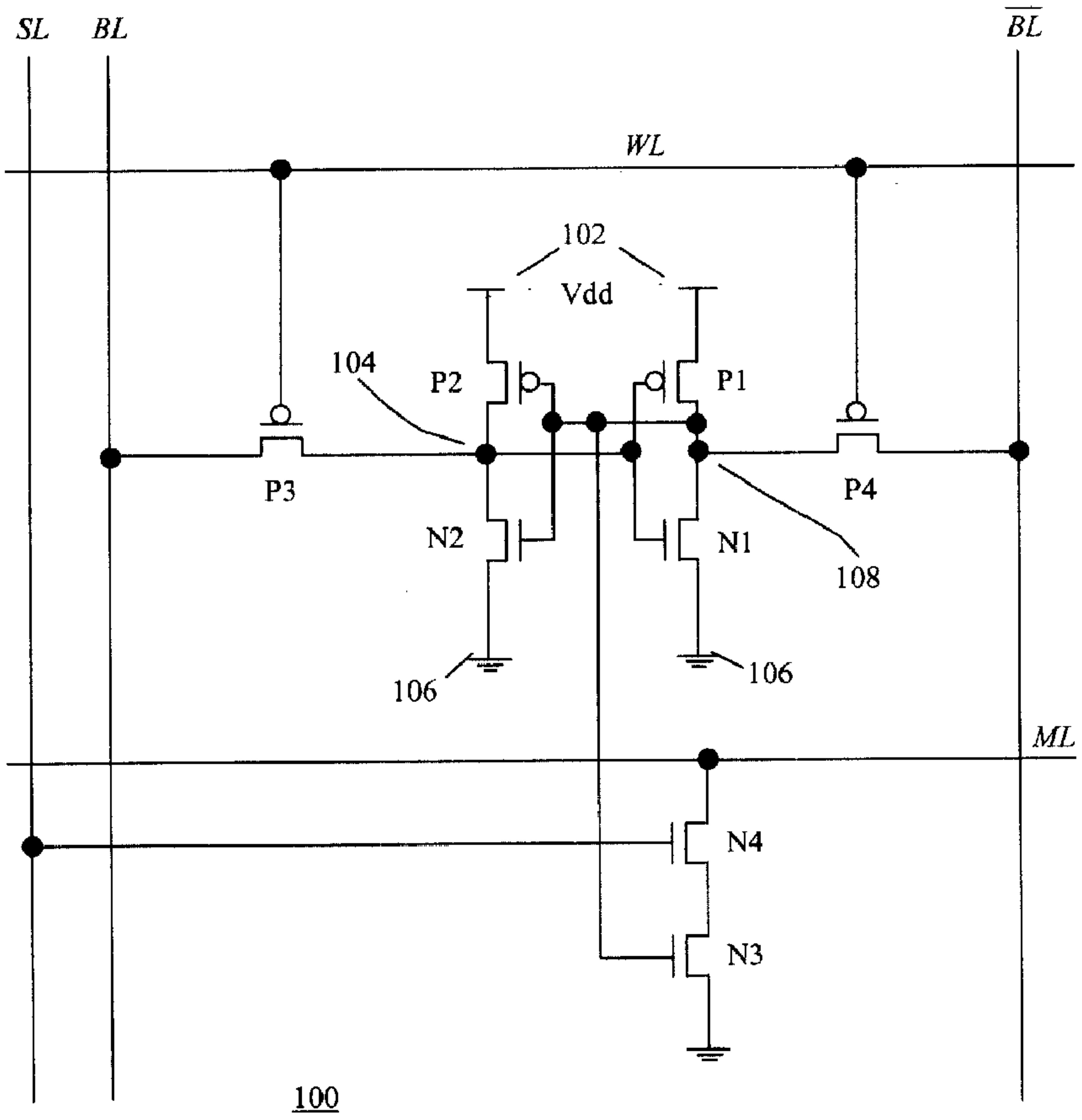
(54) **Titre** : CELLULE DE MEMOIRE ADRESSABLE PAR CONTENU
(54) **Title**: CONTENT ADDRESSABLE MEMORY CELL



(57) **Abrégé/Abstract**:

A CAM cell comprises a pair of SRAM cells, each of which comprise a pair of cross coupled inverters for storing a data value and a pair of access devices for accessing a complementary pair of bit lines. The CAM cell further comprises a pair of compare circuits,

(57) **Abrégé(suite)/Abstract(continued):**

each for comparing said data value stored in one of said SRAM cells with a search data value provided on a corresponding search line. The CAM cell has an equivalent number of n-channel and p-channel devices. The CAM cell uses p-channel transistors as access transistors to the SRAM cells in order to improve the efficiency of the layout of the cell array. The implementation ensures a balanced number of p-channel and n-channel devices per cell while still providing excellent functional characteristics.

ABSTRACT

A CAM cell comprises a pair of SRAM cells, each of which comprise a pair of cross coupled inverters for storing a data value and a pair of access devices for accessing a complementary pair of bit lines. The CAM cell further comprises a pair of compare circuits, each for comparing said data value stored in one of said SRAM cells with a search data value provided on a corresponding search line. The CAM cell has an equivalent number of n-channel and p-channel devices. The CAM cell uses p-channel transistors as access transistors to the SRAM cells in order to improve the efficiency of the layout of the cell array. The implementation ensures a balanced number of p-channel and n-channel devices per cell while still providing excellent functional characteristics.

Content Addressable Memory Cell

BACKGROUND OF THE INVENTION

Conventional content addressable memory (CAM) has been implemented primarily using static random access memory (SRAM) cells. SRAM-based CAMs have received widespread use due to the high access speed of SRAM memory cells and the static nature of the cells. Furthermore, SRAM cells can be manufactured using a pure-logic type fabrication process, which is commonly used for non-memory circuit blocks.

In addition to random access memory (RAM) functions of writing and storing data, the CAM also searches and compares the stored data to determine if the data matches search data applied to the memory. When the newly applied search data matches the data already stored in the memory, a match result is indicated, whereas if the search and stored data do not match, a mismatch result is indicated. CAMs are particularly useful for fully associative memories such as look-up tables and memory-management units.

Many current applications utilise ternary CAMs, which are capable of storing three logic states. For example, the three logic states are logic '0', logic '1' and "don't care". Therefore, such CAM cells require two memory cells to store the logic states, as well as a comparison circuit for comparing stored data with search data provided to the CAM.

In ternary form, each conventional SRAM-based CAM memory cell comprises a regular six-transistor (6T) SRAM cells. Therefore, SRAM-based CAM cells typically use 12 transistors to implement two 6T SRAM cells. That is, each SRAM cell requires 2 p-channel transistors and 2 n-channel transistors in a cross-coupled inverter relationship and a further 2 n-channel transistors as access devices from the bit lines.

Furthermore, four additional transistors are required for each ternary CAM memory cell for implementing an exclusive-NOR function for comparing the search data with the stored data. For ternary CAM cells, n-channel devices are typically used in the comparison circuit.

Previous approaches in the art store data in a main memory cell and mask data in a mask memory cell. The comparison circuit is then either enabled or disabled by the mask memory cell contents. Examples of memory cells implementing such an approach are illustrated by U.S. Patent No. 6,154,384, issued to Nataraj et al. and U.S. Patent No. 6,108,227 issued to Voelkel. Although this approach is functional from a circuit point of view, difficulty arises when attempting to layout the elements of the CAM cells. The main problem is a non-optimised layout of the CAM cell, which takes up more silicon area than desired.

DRAM-based CAMs have also been proposed in the art. DRAM cells are typically physically smaller than SRAM cells. Therefore, DRAM-based CAMs have the advantage of being able to store much more data than SRAM-based CAMs for a given area due to the much smaller CAM cell size. However, because of the dynamic nature of the DRAM cell, which is used to implement a DRAM-based CAM cell, such cells require regular refresh operations in order to maintain the data.

U.S. Patent No. 6,188,594 issued to Ong describes a CAM cell using only n-channel transistors. The CAM cell uses only n-channel transistors. The size of the cell is significantly reduced since the p-channel transistors are eliminated. The cell size is further reduced by using dynamic storage rather than static storage in the CAM cell. The dynamic CAM cell as described has as few as six transistors, and a compact layout is facilitated. However, as previously mentioned, dynamic cells require regular refresh operations in order to maintain the data and such refresh circuitry takes up additional silicon area.

Therefore, there is a need for an SRAM-based CAM cell that achieves a more efficient spatial layout than the prior art, while maintaining the static characteristic of the SRAM-based CAM cell.

BRIEF DESCRIPTION OF DRAWINGS:

Figure 1 is a circuit diagram of a ternary CAM half-cell according to an embodiment of the invention;

Figure 2 is a circuit diagram of a full ternary SRAM-based CAM cell according to a first embodiment of the invention;

Figure 3 is a circuit diagram of a full ternary SRAM-based CAM cell according to a second embodiment of the invention;

Figure 4 is a plan view of a half-cell layout corresponding to circuit in figure 1; and

Figure 5 is a circuit diagram of a full ternary SRAM-based CAM cell according to the prior art.

SUMMARY OF THE INVENTION

In accordance with an aspect of the invention, there is provided a ternary data content addressable memory (CAM) half-cell. The CAM half-cell comprises a static random access memory (SRAM) cell, which comprises a pair of cross-coupled inverters, for storing a data value and a pair of access devices for accessing a pair of complementary bit lines. The CAM half-cell further comprises a compare circuit for comparing the data value stored in the SRAM cell with a search data value provided on a search line. The CAM half-cell comprises an equivalent number of n-channel and p-channel devices.

In accordance with a further aspect of the invention, there is provided a CAM cell comprising a pair of SRAM cells, each of which comprise a pair of cross coupled inverters for storing a data value and a pair of access devices for accessing a complementary pair of bit lines. The CAM cell further comprises a pair of compare circuits, each for comparing said data value stored in one of said SRAM cells with a search data value provided on a corresponding search line. The CAM cell has an equivalent number of n-channel and p-channel devices.

In accordance with yet a further aspect of the invention, the CAM cell has only one p+ region to n+ region separation.

The ternary SRAM-based CAM cell uses p-channel transistors as access transistors to the SRAM cells in order to improve the efficiency of the layout of the cell array. The implementation ensures a balanced number of p-channel and n-channel devices per cell while still providing excellent functional characteristics.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to figure 5, an SRAM-based CAM cell that is standard in the art is illustrated generally by numeral 500. The CAM cell comprises two 6T SRAM cells 502. Each SRAM cell 502 comprises two p-channel transistors and two n-channel transistors in a cross-coupled inverter relationship 506, and a further two n-channel transistors 508 as access devices from a pair of bit lines 510. The CAM cell further comprises a comparison circuit 512 with four additional n-channel transistors 508 for implementing an exclusive-NOR function for comparing search data with stored data.

The main problem with the implementation illustrated in figure 5 is an imbalance between transistor types, which leads to a non-optimised layout of the CAM cell. Specifically, out of the total of 16 transistors, only four are p-channel devices. Moreover, all n-channel devices in a cell need to be positioned in a common p diffusion region. This region includes the n-channel access devices 508, the n-channels of the cross-coupled inverters 506 and the n-channels of the comparison circuit 512. The inevitable result is an unbalanced layout with regions containing the n-channels highly congested and wasted space around the two remaining p-channels used for the pull-up devices in the cross-coupled inverter transistors 504.

It is a well-known design layout rule in the industry that n+ to p+ spacing is usually large relative to other design rules in a typical CMOS fabrication process. Also, the n+ to p+ spacing cannot contain transistors therein. Therefore, the aspect ratio of the cell should be made narrow. That is, the smaller dimension of a typical cell is in the direction of the line of the p-well separating n-channels and p-channels in the cell array. This minimises the area wasted in the p+ to n+ spacing. However, this is difficult to achieve given the imbalance between n-type and p-type devices in the conventional approach.

A reduction in ternary CAM cell area and optimization of a CAM cell layout is achieved by replacing n-channel access devices used for the SRAM cells with p-channel access devices and providing an active logic ‘0’ activated word line instead of an active logic ‘1’ activated word line. An SRAM cell with p-channel access devices is not normally used in conventional commodity or embedded SRAM applications due to the speed advantage of switching n-channel devices over p-channel devices. In a regular SRAM memory, the switching speed and other characteristics would suffer as a result. However, in a CAM cell, performance of the read/write is less critical than in a conventional SRAM cell since the primary task a CAM memory performs on a regular basis is a search and compare function.

Using p-channel access devices instead of n-channel access devices results in a full ternary CAM cell with a more balanced number of p-channel transistors and n-channel transistors. It is further preferable that the devices are balanced such that 8 n-channel devices and 8 p-channel devices are used in the layout.

Referring to figure 1, a CAM half-cell in accordance with an embodiment of the invention is illustrated generally by numeral 100. The half-cell 100 comprises a complimentary bit line pair BL and $\overline{BL}$, a word line WL, a search line SL, a match line ML, cross-coupled inverter transistors P1, N1, P2, and N2 and p-channel access devices P3 and P4.

P2 is coupled between a positive supply voltage 102 and a first node 104. N2 is coupled between the first node 104 and a ground supply voltage 106. Both P2 and N2 are gated by a second node 108. P1 is coupled between a positive supply voltage 102 and the second node 108. N1 is coupled between the second node 108 and a ground supply voltage 106. Both P1 and N1 are gated by the first node 104.

The first node 104 is coupled to bit line BL via access transistor P3. P3 is gated by the word line WL. The second node 108 is couple to bit line $\overline{BL}$ via access transistor P4. P4 is also gated by the word line WL. The p-channel access devices P3 and P4 selectively connect the cross-coupled inverters to complementary bit lines BL and $\overline{BL}$ which carry read/write data.

The match line ML is coupled to ground via serially coupled transistors N3 and N4. N4 is gated by the search line SL and N3 is gated by the second node 108. As can be seen from figure 1, there are four p-channel transistors and four n-channel transistors comprising the half-cell as opposed to two p-channel transistors and six n-channel transistors as discussed regarding the prior art approach.

Referring to figure 2 a full ternary CAM cell in accordance with an embodiment of the present invention is illustrated generally by numeral 200. The full ternary CAM cell comprises 8 p-channel transistors and 8 n-channel transistors. The transistors of the first SRAM cell component of the full ternary CAM cell are numbered similarly to the corresponding transistors in figure 1 for convenience. For the second SRAM cell component of the CAM cell, the cross-coupled inverter transistors are labelled P12, N12, P11 and N11, the access transistors are labelled P13 and P14, and the transistors serially coupled between the match line ML and ground are labelled N14 and N13 respectively. It will be noted that for a full ternary CAM cell there are two complementary bit line pairs, $BL1$, $\overline{BL1}$ and $BL2$, $\overline{BL2}$ and two search lines $SL1$ and $SL2$.

The general operation of the full ternary CAM cell 200 illustrated in figure 2 is now described. To perform a write operation, data to be stored in the CAM cell is loaded onto bit line pairs BL1, $\overline{BL1}$, and BL2, $\overline{BL2}$. The word line WL is asserted active logic '0' turning on p-channel access transistors P3, P4, P13 and P14. The data carried on the complementary bit line pairs is thereby written into the two SRAM cells and the word line is de-asserted.

For a read operation, the complementary bit line pairs are precharged to VDD/2. The word line is asserted active logic '0' and the data from the SRAM cells is read onto the bit line pairs. The data then is transferred to data buses (not shown).

For a search and compare operation, the match line is precharged to logic '1' and data is placed on the search lines SL1 and SL2. Typically, search data and stored data are provided in such a manner that in the case of a mismatch a change occurs in the match line state. It is preferable to change the match line state for a mismatch rather than a match because a mismatch is a more infrequent occurrence. Therefore, a change in match line state will occur infrequently, reducing power dissipated by discharging match lines. The match line *ML* is precharged to a logic '1' and a mismatch discharges the match line to ground, whereas in the case of a match no change occurs in the state of the match line. Alternatively, in another match line sensing approach, the match line is precharged to logic '0' and detection of a match is made by pulling up with a device that is weaker than the two series devices holding the match line at logic '0'.

If the CAM cell 200 stores a logic '1' in the left SRAM cell and a logic '0' in the right SRAM cell, *SL1* has logic '1', and *SL2* has logic '0', a mismatch will result as follows. The output of the left SRAM cell provides a logic '1' to transistor N3, turning it on. The search line *SL1* provides a logic '1' to transistor N4, turning it on. Since N3 and N4 are both turned on, they provide a path to discharge the match line *ML* to ground and thus indicate a mismatch.

If the CAM cell stores a logic '0' in the left SRAM cell and a logic '1' in the right SRAM cell, a match condition will result as follows. The output of the left SRAM cell provides a logic '0' to the gate of transistor N3, leaving it turned off. The search line *SL1* provides a logic '1' to the gate of transistor N4, turning it on. However, since N3 and N4 are serially connected, a path to ground does not exist for discharging the match line *ML* to ground. Similarly, the right SRAM cell provides a logic '1' to transistor N13, turning it on. The search line *SL2* provides a logic '0' to transistor N14, leaving it turned off. Therefore, similarly to the left SRAM cell, transistors N13 and N14 do not provide a path to discharge the match line *ML* to ground. As a result, the match line remains precharged to logic '1' indicating a match condition.

If the CAM cell stores a logic '0' in both the right and left SRAM cells a "don't care" state exists. The output from each SRAM cell produces a logic '0'. The logic '0' is provided to the gate of transistors N3 and N13, ensuring that a match condition is detected regardless of the data provided on the search lines SL1, SL2, and the match line remains unchanged.

This description of the basic operation only covers one possible match line detection scheme. However other approaches, including those common in the art as well as proprietary approaches, may be implemented without departing from the scope of the invention.

Referring to figure 3, an alternate embodiment of the invention is illustrated generally by numeral 300. In the present embodiment, access devices of the SRAM cells N23, N24, N33, N34 are n-channel devices and the transistors of the comparison circuit P23, P24, P33, P34 are p-channel devices. The operation is similar to the operation of the embodiment illustrated in figure 2 with the appropriate voltages reversed for devices of different polarities, as will be apparent to a person skilled in the art. For example, the word line *WL* is asserted active logic '1'. Further, the match line *ML* is logic '0' and a mismatch charges the match line *ML* to logic '1'.

Referring to Figure 4, a layout of a ternary CAM half-cell in accordance with the present embodiment is illustrated generally by numeral 400. The layout 400 corresponds to the circuit 100 illustrated in figure 1. For convenience, the transistor labels from figure 1, that is P1, P2, P3, P4, N1, N2, N3, and N4, are provided for indicating corresponding areas in the layout 400. In the layout 400, broken lines enclose regions representing active semiconductor areas 405 (for example, diffusion or ion-implanted areas). These areas include p-type active regions 405a and n-type active regions 405b. Thick, solid, continuous lines enclose a polysilicon layer 410 while thin solid continuous lines enclose a metal 1 layer 420. The metal 1 layer 420 provides a metal interconnect between a plurality of metal contacts 404. The metal contacts 404 are represented by squares with an X symbol therein. Of special note is the metal 1 layer 420 connection for the cross coupled inverters formed by P2, N2, and P1, N1. Other higher metal layers (there are typically several metal layers) are not illustrated for simplicity. These include the search lines SL, complementary bit lines BL and $\overline{BL}$, which are in a metal 3 *M3* layer. These and other layers will be apparent to a person skilled in the art.

As can be seen in figure 4 the p-channel devices P1, P2, P3, and p4 are grouped at the top of the figure, using a single n-well, while the n-channel devices N1, N2, N3, and N4 are grouped at the bottom, using a single p-well. This grouping results in a well-balanced use of cell area. Further, the compare circuitry N3 and N4 is separated spatially from the access devices P3 and P4, which yields a well-packed efficient layout with a desirably narrow aspect ratio. As such, only one p+ region to n+ region separation is necessary for the entire cell unlike prior art approaches which required at least two p+ region to n+ region separations. Further advantages of the layout described above include having the connections to the search transistors (N3, N4) at the opposite end of the connections to the access transistors (P3, P4). This separation eases congestion in the upper layers of metal. Furthermore, the cell is close to the minimum width set by transistor geometries, local interconnect (or metal 1), and upper metals simultaneously.

A minimal width and improved aspect ratio mean smaller area and reduced match line length, which is important to increasing speed and reducing power consumption. Analysis reports demonstrate that prior art approaches using a 0.13um pure logic process utilise a cell size that is approximately 40% larger than a cell implemented using a layout in accordance with the present invention.

Although the invention has been described with reference to specific embodiments, various modifications will become apparent to a person skilled in the art with departing from the spirit of the invention.

CLAIMS:

1. A ternary content addressable memory (CAM) half-cell comprising:

(a) a static random access memory (SRAM) cell having:

i. a pair of cross coupled inverters for storing a data value;

ii. a pair of access devices, each coupled between respective ones of said pair of cross coupled inverters and a pair of complementary bit lines for accessing said pair of complementary bit lines; and

(b) a compare circuit for comparing said data value stored in said SRAM cell with a search data value provided on a search line, said CAM cell having an equivalent number of n-channel and p-channel devices.

2. The ternary CAM half-cell as defined in claim 1, wherein said cross coupled inverter comprises a pair of n-channel devices and a pair of p-channel devices.

3. The ternary CAM half-cell as defined in claim 2, wherein said pair of access devices comprises p-channel devices and said compare circuit comprises n-channel devices.

4. The ternary CAM half-cell as defined in claim 2, wherein said pair of access devices comprises n-channel devices and said compare circuit comprises p-channel devices.

5. A ternary content addressable memory (CAM) cell comprising:

(a) a pair of static random access memory (SRAM) cells, each of said SRAM cells having:

i. a pair of cross coupled inverters for storing a data value;

ii. a pair of access devices, each coupled between respective ones of said pair of cross coupled inverters and a pair of complementary bit lines for accessing said pair of complementary bit lines; and

(b) a pair of compare circuits, each for comparing said data value stored in one of said SRAM cells with a search data value provided on an associated search line, said CAM cell having an equivalent number of n-channel and p-channel devices.

6. The ternary CAM cell as defined in claim 5, wherein all p-channel devices are formed in one n-well region and all n-channel devices are formed in one p-well region.

7. The ternary CAM cell as defined in claim 5, wherein said cross coupled inverter comprises a pair of n-channel devices and a pair of p-channel devices.

8. The ternary CAM cell as defined in claim 7, wherein said pair of access devices comprises p-channel devices and said compare circuit comprises n-channel devices.

9. The ternary CAM cell as defined in claim 7, wherein said pair of access devices comprises n-channel devices and said compare circuit comprises p-channel devices.

10. The ternary CAM cell as defined in claim 5, wherein all p-channel devices are formed in one n-well region and all n-channel devices are formed in one p-well region.

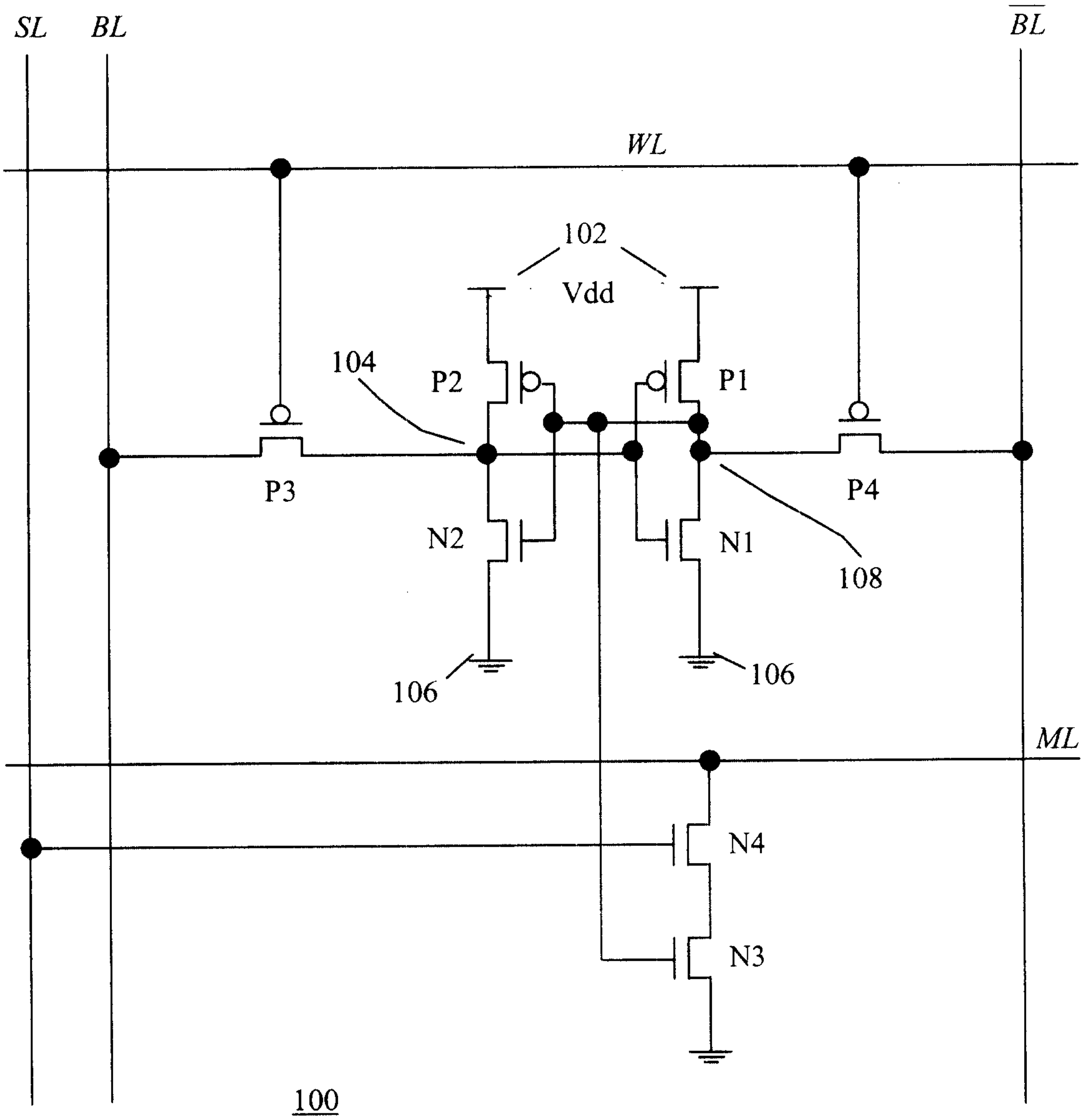
11. A ternary content addressable memory (CAM) half-cell comprising:

(a) a static random access memory (SRAM) cells having:

i. a pair of cross coupled inverters for storing a data value;

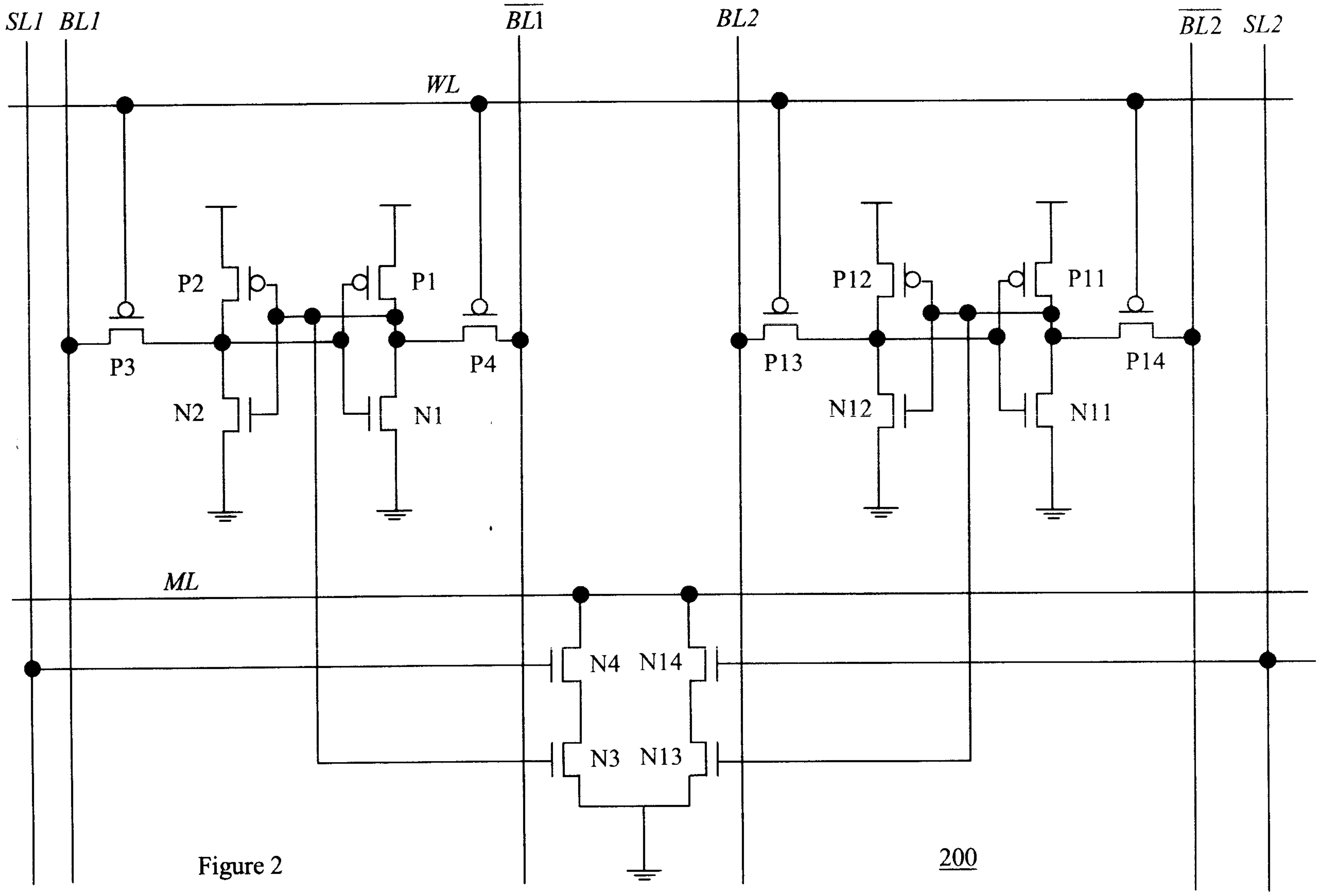
ii. a pair of access devices, each coupled between respective ones of said pair of cross coupled inverters and a pair of complementary bit lines for accessing said pair of complementary bit lines; and

(b) a compare circuit for comparing said data value stored in said SRAM cell with a search data value provided on a search line, said CAM cell having only one p+ region to n+ region separation.



SL
BL
$\overline{BL}$
WL
102
Vdd
104
P2
P1
P3
P4
N2
N1
108
106
106
ML
N4
N3
100

Figure 1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BL1
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BL2
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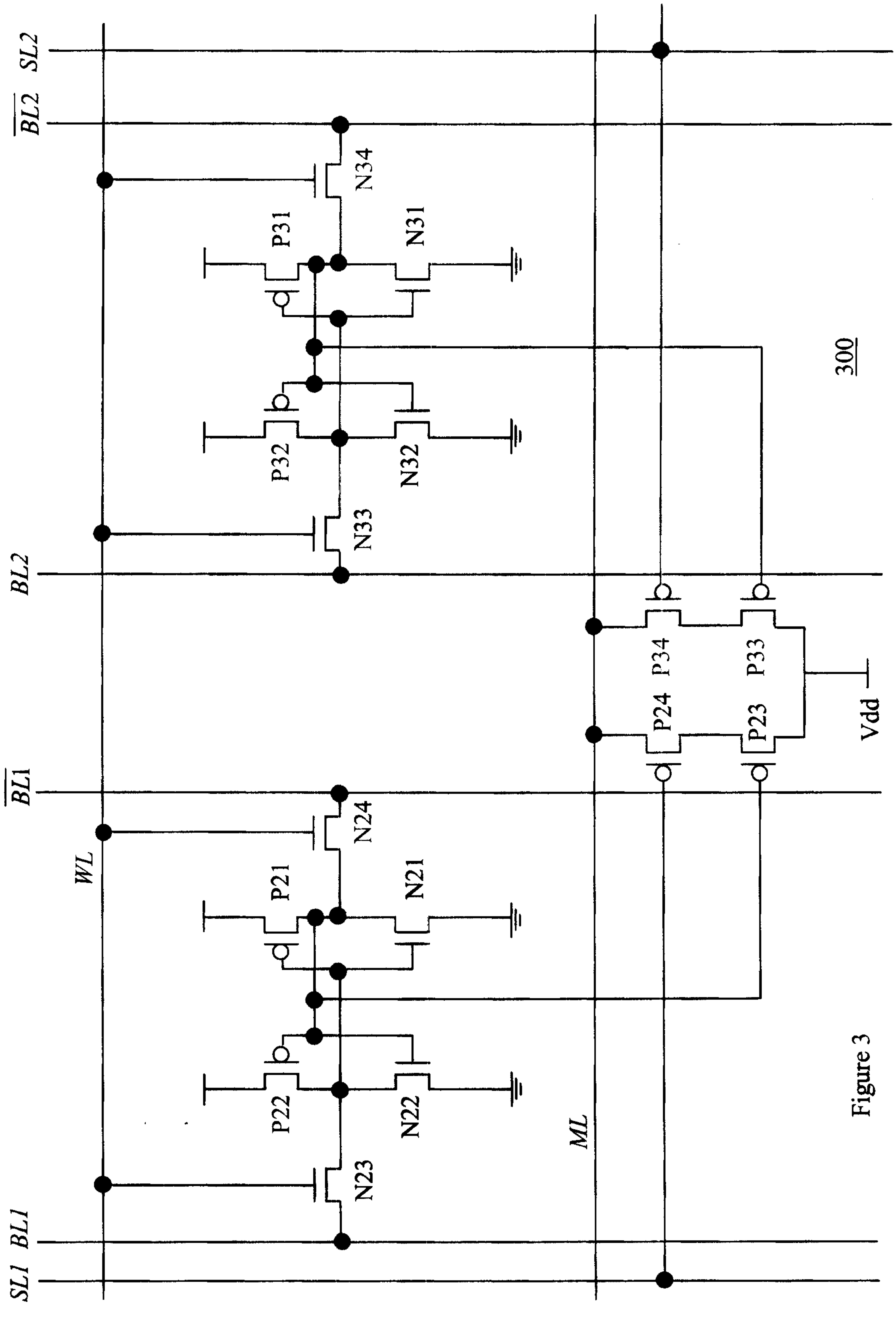
SL2
WL
P2
P1
P12
P11
P3
P4
P13
P14
N2
N1
N12
N11
ML
N4
N14
N3
N13
200

Figure 2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N34
P31
N31
P32
N32
N33
BL2
P34
P33
P24
P23
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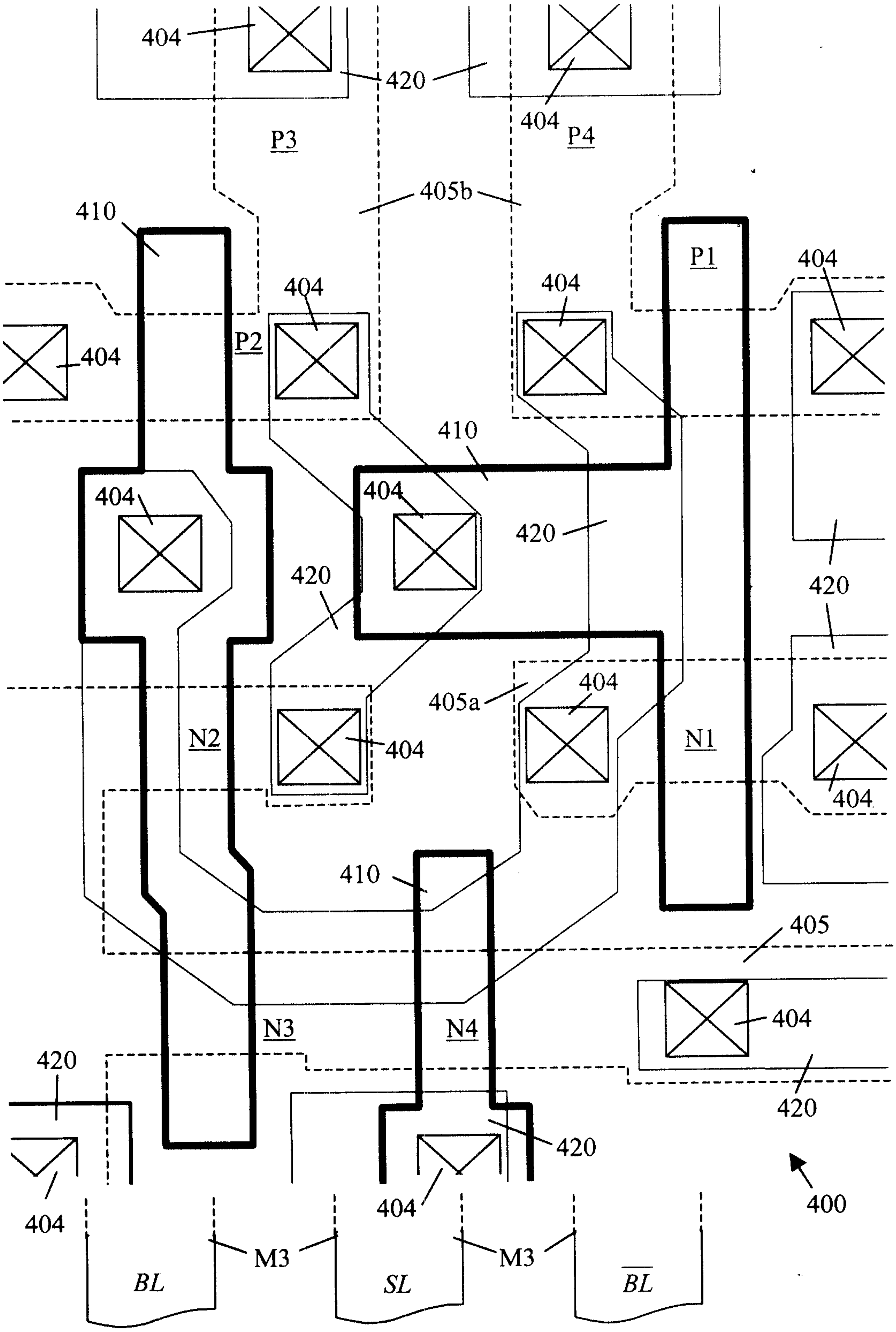
N24
WL
P21
N21
P22
N22
N23
ML
BL1
SL1
300

Figure 3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405a
404
N2
404
N1
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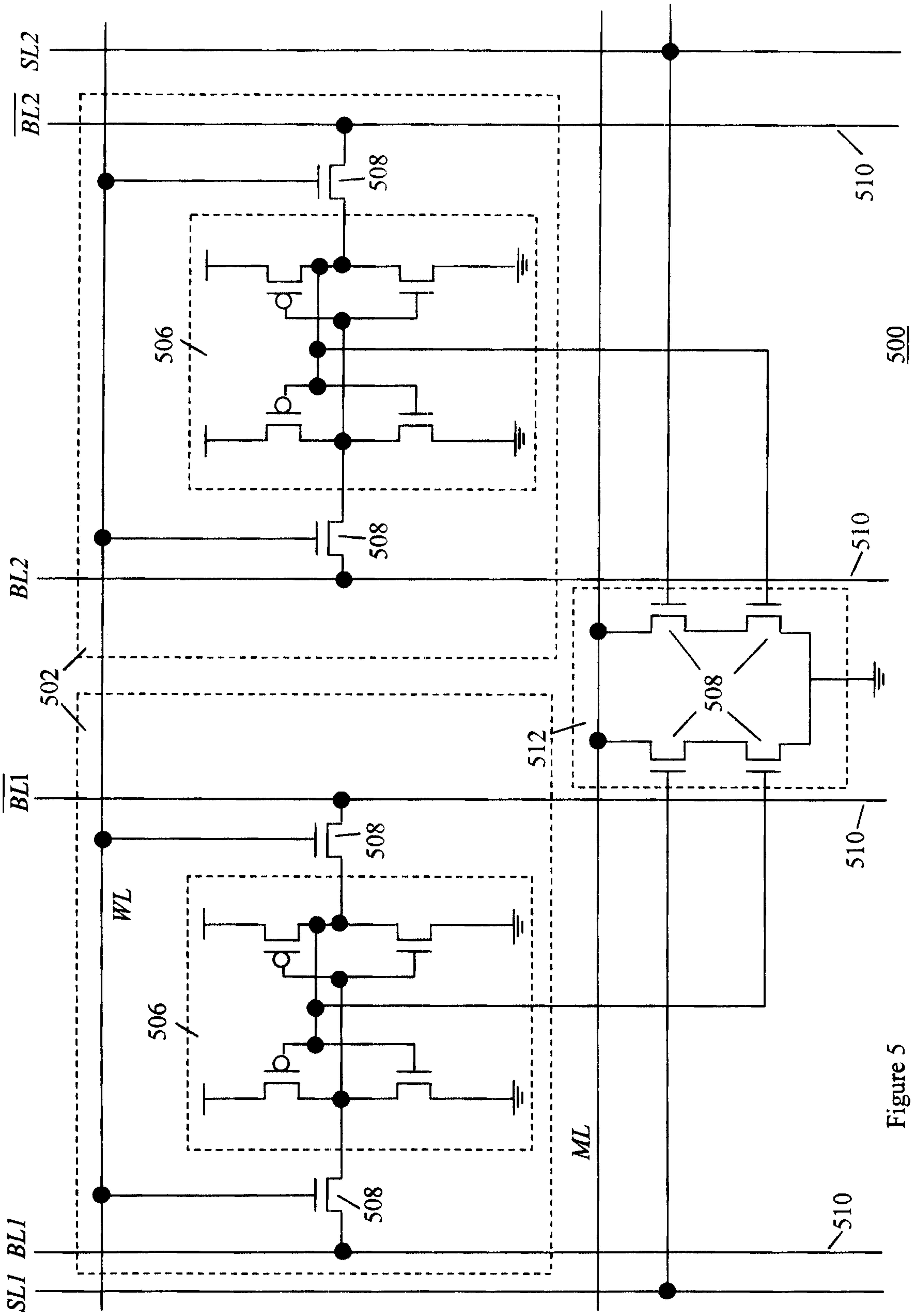
404
400
M3
M3
BL
SL
$\overline{BL}$

Figure 4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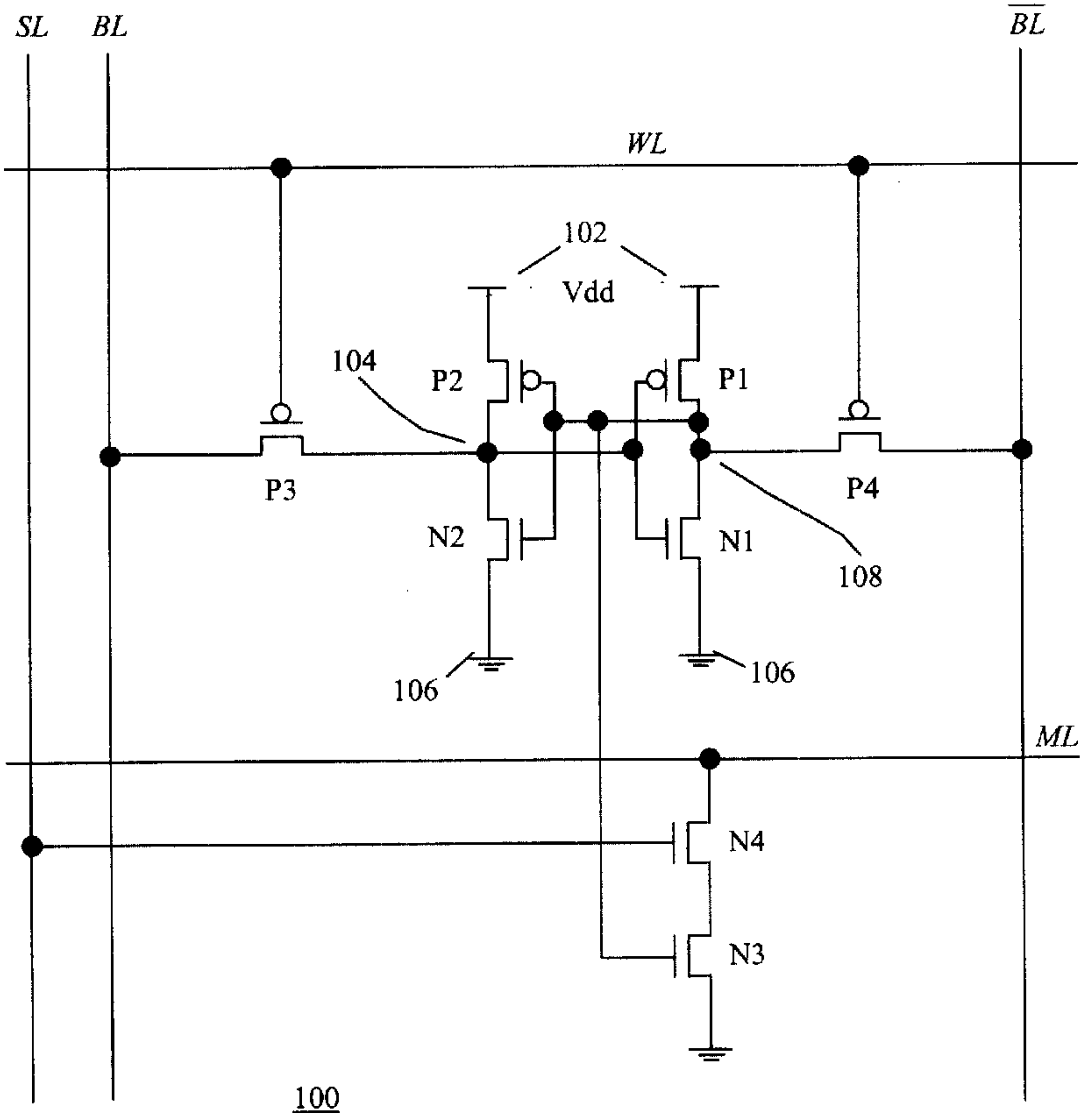
500

Figure 5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P3
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N3
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