(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 July 2014 (10.07.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/107301 A1

(51) International Patent Classification:
H01L 23/498 (2006.01) *H01L 23/00* (2006.01)
H01L 25/10 (2006.01) *H01L 23/31* (2006.01)
H01L 25/065 (2006.01)

(21) International Application Number:
PCT/US2013/075672

(22) International Filing Date:
17 December 2013 (17.12.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/722,189 20 December 2012 (20.12.2012) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: STRUCTURE FOR MICROELECTRONIC PACKAGING WITH ENCAPSULATED BOND ELEMENTS

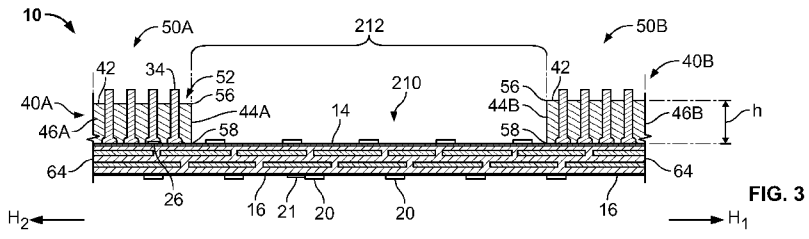

FIG. 3

(57) Abstract: A structure (10) may include bond elements (24) having bases joined to conductive elements (18) at a first portion of a first surface and end surfaces remote from the substrate (12). A dielectric encapsulation element (40) may overlie and extend from the first portion and fill spaces between the bond elements (24) to separate the bond elements (24) from one another. The encapsulation element (40) has a third surface facing away from the first surface. Unencapsulated portions of the bond elements (24) are defined by at least portions of the end surfaces uncovered by the encapsulation element at the third surface. The encapsulation element (40) at least partially defines a second portion (210) of the first surface that is other than the first portion and has an area sized to accommodate an entire area of a microelectronic element (602). Some conductive elements (18) are at the second portion and configured for connection with such microelectronic element (602).

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STRUCTURE FOR MICROELECTRONIC PACKAGING WITH ENCAPSULATED BOND ELEMENTS

CROSS-REFERENCE TO RELATED APPLICATIONS.

[0001] The present application is a continuation of U.S. Application No. 13/722,189, filed on December 20, 2012, the disclosure of which is hereby incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to structures for microelectronic packaging.

BACKGROUND OF THE INVENTION

[0003] Microelectronic elements such as semiconductor chips commonly are provided with elements which protect the microelectronic element and facilitate its connection to other elements of a larger circuit. For example, a semiconductor chip typically is provided as a small, flat element having oppositely facing front and rear surfaces and contacts at the front surface. The contacts are electrically connected to the numerous electronic circuit elements formed integrally within the chip. Such a chip most commonly is provided in a package having a miniature circuit panel referred to as a substrate. The chip is typically mounted to the substrate with the front or rear surface overlying a surface of the substrate, and the substrate typically has terminals at a surface of the substrate. The terminals are electrically connected to the contacts of the chip. The package typically also includes some form of covering overlying the chip on the side of the chip opposite from the substrate. The covering serves to protect the chip and, in some cases, the connections between the chip and the conductive elements of the substrate. Such a packaged chip may be mounted to a circuit panel, such as a circuit board,

by connecting the terminals of the substrate to conductive elements such as contact pads on the larger circuit panel.

[0004] In certain packages, the chip is mounted with its front or back surface overlying an upper surface of the substrate, whereas terminals are provided on the oppositely facing lower surface. A mass of a dielectric material overlies the chip and, most typically, the electrical connections between the chip and the conductive elements of the substrate. The dielectric mass may be formed by molding a flowable dielectric composition around the chip so that the dielectric composition covers the chip and all or part of the top surface of the substrate. Such a package is commonly referred to as an "overmolded" package, and the mass of dielectric material is referred to as the "overmold." Overmolded packages are economical to manufacture and thus are widely used.

[0005] In some applications, it is desirable to stack chip packages on top of one another, so that plural chips may be provided in the same space on the surface of the larger circuit panel. Also, it is desirable to have a large number of input/output interconnections to the chips. Certain overmolded packages incorporate stacking contacts at the top surface of the substrate outside of the area covered by the chip and, typically, outside of the area covered by the overmold. Such packages may be stacked one atop the other with interconnecting elements such as solder balls, elongated posts, wire bonds or other conductive connections extending between the stacking contacts of the lower package and the terminals of the next higher package in the stack. In such an arrangement, all of the packages in the stack are electrically connected to the terminals on the package at the bottom of the stack. In addition, because the substrate of the higher package in the stack sits above the dielectric

overmold in the next lower package, there is an appreciable gap in the vertical direction between the terminals of the higher package and the stacking contacts of the lower package. The interconnecting elements must bridge this gap.

[0006] Despite the considerable effort devoted in the art to development of stackable packages and other packages having top-surface mounting pads, further improvement would be desirable.

SUMMARY OF THE INVENTION

[0007] In accordance with one embodiment, a structure may include a substrate having first and second oppositely facing surfaces and a plurality of electrically conductive elements at the first surface. In addition, the structure may include bond elements having bases joined to respective ones of the conductive elements at a first portion of the first surface and end surfaces remote from the substrate and the bases, where each of the bond elements extend from the base to the end surface thereof. Further the structure may include a dielectric encapsulation element overlying and extending from the first portion of the first surface of the substrate and filling spaces between the bond elements such that the bond elements are separated from one another by the encapsulation element, the encapsulation element having a third surface facing away from the first surface of the substrate and having an edge surface extending from the third surface towards the first surface, where unencapsulated portions of the bond elements are defined by at least portions of the end surfaces of the bond elements that are uncovered by the encapsulation element at the third surface, the encapsulation element at least partially defines a second portion of the first surface, the second portion being other than the first portion of the first surface and having an area sized to accommodate an entire area of a microelectronic element, and

at least some of the conductive elements at the first surface are at the second portion and configured for connection with such microelectronic element.

[0008] In accordance with another embodiment, a method of making a structure may include forming a dielectric encapsulation element on a substrate, the substrate having first and second oppositely facing surfaces and a plurality of electrically conductive elements at the first surface, where bond elements are joined at bases thereof to respective ones of the conductive elements at a first portion of the first surface and end surfaces of the bond elements are remote from the substrate and the bases, each of the bond elements extending from the base to the end surface thereof, where the dielectric encapsulation element is formed overlying and extending from the first portion of the first surface of the substrate and filling spaces between the bond elements such that the bond elements are separated from one another by the encapsulation element, the encapsulation element having a third surface facing away from the first surface of the substrate and having an edge surface extending from the third surface towards the first surface, where unencapsulated portions of the bond elements are defined by at least portions of the end surfaces of the bond elements that are uncovered by the encapsulation element at the third surface, where the encapsulation element at least partially defines a second portion of the first surface, the second portion being other than the first portion of the first surface and having an area sized to accommodate an entire area of a microelectronic element, and at least some of the conductive elements at the first surface are at the second portion and configured for connection with such microelectronic element.

[0009] In accordance with another embodiment, a structure may include an active die having first and second oppositely facing surfaces and a plurality of electrically conductive elements at the first surface. In addition, the structure may include bond elements having bases joined to respective ones of the conductive elements at a first portion of the first surface and end surfaces remote from the die and the bases, each of the bond elements extending from the base to the end surface thereof. Further, the structure may include a dielectric encapsulation element overlying and extending from the first portion of the first surface of the die and filling spaces between the bond elements such that the bond elements are separated from one another by the encapsulation element, the encapsulation element having a third surface facing away from the first surface of the die and having an edge surface extending from the third surface towards the first surface, wherein unencapsulated portions of the bond elements are defined by at least portions of the end surfaces of the bond elements that are uncovered by the encapsulation element at the third surface. The encapsulation element may at least partially define a second portion of the first surface, the second portion being other than the first portion of the first surface and having an area sized to accommodate an entire area of a microelectronic element, and at least some of the conductive elements at the first surface are at the second portion and configured for connection with such microelectronic element.

[0010] In accordance with another embodiment, a method of making a structure may include forming a dielectric encapsulation element on an active die provided at wafer level. The die may have first and second oppositely facing surfaces and a plurality of electrically conductive elements at the first surface, where bond elements may be joined at

bases thereof to respective ones of the conductive elements at a first portion of the first surface and end surfaces of the bond elements are remote from the substrate and the bases, each of the bond elements extending from the base to the end surface thereof, where the dielectric encapsulation element is formed overlying and extending from the first portion of the first surface of the die and filling spaces between the bond elements such that the bond elements are separated from one another by the encapsulation element, the encapsulation element having a third surface facing away from the first surface of the die and having an edge surface extending from the third surface towards the first surface, where unencapsulated portions of the bond elements are defined by at least portions of the end surfaces of the bond elements that are uncovered by the encapsulation element at the third surface, and where the encapsulation element at least partially defines a second portion of the first surface, the second portion being other than the first portion of the first surface and having an area sized to accommodate an entire area of a microelectronic element, and at least some of the conductive elements at the first surface are at the second portion and configured for connection with such microelectronic element.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. 1 is a diagrammatic sectional view depicting a substrate used in a method of manufacturing a structure, according to an embodiment of the disclosure.

[0012] FIG. 2 is a diagrammatic sectional view depicting the substrate and associated elements at a later stage of manufacturing operations, according to an embodiment of the disclosure.

[0013] FIG. 3 is a diagrammatic sectional view depicting a structure made using the substrate and the associated

elements of FIGs. 1-2, according to an embodiment of the disclosure.

[0014] FIG. 4A is a diagrammatic sectional view of an exemplary structure, according to an embodiment of the disclosure.

[0015] FIG. 4B is a diagrammatic sectional view of the structure of FIG. 4A at a later stage of manufacturing operations.

[0016] FIG. 4C is a diagrammatic sectional view of another exemplary structure, according to an embodiment of the disclosure.

[0017] FIG. 4D is a diagrammatic sectional view of the structure of FIG. 4C at a later stage of manufacturing operations.

[0018] FIG. 5 is a diagrammatic sectional view of another exemplary structure, according to an embodiment of the disclosure.

[0019] FIG. 6 is a diagrammatic sectional view of another exemplary structure, according to an embodiment of the disclosure.

[0020] FIG. 7A is a diagrammatic top plan view depicting the structure of FIG. 3.

[0021] FIGs. 7B-7C are diagrammatic top plan views depicting exemplary structures, in accordance with the disclosure.

[0022] FIG. 7D is a diagrammatic top plan view depicting the structure of FIG. 5.

[0023] FIG. 7E is a diagrammatic top plan view depicting an exemplary structure, in accordance with the disclosure.

[0024] FIG. 8 is a diagrammatic sectional view of an exemplary package assembly including the structure of FIG. 3, in accordance with the disclosure.

[0025] FIG. 9 is a diagrammatic sectional view of another exemplary package assembly including the structure of FIG. 3, in accordance with the disclosure.

[0026] FIG. 10A is a diagrammatic sectional view of another exemplary package assembly including the structure of FIG. 3, in accordance with the disclosure.

[0027] FIG. 10B is a diagrammatic sectional view of another exemplary package assembly including the structure of FIG. 3, in accordance with the disclosure.

[0028] FIG. 11 is a bottom plan view of the package assembly of FIG. 10A.

[0029] FIG. 12 is a diagrammatic sectional view of an exemplary package assembly including the structure of FIG. 5, in accordance with the disclosure.

[0030] FIG. 13 is a diagrammatic view depicting a system according with the disclosure.

[0031] FIG. 14 is a diagrammatic sectional view depicting an active die and associated elements at a stage of manufacturing a structure, according to an embodiment of the disclosure.

[0032] FIG. 15 is a diagrammatic sectional view depicting the structure made using the die and the associated elements of FIG. 14, according to an embodiment of the disclosure.

[0033] FIG. 16A is a diagrammatic sectional view of an exemplary structure including an active die, according to an embodiment of the disclosure.

[0034] FIG. 16B is a diagrammatic sectional view of the structure of FIG. 16A at a later stage of manufacturing operations.

[0035] FIG. 16C is a diagrammatic sectional view of another exemplary structure including an active die, according to an embodiment of the disclosure.

[0036] FIG. 16D is a diagrammatic sectional view of the structure of FIG. 16C at a later stage of manufacturing operations.

[0037] FIG. 17 is a diagrammatic sectional view of an exemplary package assembly including the structure of FIG. 15, in accordance with the disclosure.

[0038] FIG. 18 is a diagrammatic sectional view of an exemplary package assembly including the structure of FIG. 15, in accordance with the disclosure.

[0039] FIG. 19 is a diagrammatic sectional view of an exemplary package assembly including the structure of FIG. 15, in accordance with the disclosure.

[0040] FIG. 20 is a diagrammatic sectional view of an exemplary package assembly including a structure, in accordance with the disclosure.

[0041] FIG. 21 is a diagrammatic sectional view of an exemplary package assembly including a structure, in accordance with the disclosure.

DETAILED DESCRIPTION

[0042] A structure 10 (see FIG. 3) according to one embodiment of the disclosure may include a substrate 12 (see FIG. 1) having a first surface 14 and a second surface 16. The substrate 12 typically is in the form of a dielectric element, which is substantially flat. The dielectric element may be sheet-like and thin. In particular embodiments, the dielectric element may include one or more layers 23 of organic dielectric material or composite dielectric materials, such as, without limitation: polyimide, polytetrafluoroethylene ("PTFE"), epoxy, epoxy-glass, FR-4, BT resin, thermoplastic, or thermoset plastic materials. The first surface 14 and second surface 16 are preferably substantially parallel to each other and are spaced apart at a distance perpendicular to the surfaces 14 and 16 defining

the thickness of the substrate 12. The thickness of substrate 12 is preferably within a range of generally acceptable thicknesses for the present application. In an embodiment, the distance between the first surface 14 and the second surface 16 is between about 25 and 500 µm. For purposes of this discussion, the first surface 14 may be described as being positioned opposite or remote from the second surface 16. Such a description, as well as any other description of the relative position of elements used herein that refers to a vertical or horizontal position of such elements is made for illustrative purposes only to correspond with the position of the elements within the Figures, and is not limiting.

[0043] Electrically conductive elements 18, which may include contacts or pads, traces or terminals, are at the first surface 14 of the substrate 12. As used in this disclosure, a statement that an electrically conductive element is "at" a surface of a substrate indicates that, when the substrate is not assembled with any other element, the electrically conductive element is available for contact with a theoretical point moving in a direction perpendicular to the surface of the substrate toward the surface of the substrate from outside the substrate. Thus, a terminal or other conductive element which is at a surface of a substrate may project from such surface; may be flush with such surface; or may be recessed relative to such surface in a hole or depression in the substrate. In addition, as used in this disclosure a statement that an electrically conductive element is "at" a surface of a circuit panel, a microelectronic element such as a semiconductor chip or a like element, indicates that, when the panel or the element is not assembled with any other element, the electrically conductive element is available for contact with a

theoretical point moving in a direction perpendicular to the surface of the panel or element toward the surface of the panel or element from outside the panel or element. Further, as used in this disclosure, a statement that a trace extends "along" a surface means that the trace extends in proximity to the surface and substantially parallel to the surface.

[0044] Traces 29 included as the conductive elements 18 may be formed as flat, thin, elongated strips of conductive material at the surface 14. In some embodiments, the traces may be formed integrally with and extend from terminals 27 included as the conductive elements 18 having a similar composition. In addition, contact pads 26 included as the conductive elements 16 on the surface 14 may be interconnected by traces 29 on the surface 14.

[0045] The terminals, pads or traces serving as the conductive elements 18 may be fabricated by numerous known methods, such as by plating the terminals, pads and traces onto the surface 14 of the substrate. In one embodiment, the traces may be embedded in the surfaces of the substrate, with the surfaces of the traces lying substantially flush with the surfaces of the substrate. In one embodiment, the conductive elements 18 may be formed from a solid metal material such as copper, copper, gold, nickel, or other materials that are acceptable for such an application, including various alloys including one or more of copper, gold, nickel or combinations thereof.

[0046] At least some of conductive elements 18 may be interconnected with second conductive elements 20, which may include conductive pads, traces or terminals similarly as described with respect to the conductive elements 18, at the second surface 16 of the substrate 12. Such an interconnection may be completed using vias 22 formed in the substrate 12 that may be lined or filled with conductive

metal that may be of the same material as the conductive elements 18 and 20. The vias 22 in the substrate 12 desirably are fully closed by traces at the surfaces 14 or 16 of the substrate 12 or traces 19 within the substrate 12. The substrate 12 may include a plurality of dielectric material layers 23 with a layer of traces 19 disposed between adjacent ones of the layers 23. Contact pads 25 and terminals 31 included as the conductive elements 18 may be further interconnected by traces 33 on the surface 16 also serving as the conductive elements 18.

[0047] Referring to FIG. 2, the structure 10 may further include a plurality of bond elements 24 joined with at least some of the conductive elements 18, such as on pads 26 thereof, at a portion 50 of the surface 14. The portion 50 may include one or more areas of the surface 14, such as portions 50A and 50B as shown in FIG. 7A. The bond elements 24 are joined at a base 28 thereof to the pads 26 and may extend to a free end 30 remote from the respective bases 28 and from the substrate 12. The ends 30 of the bond elements 24 are characterized as being free in that they are not electrically connected or otherwise joined to a microelectronic element electrically connected to the conductive elements 18 at the surface 14 or any other conductive features within a microelectronic assembly including the structure 10 that are, in turn, connected to such microelectronic element. In other words, the free ends 30 are available for electronic connection, either directly or indirectly as through a solder ball or other features discussed herein, to a conductive feature external to a microelectronic assembly including the structure 10. The fact that the ends 30 may be held in a predetermined position by, for example, an encapsulant material, such as forming a dielectric encapsulation element 40 as discussed below in the

text accompanying the description of FIGs. 3 and 4A-4D, or otherwise joined or electrically connected to another conductive feature, does not mean that they are not "free" as described herein, so long as any such feature is not electrically connected to a microelectronic element joined with the conductive elements at the surfaces, such as the surfaces 14 or 16, to which the bases thereof are joined. Conversely, base 28 is not free as it is either directly or indirectly electrically connected to a microelectronic element connected at the surfaces 14 or 16, as described herein.

[0048] As shown in FIG. 2, the base 28 may be substantially rounded in shape, extending outward from an edge surface 32 of the bond element 24, which may be a wire bond, defined between the base 28 and the end 30. The particular size and shape of the base 30 may vary according to the type of material used to form the wire bond 24, the desired strength of the connection between the wire bond 24 and the conductive element 18, or the particular process used to form the wire bond 24. Exemplary methods for making the wire bonds 24 are described in U.S. Pat. No. 7,391,121 to Otremba and in U.S. Pat. App. Pub. No. 2005/0095835, the disclosures of which are both incorporated herein by reference in their entireties. In an alternative embodiment, some of the wire bonds 24 may be joined to conductive elements 20 at the second surface 16 of substrate 12, through the conductive elements 19 and conductive material in the vias 22 within the substrate 12.

[0049] The bond elements 24 may be made from a conductive material such as copper, gold, nickel, solder, aluminum or the like. Additionally, the bond elements 24 may be made from combinations of materials, such as from a core of a conductive material, such as copper or aluminum, for example,

with a coating applied over the core. The coating may be of a second conductive material, such as aluminum, nickel or the like. Alternatively, the coating may be of an insulating material, such as an insulating jacket. In an embodiment, the wire used to form bond elements 24 may have a thickness, *i.e.*, in a dimension transverse to the wire's length, of between about 15 µm and 150 µm.

[0050] In other embodiments, including those in which wedge bonding is used, wire bonds 24 may have a thickness of up to about 500 µm. In general, a wire bond is formed on a conductive element, such as conductive element 26 that is a pad or the like, using specialized equipment that is known in the art. A leading end of a wire segment is heated and pressed against the receiving surface to which the wire segment bonds, typically forming a ball or ball-like base 28 joined to the surface of the pad 26. The desired length of the wire segment to form the wire bond is drawn out of the bonding tool, which may then cut the wire bond at the desired length. Wedge bonding, which may be used to form wire bonds of aluminum, for example, is a process in which the heated portion of the wire is dragged across the receiving surface to form a wedge that lies generally parallel to the surface. The wedge-bonded wire bond may then be bent upward, if necessary, and extended to the desired length or position before cutting. In a particular embodiment, the wire used to form a wire bond may be cylindrical in cross-section. Otherwise, the wire fed from the tool to form a wire bond or wedge-bonded wire bond may have a polygonal cross-section such as rectangular or trapezoidal, for example.

[0051] The free end 30 of the wire bond 24 has an end surface 34. The end surface 34 may form at least a part of a contact in an array formed by respective end surfaces 34 of a plurality of wire bonds 24.

[0052] Referring to FIG. 3, the structure 10 may further include encapsulation elements 40A and 40B formed from a dielectric material. In the embodiment of FIG. 3, the encapsulation elements 40 may be formed over the portion 50 of the first surface 14 of the substrate 12, and define a top surface 42 remote and facing away from the substrate 12. The material of the element 40 fills spaces between the bond elements 24, such that the bond elements 24 are separated from one another by the material of the encapsulation elements 40. Unencapsulated portions 52 of the bond elements 24 are defined by at least a portion of the end 30 of the bond elements 24, desirably by the end surface 34 thereof, and are uncovered by the encapsulation elements 40, for example, at the surface 42.

[0053] In a particular embodiment, the substrates of numerous structures are provided as a continuous or semi-continuous element such as a strip, tape or sheet, although in FIGs. 1-2 there are no visible borders between the individual substrates. After the encapsulation elements 40 are formed on the substrates, the structures 10 are then severed along lines of separation 62 (see FIG. 2 which does not show visible borders between the individual substrates) to yield the individual structure 10 having the configuration illustrated in FIG. 3, and where the substrate 12 of the structure 10 extends between opposing edges 64. FIGs. 1-2 depict only a portion of a substrate sheet suitable for making a plurality of structures that may accommodate a microelectronic element over a defined portion of the substrate thereof, as described in detail below.

[0054] Referring to FIG. 3, the encapsulation elements 40A and 40B may define first edge surfaces 44A and 44B, respectively, extending downwardly from a top border 56 adjacent the top surface 42 to a bottom border 58 adjacent

the substrate 12 and disposed inside the edges 64 of the substrate 12. Further referring to FIG. 7A, bottom border 58 is disposed within a horizontal area 66 bounded by the edges 64 of the substrate. In one embodiment, the first edge surfaces 44A and 44B extend orthogonally from the surface 42 of the elements 40A, 40B, respectively, and the surface 14, and the surfaces 42 and 14 extend parallel to each other, such that the borders 56, 58 are aligned in a thickness direction of the structure 10.

[0055] In another embodiment, one or both of the first edge surfaces 44A and 44B may slope away from the top surface 42 in a horizontal direction toward the other element 40A or 40B opposite thereto, at an incline of less than 90 degrees with respect to the top surface 42, so that the bottom border 58 of the first edge surface 44 is further from the top surface 42 than the top border 56 in the horizontal direction toward the opposite element 40, similarly as described in U.S. Application No. 13/674,280 filed November 12, 2012, incorporated by reference herein.

[0056] In one embodiment, referring to FIG. 7A, the first edge surfaces 44 may be shaped such that any straight line extending along the first edge surface 44 at a constant vertical distance from the substrate 12 is disposed at a constant location in a first horizontal direction H_1. For example, an imaginary line 68 (FIG. 7A) extending at a constant vertical distance from the substrate would also lie at a constant horizontal location. In some embodiments, the first edge surfaces 44 may be substantially planar.

[0057] The elements 40A and 40B further may include second edge surfaces 46A and 46B, respectively, extending downwardly from the top surface 42 toward the substrate. The surfaces 46A, 46B, similar to the surfaces 44, may extend orthogonally from the surfaces 42 and 14, or alternatively

may slope away from the surface 42 in horizontal directions H_2 and H_1, respectively. Similar to the edge surfaces 44, the edge surfaces 46 may be shaped such that any straight line extending along the surfaces 46 at a constant vertical distance from the substrate 12 is disposed at a constant location in the horizontal directions H_2 and H_1, respectively, similarly as described above for the edge surfaces 44.

[0058] The encapsulation elements 40 may have a thickness (h) of at least about 150 micrometers extending away from the surface 14 in a direction orthogonal to the horizontal directions H_2 and H_1. The encapsulation elements 40 may also cover some conductive elements 18 within the region 50, including pads 26 thereof, that are not otherwise covered by bond elements 24.

[0059] The encapsulation elements 40 may at least partially, and desirably substantially, encapsulate the wire bonds 24 joined with the conductive elements 26 within the region 50, including the bases 28 and at least a portion of the edge surfaces 32 of the bond elements. A portion of the wire bonds 24 may remain uncovered by the encapsulation element, which may also be referred to as unencapsulated, thereby making the wire bond 24 available for electrical connection to a feature or element located outside of encapsulation element 40. In an embodiment, end surfaces 34 of wire bonds 24 remain uncovered by the encapsulation element 40 at the surface 42 of the encapsulation element 42. Other embodiments are possible in which a portion of edge surface 32 is uncovered by encapsulation element 40 in addition to or as an alternative to having end surface 34 remain uncovered by encapsulation layer 40. In other words, encapsulation element 40 may cover all portions of components overlying the portion 50 of the first surface 14, with the exception of a portion of the wire bonds 24, such as at least

the end surfaces 34, and optionally portions of the edge surfaces 32 or combinations of the two. In the embodiments shown in the drawings, the surface 42 of the encapsulation layer 40 may be spaced apart from first surface 14 of substrate 12 at a distance great enough to cover all but a portion of the bond element 24 at the end 30. Referring to FIG. 3, embodiments of the structure 10 may have end surfaces 30 of the wire bonds 24 other than flush with the surface 42, such as wire bonds 24 having ends that project from the surface 42 and terminate at end surfaces 34 that are at a same distance from the surface 42.

[0060] Alternatively, an embodiment of the disclosure may include a structure 10-1 as shown in FIG. 4A, which includes components similar to those of the structure 10 described above. Referring to FIG. 4A, the structure 10-1 may include encapsulation elements 40A' and 40B' each having a top surface 42 that is substantially planar and parallel to planar surface 14 of the substrate 12. The elements 40A' and 40B' may encapsulate wire bonds 24' and 24'' having end surfaces 34' and 34'', respectively, at different distances from the surface 42, and define unencapsulated portions 52' and 52'' including the end surfaces 34' and 34'' and portions of edges surfaces 32' and 32'', respectively. In some embodiments, the end surface 34 of the bond element 24 may be planar and an edge surface 32 thereof may be planar and extend perpendicular to the end surface 34.

[0061] The configuration of the bond elements 24 having the unencapsulated portions 52, such as shown in FIGs. 3 and 4A, may provide for a connection, such as by a solder ball 170 or the like as shown in FIG. 4B, to another conductive element by allowing the solder to wick along edge surfaces 32 and join thereto in addition to joining to end surfaces 34.

The solder ball 170 also may extend onto uncovered portions of the surface 42 from the edge surfaces 32.

[0062] Other configurations for bond elements 24 encapsulated by encapsulation elements 40 of a structure according to the disclosure also are possible. For example, FIG. 4C shows an embodiment of a structure 10-2 having a wire bond 24-1 encapsulated by an encapsulation element 140A with an end 30-1 thereof that is not positioned directly above base 28-1 thereof. That is, considering the first surface 14 of the substrate 12 as extending in two lateral directions, so as to substantially define a plane (see FIG. 7A), an end 30-1 of a wire bond 24-1 extending through the encapsulation element 140A may be displaced in at least one of these lateral directions from a corresponding lateral position of base 28-1. As shown in FIG. 4C, the wire bond 24-1 may be substantially straight along the longitudinal axis thereof, as in the embodiment of FIGs. 3 and 4A, with the longitudinal axis being angled at an angle 116 with respect to the first surface 14 of the substrate 12. Although the cross-sectional view of FIG. 4C only shows the angle 116 through a first plane perpendicular to the first surface 14, the wire bond 24-1 may also be angled with respect to the first surface 14 in another plane perpendicular to both that first plane and to the first surface 14. Such an angle may be substantially equal to or different than angle 116. That is the displacement of end 30-1 relative to base 28-1 may be in two lateral directions and may be by the same or a different distance in each of those directions.

[0063] In an embodiment, various ones of wire bonds 24-1 and 24-2 encapsulated by the element 140A may be displaced in different directions and by different amounts along the first surface 14 and within the encapsulation element 140A. Such an arrangement allows the structure 10-2 to have an array

that is configured differently at the level of the surface 142 of the element 140A compared to at the level of substrate 12. For example, an array may cover a smaller or larger overall area or have a smaller or larger pitch at the surface 142 level compared to that at the first surface 14 of the substrate 12. Further, some wire bonds 24-1 may have ends 30-1 positioned above the substrate 12 to accommodate a stacked arrangement of packaged microelectronic elements of different sizes. In another example, the wire bonds 24-1 may be configured such that the end 30-1 of one wire bond 24-1 is positioned substantially above the base 28-1 of another wire bond 24-1, and the end 30-1 of the another wire bond 24-1 is positioned elsewhere. Such an arrangement may be referred to as changing the relative position of a contact end surface 34 within an array of contacts, compared to the position of a corresponding contact array on another surface, such as the surface 14. Within such an array, the relative positions of the contact end surfaces may be changed or varied, as desired, depending on application of a microelectronic assembly formed from the structure 10-2 or other requirements.

[0064] In a further example as shown in FIG. 4C, wire bonds 24-1 encapsulated by the element 140A may be arranged such that the bases 28-1 are arranged in a first pattern having a pitch thereof. The wire bonds 24-1 may be configured such that the unencapsulated portions 52 thereof, which include end surfaces 30-1, may be disposed in a pattern at positions at the surface 142 of the encapsulation element 140A which have a minimum pitch that is greater than a minimum pitch between the respective adjacent bases 28-1 of the wire bonds 24-1 attached to conductive pads 26 within the region 50. Accordingly, the minimum pitch between adjacent wire bonds at the surface 142 may be greater than the

corresponding minimum pitch between the conductive pads 26 of the substrate to which the wire bonds are attached. To achieve this, the wire bonds may be angled or curved as shown, for example, in FIG. 4C, such that the ends 30 are displaced in one or more lateral directions from the bases 28, as discussed above. In one embodiment, the conductive elements 26 and the ends 30 may be arranged in respective rows or columns and the lateral displacement of end surfaces 34 in one row may be greater than in another row. To achieve this, the wire bonds 24 can, for example be at different angles 116 with respect to the surface 14 of the substrate 12.

[0065] FIG. 4C shows a further embodiment in which wire bonds 24-2 have ends 30-2 in displaced lateral positions with respect to the bases 24-2 thereof. In the embodiment of FIG. 4C, the wire bonds 24-2 achieve this lateral displacement by including a curved portion 118 therein. The curved portion 118 may be formed in an additional step during a wire bond formation process and may occur, for example, while the wire portion is being drawn out to the desired length. This step may be carried out using available wire-bonding equipment, which may include the use of a single machine.

[0066] The curved portions 118 may take on a variety of shapes, as needed, to achieve the desired position of the end 30-2 of the wire bond 24-2. For example, as shown in FIG. 4C, the curved portions 118 may be formed as S-curves of various shapes, such as included in wire bond 24-2(A), or of a smoother form as in wire bond 24-2(B). Additionally, the curved portion 118 may be positioned closer to base 28-2 than to end 30-2 or vice-versa. The curved portion 118 may also be in the form of a spiral or loop, or may be compound including curves in multiple directions or of different shapes or characters.

[0067] In one embodiment, the structure 10-2 may include encapsulation elements 140 each having a different type of bond elements 24 encapsulated therein. Referring to FIG. 4C, the element 140A may include wire bonds or wires as the bond elements 24, and encapsulation element 140B may include substantially vertical conductive features, such as micro-pillars or posts, as the bond elements 124.

[0068] It is to be understood that, as shown FIG. 4C, a structure may include any combination of bond elements having various shapes leading to various relative lateral displacements between bases and ends thereof. Some of the bond elements 24 are substantially straight with ends 30 positioned above their respective bases 28 as shown in FIG. 3 and FIG. 4A, while other bond elements 24 include a curved portion 118 leading to a somewhat slight relative lateral displacement between end 30 and base 28. Further, some bond elements 24 include curved portions 118 having a sweeping shape that result in ends 30 that are laterally displaced from the relative bases 28 at a greater distance than that of ends 28.

[0069] In such embodiments of the bond elements 24, wire bonds thereof may be configured to be uncovered by the encapsulation element at an end 30 and along at least a portion of the edge surface thereof extending away from the end surface 34. As shown in FIGs. 3 and 4A, 4C, free ends of the bond elements are uncovered, however, a portion of edge surface 32 may additionally or alternatively be uncovered by the encapsulation element. Such a configuration may be used for grounding of a microelectronic assembly including the structure by electrical connection to an appropriate feature or for mechanical or electrical connection to other features disposed laterally to the microelectronic assembly.

[0070] Additionally, referring to FIG. 4C, the encapsulation element 140B may encapsulate bond elements 124 that are in the form of posts or micro-pillars connected at bases 128 thereof with conductive elements 26 at the surface 14. The element 140B may be configured to include an area that has been etched away, molded, or otherwise formed to define a recessed surface 144 that is positioned closer to substrate 12 than the surface 142. One or more micro-pillars 124-1 may be uncovered within an area along the recessed surface 144. In the exemplary embodiment shown in FIG. 4C, end surface 134-1 and a portion of edge surface 132-1 of the micro-pillar 124-1 may be uncovered by encapsulation element 140B to form an unencapsulation portion 152 of the bond element 124-1.

[0071] In one embodiment, base 128-1 of a post 124-1 may be joined by a stud bump 165 with the conductive element 26 on the surface 14. The stud bump may consist essentially of one or more of copper, nickel, silver, platinum and gold ends 38 and provide a way of forming conductive interconnects when the post 124-1 is made from a non-wettable metal.

[0072] Similar to the bond elements 24, referring to FIG. 4D, such a configuration of the bond element 124 may provide a connection, such as by a solder ball 170 or the like, to another conductive element by allowing the solder to wick along edge surface 132-1 and join thereto in addition to joining to end surface 134-1, and where the solder may extend along the surface 144 from the edge surface 132-1. Other configurations by which a portion of the bond element 124 may be uncovered by encapsulation element 140B along recessed surface 144 are possible, including ones in which the end surfaces are substantially flush with recessed surface 144.

[0073] Referring again to FIG. 4C, the structure 10-2 may include a bond element 124-2 in the form of a micro-pillar

having a base 128-2 joined by the stud bump 165 to a conductive element 26, and an end surface 134-2 and an edge surface 132-2 extending from the end surface 134-2 defining an unencapsulated portion 152 of the wirebond 124-2 at the surface 142. In another embodiment, the structure 10-2 may include a bond element 124-3 in the form of a micro-pillar formed integrally with the conductive element 26 at the surface 14 and extending from the surface 14 to an end surface 134-3. The bond element 124-3 includes the end surface 134-3 and an edge surface 132-3 extending therefrom as an unencapsulated portion 152 at the surface 142.

[0074] In a further embodiment, the element 140B may be configured to include an area that has been etched away, molded, or otherwise formed to define a cavity 175 extending from the surface 142 to the surface 14 of the substrate. The cavity 175 may have any suitable shape to permit electrical connection at an end surface 134-4 of a bond element 124-4 that may be formed in the cavity 175, such as by deposition of electrically conductive material therein, where the bond element 124-4 has an end surface 134-4 as the unencapsulated portion 152. In one embodiment, the bond element 124-4 may be formed in a trapezoidally shaped cavity 175, with tapered side walls. The bond element 124-4 may have an end surface 134-4 wider in cross-section than a cross-section of a portion between the base 128-4 and end surface 134-4, where the base 128-4 and end surface 134-4 are parallel and edge surfaces 132-4 extend tapered toward each other from the base 128-4 to the end surface 134-4.

[0075] Referring FIG. 4D, solder 170 may be deposited in the cavity 175 to extend from the end surface 134-4 to above the surface 142 and along portions of the surface 142 extending away from the cavity 175.

[0076] It is to be understand that, in accordance with the disclosure, a structure may include other configurations by which a portion of a bond element is uncovered by an encapsulation element, such at an end surface and optionally along an edge surface thereof, which are similar to those discussed herein with respect to the variations of the configuration of the surface of the encapsulation element remote and facing away from the surface of the substrate.

[0077] Referring again to FIG. 3, for example, the encapsulation elements 40 serve to protect conductive elements 18 within the region 50, including the bond elements 24 connected with the pads 26 within the region 50. This allows for a more robust structure that is less likely to be damaged by testing thereof or during transportation or assembly to other microelectronic structures. Encapsulation element 40 may be formed from a dielectric material with insulating properties such as that described in U.S. Patent App. Pub. No. 2010/0232129, which is incorporated by reference herein in its entirety.

[0078] Referring to FIGs. 3 and 7A, an exemplary pattern for an array of contacts formed by end surfaces 34 of the bond elements 24 of the structure 10 is shown. Such an array may be formed in an area array configuration, variations of which could be implemented using the structures described herein. Such an array may be used to electrically and mechanically connect a microelectronic assembly including the structure 10 to another microelectronic structure, such as to a printed circuit board ("PCB"), or to other packaged microelectronic elements. In such a stacked arrangement, wire bonds 24 and conductive elements 18 and 20 may carry multiple electronic signals therethrough, each having a different signal potential to allow for different signals to be processed by different microelectronic elements in a

single stack. Solder masses may be used to interconnect the microelectronic assemblies in such a stack, such as by electronically and mechanically attaching end surfaces 34 to conductive elements of an external component.

[0079] Referring to FIGs. 3 and 7A, the surfaces 14 and 16 of the substrate 14 of the structure 10 extend in horizontal directions H_1 and H_2 and the edges 64 of the structure 90 extend between the upper and lower surfaces. The encapsulation elements 40A and 40B may define a microelectronic element receiving region 210 of predetermined size and predetermined shape to accommodate a microelectronic element, such as a semiconductor chip alone, a microelectronic assembly or a microelectronic package containing at least one chip, disposed laterally from the elements 40A and 40B and connected to the substrate 12 at a portion of the surface 14 that a bottom portion 212 of the region 210 overlies. For example, referring to FIG. 7A, the bottom portion 212 may have a linear dimension R1 extending in the horizontal direction H_1 from the bottom border 58 of the element 40A to the bottom border 58 of the element 40B, and a linear dimension R2 extending in a horizontal direction orthogonal to the direction H_1 between opposing ends 205 of the elements 40 extending in a direction parallel to the horizontal direction H_1. The region 210 includes a space that extends, at the bottom portion 212, upwardly from exposed portions of the surface 14 and conductive elements 18 at the surface face 14, to a predetermined vertical distance from the surface 14 of the substrate, which may be a height above, the same or below the height of the surface 42 of one or both of the elements 40 as measured vertically from the surface 14. The region 210, thus, includes a space defined between the surfaces 44A, 44B of the encapsulation elements 40A, 40B, respectively. The region 210 is of a predetermined size and

shape that is based on size, shape and positioning of the encapsulation elements 40 on the surface 14 of the substrate, and provides that a portion of a microelectronic element by itself, or within a package or assembly, to be connected to a portion of the substrate that the portion 212 overlies may be disposed in the region 210 without the element, package or assembly contacting the surfaces 42A and 42B.

[0080] A process according to a further embodiment of the invention for manufacture of the structure 10 may use a pre-formed dielectric mass, such as a substrate consisting essentially of dielectric material, and use a mold element (not shown) to form a dielectric mass of the encapsulation element 40 that encapsulates the bond elements 24. In this process, the bond elements connected with pads 26 at the surface 14 of substrate 12 may be present at the time of molding. In one embodiment, the dielectric mass forming the element 40 may be molded over the bond elements 24, which are connected to traces 18 on the surface 14 of the substrate 12.

[0081] In addition, a pre-formed dielectric mass serving as the encapsulation element encapsulating the bond elements to define unencapsulated portions, and having a top surface 42 and edge surfaces 44 and 46, as described above and shown in FIG. 3, may be attached to the portion 50 of the surface 14 of the substrate 12, laterally spaced from another similar encapsulation element, using an adhesive, such as curable adhesive or epoxy.

[0082] In a further step of manufacture of the structure 10 before the encapsulation elements are formed on the substrate 12, traces and pads as the conductive elements 18 may be patterned onto the surface 14. For example, the entire surface 14 may be plated, masked and selectively etched to form the traces. Alternatively, the surface 14 may be covered with a mask material, and then selectively exposed

to laser radiation to cut grooves through the mask. A seed layer may be applied over the mask and into the grooves, whereupon the mask is removed so as to lift off the seed layer everywhere except at the grooves. The surface is then exposed to a plating bath, so that metal is deposited only at the grooves where the seed is present. Any other technique for forming metallic features on a dielectric body may be used.

[0083] In other embodiments, flowable dielectric material used to form the encapsulation element 40 may serve as an adhesive which bonds the encapsulation element to the substrate 12.

[0084] Referring to FIGs. 7B, 7C and 7E, alternative arrangements of encapsulation elements on a substrate, which encapsulate bond elements connected with the substrate, may be used to obtain a microelectronic element receiving region, in accordance with embodiments of the disclosure. For example, one or more encapsulation elements 300 may be formed on an upper surface 304 of a substrate 312, such as similar to the substrate 12, to have a size, shape and arrangement on the upper surface 304, such as relative to one another, to define a microelectronic element receiving region 302 of size and shape that may accommodate a microelectronic element, package or assembly, similarly as described above for the region 210. Referring to FIG. 7B, four encapsulation elements 300 may be arranged to define the region 302 overlying the upper surface 304 of the substrate 312 and having a bottom portion 306 having horizontally extending dimensions R3 and R4, where R4 is aligned in a thickness direction of the structure with the upper and lower borders of the elements 300A and 300B at the facing edge surfaces thereof, respectively, and R3 is aligned in the thickness direction of the structure with the upper and lower borders

of elements 300C and 300D at the facing edge surfaces thereof, respectively. Referring to FIG. 7C, the encapsulation element 300 may be a single element that defines a region 302 having a rectangularly-shaped bottom portion 306, three sides of which are defined by the single element. Referring to FIG. 7E, a single encapsulation element 450 may be arranged overlying upper surface 454 of substrate 456 to define a microelectronic element receiving region 452 having a bottom portion 456 overlying a portion 454A of the surface 454. The element 450 overlies a portion 454B of the surface 454, and the portion 454B completely encloses the portion 454A. The element 450, as such, completely encloses the receiving region 452, at least at a portion of the region 452 that extends vertically away from the portion 454A.

[0085] Referring to FIGs. 5 and 7D, in one embodiment a structure 400, having components similar to those of the structure 10, may include a single encapsulation element 440, or multiple encapsulation sub-elements 440A, 440B and 440C, that encapsulate bond elements 424 to provide, at surfaces 442 of sub-elements 440 facing away from the substrate, unencapsulated portions 452 defined by at least end surfaces 434 of the bond elements 424. For example, referring to FIG. 7D, a single element 440 may define a plurality of microelectronic receiving regions 402A, 402B overlying upper surface 414 of the substrate and having bottom portions 406A, 406B, respectively. Alternatively, the sub-elements 440A, 440B and 440C (indicated in FIG. 7D by portions of the element 440 that do not have cross-hatching) may be arranged in parallel and spaced from each other, similarly as the elements 40A and 40B in FIG. 3 and 4A, to define the regions 402A and 402B.

[0086] Referring to FIG. 6, in one embodiment a structure 500, having a construction similar to the structure 10, may include the encapsulation elements 40A, 40B on the surface 14 of the substrate 12 to define the region 210. In addition, an encapsulation element 540 may overlie a portion 560 of the surface 16 and encapsulate bond elements 524 joined to pads 522 within the portion 560, while providing for unencapsulated portions 550 defined by end surfaces 534 and portions of edge surfaces 532. In one embodiment, the encapsulation element 540 may at least partially overlie a portion of the surface 14 that the portion 212 overlies. In some embodiments, the encapsulation element 540 may overlie the surface 16 to define at least one microelectronic element receiving region 570 having a bottom portion 572 overlying a portion 574 of the surface 16 extending from the portion 560 to an opposing edge 64 of the substrate 12.

[0087] Referring to FIGs. 14 and 15, in another embodiment of the present disclosure a structure 1010 may include an active die 1012, such as a field programmable gate array, which is provided at the wafer level. The die 1012 may have an active surface 1014 including electrical circuitry 1016 and bond pads 1018. The die 1012 is typically silicon of thickness 730 micrometers, and the electrical circuitry 1016 may be provided by any suitable conventional technique. Alternatively, the die 1012 may be any other suitable material, such as, for example, gallium arsenide and may be of any suitable thickness. A redistribution layer 1020 of dielectric material may extend along the surface 1014. Traces 1022 may be electrically connected to contact pads 1024 at surface 1017 of the layer 1020, the surface 1017 being remote from the surface 1014, and extend through substrate 1026 of the redistribution layer 1020 to the pads 1018 at the surface 1014. Similar to the structure 10 as

shown in FIG. 2, bond elements 24 may be joined at bases thereof with at least some of the pads 1024, which are joined through traces 1022 with pads 1018 at a portion 1050 of the surface 1014. In another embodiment where the redistribution layer 1020 is omitted from the structure, the bases 28 of the bond elements 24 may be joined by solder elements (not shown) with the pads 1018 at the portion 1050.

[0088] Referring to FIG. 15, the structure 1010 may further include encapsulation elements 1040A and 1040B, having features similar to the encapsulation elements 40 in the assembly 10 as described above, formed from a dielectric material over the portion 1050 of the surface 1014 of the substrate 12, and defining a top surface 1042 remote and facing away from the die 1012. The material of the element 1040 fills spaces between the bond elements 24, and unencapsulated portions 52 are defined by at least a portion of the ends 30 of the bond elements 24. In addition, the encapsulation elements 1040A and 1040B may define first edge surfaces 1044A and 1044B, respectively, extending downwardly adjacent the top surface 1042 to the surface 1017 of the redistribution layer 1020, or to the surface 1014 if the layer 1020 is omitted, where the surfaces 1044 are disposed inside peripheral edges 1064 of the die 1012. The elements 1040A and 1040B further may include second edge surfaces 1046A and 1046B, respectively, extending downwardly from the top surface 1042 to the surface 1017 of the layer 1020 or the surface 1014 of the die 1012, similarly as described above for the surfaces 46 of the elements 40 extending to the substrate 12. The encapsulation elements 1040 may be configured similarly as the encapsulation elements 40’ and 140, as shown in FIGs. 4A and 4B, to encapsulate bond elements 24 and uncover unencapsulated portions 52 thereof.

[0089] In some embodiment, the dies of numerous structures are provided as a continuous or semi-continuous element such as a strip, tape or sheet. After the encapsulation elements 1040 are formed on the dies, the structures 1010 are then severed along lines of separation to yield the individual structure 1010 having the configuration illustrated in FIG. 15, and where the die 1012 of the structure 1010 extends between opposing edges 1064.

[0090] Alternatively, an embodiment of the disclosure may include a structure 1010-1, as shown in FIG. 16A, which includes components similar to those of the structure 1010 described above. Referring to FIG. 16A, the structure 1010-1 may include wire bonds 24-1, some of which may include curved or substantially straight portions similar to those shown in FIG. 4C, encapsulated by an encapsulation element 1040A with respective ends 30-1 thereof that are not positioned directly above bases 28-1 thereof, such that the structure 1010-1 may have an array that is configured differently at a level of the element 1040A, which is remote from the die 1012 compared to at the level of the die 1012 or the redistribution layer 1020. The element 1040A may be configured to include an area that has been etched away, molded, or otherwise formed to define a cavity 1070 extending from a surface 1042 of the element 1040A, which is remote from the die 1012, to a recessed surface 1044 that is positioned closer to the die 1012 than the surface 1042. The bond elements 24-1 may be uncovered in the cavity 1070 within an area along the recessed surface 1044. The cavity 1070 may have any suitable shape to permit electrical connection of the unencapsulated portion 52 at end 30-1 of a bond element 24-1 that is disposed in the cavity 1070. In one embodiment, the unencapsulated portion 52 of the bond element 24-1 may overlie the surface 1044, and be between tapered side walls

1045 of the encapsulation element 1040A extending from the surface 1042 to the surface 1044 that define the cavity 1070.

[0091] Additionally, the encapsulation element 1040B may encapsulate bond elements 1124 configured similar to the bond elements 124 as shown in FIG. 4C, and connected at bases 1128 thereof with pads at the surface 1017 of the redistribution layer 1020 or at the surface 1014 of the die 1012. In the exemplary embodiment shown in FIG. 16A, a bond element 1124 may be uncovered by encapsulation element 1040B to form an unencapsulation portion 1152 defined by an end surface 1134 and a portion of edge surface 1132 of the bond element within a cavity 1070 of the encapsulation element 1040B. In one embodiment, base 1128 of a post 1124 may be joined by a stud bump 1165 with a pad at the surface 1017 or 1014. Further, a cavity 1075, having a configuration similar to the cavity 175 as shown in FIG. 4C, may be formed in the encapsulation element 1040B and extend from the surface 1042 to the surface 1017, or the surface 1014 if the layer 1020 is omitted. A bond element 1124A, similar to the bond elements 124-2, 124-3 or 124-4, may extend from an end surface 1130A disposed within the cavity 1175, through the cavity 1175 to a base thereof joined with a pad of the die 1012 or layer 1020, where an unencapsulated portion 1152A of the bond element 1124A is defined by the end surface 1130A and an edge surface 1132A extending from the end surface 1130A.

[0092] Referring to FIG. 16B, the bond elements 1124 may provide a connection, such as by a solder element 1170 or the like, to another conductive element by allowing to fill the cavities 1070 or the portions of the cavities 1175 not occupied by the bond elements 1124, so as to encapsulate the unencapsulated portions 52 and 1152 of the bond elements 24-1 and 1124, respectively. In some embodiments, the material forming the solder elements 1170 may be formed on portions of

the surface 1042 extending from the cavities 1070 and 1175. In another embodiment, a surface 1172 of the solder element 1170, remote from the die 1012, may be in a same plane as planar surface 1042 of the encapsulation element 1040.

[0093] In another embodiment, a structure 1010-2 (see FIG. 16C) may have components and a configuration similar to the structure 1010-1, except for the following differences. The bond elements 24-1 may be encapsulated by the encapsulation element 1040A such that only the end surfaces 34-1 of the elements 24-1 define the unencapsulated portions 52 thereof, and the end surfaces 34-1 are flush with the surfaces 1044. In addition, the bond elements 1124 having the unencapsulated portions 1152 may be encapsulated by the encapsulation element 1040B such that only the end surfaces 1134 of the elements 1124 define the unencapsulated portions 1152, and the end surfaces 1134 are flush with the surfaces 1044. Further, the bond elements 1124A may be encapsulated by the encapsulation element 1040B such that only the end surfaces 1134A thereof define the unencapsulated portions 1152A, and the end surfaces 1134A are flush with the surfaces 1044. Referring to FIG. 16D, and similarly as described with reference to FIG. 16C, solder elements 1170 may fill the cavities 1070 or the portions of the cavities 1175 not occupied by the bond elements 1124, so as to encapsulate the unencapsulated portions 52 and 1152 of the bond elements 24-1 and 1124, respectively.

[0094] In some embodiments, the encapsulation elements overlying the substrate 112, such as in the structures 10 as described above (see FIGs. 3 and 4A-4D), may be configured to encapsulate bond elements and uncover unencapsulated portions 52 similarly as the encapsulation elements overlying the die 1012 in the embodiments of the structures 1010 as shown in FIGs. 16A-16D.

[0095] Referring to FIGs. 15 and 7E, similarly as described above for the structure 10, the encapsulation elements 1040A and 1040B may define a microelectronic element receiving region 1210 of predetermined size and predetermined shape to accommodate a microelectronic element, such as a semiconductor chip alone, a microelectronic assembly or a microelectronic package containing at least one chip, disposed laterally from the elements 1040A and 1040B and electrically connected with pads of the die 1012 at a portion of the surface 1014 that a bottom portion 1212 of the region 1210 overlies. For example, referring to FIG. 7E, the encapsulation elements 1040A and 1040B may be in the form of a single, integral encapsulation element 1040, having a configuration similar to the element 450, that overlies an area of the die 1012 that completely encloses an area 1014A or 1017A of the surfaces 1014 or 1017, so to define the region 1210. The region 1201 may have a configuration similar to the region 452 and include a portion 1212, similar to the bottom portion 456, adjacent the die 1012. The region 1210 is of a predetermined size and shape that is based on size, shape and positioning of the encapsulation elements 1040 over the surface 1014 of the die 1012, and provides that a portion of a microelectronic element by itself, or within a package or assembly, to be connected to a portion of the die that the portion 1212 overlies may be disposed in the region 1210 without the element, package or assembly contacting the surfaces 1042A and 1042B.

[0096] Referring to FIG. 8, a package assembly 600 may include a structure of the present disclosure connected to a microelectronic element, package or assembly at the microelectronic element region of the structure. The package assembly 600, for example, may include the structure 10 as described above, connected to a microelectronic element 602.

The microelectronic element or chip 602 may include oppositely facing surfaces 605, 607, and be positioned in a "face-down" orientation relative to the substrate 12 in the region 212, with the surface 605 facing the surface 14 of the substrate 12. Contacts 604 at the surface 605 may be bonded by solder elements 609 to conductive elements 618 at the surface 14. The bottom portion 212 of the region 210 overlies the conductive elements 618. The contacts 604 may be electrically connected with terminals 31 from which traces 33 extend on the surface 16 of the substrate 12, and the bond elements 24 within the elements 40A and 40B, through electrical circuitry, such the traces 19 within or the conductive vias 22 extending through, the substrate 12. The assembly 600 may be joined to an external component 690, such as a printed circuit board, by electrically connecting solder elements 625, such as solder balls, formed at the terminals 31 to contacts (not shown) on a facing surface 692 of the component 690 arranged in a pattern corresponding to that of the terminals 31 of the structure 10.

[0097] In one embodiment, the region 210 may be adapted such that, when the microelectronic element 602 is bonded to the substrate 12, opposing edge surfaces 613A and 613B of the microelectronic element 602 that face the edge surfaces 44A and 44B, respectively, are spaced a distance of at least about 200 microns from the edge surfaces 44A, 44B. In some embodiment, the distance of the spacing may permit that dielectric material, for example, underfill, may be provided between the facing surfaces 613A and 44A and the facing surfaces 613B and 44B. In another embodiment, the distance of the spacing may permit molding of dielectric material over the top surface 607 of the microelectronic element 602, which extends between the surfaces 613A and 613B, and the surfaces 613A and 613B.

[0098] A dielectric mass or overmold 626 is formed over the bottom portion 212 of the region 210, such as using any of the techniques described to form the dielectric masses of the encapsulation elements over the substrate 12 discussed above. The dielectric mass 626 has a top surface 628 remote from the surface 14 that extends over the microelectronic element 602 and away from the element 602 over the surface 14 in the horizontal directions H_1 and H_2 toward the edge surfaces 44A and 44B of the encapsulation elements 40A and 40B, respectively. In one embodiment, the top surface 628 extends to the edge surfaces 44A and 44B, and edges surfaces 628A and 628B extend downwardly thereform to the substrate 12 facing, and in some embodiments along and contacting at least portions of, portions of the edge surfaces 44A and 44B, respectively. As such, the dielectric mass 626 may be made from a first dielectric material, and the encapsulation elements 40 may be made from a second dielectric material that is different from the first dielectric material. In some embodiments, the dielectric mass 626 may be provided such that the top surface 628 thereof extends over a portion of the surface 42 of an encapsulation element 40. The dielectric mass 626 further includes a bottom surface 630 extending from the edges surfaces 628A and 628B in horizontal directions H_1 and H_2 away from the encapsulation elements 40A and 40B and along exposed portions of the surface 14 and traces 618 on the surface 14.

[0099] In one embodiment, a thickness (h) of the encapsulation elements 40, in a thickness direction T of the assembly 600 orthogonal to H_1 and H_2, extends upwardly away from the surface 14, and is the same as, greater than, or less than a thickness of the microelectronic element 602 in the direction T. In another embodiment, the thickness (h) of at least one of the elements 40 is less than or equal to the

thickness in the direction T of the dielectric mass 626 with the microelectronic element 602 encapsulated therein.

[0100] The assembly 600 may be joined with a microelectronic package 2200 that overlies the surface 14 of the substrate 12. The package 2200 may include a substrate 2206 having a first surface 2208 remote from a second surface 2210, where the first surface 2208 faces the surface 42 of the encapsulation elements 40 and the surface 628 of the mass 626. Conductive elements 2212 may extend along the surfaces 2208 and 2210. In addition, a microelectronic element 2214 is positioned in a "face down" orientation facing the surface 2210, and contacts (not shown) of the microelectronic element 2214 are bonded to the conductive elements 2212 on the surface 2210 by solder elements (not shown). Further, the conductive elements 2212 on the surface 2208 may be arranged in a pattern corresponding to the pattern of the unencapsulated portions 52 of the bond elements 24, and solder elements 2215 may electrically connect such elements 2212 with the unencapsulated portions 52. A dielectric mass 2220 may be formed over the microelectronic element 2214 and uncovered portions of the surface 2210 to encapsulate the element 2202 and the surface 2210 of the substrate 2206, such as using any of the techniques described to form a dielectric mass. A surface 2222 of the mass 2220, remote from the substrate 2206, overlies the microelectronic element 2214 and portions of the surface 2210 adjacent the element 2214. As such, the bond elements 24 may electrically interconnect conductive elements of the package 2200 with conductive elements of the assembly 600 and conductive elements of the external component 690.

[0101] In another embodiment, referring to FIG. 9, a package assembly 600’ may have a similar construction as the assembly 600 shown in FIG. 8, except that end surfaces 34 of

the bond elements 24 are flush with the surface 42, the chip 602 is joined by wire leads 622 to traces 618 on the substrate and the assembly 600' further includes a redistribution layer 654. For example, the surface 607 of the chip 602 may be attached by an adhesive layer 611 with a portion of the layer 14 that the portion 212 overlies, and the wire leads 622 may extend from the contacts 604, over the surface 607 and an edge surface 613 of the chip 602, to the traces 618. Further, the layer 654 may be formed of dielectric material and extend along a portion of the surface 42 of at least one of the encapsulation elements 40, or a portion of the surface 628 of the mass 626. In one embodiment, the redistribution layer 654 may overlie only the portion 50 of the structure 10. In an alternative embodiment, the portion 212 may overlie a portion of the redistribution layer 654. Traces 658 may be electrically connected to inner contact pads 661 which are electrically connected to the end surfaces 34 of bond elements 24 and extend through substrate 656 of the redistribution layer 654 to contact pads 660 at surface 662 of the substrate 656. Another microelectronic assembly may then be connected to the contact pads 660 by solder masses or the like. The redistribution layer 654, in effect, serves as what is known as a fan-out layer that may allow the assembly 600' to connect to an array of a different configuration than the conductive element 26 array within the portion 50 would otherwise permit.

[0102] In a further embodiment, the assembly 600' may be joined with a microelectronic package, such as the package 2200 as described above (see FIG. 8), that overlies the redistribution layer 654. The surface 2208 of the package 2202 may face the surface 662 of the layer 654, and the conductive elements 2212 of the package 220 at the surface

2208 may be arranged in a pattern corresponding to the pattern of the contact pads 660 at the surface 662 of the layer 654. Solder elements 2215 may electrically connect such elements 2212 with the contact pads 660. As such, the conductive elements of the package 2200 may be electrically connected, through conductive elements of the redistribution layer and the bond elements 24, with conductive elements of the assembly 600' and conductive elements of the external component 690.

[0103] It is to be understood that, in accordance with the disclosure, a microelectronic element or a microelectronic package may be mounted "face-up" or "face-down" and coupled to a surface, such as a surface (e.g., 14, 16) of a substrate of a structure according to the disclosure or a surface (e.g., 692) of an external component joined with a package assembly including such structure, by wire bond, ball bond or other known connection technique.

[0104] In another embodiment, referring to FIG. 10A, a package assembly 700 may include a structure, according to the disclosure, joined with a plurality of microelectronic elements, where some of the microelectronic elements may be part of microelectronic packages. Referring to FIG. 10A, the assembly 700 may include the structure 10 as described above, and a microelectronic element 702 with its contacts 703 facing the surface 16 and electrically connected to pads 25 of the conductive elements 20 at the surface 16. A dielectric mass 704 is formed over the microelectronic element 702 and the surface 16, and has a surface 706 overlying the element 702 and the surface 16. The mass 704 covers the microelectronic element 702 and the surface 16, similarly as described above for the dielectric mass 626 formed over the element 602 and the surface 14 as in FIG. 8.

[0105] In addition, the package assembly 700 may include a microelectronic element 732 connected with conductive elements at the surface 14. The microelectronic element 732, similar to the microelectronic element 602, may be positioned in a "face-down" orientation relative to the surface 14 of the substrate 12 in the region 710, with the surface 735 facing the surface 14 of the substrate 12. Contacts 736 at the surface 735 may be bonded by solder elements to conductive elements 738 at the surface 14. The bottom portion 712 of the region 710 overlies the conductive elements 738. The contacts 736 may be electrically connected with other conductive components or elements electrically connected with the contacts 736 through electrical interconnections within the substrate 12, and also the bond elements 24 encapsulated within the elements 40A and 40B.

[0106] In addition, a mass of dielectric material 748 may be formed over the portion 712 of the region 710, similarly as discussed above for the overmold 628. The dielectric mass 748 has a surface 750 remote from the surface 14 that extends over the microelectronic element 732 and away from the element 732 over the surface 14 in the horizontal directions H_1 and H_2 toward the edge surfaces 44A and 44B of the encapsulation elements 40A and 40B, respectively. In one embodiment, the surface 750 may be spaced from the edge surfaces 44A and 44B, and the mass 748 includes edge surfaces 752A and 752B extending downwardly therefrom to the substrate 12 facing and spaced from the edge surfaces 44A and 44B, respectively. In another embodiment, one of the edge surfaces 752, such as the edge surface 752A, may at least partially contact a portion of the edge surface 44A. The dielectric mass 748 may be made from a first dielectric material, and the encapsulation elements 40 may be made from a second dielectric material that is different from the first

dielectric material. The dielectric mass 748 further includes a bottom surface 754 extending along exposed portions of the surface 14 and traces 738 at the surface 14 in horizontal directions H_1 and H_2 and spaced from the elements 40A and 40B.

[0107] Referring to FIG. 11, which is a plan view of the embodiment of the assembly 700 viewed in the direction of the surface 14, the mass 748, having the microelectronic element 732 encapsulated therein to form encapsulated microelectronic unit 755, extends a predetermined length L1 less than R1 in the horizontal direction H_1 and a predetermined length W1 less than R2 in the direction orthogonal to the horizontal directions H_1 and H_2 and parallel to the surface 14. In addition, referring to FIG. 10A, the mass 748 has a thickness in the direction T of not more than a predetermined thickness H2, which is a distance in the thickness direction T from the surface 14 to a facing surface 792 of an external component 790 to which the bond elements 24 are electrically interconnected at the end surfaces 34 by solder elements 794, less an expected thickness of the solder element 794. For example, the mass 748, at the surface 754, may extend over a horizontal area having maximum dimensions of W1 and L1, have a predetermined shape in the thickness direction T and have a thickness extending from the surface 14 to the surface 750 at most equal to H3, such that the end surfaces 34 at the surfaces 42 of the elements 40 may be aligned in the thickness direction of the assembly 700 with pads (not shown) on the surface 792 of the external component 790 and the mass 750 is within the region 710 without contacting the elements 40, the component 790 or other components within the region 710.

[0108] In some embodiments, the assembly 700 including the microelectronic unit 755 as shown in FIG. 10A may also be

connected to a microelectronic package 800 arranged within the region 710 and connected to terminals 27 of conductive elements 18 that the portion 712 overlies. The package 800 may include a substrate 806 having a first surface 808 remote from a second surface 810, where the first surface 808 faces the surface 14, and conductive elements 812 extending along the surfaces 808 and 810. In addition, a microelectronic element 814 is positioned in a "face-down" orientation facing the surface 810, and contacts (not shown) of the microelectronic element 814 are bonded to the conductive elements 812 on the surface 810 by solder elements (not shown). Further, the conductive elements 812 on the surface 808 are electrically connected by solder elements 815 to the terminals 27 at the surface 14. A dielectric mass 820 is formed over the microelectronic element 814 and a portion of the surface 810 of the substrate 806 and opposing edges 819 extending between the surfaces 808 and 810 to encapsulate the element 802 and a portion of the substrate 806, such as using any of the techniques described to form a dielectric mass. A surface 822 of the mass 820, remote from the substrate 806, overlies the microelectronic element 814 and portions of the surface 810 adjacent the element 814.

[0109] Further referring to FIG. 11, the package 800 has a predetermined size and configuration and is arranged at a predetermined position over the surface 14 spaced in the direction H1 from the microelectronic unit 755, and spaced in the direction H2 from the element 40B, so not to contact the elements 40 and the unit 755. Similar to the unit 755, the package 800 may be positioned over the surface 14 with pads (not shown) at the surface 808 aligned in the thickness direction T with corresponding ones of terminals 27 at the surface 14 and so that the portion 712 overlies the package 800. The package 800 extends a predetermined length L2 less

than R1 in the horizontal direction H_1 and a predetermined length W2 less than R2 in the direction orthogonal to the horizontal directions H_1 and H_2 and parallel to the surface 14.

[0110] Further, in some embodiments, a microelectronic package 800' may be arranged within the region 710 and spaced from the other components within the region 710. For example, referring to FIGs. 10 and 11, the package 800', which may have the same or similar construction and components as the package 800, may be arranged between and spaced from the element 40B and the package 800, and extend a predetermined length L3 less than R1 in the horizontal direction H_1 and a predetermined length W3 less than R2 in the direction orthogonal to the horizontal directions H_1 and H_2 and parallel to the surface 14. The package 800' may have the surface 808 facing the surface 792 of the external component 790 and terminals 812 on the surface 808 connected with corresponding ones of pads (not shown) on the surface 792. Similar to the package 800, the package 800' has a thickness in the direction of the thickness of the assembly 700 not greater than H2.

[0111] As such, any microelectronic element in the region 710, such as part of an encapsulated microelectronic unit, a microelectronic package connected to the conductive elements at the surface 14 that portion 712 overlies, or a microelectronic package connected to pads of an external component, have a height in the thickness direction T of the assembly 700 that permits the array of the end surfaces of the bond elements 24 to connect with corresponding ones of conductive elements of the external component 790. In one embodiment, the microelectronic element 702 may be logic and the microelectronic elements arranged within the region 712 may be memory.

[0112] In some embodiments, the microelectronic elements and packages within the region 710 may extend over a horizontal area having dimension less than R1 and R2, have a predetermined shape in the thickness direction T and have a thickness extending from the surface 14 to the surface 792 at most equal to H2, such that the end surfaces of the bond elements 24, and terminals of the package 800', may be aligned in the thickness direction of the assembly 700 with pads (not shown) on the surface 792 of the external component 790, and the packages 800 and 800' and the microelectronic element 752 are within the region 712 without contacting one another and the encapsulation elements 40. Solder elements 794 may electrically interconnect the bond elements 24 with corresponding contacts of the component 790, and electrically interconnect conductive elements of the package 800' with corresponding contacts of the component 790.

[0113] In another embodiment, the package 800' has a thickness in the direction T such that the surface 822 is adjacent the surface 14 and, in some embodiments, at least partially contacts the surface 14 or is attached with an adhesive to the surface 14.

[0114] In a further embodiment, referring to FIG. 10B, a package assembly 700' may have a similar construction as the package assembly 700 (see FIG. 10A) except that a microelectronic package, such as the package 2200 as described above (see FIG. 8), overlies the surface 16 of the structure 10 instead of the microelectronic element 702 and the dielectric mass 704. The surface 2208 of the package 2202 may face the surface 16 of the substrate 12, and the conductive elements 2212 of the package 2200 at the surface 2208 may be arranged in a pattern corresponding to a pattern of conductive elements 20 at the surface 16. Solder elements 2215 may electrically connect such elements 2212 with the

conductive elements 20. As such, the conductive elements of the package 2200 may be electrically connected, through conductive elements within or at a surface of the substrate 12, with conductive elements of the packages 800 and 800', the unit 755 and the external component 790.

[0115] In another embodiment, referring to FIG. 12, a package assembly 850 may include a structure 400' similar to the structure 400 (see FIG. 5) having encapsulation sub-elements 440A, 440B and 440C overlying a portion 450 of surface 414 of substrate 412. The elements 440A, 440B and 440C define a plurality of microelectronic receiving regions 402A and 402B having top portions 406A and 406B, respectively. A microelectronic element 702 is encapsulated by dielectric mass 704 over surface 416 of the substrate 412, where the surface 416 is opposite the surface 414 defining the microelectronic element receiving region, similarly as in the assembly 700. A microelectronic package 800 is arranged in the region 402A, connected to conductive elements at the surface 404 that the portion 406A overlies similarly as described for the assembly 700 of FIG. 10A, and so as not to contact the elements 440A and 440C. In addition, an encapsulated microelectronic unit 755 is arranged in the region 402B, connected to conductive elements at the surface 404 that the portion 406B overlies similarly as described for the assembly 700 of FIG. 10A, and so as not to contact the elements 440A and 440C. The package 800 and the unit 755 have a predetermined shape having height in the thickness direction of the assembly 800 to provide, similarly as described above with respect to FIG. 10A, that the end surfaces of the bond elements 424 may be electrically connected with corresponding ones of pads on a surface of an external component facing the surface 442 of the elements 440.

[0116] In another embodiment, referring to FIGs. 17 and 18, a package assembly 1600 may include the structure 1010 of the present disclosure (see FIG. 15) connected to a microelectronic element, package or assembly at the microelectronic element region 1210 thereof. In one embodiment, the package assembly 1600 may include the structure 1010 connected to a microelectronic element 1602, such as a DRAM, having oppositely facing surfaces 1605, 1607 and positioned in a "face-down" orientation relative to the die 1012 in the region 1212, with the surface 1605 facing the surface 1014 of the die 1012. Contacts 1604 at the surface 1605 may be bonded by solder elements 1609 to traces 1024' at the surface 1017 of the redistribution layer 1020, or pads 1018' at the surface 1014 of the die 1012 where the layer 1020 is omitted from the structure 1010. The bottom portion 1212 of the region 1210 overlies the traces 1024' and pads 1018'. The contacts 1604 may be electrically connected with the bond` elements 24 within the elements 1040, through the traces 1024', the pads 1018' and 1018 of the die 1012 and electrical circuitry (not shown) within the die 1012.

[0117] A dielectric mass or overmold 1626, having a configuration similar to the mold 626 (see FIG. 8), may be formed over the bottom portion 1212 of the region 1210. The dielectric mass 1626 has a surface 1628 remote from the surface 1014 that extends over the microelectronic element 1602 and away from the element 1602 over the surface 1014 in the horizontal directions H_1 and H_2 toward the edge surfaces 1044A and 1044B of the encapsulation elements 1040A and 1040B, respectively. In one embodiment, the surface 1628 extends to the edge surfaces 1044A and 1044B, and edge surface 1628A and 1628B extend downwardly thereform to the layer 1020 or the die 12 facing, and in some embodiments along and contacting at least portions of, portions of the

edge surfaces 1044A and 1044B, respectively. The dielectric mass 1626 may be made from a first dielectric material, and the encapsulation elements 1040 may be made from a second dielectric material that is different from the dielectric material of the mass 1626. The dielectric mass 1626 further includes a bottom surface 1630 extending from the edges surface 1628A and 1628B in horizontal directions H_1 and H_2 away from the encapsulation elements 1040A and 1040B and along exposed portions of the surface 1017 or 1014 and traces 1024' or pads 1018' thereon, respectively.

[0118] Referring to FIG. 18, the assembly 1600 may be positioned in a "face-down" or "flip assembly" orientation relative to an external component, such as the component 790 (see FIG. 10A), with the unenapsulated portions 52 of the bond elements 24 facing the surface 790 and electrically connected by solder elements 794 to contacts (not shown) on the surface 792 arranged in a pattern corresponding to the unenapsulated portions 52 of the structure 1010 within the assembly 1600. A dielectric mass 1726 may be formed over the microelectronic element 1602 and extend from a surface 1728, which extends along the surface 1628 and the surfaces 1042 of the encapsulation elements 1040, to an opposite surface 1730, which is remote from the mass 1626. The surface 1730 may extend along the surface 1728 in the directions H_1 and H_2 to be aligned in the direction H_1 and H_2 with, or extend beyond, the edges 1046A and 1046B, respectively. Opposite edge surfaces 1735A and 1735B of the mass 1726 may extend from the surface 792 to the surfaces 1046A and 1046B, respectively, in a vertical direction or angled with respect to the surfaces 792 and 1042. The dielectric material of the mass 1726 may fill any empty space between the component 790 and each of the mass 1626 and the encapsulation elements 1040, so as to encapsulate the unencapsulated portions 52 of the bond

elements 24, the solder elements 794 and conductive elements on the surface 792 opposite the assembly 1600. As such, similar to the connection of the assembly 700 to the component 790 as shown in FIG. 10A, the assembly 1600 may be electrically connected to the conductive elements of the component 790 where the height of the assembly 1600 in the thickness direction T permits the array of the end surfaces of the bond elements 24 to connect with corresponding ones of conductive elements of the external component 790. In addition, the external component may include traces (not shown) on a surface 794 opposite and remote from the surface 792 and to which solder elements 796 may be joined to provide for electrical connection of the die 1012 and the microelectronic element 1602 to still another external component (not shown) through the bond elements 24 and conductive elements on and within the substrate 790.

[0119] In some embodiments, such as in the assembly 1600 (see FIG. 18), the mass 1626, the mass 1726 and the encapsulation element 1040 may be formed, respectively, from different dielectric materials. In a further embodiment as shown in FIG. 19, the assembly 1600 may be joined with an external component, similarly as illustrated in FIG. 18, except that a dielectric mass 1800 of a same dielectric material, having the configuration of the mass 1626 and the mass 1726 as described above, encapsulates the microelectronic element 1602, the unencapsulation portions 52 of the bond elements and conductive elements at the surface 792. The mass 1800, however, is made from a different dielectric material than the encapsulation elements 1040.

[0120] In another embodiment, referring to FIG. 20, a package assembly 1800 may include a structure 1900 having a single encapsulation element 1840 overlying the die 1012 in a configuration similar to the encapsulation element 450

overlying the substrate as shown in FIG. 7D, to define a plurality of microelectronic receiving regions 402. The element 1840 includes portions 1840A, 1840B and 1840C that define a plurality of microelectronic receiving regions 402A and 402B similarly as shown in FIG. 7D, having portions 406A and 406B, respectively, overlying portions 1017A and 1017B of the layer 1020, which in turn overlie portions 1014A and 1014B of the surface 1014 of the die 1012. A microelectronic package 800, similarly as in the assembly 700 of FIG. 10A, may be arranged in the region 402A and connected to conductive elements at the surface 1017A that the portion 406A overlies, and does not contact adjacent portions 1840A and 1840C of the encapsulation element 1840 that define the region 402A. In addition, a microelectronic package 800', also similarly as shown in FIG. 10A, may be arranged within the region 402B, spaced from the portions 1840C and 1840B and connected to the component 790 at the surface 792. The packages 800 and 800' may have a predetermined shape having height in the thickness direction of the structure 1900 to provide, similarly as described above with respect to FIG. 10A, that the end surfaces of the bond elements 24 may be electrically connected with corresponding ones of pads on a surface of an external component facing the unencapsulated portions 52 of the bond elements 24 at the surface 1842 of the elements 1840 remote from the die 1012.

[0121] In another embodiment, referring to FIG. 21, a package assembly 2000 may include the structure 1900 (see FIG. 20) connected to microelectronic elements 2102A and 2102B arranged within the regions 402A and 402B and overlying the portions 406A and 406B, respectively, thereof. Similar to the microelectronic element 1602 in FIG. 18, the pads of the microelectronic elements 2101A and 2101B are joined by solder elements 1609 with traces at the portions 1017A and

1017B, respectively. Dielectric masses 2026A and 2026B are formed overlying the microelectronic elements 2102A and 2102B and have configurations similar to the mass 1626 as shown in FIG. 18, where respective opposite edge surfaces 2028A and 2028B thereof face, and in some embodiments contact, at least portions of facing edge surfaces 1844 of the elements 1840. For example, portions of the opposite edges surfaces 2028A may contact portions of the facing edge surface 1844A and 1844C, respectively, and portions of the opposite edges surfaces 2028B may contact portions of the facing edge surfaces 1844C and 1844B, respectively. The dielectric masses 2026A and 2026B may be made from a same or different dielectric material, and the material of the masses 2026 is different from the dielectric material of the encapsulation elements 1840.

[0122] The assemblies discussed above may be utilized in construction of diverse electronic systems. For example, a system 900 (FIG. 13) in accordance with a further embodiment of the invention includes a first package assembly 902, such as the assembly 850, and a second package assembly 904, such as the assembly 2000, and in conjunction with other electronic components 908 and 910. In the example depicted, component 908 is a semiconductor chip whereas component 910 is a display screen, but any other components may be used. Of course, although only two additional components are depicted in FIG. 13 for clarity of illustration, the system may include any number of such components. Package assemblies 902 and 904 and components 908 and 910 are mounted to a common housing 901, schematically depicted in broken lines, and are electrically interconnected with one another as necessary to form the desired circuit. In the exemplary system shown, the system includes a circuit panel 907 such as a flexible or rigid printed circuit board, and the circuit

panel includes numerous conductors 909, of which only one is depicted in FIG. 13, interconnecting the components with one another. An off-board connector connects component 910 to the circuit panel. However, this is merely exemplary; any suitable structure for making electrical connections may be used. The housing 901 is depicted as a portable housing of the type usable, for example, in a cellular telephone or personal digital assistant, and screen 910 is exposed at the surface of the housing. Again, the simplified system shown in FIG. 13 is merely exemplary; other systems, including systems commonly regarded as fixed structures, such as desktop computers, routers and the like may be made using the packages discussed above.

[0123] As these and other variations and combinations of the features discussed above may be utilized without departing from the present invention, the foregoing description of the preferred embodiments should be taken by way of illustration rather than by way of limitation of the invention as defined by the claims.

CLAIMS

1. A structure comprising:

a substrate having first and second oppositely facing surfaces and a plurality of electrically conductive elements at the first surface;

bond elements having bases joined to respective ones of the conductive elements at a first portion of the first surface and end surfaces remote from the substrate and the bases, each of the bond elements extending from the base to the end surface thereof; and

a dielectric encapsulation element overlying and extending from the first portion of the first surface of the substrate and filling spaces between the bond elements such that the bond elements are separated from one another by the encapsulation element, the encapsulation element having a third surface facing away from the first surface of the substrate and having an edge surface extending from the third surface towards the first surface, wherein unencapsulated portions of the bond elements are defined by at least portions of the end surfaces of the bond elements that are uncovered by the encapsulation element at the third surface;

wherein the encapsulation element at least partially defines a second portion of the first surface, the second portion being other than the first portion of the first surface and having an area sized to accommodate an entire area of a microelectronic element, and at least some of the conductive elements at the first surface are at the second portion and configured for connection with such microelectronic element.

2. The structure of claim 1, wherein the bond elements include at least one of a wire bond, a micro-pillar or a wire.

3. The structure of claim 1 further comprising:

solder at at least one of the base or the end surface of at least one of the bond elements.

4. The structure of claim 3, wherein the solder at the end surface of the at least one bond element is at the third surface.

5. The structure of claim 3, wherein the solder extends from the end surface of the at least one bond element through a portion of the encapsulation element towards the third surface.

6. The structure of claim 1, wherein at least a portion of at least one of the bond elements adjacent the end surface thereof is perpendicular to the third surface.

7. The structure of claim 1, wherein at least one of the bond elements includes a stud bump joined to the end surface thereof.

8. The structure of claim 1, wherein at least one of the bond elements extends along a substantially straight line between the base and the unencapsulated portion thereof, and wherein the substantially straight line forms an angle of less than 90° with respect to the first surface of the substrate.

9. The structure of claim 1, wherein at least one of the bond elements includes a substantially curved portion between the base and the end surface thereof.

10. The structure of claim 1, wherein the third surface includes a first surface portion at a first distance from the first surface of the substrate and a second surface portion at a second distance from the first surface of the substrate that is less than the first distance, and wherein the unencapsulated portion of at least one of the bond elements is uncovered by the encapsulation element at the second surface portion.

11. The structure of claim 1, wherein the encapsulation element includes a cavity formed therein extending from the third surface toward the substrate, and wherein the unencapsulated portion of one of the bond elements is disposed within the cavity.

12. The structure of claim 1, wherein at least one of the bond elements includes at least one of copper, gold, aluminum or solder.

13. The structure of claim 1, wherein the ones of the conductive elements to which the bond elements are respectively joined are arranged in a first array of a first predetermined configuration, and wherein the unencapsulated portions of the bond elements to which the ones of the conductive elements are joined are arranged in a second array of a second predetermined configuration that is different from the first predetermined configuration.

14. The structure of claim 13, wherein the first predetermined configuration is characterized by a first pitch and wherein the second configuration is characterized by a second pitch that is finer than the first pitch.

15. The structure of claim 1, wherein the end surfaces of the bond elements are configured for connection to a first component.

16. The structure of claim 1, wherein the second portion of the first surface of the substrate includes first and second sub-portions having areas sized to accommodate entire areas, respectively, of first and second microelectronic elements, and at least some of the conductive elements at the first surface are at the first and second sub-portions of the second portion and configured to permit connection, respectively, with the first and second microelectronic elements.

17. The structure of claim 16, wherein the encapsulation element includes a plurality of encapsulation sub-elements arranged spaced from each other, wherein the area of at least one of the first or second sub-portions is at least partially defined by first and second encapsulation sub-elements of the plurality of encapsulation sub-elements.

18. The structure of claim 1 further comprising:

a plurality of second electrically conductive elements at the second surface of the substrate;

second bond elements having bases joined to respective ones of the second conductive elements at a first portion of the second surface and end surfaces remote from the substrate and the bases thereof, each of the second bond elements extending from the base to the end surface thereof; and

a second dielectric encapsulation element overlying and extending from the first portion of the second surface and filling spaces between the second bond elements such that the second bond elements are separated from one another by the

second encapsulation element, the second encapsulation element having a fourth surface facing away from the second surface and an edge surface extending from the fourth surface toward the second surface of the substrate, wherein unencapsulated portions of the second bond elements are defined by at least portions of the end surfaces of the second bond elements that are uncovered by the second encapsulation element at the fourth surface.

19. The structure of claim 18, wherein the second encapsulation element at least partially defines a second portion of the second surface, the second portion of the second surface being other than the first portion of the second surface and having an area sized to accommodate an entire area of another microelectronic element, and at least some of the second conductive elements at the second surface are at the second portion of the second surface and configured for connection with the another microelectronic element.

20. The structure of claim 1 further comprising:

a plurality of first terminals at the second

surface configured for connection to a first component, at least

some of the first terminals electrically connected with the conductive elements.

21. A package assembly including a structure of claim 1 and further comprising:

a first microelectronic element disposed over the second portion and electrically connected to at least one of the some of the conductive elements; and

a dielectric mass covering the first microelectronic element and at least a part of the second portion, the dielectric mass defining a fourth surface remote from and facing away from the first surface, at least a part of the fourth surface extending over the microelectronic element and the second portion, the dielectric mass defining a second edge surface facing at least a part of the edge surface,

wherein the dielectric mass is other than the encapsulation element.

22. The package assembly of claim 21, wherein at least a portion of the edge surface contacts at least a portion of the second edge surface.

23. The package assembly of claim 22, wherein at least a portion of at least one of the edge surface or the second edge surface is planar.

24. The package assembly of claim 21, wherein a thickness of the dielectric mass from the second surface of the substrate is less than a thickness of the encapsulation element from the second surface of the substrate.

25. The package assembly of claim 21, wherein the first microelectronic element has fifth and sixth oppositely facing surfaces, the fifth surface facing the first surface, and wherein the first microelectronic element is electrically connected with the at least one of the some of the first conductive elements at at least one of the fifth and sixth surfaces.

26. The package assembly of claim 25, wherein a bond wire extending from the sixth surface electrically connects

the first microelectronic element with the at least one of the some of the conductive elements.

27. The package assembly of claim 25, wherein a contact at the fifth surface of the first microelectronic element is electrically connected with the at least one of the some of the first conductive elements.

28. The package assembly of claim 21 further comprising:

a redistribution layer extending along at least a portion of at least one of the third surface or the fourth surface, wherein the redistribution layer includes a redistribution substrate having a fifth surface adjacent the least one of the third surface or the fourth surface and an sixth surface remote from the fifth surface, first conductive pads at the fifth surface of the redistribution substrate and aligned with and mechanically connected to respective ones of the unencapsulated portions of the bond elements, and second conductive pads at the sixth surface of the redistribution substrate electrically connected to the first conductive pads.

29. A package assembly including a structure of claim 1 and further comprising:

a first microelectronic element disposed over the second surface of the substrate and electrically connected with at least one of the conductive elements through at least one of a plurality of second conductive elements at the second surface; and

a dielectric mass covering the first microelectronic element and at least a part of the second surface extending away from the first microelectronic element, the dielectric

mass defining a fourth surface remote from and facing away from the second surface.

30. The package assembly of claim 29, wherein the first microelectronic element has fifth and sixth oppositely facing surfaces, the fifth surface facing the second surface, and wherein the first microelectronic element is electrically connected at at least one of the fifth and sixth surfaces with at least one of the second conductive elements.

31. The package assembly of claim 30, wherein a bond wire extending from the sixth surface electrically connects the first microelectronic element with the at least one of second conductive elements.

32. The package assembly of claim 30, wherein a contact at the fifth surface of the first microelectronic element is electrically connected with the at least one of the second conductive elements.

33. The package assembly of claim 29 further comprising:

at least one second microelectronic element disposed over the second portion and electrically connected with at least one of the conductive elements.

34. The package assembly of claim 33, wherein the second microelectronic element has seventh and eighth oppositely facing surfaces, the seventh surface facing the first surface, and wherein the second microelectronic element is electrically connected at at least one of the seventh and eighth surfaces with the at least some of the conductive elements.

35. The package assembly of claim 34, wherein a bond wire extending from the eighth surface electrically connects the second microelectronic element with one of the at least some of the first conductive elements.

36. The package assembly of claim 34, wherein a contact at the seventh surface of the second microelectronic element is electrically connected with one of the at least some of the conductive elements.

37. The package assembly of claim 33, wherein the second microelectronic element is part of a microelectronic package,

wherein the microelectronic package includes a second substrate having seventh and eighth oppositely facing surfaces, the second microelectronic element disposed over the eight surface, electrically conductive elements on the second substrate, the conductive elements on the second substrate including terminals at the seventh surface, the second microelectronic element being electrically connected with at least one of the conductive elements on the second substrate,

wherein the seventh surface faces the first surface and the terminals of the microelectronic package are electrically connected by respective solder elements with the conductive elements of the structure.

38. The package assembly of claim 33, wherein the second microelectronic element is part of a microelectronic package including terminals on a surface thereof,

wherein the second microelectronic element is electrically connected with at least one of the some of the

conductive elements through conductive elements of an external component to which the terminals of the microelectronic package and at least one of the bond elements are electrically connected.

39. The package assembly of claim 33, wherein the at least one second microelectronic element includes a plurality of the second microelectronic elements, and at least one of the second microelectronic elements is part of a microelectronic package electrically connected with at least some one of the conductive elements of the structure.

40. The package assembly of claim 39, wherein one of the second microelectronic elements is part of a microelectronic package having terminals at a surface thereof electrically connected by respective solder elements with the some of the conductive elements of the structure, and another of the second microelectronic elements is part of a microelectronic package having terminals at a surface thereof electrically connected with some of the conductive elements through conductive elements of an external component to which the terminals of the another of the second microelectronic packages and at least one of the bond elements are electrically connected.

41. The package assembly of claim 39,

wherein the second portion of the first surface of the substrate includes first and second sub-portions having areas sized to accommodate entire areas, respectively, a first of the second microelectronic elements and the microelectronic package which includes another of the second microelectronic elements, and at least some of the conductive elements at the first surface are at the first and second sub-portions of the

second portion and configured to permit connection, respectively, with the first of the second microelectronic elements and the microelectronic package.

42. The structure of claim 1, wherein the encapsulation element extends a length of at least 150 micrometers from the first portion of the first surface of the substrate to the third surface.

43. The structure of claim 1, wherein the first portion of the first surface of the substrate that the encapsulation element overlies completely encloses the second portion of the first surface of the substrate.

44. A method of making a structure comprising:

forming a dielectric encapsulation element on a substrate, the substrate having first and second oppositely facing surfaces and a plurality of electrically conductive elements at the first surface, and wherein bond elements are joined at bases thereof to respective ones of the conductive elements at a first portion of the first surface and end surfaces of the bond elements are remote from the substrate and the bases, each of the bond elements extending from the base to the end surface thereof,

wherein the dielectric encapsulation element is formed overlying and extending from the first portion of the first surface of the substrate and filling spaces between the bond elements such that the bond elements are separated from one another by the encapsulation element, the encapsulation element having a third surface facing away from the first surface of the substrate and having an edge surface extending from the third surface towards the first surface, wherein unencapsulated portions of the bond elements are defined by at least portions of the end surfaces of the bond elements

that are uncovered by the encapsulation element at the third surface, and

wherein the encapsulation element at least partially defines a second portion of the first surface, the second portion being other than the first portion of the first surface and having an area sized to accommodate an entire area of a microelectronic element, and at least some of the conductive elements at the first surface are at the second portion and configured for connection with such microelectronic element.

45. The method of claim 44, wherein the bond elements include at least one of a wire bond, a micro-pillar or a wire.

46. The method of claim 44, wherein the bond elements include at least one wire soldered at the base thereof to one of the conductive elements before the encapsulation element is formed on the substrate.

47. The method of claim 44 further comprising:

after the forming of the encapsulation element, forming a dielectric mass covering a first microelectronic element and at least a part of the second portion, the first microelectronic element disposed over the second portion and electrically connected with at least some of the conductive elements, the dielectric mass defining a fourth surface remote from and facing away from the first surface, at least a part of the fourth surface extending over the microelectronic element and the second portion, the dielectric mass defining a second edge surface facing at least a part of the edge surface,

wherein the dielectric mass is other than the encapsulation element.

48. The method of claim 47, wherein at least a portion of the edge surface contacts at least a portion of the second edge surface.

49. The method of claim 44 further comprising:

forming a dielectric mass covering a first microelectronic element and at least a part of the second surface extending away from the first microelectronic element, the first microelectronic element disposed over the second surface of the substrate and electrically connected with at least one of the conductive elements through at least one of a plurality of second conductive elements at the second surface.

50. The method of claim 49 further comprising:

electrically connecting at least one second microelectronic element with some of the conductive elements at the second portion of the first surface of the substrate.

51. The method of claim 50, wherein the at least one second microelectronic element includes a plurality of the second microelectronic elements, and at least one of the second microelectronic elements is part of a microelectronic package electrically connected with at least some of the first conductive elements.

52. The method of claim 50, wherein one of the second microelectronic elements is part of a microelectronic package having terminals at a surface thereof electrically connected by respective solder elements to the some of the conductive

elements of the structure, and another of the second microelectronic elements is part of a microelectronic package having terminals at a surface thereof electrically connected with some of the conductive elements at the first surface through conductive elements of an external component to which the terminals of the another of the second microelectronic packages and at least one of the bond elements are electrically connected.

53. A structure comprising:

an active die having first and second oppositely facing surfaces and a plurality of electrically conductive elements at the first surface;

bond elements having bases joined to respective ones of the conductive elements at a first portion of the first surface and end surfaces remote from the die and the bases, each of the bond elements extending from the base to the end surface thereof; and

a dielectric encapsulation element overlying and extending from the first portion of the first surface of the die and filling spaces between the bond elements such that the bond elements are separated from one another by the encapsulation element, the encapsulation element having a third surface facing away from the first surface of the die and having an edge surface extending from the third surface towards the first surface, wherein unencapsulated portions of the bond elements are defined by at least portions of the end surfaces of the bond elements that are uncovered by the encapsulation element at the third surface;

wherein the encapsulation element at least partially defines a second portion of the first surface, the second portion being other than the first portion of the first surface and having an area sized to accommodate an entire

area of a microelectronic element, and at least some of the conductive elements at the first surface are at the second portion and configured for connection with such microelectronic element.

54. The structure of claim 53, wherein the die is a field programmable gate array.

55. The structure of claim 53, wherein the third surface includes a first surface portion at a first distance from the first surface of the die and a second surface portion at a second distance from the first surface of the die that is less than the first distance, and wherein the unencapsulated portion of at least one of the bond elements is uncovered by the encapsulation element at the second surface portion.

56. The structure of claim 53, wherein the encapsulation element includes a cavity formed therein extending from the third surface toward the die, and wherein the unencapsulated portion of one of the bond elements is disposed within the cavity.

57. A package assembly including a structure of claim 53 and further comprising:

a first microelectronic element disposed over the second portion and electrically connected to at least one of the some of the conductive elements; and

a dielectric mass covering the first microelectronic element and at least a part of the second portion, the dielectric mass defining a fourth surface remote from and facing away from the first surface, at least a part of the fourth surface extending over the microelectronic element and

the second portion, the dielectric mass defining a second edge surface facing at least a part of the edge surface,

wherein the dielectric mass is other than the encapsulation element.

58. The package assembly of claim 57, wherein at least a portion of the edge surface contacts at least a portion of the second edge surface.

59. The package assembly of claim 58, wherein at least a portion of at least one of the edge surface or the second edge surface is planar.

60. The package assembly of claim 57, wherein the dielectric mass encapsulates the unencapsulated portions of the bond elements and overlies the third surface of the encapsulation element.

61. The package assembly of claim 57 further comprising:

a second dielectric mass overlying the fourth surface of the dielectric mass and the third surface of the encapsulation element, and encapsulating the unencapsulated portions of the bond elements,

wherein the second dielectric mass is other than the encapsulation element and the dielectric mass.

62. The structure of claim 57, wherein the second portion of the first surface of the die includes first and second sub-portions having areas sized to accommodate entire areas, respectively, of first and second microelectronic elements, and at least some of the conductive elements at the first surface are at the first and second sub-portions of the

second portion and configured to permit connection, respectively, with the first and second microelectronic elements.

63. A package assembly including a structure of claim 62 and further comprising:

the first and second microelectronic elements, wherein the first and second microelectronic elements are disposed over the first and second sub-portions, respectively, and electrically connected to at least one of the some of the conductive elements;

a first dielectric mass covering the first microelectronic element and at least a part of the first sub-portion, the first dielectric mass defining a fourth surface remote from and facing away from the first surface, at least a part of the fourth surface extending over the first microelectronic element and the first sub- portion, the first dielectric mass defining a second edge surface facing at least a part of the edge surface; and

a second dielectric mass covering the second microelectronic element and at least a part of the second sub-portion, the second dielectric mass defining a fifth surface remote from and facing away from the first surface, at least a part of the fifth surface extending over the second microelectronic element and the second sub-portion, the second dielectric mass defining a second edge surface facing at least a part of the edge surface,

wherein each of the first and second dielectric mass is other than the encapsulation element.

64. The package assembly of claim 63, wherein at least a portion of the edge surface contacts at least a portion of

the second edge surface of at least one of the first or second dielectric mass.

65. A package assembly including a structure of claim 62 and further comprising the first and second microelectronic elements,

wherein the first microelectronic element is of a first microelectronic package disposed over the first sub-portion and electrically connected with at least one of the conductive elements at the second surface; and

wherein the second microelectronic element is of a second microelectronic package disposed over the second sub-portion and electrically connected with at least one of the conductive elements at the second surface through conductive elements of an external component to which terminals of the second package and at least one of the bond elements are electrically connected.

66. A method of making a structure comprising:

forming a dielectric encapsulation element on an active die provided at wafer level, the die having first and second oppositely facing surfaces and a plurality of electrically conductive elements at the first surface, and wherein bond elements are joined at bases thereof to respective ones of the conductive elements at a first portion of the first surface and end surfaces of the bond elements are remote from the substrate and the bases, each of the bond elements extending from the base to the end surface thereof,

wherein the dielectric encapsulation element is formed overlying and extending from the first portion of the first surface of the die and filling spaces between the bond elements such that the bond elements are separated from one another by the encapsulation element, the encapsulation

element having a third surface facing away from the first surface of the die and having an edge surface extending from the third surface towards the first surface, wherein unencapsulated portions of the bond elements are defined by at least portions of the end surfaces of the bond elements that are uncovered by the encapsulation element at the third surface, and

wherein the encapsulation element at least partially defines a second portion of the first surface, the second portion being other than the first portion of the first surface and having an area sized to accommodate an entire area of a microelectronic element, and at least some of the conductive elements at the first surface are at the second portion and configured for connection with such microelectronic element.

67. The method of claim 66 further comprising:

after the forming of the encapsulation element, forming a dielectric mass covering a first microelectronic element and at least a part of the second portion, the first microelectronic disposed over the second portion and electrically connected with at least some of the conductive elements, the dielectric mass defining a fourth surface remote from and facing away from the first surface, at least a part of the fourth surface extending over the microelectronic element and the second portion, the dielectric mass defining a second edge surface facing at least a part of the edge surface,

wherein the dielectric mass is other than the encapsulation element.

68. The method of claim 67, wherein at least a portion of the edge surface contacts at least a portion of the second edge surface.

69. The method of claim 67, wherein the dielectric mass encapsulates the unencapsulated portions of the bond elements and overlies the third surface of the encapsulation element.

70. The method of claim 67 further comprising:

forming a second dielectric mass overlying the fourth surface of the dielectric mass and the third surface of the encapsulation element, and encapsulating the unencapsulated portions of the bond elements,

wherein the second dielectric mass is other than the encapsulation element and the dielectric mass.

71. The method of claim 66 further comprising:

electrically connecting at least one microelectronic element with some of the conductive elements at the second portion of the first surface of the die.

72. The method of claim 66 further comprising:

electrically connecting at least one first microelectronic element at a first sub-portion of the second portion of the first surface of the die and at least one second microelectronic element at a second sub-portion of the second portion of the first surface of the die, wherein each of the first and second sub-portions has an area sized to accommodate an entire area, respectively, of the first and second microelectronic elements and at least some of the conductive elements at the first surface are at the first and second sub-portions of the second portion and configured to

permit connection, respectively, with the first and second microelectronic elements.

73. The method of claim 72 further comprising:

forming a first dielectric mass covering the first microelectronic element and at least a part of the first sub-portion, the first dielectric mass defining a fourth surface remote from and facing away from the first surface, at least a part of the fourth surface extending over the first microelectronic element and the first sub-portion, the first dielectric mass defining a second edge surface facing at least a part of the edge surface; and

forming a second dielectric mass covering the second microelectronic element and at least a part of the second sub-portion, the second dielectric mass defining a fifth surface remote from and facing away from the first surface, at least a part of the fifth surface extending over the second microelectronic element and the second sub-portion, the second dielectric mass defining a second edge surface facing at least a part of the edge surface,

wherein each of the first and second dielectric mass is other than the encapsulation element.

74. The method of claim 72, wherein the first microelectronic element is of a first microelectronic package disposed over the first sub-portion and electrically connected with at least one of the conductive elements at the second surface; and

wherein the second microelectronic element is of a second microelectronic package disposed over the second sub-portion and electrically connected with at least one of the conductive elements at the second surface through conductive elements of an external component to which terminals of the

second package and at least one of the bond elements are electrically connected.

FIG. 1

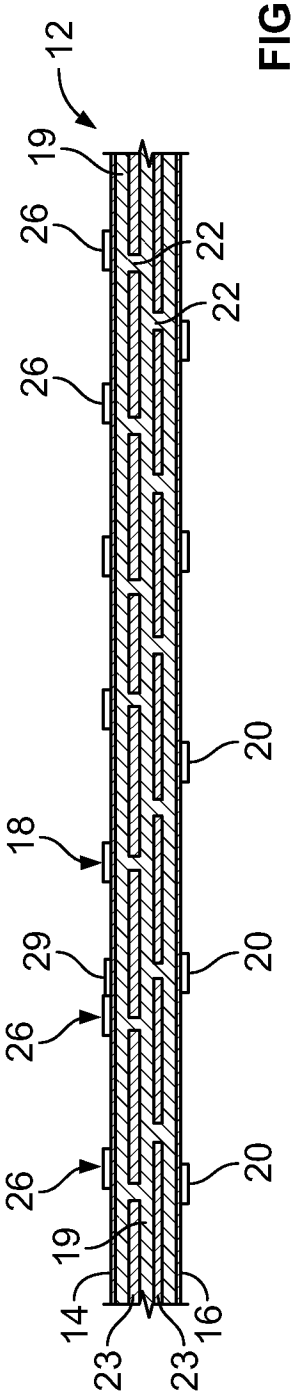


FIG. 2

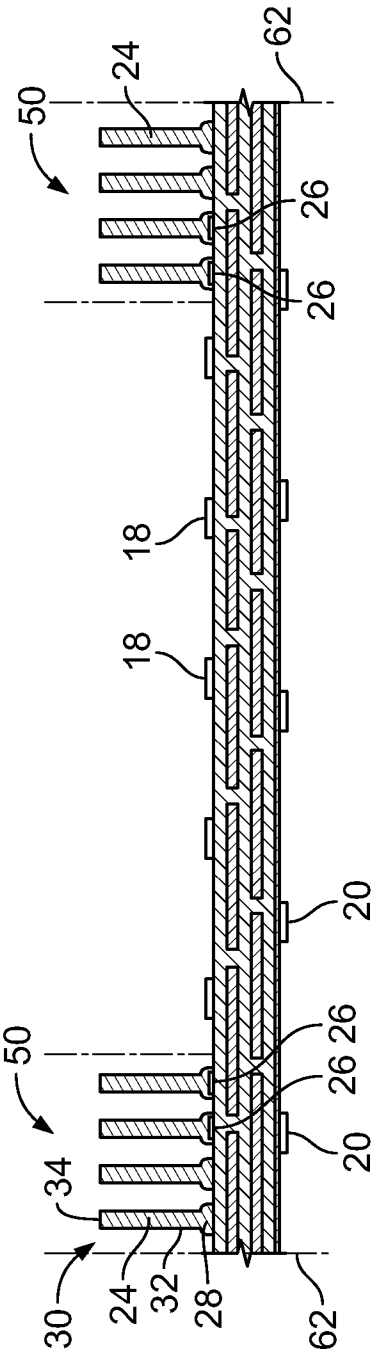
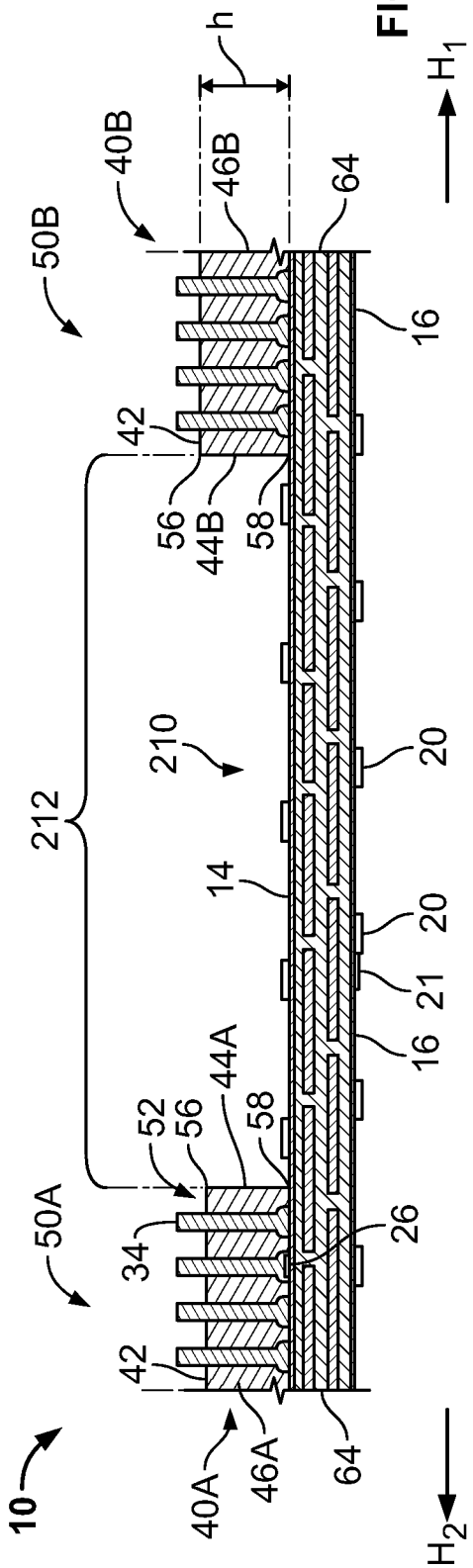


FIG. 3



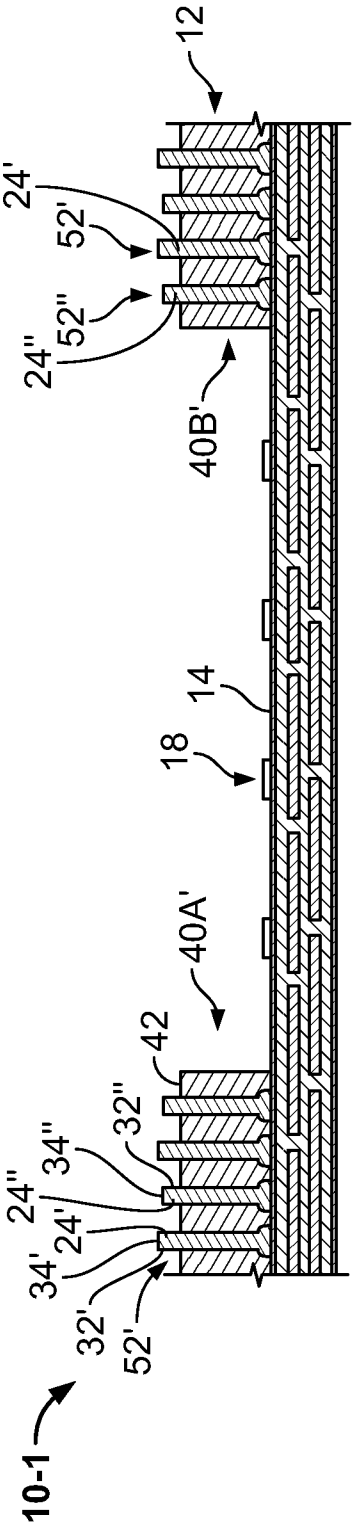

12
24'
52'
52''
24''
40B'
18
14
40A'
42
32''
34''
24''
24'
34'
32'
52'
10-1

FIG. 4A

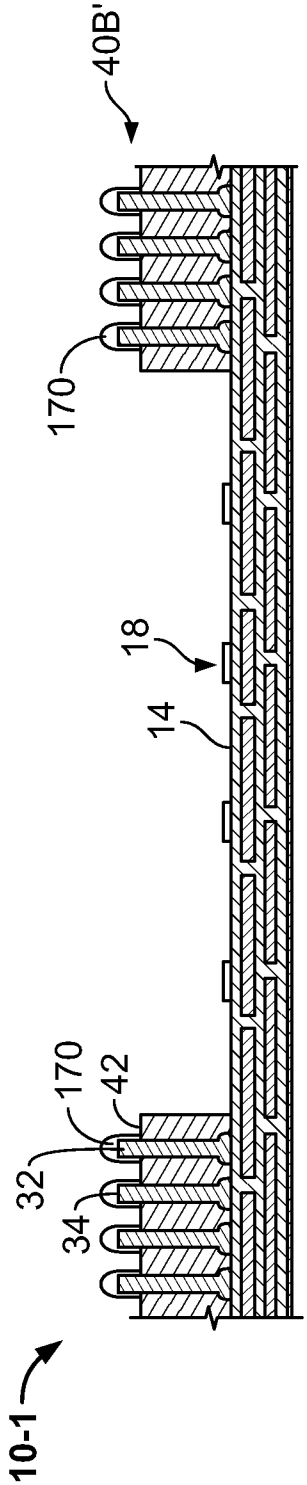

40B'
170
18
14
170
42
32
34
10-1

FIG. 4B

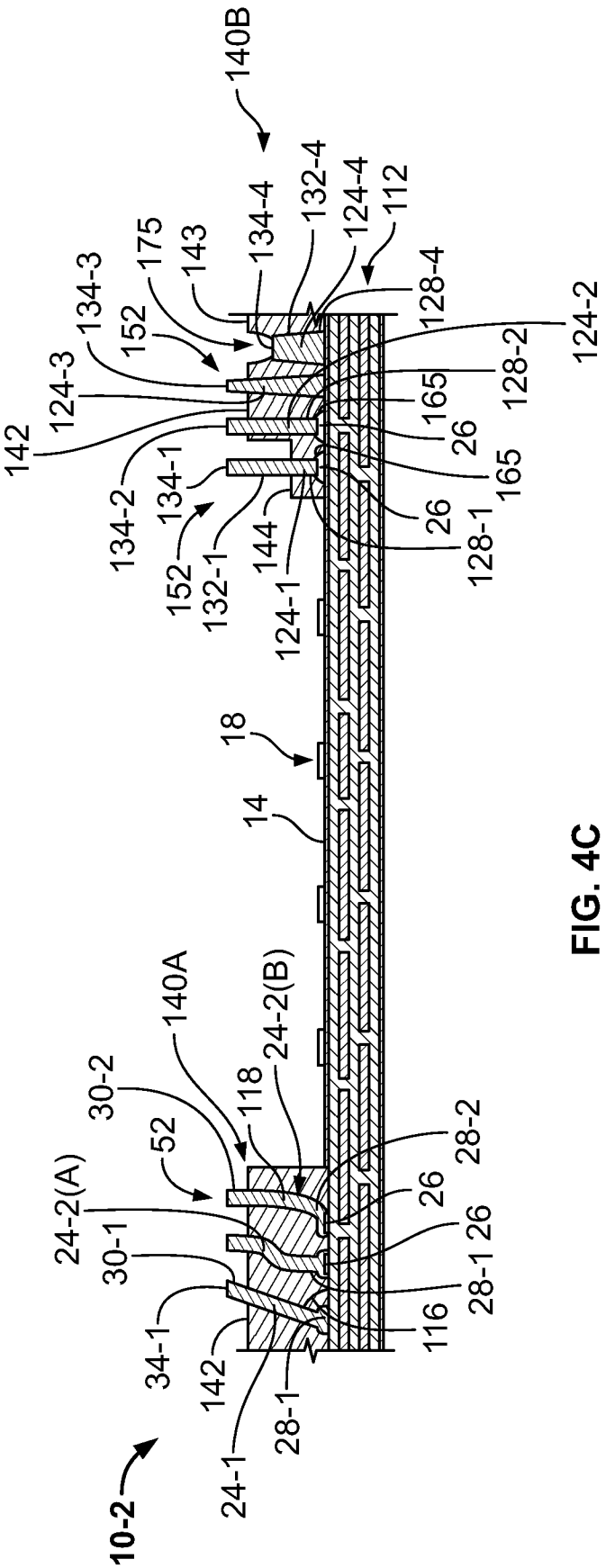

140B
134-4
132-4
124-4
112
175
143
134-3
152
128-4
124-2
124-3
128-2
142
165
26
134-2
134-1
165
152
132-1
144
26
124-1
128-1
18
14
140A
24-2(B)
30-2
118
52
28-2
24-2(A)
26
30-1
28-1 26
34-1
116
142
28-1
24-1
10-2

FIG. 4C

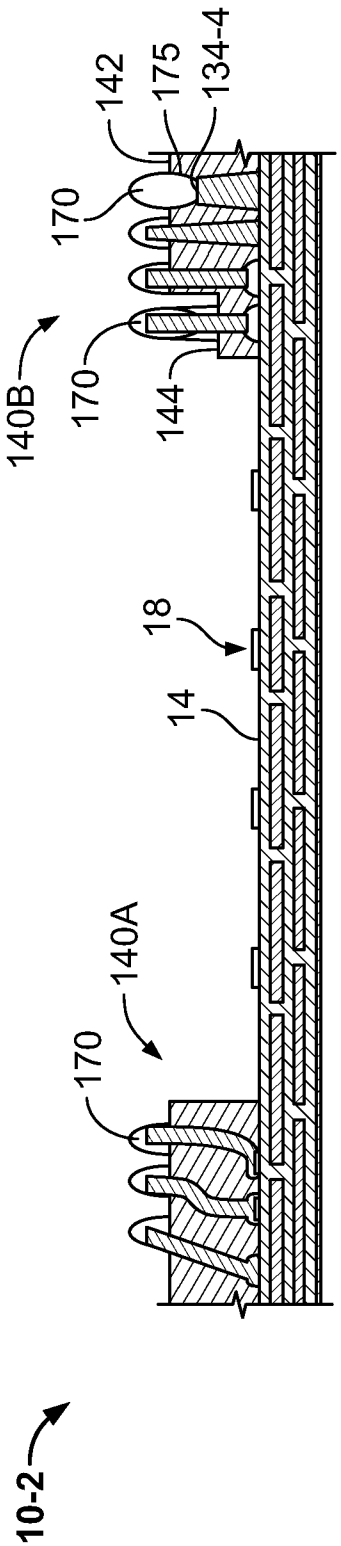

142
175
134-4
170
140B
170
144
18
14
140A
170
10-2

FIG. 4D

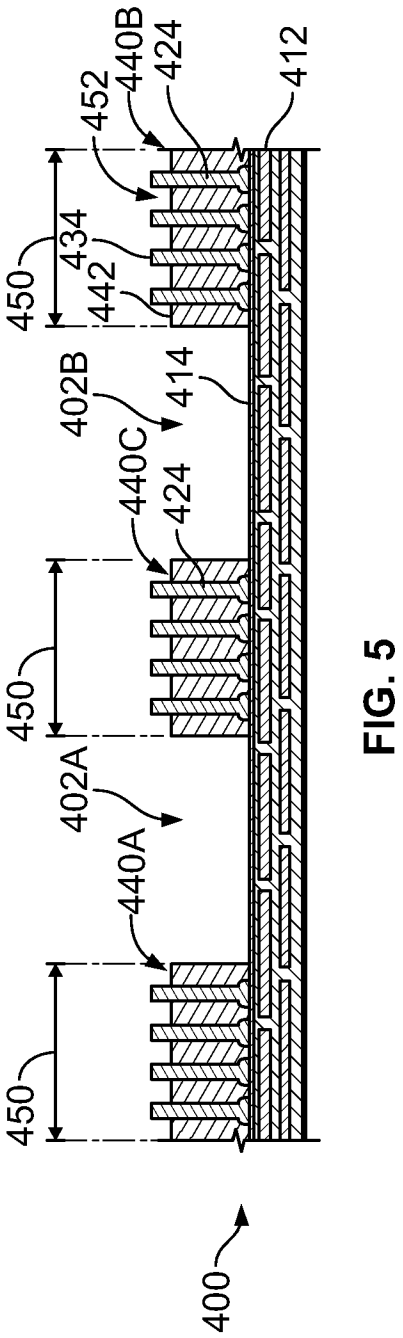

400
450
450
450
402A
440A
402B
440C
414
424
424
434
442
452
440B
412

FIG. 5

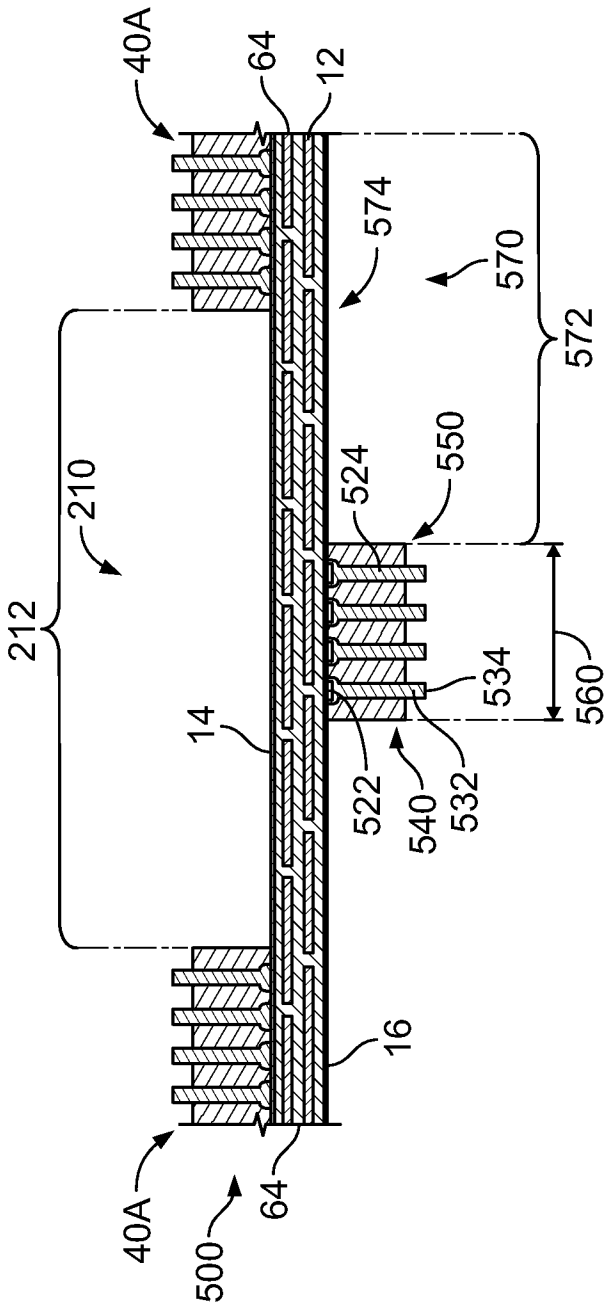

40A
500
64
40A
64
12
574
570
572
210
212
524
550
534
560
14
522
540
532
16

FIG. 6

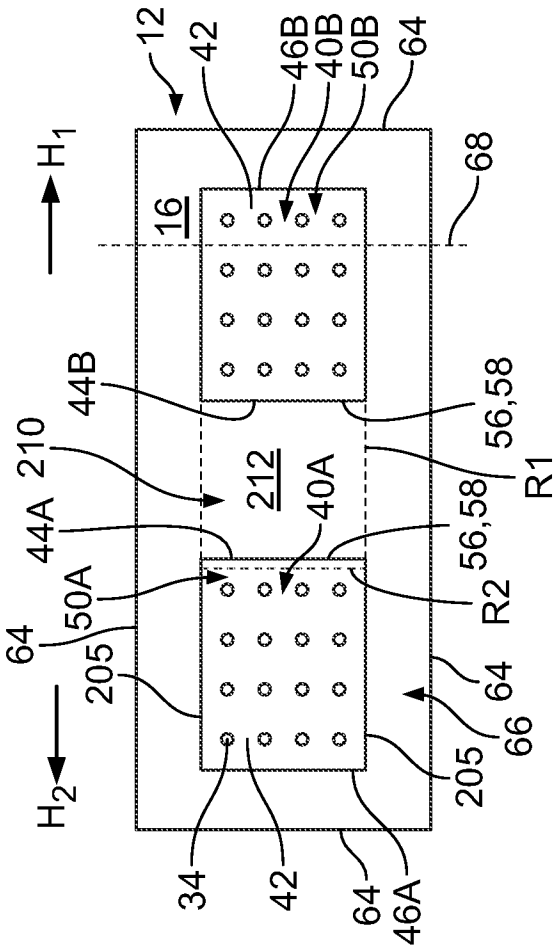

12
42
46B
40B
50B
64
68
H1
16
44B
210
212
40A
44A
50A
64
205
H2
56,58
R1
56,58
R2
64
66
205
34
42
64
46A

FIG. 7A

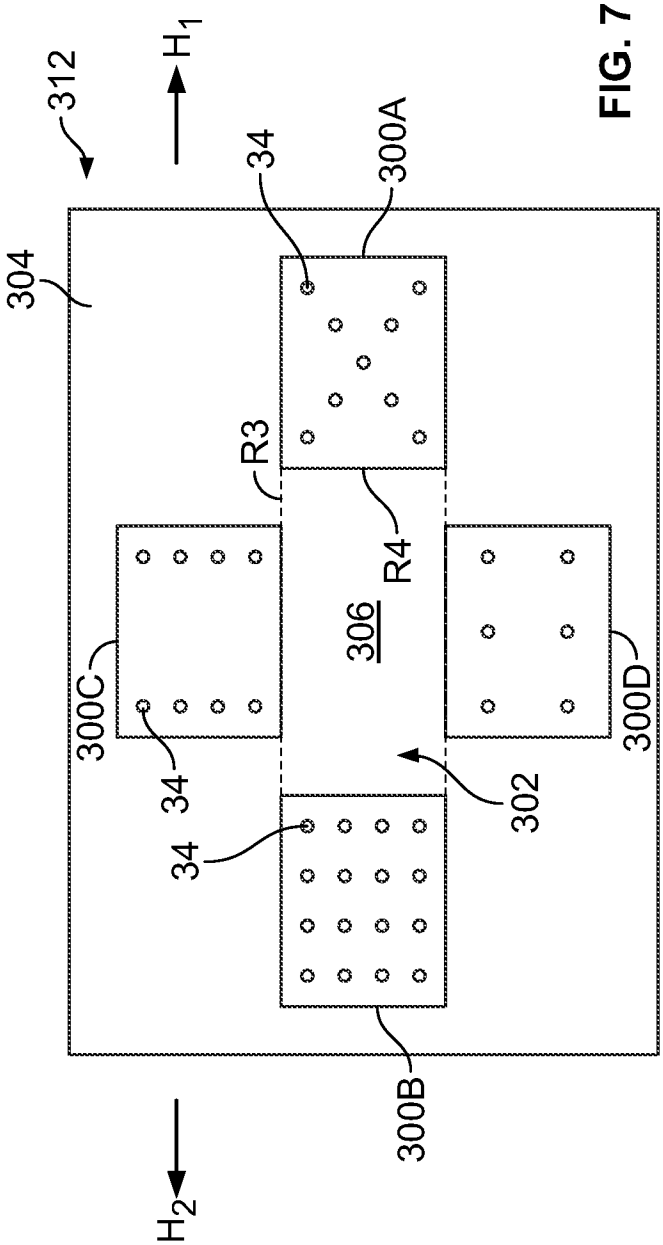

312
H1
34
300A
304
R3
R4
306
300C
300D
34
34
302
300B
H2

FIG. 7B

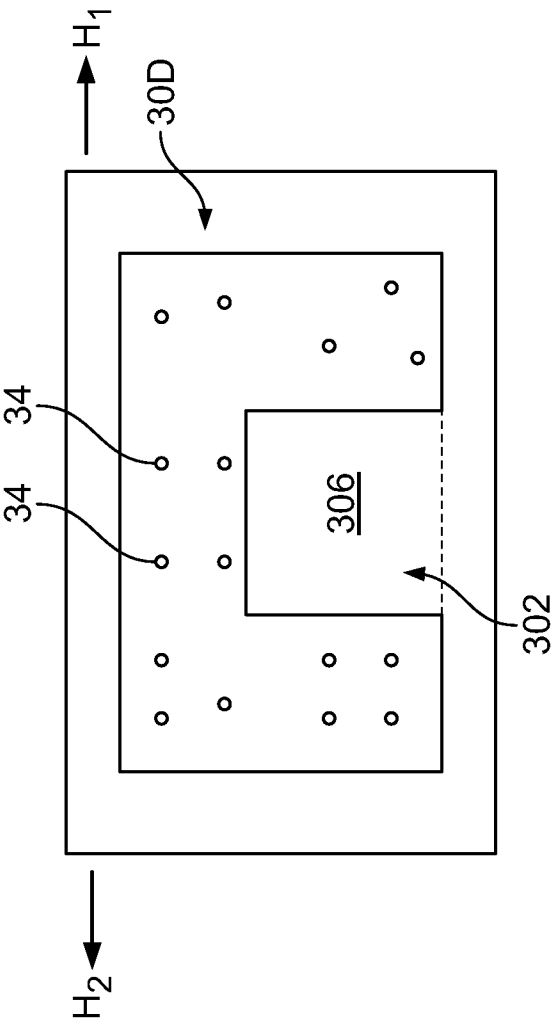

H1
30D
34
34
306
302
H2

FIG. 7C

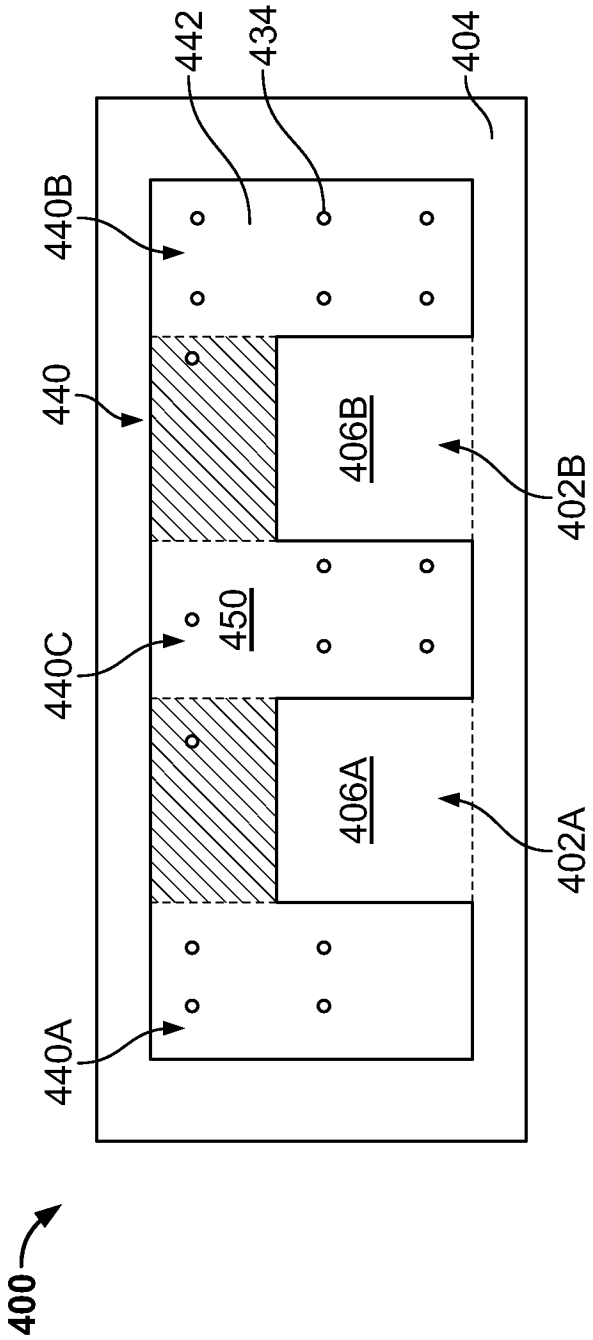

442
434
404
440B
440
406B
402B
450
440C
406A
402A
440A
400

FIG. 7D

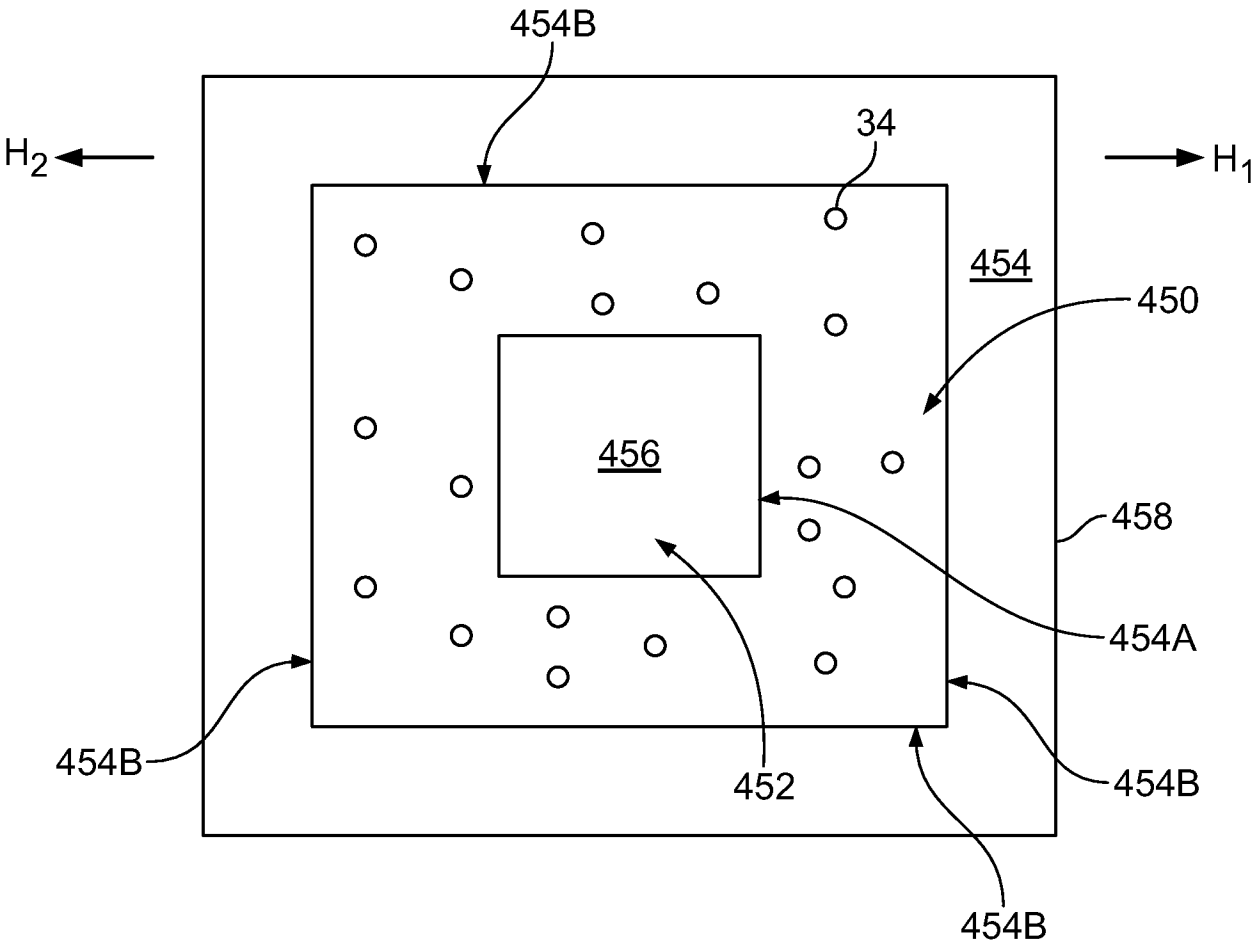


FIG. 7E

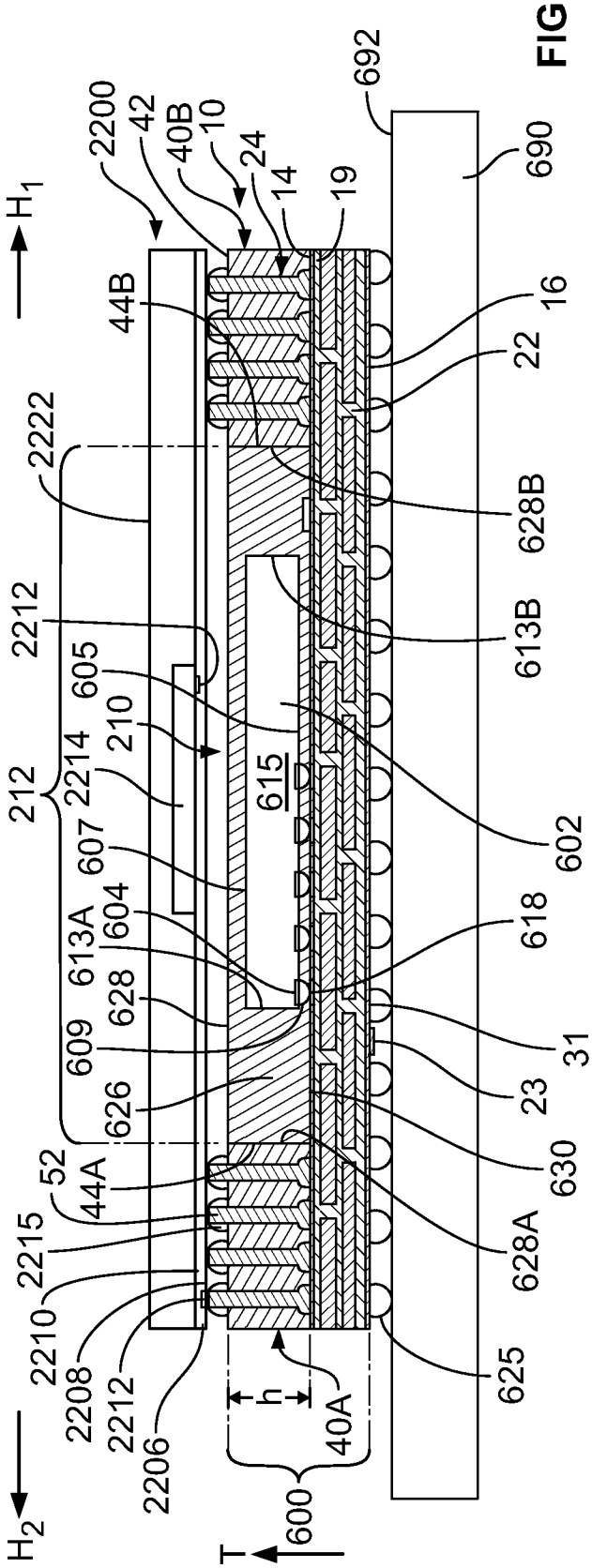

H1
H2
T
2200
42
40B
10
24
14
19
692
690
44B
16
22
2222
628B
2212
613B
605
210
214
615
602
212
607
613A
604
618
628
609
31
626
23
52
630
44A
628A
2215
2210
625
2208
h
2212
40A
2206
600

FIG. 8

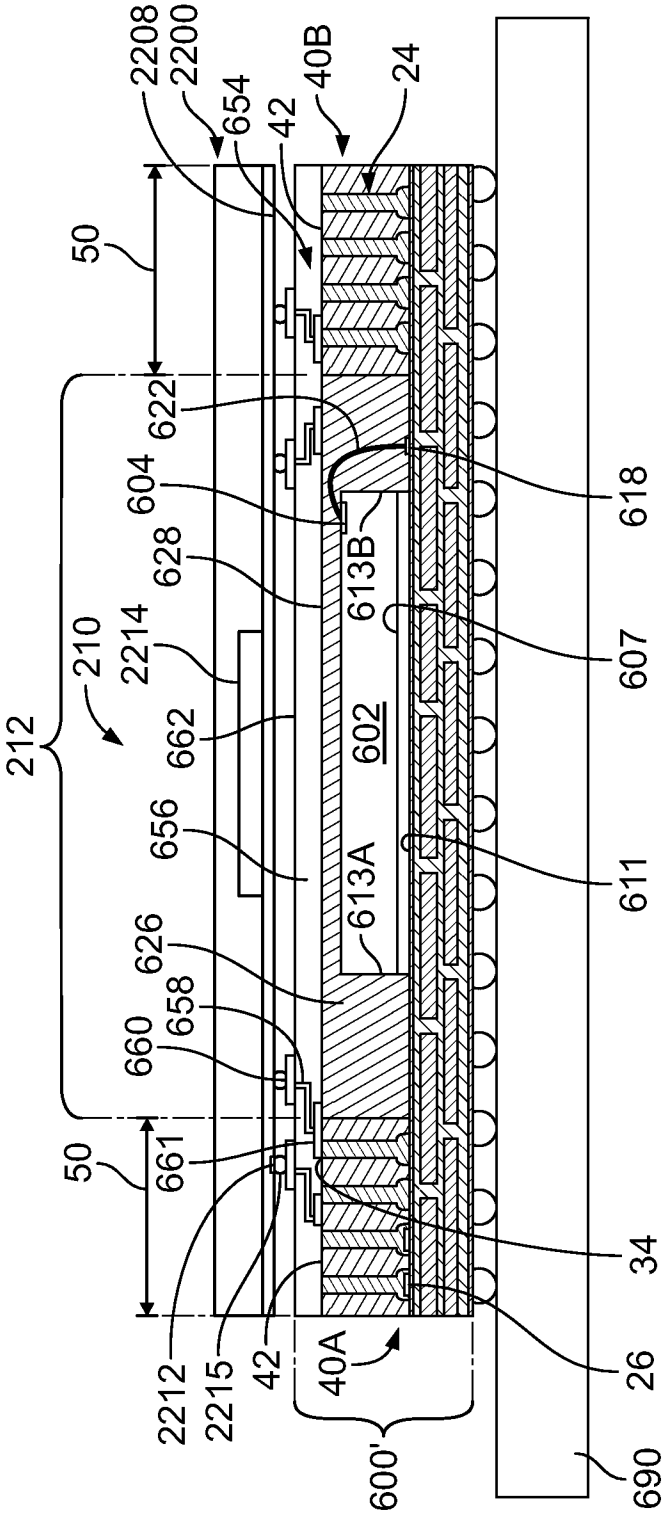

2208
2200
654
42
40B
24
50
622
618
604
613B
628
607
210
2214
602
662
212
656
611
613A
626
658
660
661
50
34
2212
2215
42
40A
26
600'
690

FIG. 9

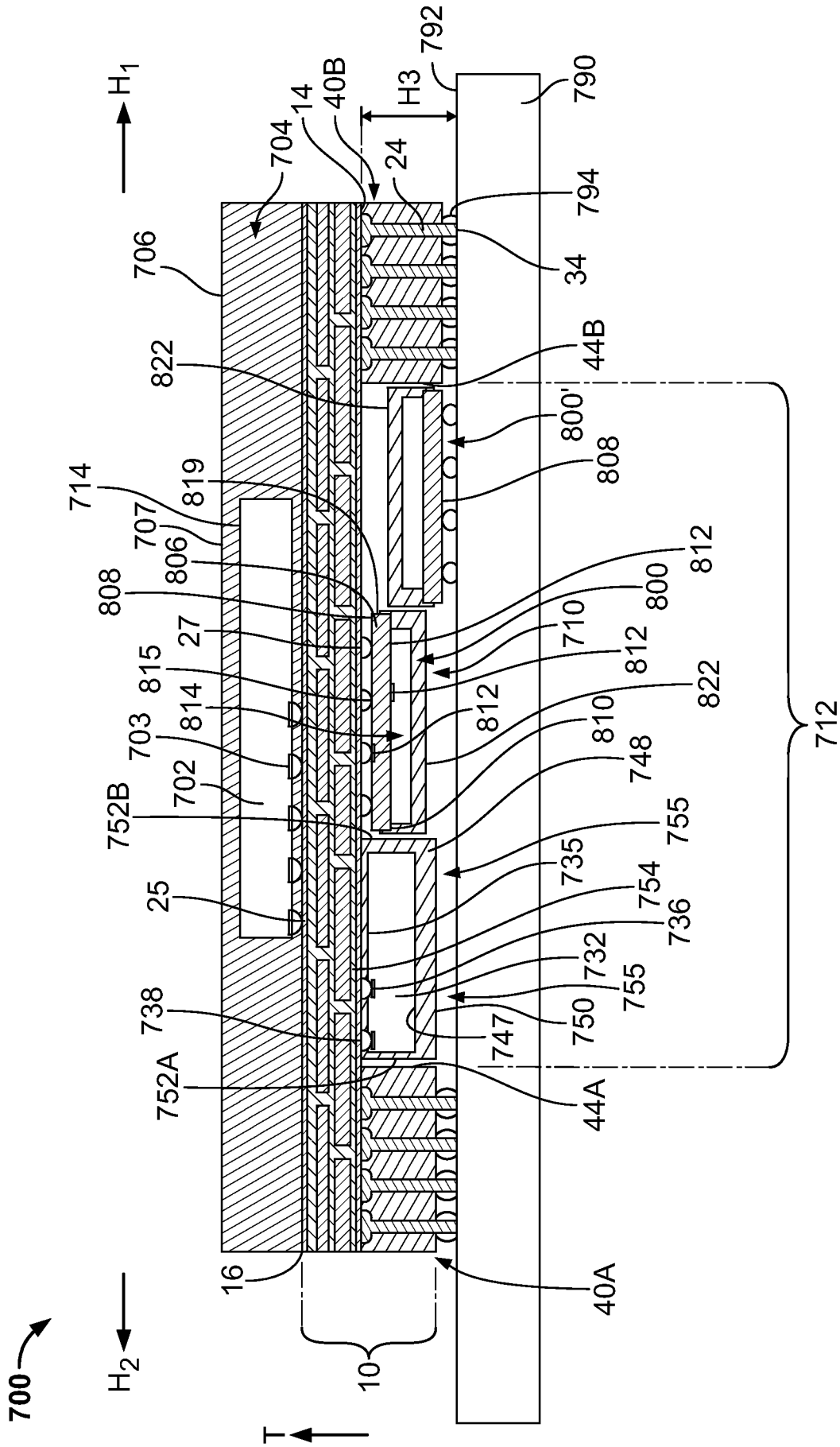

700
H1
H2
T
H3
792
790
704
14
40B
24
794
34
706
822
44B
800'
808
714
819
707
806
808
812
800
710
812
27
815
814
703
702
752B
812
822
810
748
755
735
754
736
732
755
750
747
738
752A
25
44A
16
40A
10
712

FIG. 10A

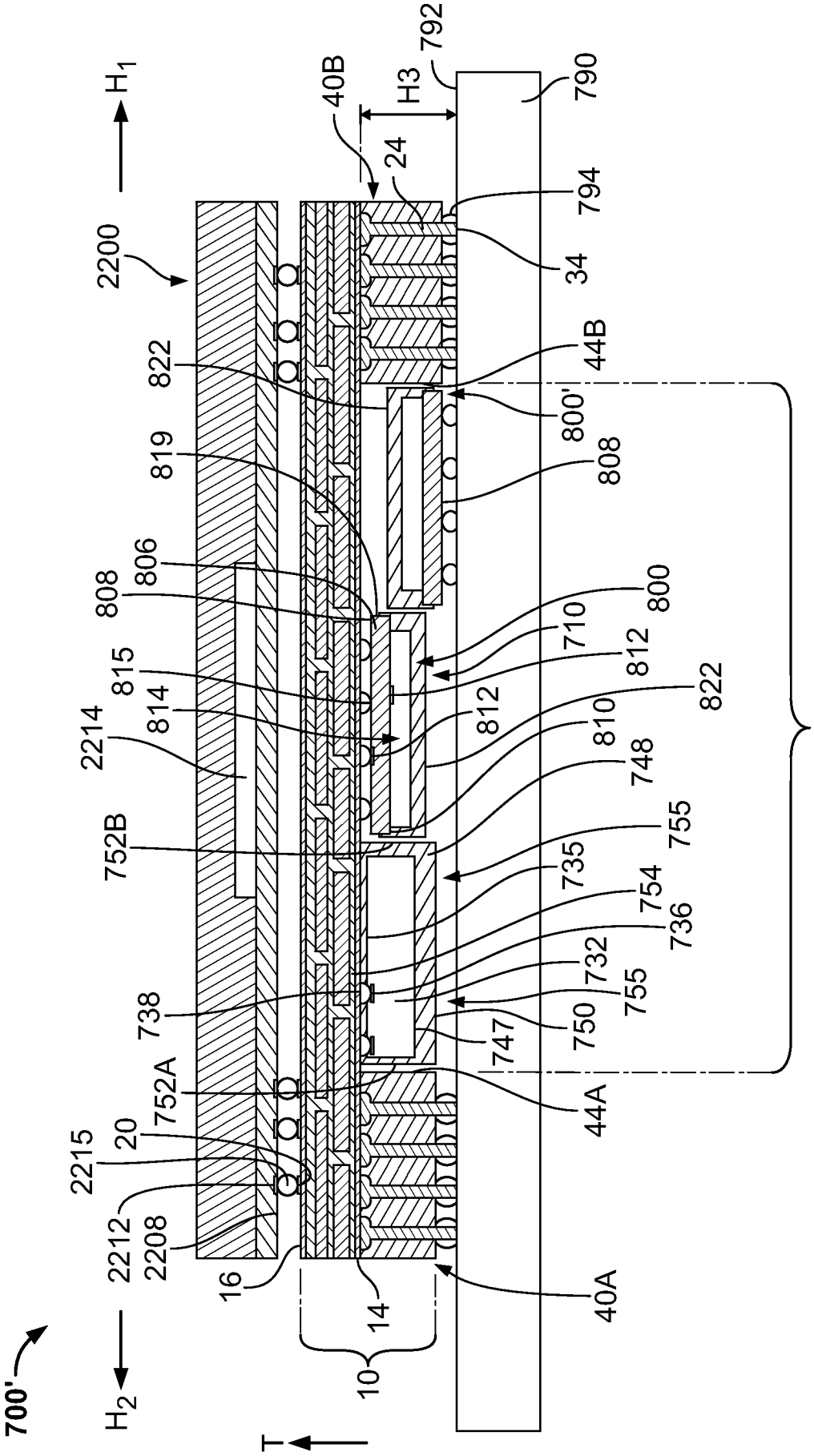

700'
H_1
H_2
T
2200
40B
H3
792
790
24
794
34
44B
822
800'
819
808
806
808
800
710
812
815
814
812
822
2214
810
748
752B
755
735
754
736
732
755
738
750
747
752A
44A
20
2215
2212
2208
16
14
40A
10
712

FIG. 10B

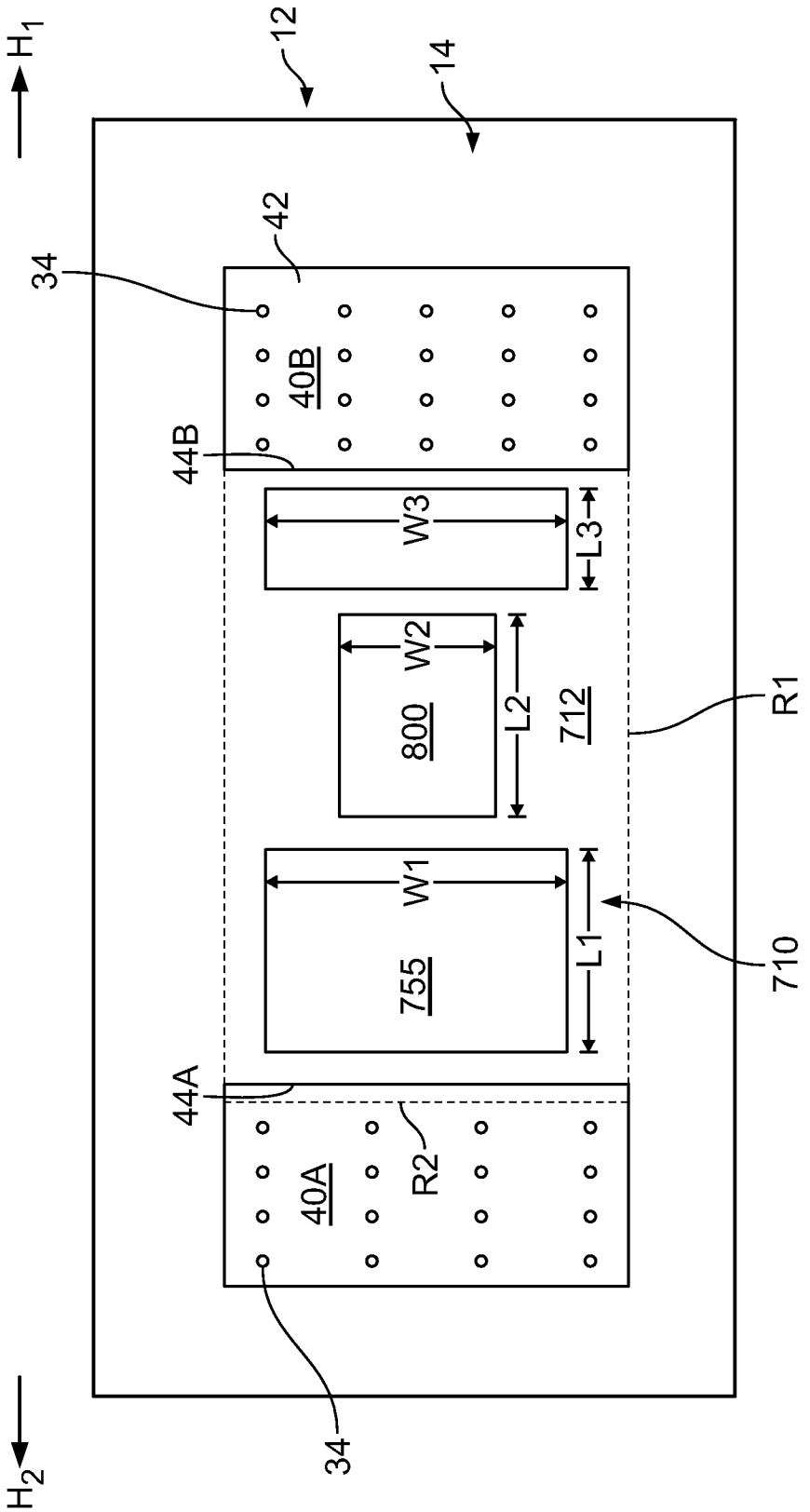

H1
12
14
42
34
40B
44B
W3
L3
W2
800
L2
712
R1
W1
755
L1
710
44A
R2
40A
34
H2

FIG. 11

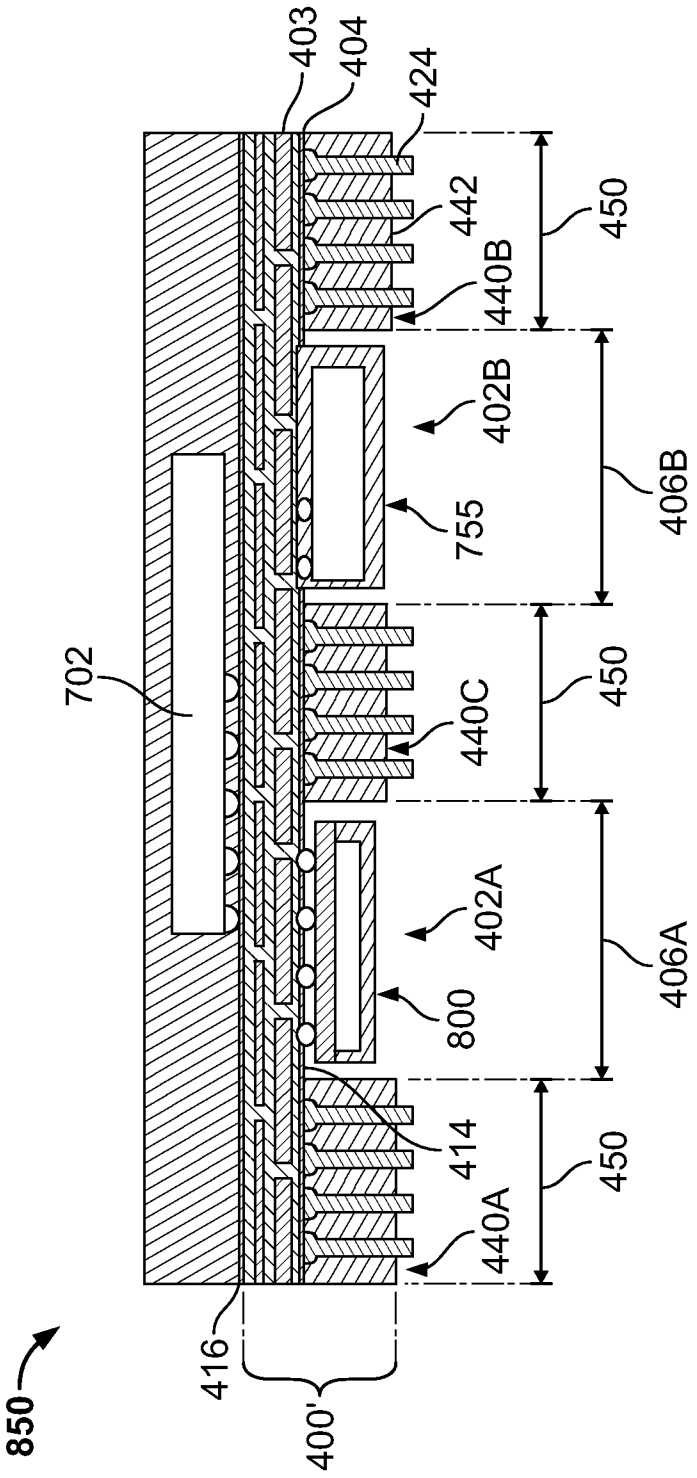

403
404
424
442
450
440B
402B
406B
755
702
450
440C
402A
406A
800
414
450
440A
416
400'
850

FIG. 12

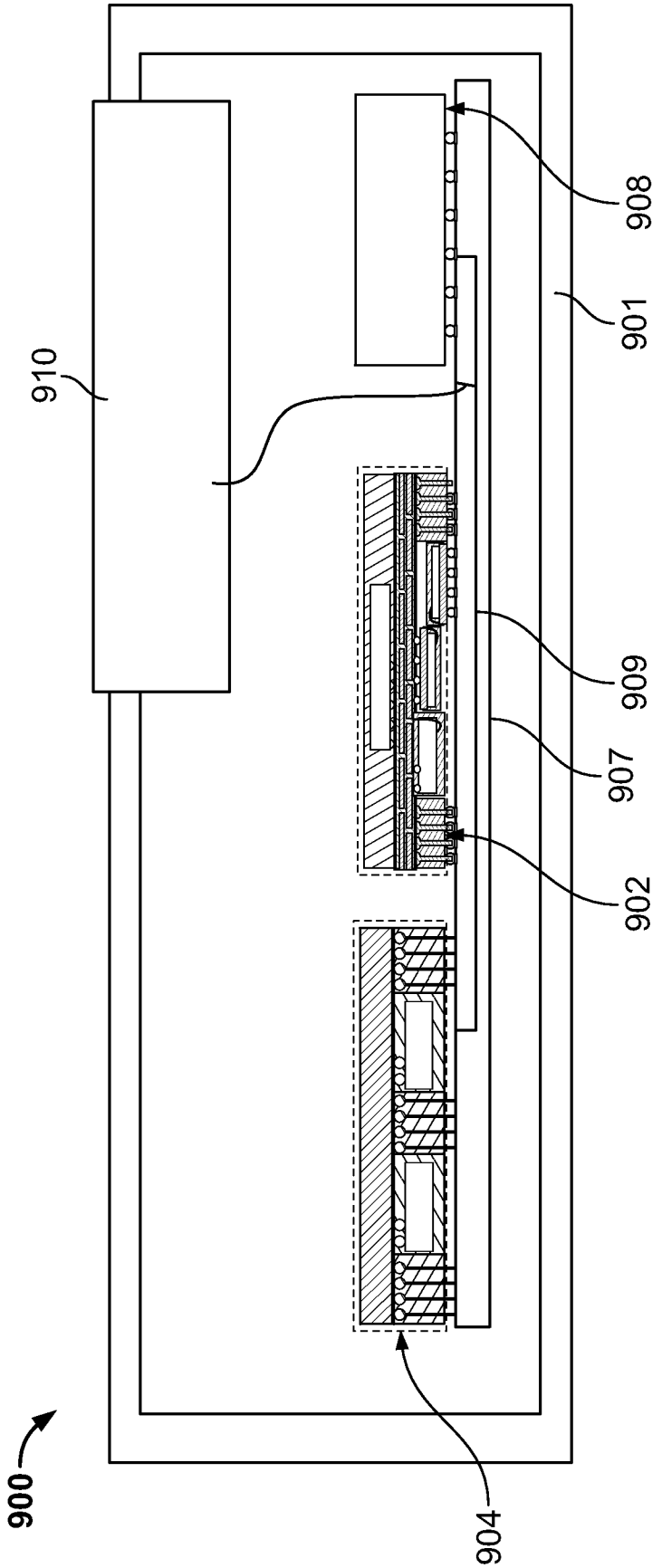
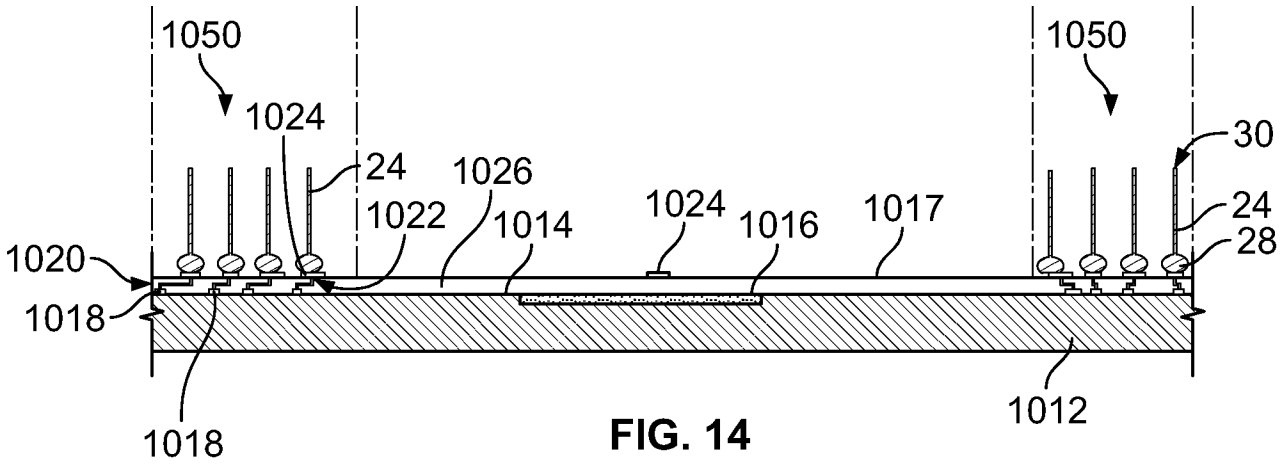


FIG. 13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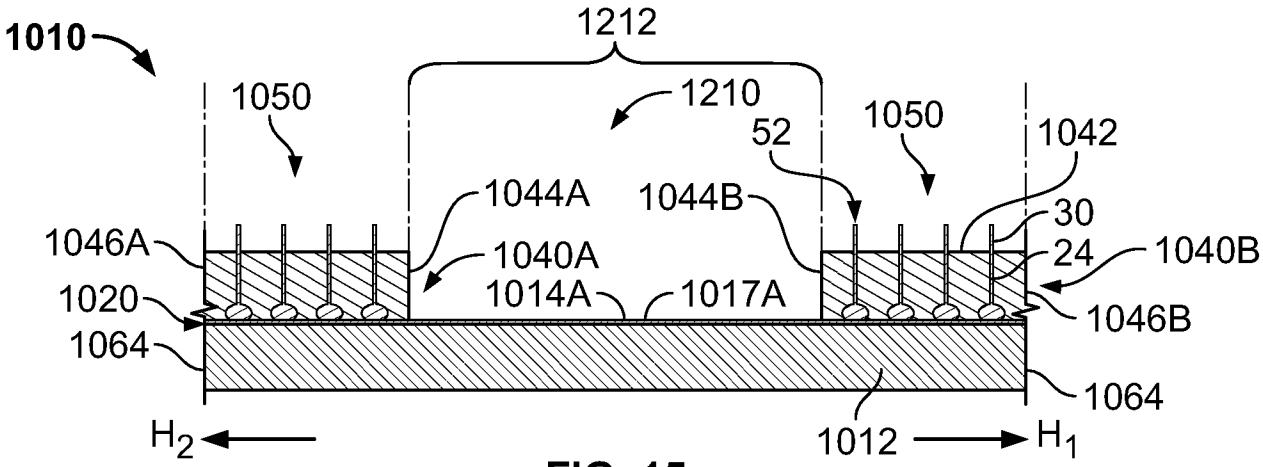
28
1020
1018
1018
1012

FIG. 14


1010
1212
1050
1210
52
1050
1042
1044A
1044B
30
1046A
1040A
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1040B
1020
1014A
1017A
1046B
1064
1064
H2
1012
H1

FIG. 15

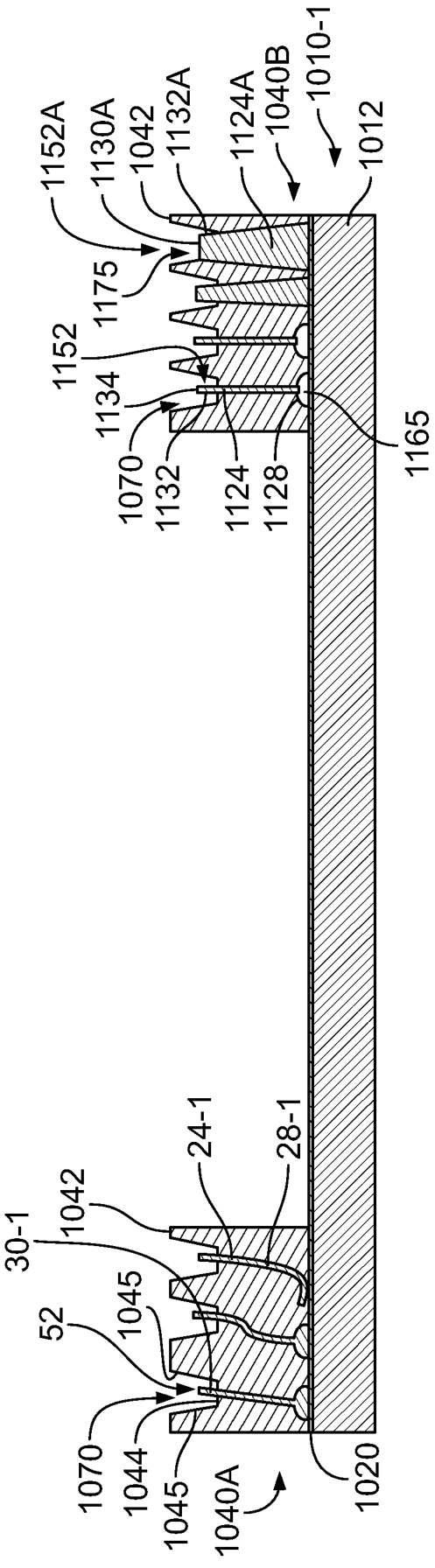


FIG. 16A

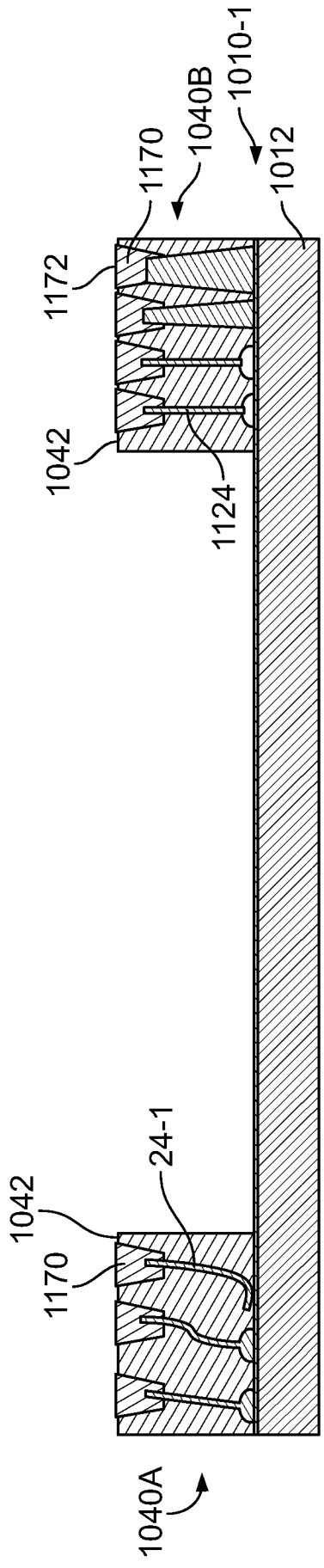


FIG. 16B

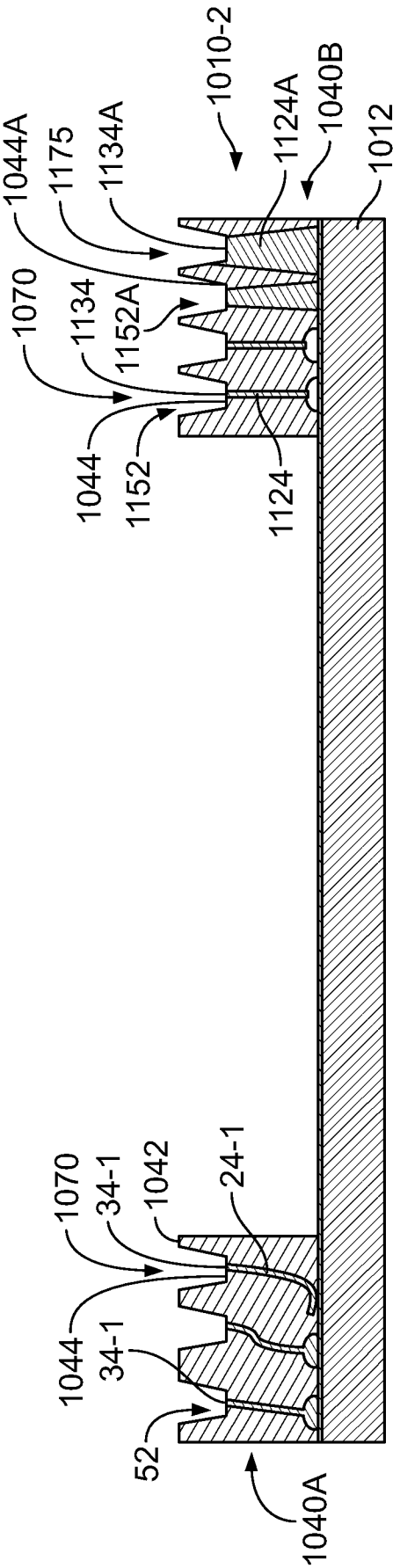


FIG. 16C

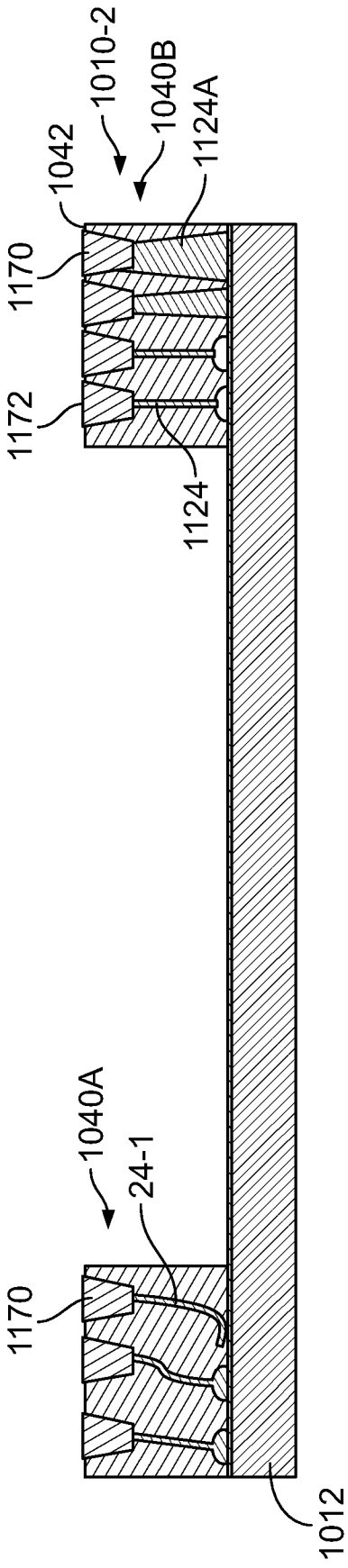
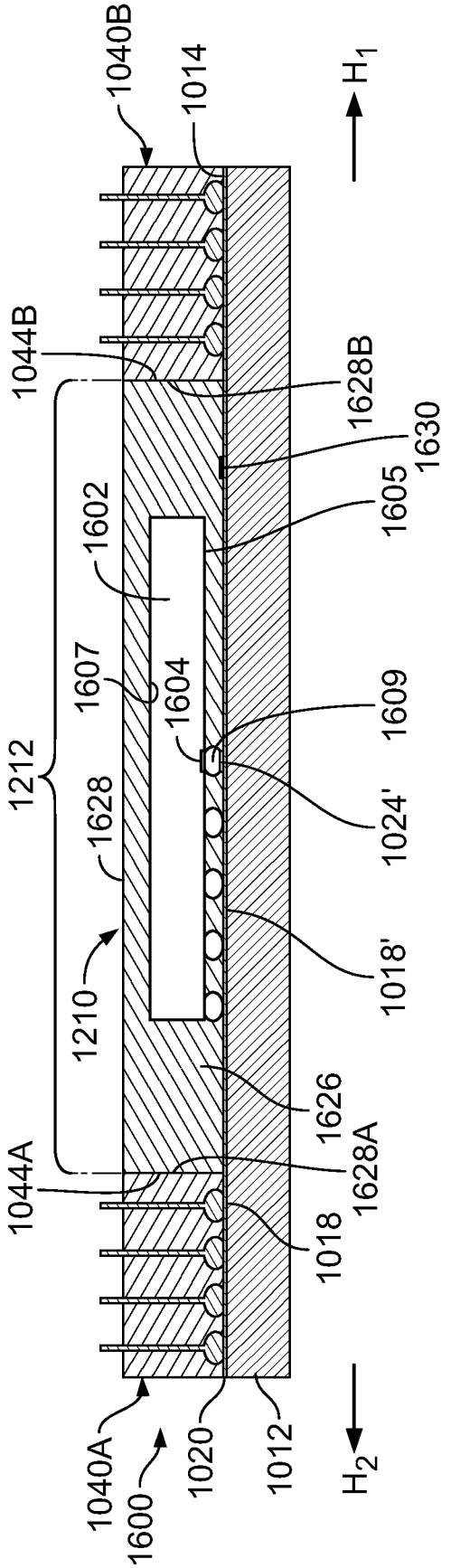


FIG. 16D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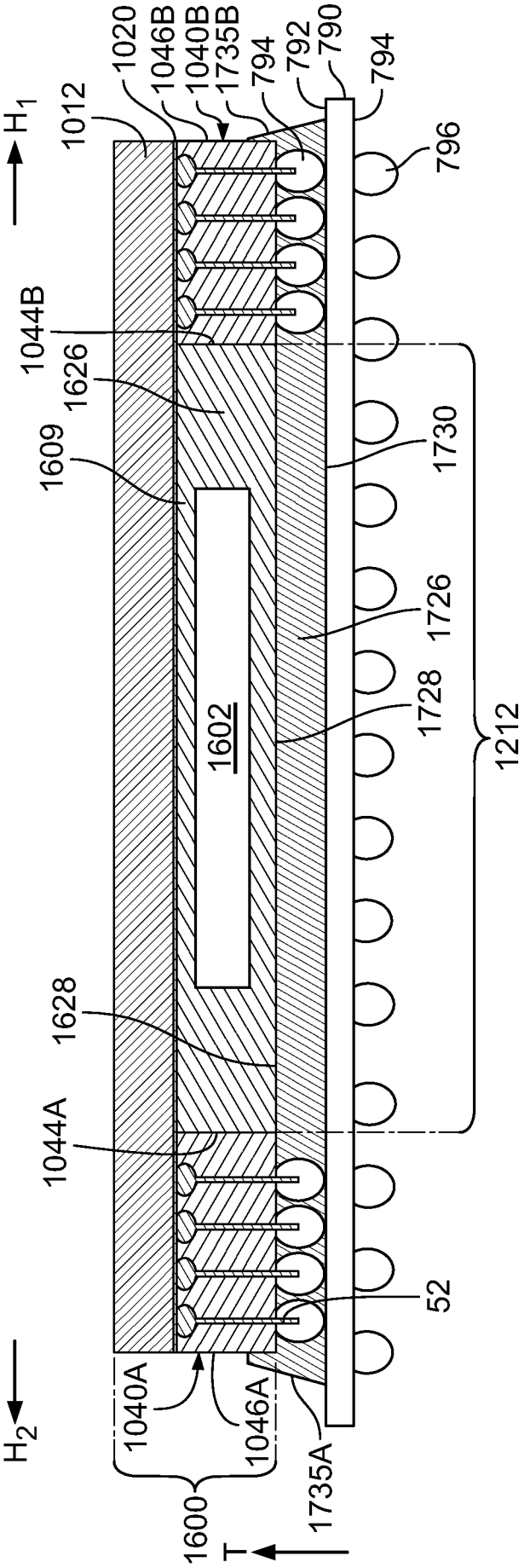
1014
H_1
1044B
1628B
1630
1605
1602
1607
1604
1609
1212
1628
1024'
1210
1018'
1626
1044A
1628A
1018
1040A
1600
1020
1012
H_2

FIG. 17


H1
H2
T
1012
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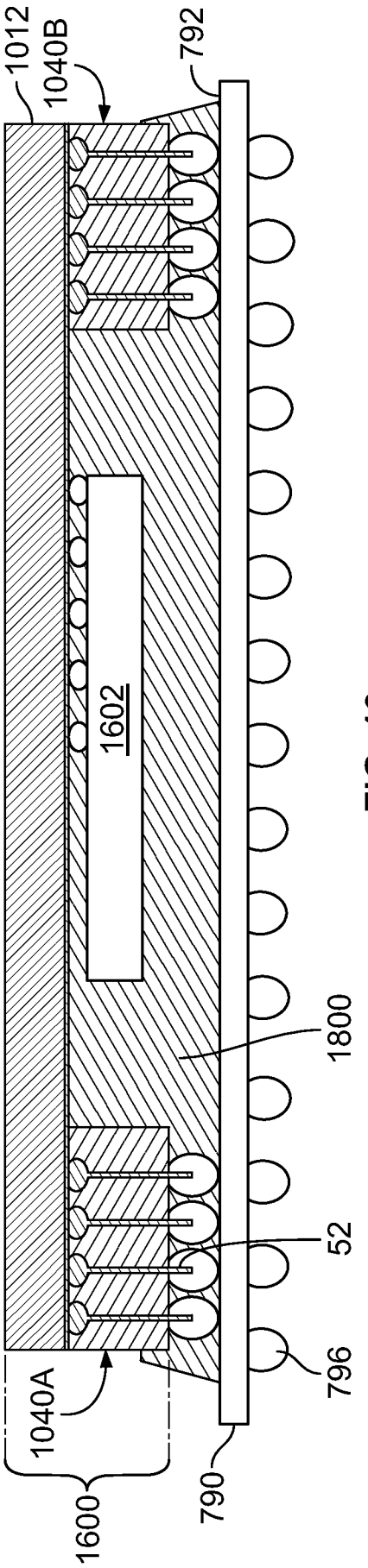
1046B
1040B
1735B
794
792
790
794
796
1044B
1626
1609
1730
1726
1728
1602
1212
1628
1044A
52
1040A
1046A
1735A
1600

FIG. 18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1040B
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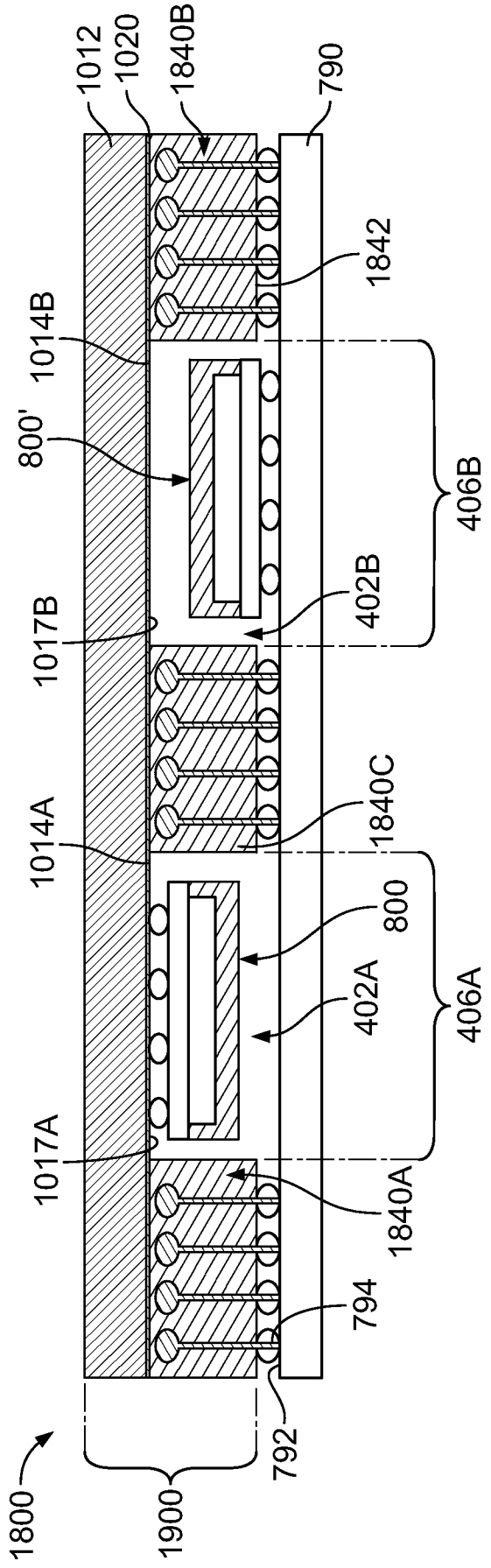
1602
1800
52
796
1040A
1600
790

FIG. 19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790
1842
1014B
800'
406B
402B
1017B
1840C
1014A
800
402A
406A
1017A
1840A
794
792
1800
1900

FIG. 20

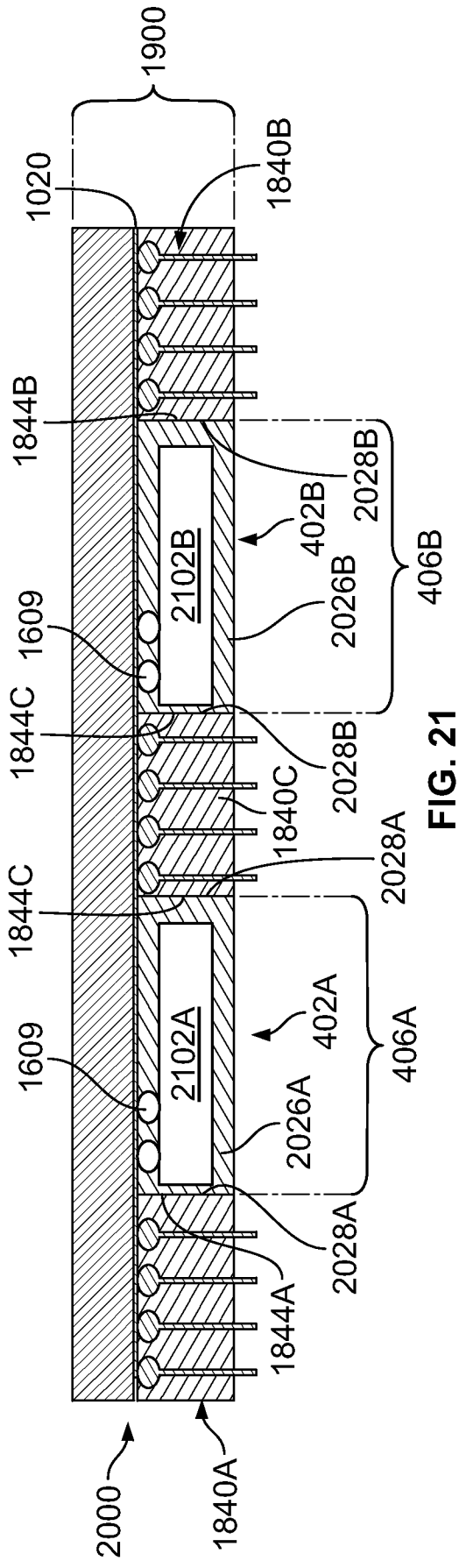
1900
1020
1840B
1844B
2028B
402B
2102B
2026B
406B
1609
1844C
2028B
1840C
2028A
1844C
402A
1609
2102A
2026A
406A
2028A
1844A
2000
1840A

FIG. 21

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/075672

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/498 H01L25/10 H01L25/065 H01L23/00 H01L23/31
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/284001 A1 (MORI KENTARO [JP] ET AL) 20 November 2008 (2008-11-20)	1,16,17, 21-27, 42-44, 47,48
Y	paragraph [0107] - paragraph [0118]; figure 7 paragraph [0195] - paragraph [0202]; figures 18A-18D paragraph [0203] - paragraph [0208]; figures 19A-19D paragraph [0075]; figure 3	1-17, 21-28, 42-48
Y	US 2012/280386 A1 (SATO HIROAKI [JP] ET AL) 8 November 2012 (2012-11-08) the whole document	1-17, 21-28, 42-48

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 February 2014	22/04/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Le Gallo, Thomas

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012/015481 A1 (KIM WOO-JAE [KR]) 19 January 2012 (2012-01-19) paragraph [0067]; figure 9 paragraph [0070] - paragraph [0073]; figures 12-16 -----	46

1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/075672

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-17, 21-28, 42-48

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-17, 21-28, 42-48

   details relating to the first surface side of the substrate in the structure of claim 1 / package of claim 21 an related methods

   ---

2. claims: 18-20, 29-41, 49-52

   structure and package also including conductive elements on the second surface of the substrate as well as bond elements or a microelectronic element connected to some of said conductive elements on the second surface of the substrate and methods of manufacturing thereof.

   ---

3. claims: 53-74

   structure including an active die, bond elements and a dielectric encapsulation element and method of manufacturing thereof

   ---

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/075672

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008284001 A1	20-11-2008	CN 101286484 A	15-10-2008
		JP 5003260 B2	15-08-2012
		JP 2008263121 A	30-10-2008
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US 2012280386 A1	08-11-2012	US 2012280386 A1	08-11-2012
		US 2013203216 A1	08-08-2013
US 2012015481 A1	19-01-2012	KR 20120007839 A	25-01-2012
		US 2012015481 A1	19-01-2012