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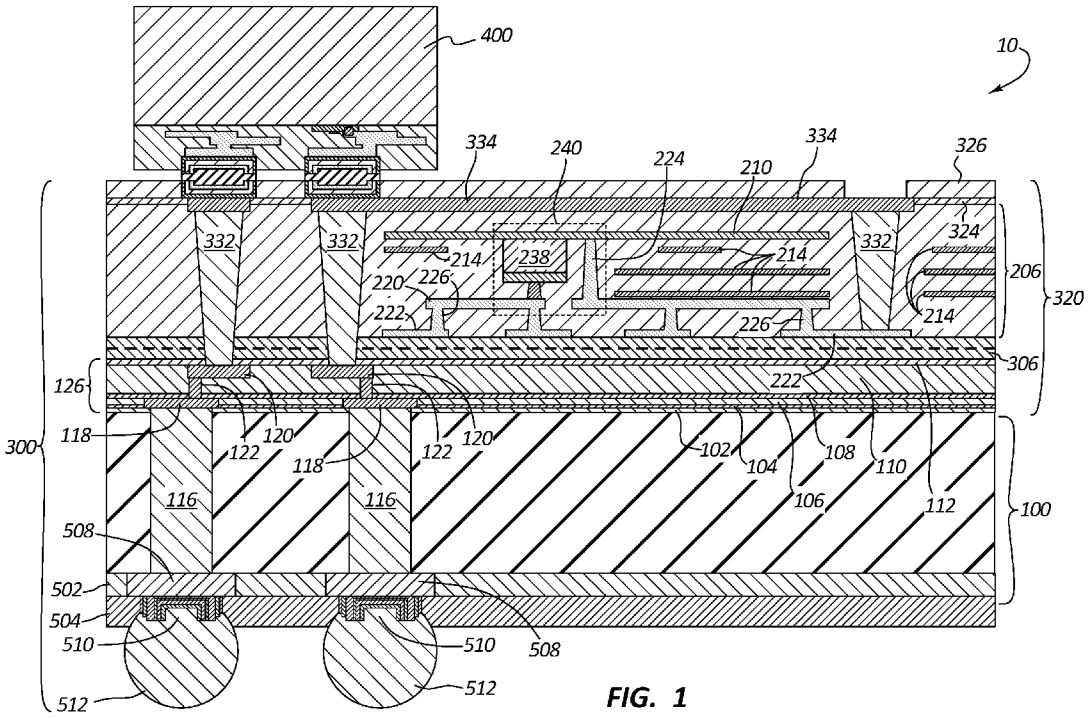

FIG. 1

(57) Abstract: There is set forth herein a method including building an interposer base structure on a first wafer having a first substrate, wherein the building an interposer base structure includes fabricating a plurality of through vias that extend through the first substrate and fabricating within an interposer base dielectric stack formed on the first substrate one or more metallization layer; building a photonics structure on a second wafer having a second substrate, wherein the building a photonics structure includes fabricating within a photonics device dielectric stack formed on the second substrate one or more photonics device; and bonding the photonics structure to the interposer base structure to define an interposer having the interposer base structure and one or more photonics device fabricated within the photonics device dielectric stack.

[Continued on next page]

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WAFER SCALE BONDED ACTIVE PHOTONICS INTERPOSER

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of priority of U.S. Provisional Application No.: 62/490,665 filed April 27, 2017 entitled "Wafer Scale Bonded Active Photonics Interposer" which is incorporated herein by reference in its entirety. This application also claims the benefit of priority of U.S. Non-Provisional Application No. 15/891,847 filed February 8, 2018 entitled "Wafer Scale Bonded Active Photonics Interposer," which is incorporated herein by reference in its entirety. The aforementioned U.S. Non-Provisional Application No. 15/891,847 entitled "Wafer Scale Bonded Active Photonics Interposer" filed February 8, 2018, which is incorporated herein by reference in its entirety, claims the benefit of priority of the aforementioned U.S. Provisional Application No.: 62/490,665 filed April 27, 2017 entitled "Wafer Scale Bonded Active Photonics Interposer" which is incorporated herein by reference in its entirety.

GOVERNMENT RIGHTS STATEMENT

[0002] This invention was made with government support under the Department of Defense (DOD) of the United States, under grant contract number FA8650-15-2-5220. The government may have certain rights in the invention.

FIELD

[0003] The present disclosure relates to photonics generally and specifically to photonics structures and processes for fabrication.

BACKGROUND

[0004] Commercially available photonics integrated circuits are fabricated on wafers, such as bulk silicon or silicon-on-insulator wafers. Commercially available prefabricated photonics integrated circuit chips can include waveguides for transmission of optical signals between different areas of a prefabricated photonics integrated circuit chip. Commercially available waveguides are of rectangular or ridge geometry and are fabricated in silicon (single or polycrystalline) or silicon nitride. Commercially available photonics integrated circuit chips are available on systems having a photonics integrated circuit chip disposed on a printed circuit board.

BRIEF DESCRIPTION

[0005] The shortcomings of the prior art are overcome, and additional advantages are provided, through the provision, in one aspect, of a photonics structure.

[0006] There is set forth herein a method including building an interposer base structure on a first wafer, wherein the building an interposer base structure includes fabricating a plurality of through vias that extend through a substrate and fabricating within an interposer base dielectric stack one or more metallization layer; building a photonics structure on a second wafer, wherein the building a photonics structure includes fabricating within a photonics device dielectric stack one or more photonics device; and bonding the photonics structure to the interposer base structure to define an interposer having the interposer base structure and one or more photonics device. There is set forth herein an optoelectrical system including a substrate; an interposer dielectric stack formed on the substrate, the interposer dielectric stack including a base interposer dielectric stack, and a photonics device dielectric stack, and a bond layer dielectric stack that integrally bonds the photonics device dielectric stack to the base interposer dielectric stack.

[0007] Additional features and advantages are realized through the techniques of the present disclosure.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0008] One or more aspects of the present disclosure are particularly pointed out and distinctly claimed as examples in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the disclosure are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0009] Fig. 1 is a cutaway side view of an optoelectronic system having an interposer that includes an interposer dielectric stack in which there is fabricated and defined one or more photonics device;

[0010] Fig. 2 illustrates an optoelectronic system in an intermediary stage of fabrication after build of an interposer base on a bulk wafer having a wafer substrate;

[0011] Fig. 3 is a cross sectional side view illustrating an optoelectrical system in a partial stage of fabrication after build of a photonics structure having a photonics structure dielectric stack in which there is integrally fabricated and defined one or more photonics device, and wherein the build is performed using a silicon over on insulator (SOI) wafer;

[0012] Fig. 4 is a cross sectional side view illustrating fabrication of an optoelectrical system showing interposer base structure of Fig. 2 being aligned with the photonics structure of Fig. 3;

[0013] Fig. 5 is a cross sectional side view illustrating the photonics structure shown in Fig. 3 being bonded to the interposer base structure of Fig. 2;

[0014] Fig. 6 is a cross sectional side view of an optoelectrical system in a partial stage of fabrication as shown in Fig. 5 after removal of a substrate from a photonics structure;

[0015] Fig. 7 is a cross sectional side view of an optoelectrical system as shown in Fig. 6 in an intermediary stage of fabrication after further patterning to define inter and intra layer vias and metallization layer(s) for connectivity between bonded device layers and to provide electrical connectivity to a backside of a fabricated interposer having an interposer substrate;

[0016] Fig. 8 is a cross sectional side view of the optoelectrical system as shown in Fig. 7 in an intermediary stage of fabrication after further patterning to define under bump metallization formations;

[0017] Fig. 9 illustrates a cross sectional side view of the optoelectrical system as shown in Fig. 8 in an intermediary stage of fabrication after metal solder attachment of an integrated circuit chip to the under bump metallization formations fabricated as shown in Fig. 8;

[0018] Fig. 10 is a cross sectional side view illustrating the optoelectrical system as shown in Fig. 9 in an intermediary stage of fabrication after attachment of a handle wafer to the structure as shown in Fig. 9 using an adhesive, epoxy, or other permanent organic polymer;

[0019] Fig. 11 is a cross sectional side view illustrating the optoelectrical system as shown in Fig. 10 after removal of material of a substrate defining an interposer base;

[0020] Fig. 12 is a cross sectional side view of the optoelectrical system as shown in Fig. 11 after depositing of a dielectric layer;

[0021] Fig. 13 is a cross sectional side view of the optoelectrical system as shown in Fig. 12 in an intermediary stage of fabrication after patterning to define an interposer backside redistribution layer;

[0022] Fig. 14 is a cross sectional side view illustrating the optoelectrical system as shown in Fig. 13 in an intermediary stage of fabrication after depositing of a dielectric layer which can be a dielectric passivation layer; and

[0023] Fig. 15 is a cross sectional side view of the optoelectrical system as shown in Fig. 14 after further patterning to define under bump metallization formations and fabricating solder bumps within the under bump metallization formations.

DETAILED DESCRIPTION

[0024] Aspects of the present disclosure and certain features, advantages, and details thereof, are explained more fully below with reference to the non-limiting examples illustrated in the accompanying drawings. Descriptions of well-known materials, fabrication tools, processing techniques, etc., are omitted so as not to unnecessarily obscure the disclosure in detail. It should be understood, however, that the detailed description and the specific examples, while indicating aspects of the disclosure, are given by way of illustration only, and not by way of limitation. Various substitutions, modifications, additions, and/or arrangements, within the spirit and/or scope of the underlying inventive concepts will be apparent to those skilled in the art from this disclosure.

[0025] In Fig. 1, there is shown an optoelectrical system 10 having an active photonics interposer 300 that can include one or more active photonics device that can convert a photonics signal to an electrical signal. Photonics interposer 300 can include an interposer base defined by substrate 100.

[0026] Interposer 300 can include an interposer base having substrate 100 and interposer base dielectric stack 126. There can be fabricated within interposer base dielectric stack 126 one or more metallization layer e.g. metallization layer 118 metallization layer 122 as well as vertically extending vias 122. The interposer base can support through vias 116 which can extend through a thickness of substrate 100. In one embodiment, through vias 116 can extend through a thickness of substrate 100 by extending entirely (completely) through a thickness of substrate 100. In one embodiment, through vias 116 can extend through a thickness of

substrate 100 by extending partially through a thickness of substrate 100. Substrate 100 can be formed of e.g. silicon, Si, sapphire, or glass. On substrate 100 there can be fabricated a backside redistribution layer 508 for fanning out electrical signals to and from through vias 116.

[0027] Interposer 300 can also include photonics device dielectric stack 206 in which there can be fabricated and defined one or more photonics device e.g. one or more waveguide 210, one or more waveguide 214, and one or more photodetector 240. Photonics device dielectric stack 206 can support one or more through vias 332 which can extend through a thickness of photonics device dielectric stack 206. In one embodiment, through vias 332 can extend through photonics device dielectric stack 206 by extending entirely (completely) through photonics device dielectric stack 206. In one embodiment, through vias 332 can extend through photonics device dielectric stack 206 by extending through bottom and top elevations of one or more photonics device. In one embodiment, through vias 332 can extend through photonics device dielectric stack 202 by extending through bottom and top elevations of a plurality of photonics devices. In one embodiment, through vias 332 can extend through photonics device dielectric stack 206 by extending partially through photonics device dielectric stack 206. There can be fabricated within photonics device dielectric stack 206 one or more metallization layer e.g. metallization layer 220 metallization layer 222 as well as vertically extending vias 226. Metallization layers as set forth herein define horizontally extending wires to carry one or more of control, logic and/or power signals.

[0028] In one aspect vias of through vias 332 extending through photonics device dielectric stack 206 can be associated to respective through vias 116 extending through a thickness of substrate 100. Advantageously through vias 332 can be sized significantly smaller than through vias 116 thus freeing up real estate in photonics device dielectric stack 206, permitting fabrication of additional and/or larger photonics devices in photonics device dielectric stack 206. A through via 116 can be connected to an associated through via 332 by way of a bridge connection. Interposer 300 can include a bond layer 306 that bonds interposer base dielectric stack 126 to photonics device dielectric stack 206. Supported on substrate 100, interposer 300 can include an interposer dielectric stack 320 that includes interposer base dielectric stack 126, bond layer 306, and photonics device dielectric stack 206.

[0029] Interposer 300 as shown in Fig. 1 can feature backside to frontside electrical connectivity e.g. as provided by through vias of a plurality of through vias 116 extending

through base interposer substrate 100 and being associated to respective through vias of a plurality of through vias 332 extending through photonics device dielectric stack 206. Interposer 300 as shown in Fig. 1 can feature backside and frontside wiring, e.g. for horizontal distribution of one or more of control, logic and/or power signals. A backside of interposer 300 can include one or more redistribution layer e.g. redistribution layer 508 defining backside wiring. A frontside of interposer 300 can include one or more metallization layer e.g. metallization layer 334 defining frontside wiring.

[0030] Optoelectrical system 10 can include under bump metallization formations 510 provided in the embodiment shown by pads that are in electrical communication with vertically extending through vias 116 that extend through substrate 100. Solder bumps 512 of interposer 300 can be formed on under bump metallization pads 510.

[0031] Fig. 2 illustrates fabrication of an interposer base structure which can include substrate 100 and interposer base dielectric stack 126. Substrate 100 can support through vias 116 which can be referred to as through silicon vias (TSVs) in the case that substrate 100 is a silicon substrate. Substrate 100 can be provided by a bulk silicon wafer in one embodiment. For formation of through vertically extending through vias 116, substrate 100 can be subject to etching e.g. reactive ion etching (RIE) and the resulting trenches can be filled with conductive material. The structure of Fig. 2 can be patterned to include multiple dielectric layers such as dielectric layers 102, 104, 106, 108, 110, and 112 supported by substrate 100 and defining interposer base dielectric stack 126. Within interposer base dielectric stack 126 there can be patterned multiple metallization layers, such as metallization layer 118 and metallization layer 120.Vertically extending through vias 116 can be fabricated within interposer base dielectric stack 126 to provide electrical connectivity between metallization layers on front and backside of a fabricated photonics interposer 300 as set forth in Fig. 1. In some embodiments, the materials of the different dielectric layers 102, 104, 106, 108, 110, and 112 can be differentiated. For example, dielectric layer 102 can be used as a hardmask for patterning of through vias 116 and can be selected for optimization of its functioning as a hardmask. Dielectric layers such as dielectric layers 104, 108, and 112 can be deposited over respective metallization layers or other conductive material formations and can be selected to inhibit conductive material migration. Remaining dielectric layers such as layers 104 and 106 can be formed of dielectric material other than dielectric material defining remaining dielectric layers of interposer base dielectric stack 126. In one embodiment dielectric layers

104 and 106 can be formed of tetraethyl orthosilicate (TEOS) or other appropriate SiOx derivatives.

[0032] Fig. 3 illustrates fabrication of photonics structure having a photonics dielectric stack 206 in which there can be fabricated and defined one or more photonics device such as one or more waveguide of waveguides 210, one or more waveguide of waveguides 214, or one or more photodetector 240. The photonics structure as shown in Fig. 3 can be fabricated using a silicon on insulator (SOI) wafer. Such SOI wafer can be prefabricated to include an insulator formed on a substrate and a thin silicon layer formed on the insulator. Fig. 3 illustrates remaining elements of a SOI wafer after patterning. Namely, substrate 200 can be the substrate of a SOI wafer, dielectric layer 202 can be the insulator layer of a SOI wafer, and waveguide 210 as shown in Fig. 3 can be defined by a remaining portion of a silicon layer of a SOI wafer after patterning of such layer to define waveguide 210.

[0033] Referring to Fig. 3, one or more dielectric layer 204 can be formed on dielectric layer 204 which in one embodiment can be provided by the insulator layer of a SOI wafer to define photonics device dielectric stack 206. In dielectric stack 206, there can be patterned waveguides formed of different materials. For example, waveguides 210 can be formed of silicon whereas waveguides 214 can be formed of different material such as silicon nitride SiN. Some applications may favor use of silicon waveguides, whereas other applications may favor use of silicon nitride waveguides. The providing of waveguides of different materials can enhance performance and flexibility of the structure shown in Fig. 3. In dielectric stack 206, there can be patterned waveguides formed at different elevations. For example, waveguides 210 which can be formed of silicon can be formed at a first elevation and waveguides 214 which can be formed of nitride can be formed respectively at second, third, and fourth elevations as shown.

[0034] Referring to additional features shown in the intermediary fabrication stage view of Fig. 3 optoelectrical system 10 can include one or more photonics device formed integral with photonics device dielectric stack 206. In some embodiments, material, e.g. monocrystalline silicon, polycrystalline silicon, germanium forming photonics devices such as photodetector 240 can be epitaxially grown. Embodiments herein recognize that while a thick layer of silicon may accommodate epitaxially growing a resulting photonics device may exhibit light losses through the thick silicon layer. In one embodiment, for accommodating epitaxially growth of epitaxially growth material, a structure having seed layer of silicon (a

silicon template) on an insulator can be provided. The seed layer can be a crystalline seed layer. For providing a structure having a seed layer of silicon, a silicon on insulator (SOI) wafer (having a thin layer of oxide on a bulk silicon substrate and a thin layer of silicon on the oxide) can be selected. In one embodiment where an SOI wafer is used for fabrication of interposer 300, substrate 200 can be provided by a bulk silicon substrate of a SOI wafer.

[0035] As shown in the Fig. 3 one or more photonics device fabricated within photonics device dielectric stack 206 can include waveguides 214 defined by waveguiding material layer. In one embodiment, waveguides 214 can be fabricated by depositing material forming a waveguiding material layer, masking and etching to remove unwanted areas of waveguiding material layer and depositing a dielectric layer over the remaining portion of the waveguiding material layer. Waveguiding material layers defining waveguides 214 can include e.g. monocrystalline silicon, polycrystalline silicon, amorphous silicon, silicon nitride, or silicon oxynitride. In one embodiment photonics device dielectric stack 206 can be fabricated to include a silicon on insulator interface at an elevation above and spaced apart from substrate 200. For example, a thick layer of silicon above a top elevation of substrate 200, e.g. epitaxially grown on a substrate 200 where formed of silicon, can be subject to separation by local or non-local implanted oxygen (SIMOX) processing to define a thin silicon layer and buried oxide layer below the thin silicon layer.

[0036] Waveguides fabricated of different materials within photonics device dielectric stack 206 as shown in Fig. 3 can be used for performance of different functions. For example, waveguides formed of silicon might be selected for fabrication of waveguides included in active devices such as photodetectors or modulators. Dielectric waveguides (e.g. formed of silicon nitride) can be adapted for transmission of optical signals to longer distances. Other materials such as amorphous silicon might be selected for applications where a balance of current conduction properties and light conduction properties is emphasized. Patterning of a waveguide can include patterning of material defining the waveguide as well as patterning of material surrounding the waveguide having an index of refraction differentiated from an index of refraction of a material of the waveguide. Patterning of a waveguides 210 and waveguides 214 can include patterning to define different alternative geometries.

[0037] With appropriate fabrication methodologies photonics devices provided by or having waveguides of different waveguiding material can be fabricated at any elevation of photonics device dielectric stack 206. In one embodiment, epitaxially grown photonics

devices can be fabricated at on substrate locations of photonics device dielectric stack 206, and photonics devices formed of deposited materials, e.g. formed of deposited silicon nitride or silicon oxynitride can be formed at an above substrate elevation of photonics device dielectric stack 206. Photonics device dielectric stack 206 can be fabricated to conduct light between elevations by evanescent coupling between waveguides at different elevations.

[0038] Various processes can be performed for modifying a grain structure of a material layer from which various photonics devices can be fabricated. In one embodiment, a material layer can be formed of polycrystalline silicon (polysilicon). In one embodiment, ion implantation can be performed to modify the silicon crystal structure of a material layer. On modification, polysilicon material can be transformed into amorphous polysilicon material. Ion implant species can include one or more of silicon, argon (*e.g.*, Ar or Ar+), xenon (*e.g.*, Xe or Xe+) or germanium. In another aspect, an annealing process, *e.g.*, a recrystallization annealing process can be performed to further improve a grain structure of a material layer. In one embodiment, with or without ion implantation, a material layer can be subject to annealing for modification of a grain structure.

[0039] For enhancing performance of photonics devices integrally formed in photonics device dielectric stack 206, photonics device dielectric stack 206 can include features for reducing coupling between integrally fabricated photonics devices and substrate 200. In one embodiment substrate 200 can include deep trench isolation features in regions of the structure shown in Fig. 3 in which photonics devices are integrally formed.

[0040] Patterned within photonics dielectric stack 206 there can also be metallization layer 220 and metallization layer 222. There can also be patterned vertically extending vias 224 providing electrical communication between metallization layer 220 and waveguide 210. There can also be patterned vertically extending vias 226 providing electrical communication between metallization layer 220 and metallization layer 222. Regarding photodetector 240, photodetector 240 can include formation 230 which can be defined by photon sensitive material disposed in a trench e.g. a germanium filled trench. Photon sensitive material can convert photons into electrons, and accordingly can convert a photon based signal into an electrical based signal. Referring to photodetector 240, the conductive path defined by via 224, can be used for voltage input into waveguide 210. The conductive path having metallization layer 220 above the elevation of formation 238 can be used for electrical signal

detection, wherein an electrical signal can be output based on photonics signal transmittal through waveguide 210 for detection by photodetector 240.

[0041] As set forth herein, photonics device dielectric stack 206 can be patterned to define one or more photonics device so that one or more photonics device is fabricated within dielectric stack 20. One or more layer of photonics dielectric stack 206 can be patterned to define one or more waveguide, e.g., according to waveguides 210 and/or waveguides 214, so that one or more waveguide is integrally fabricated within dielectric stack 206. One or more layer of photonics device dielectric stack 206 can be patterned to define one or more photodetector, e.g. according to photodetector 240, so that one or more photodetector is integrally fabricated within dielectric stack 206. One or more layer of photonics device dielectric stack 206 can be patterned to define one or more grating coupler so that one or more grating coupler is integrally fabricated within dielectric stack 206. One or more layer of photonics device dielectric stack 206 can be patterned to define one or more grating coupler so that one or more grating coupler is integrally fabricated within dielectric stack 206. One or more layer of photonics device dielectric stack 206 can be patterned to define one or more modulator so that one or more modulator is integrally fabricated within dielectric stack 206. One or more layer of photonics device dielectric stack 206 can be patterned to define one or more polarizer so that one or more polarizer is integrally fabricated within dielectric stack 206. One or more layer of photonics device dielectric stack 206 can be patterned to define one or more splitter so that one or more splitter is integrally fabricated within dielectric stack 206. One or more layer of photonics device dielectric stack 206 can be patterned to define one or more resonator so that one or more resonator is integrally fabricated within dielectric stack 206.

[0042] Metallization layer 220 and metallization layer 222 can define horizontally extending wires. Wires defined by metallization layers 220 and 222 can be horizontally extending through areas of photonics device dielectric stack 206. Metallization layers 220 and 222 can be formed generally by depositing one or more interposer material layer to at least top elevation of the respective metallization layer 220 and 222, etching to define trenches for receiving conductive material, filling the cavities with conductive material, and then planarizing to the top elevation of the respective metallization layer 220 and 222. Metallization layers 220 and 222 can also be formed generally by depositing uniform thickness metallization layers, and then masking and etching to remove layer material from

unwanted areas. Metallization layers 220 and 222 can be formed from metal or other conductive material. Horizontally extending wires defined by metallization layer 222 can be electrically connected to one or more vertically extending vias 226 for distribution of one or more of control, logic and/or power signals vertically and horizontally to different areas of photonics device dielectric stack 206 having fabricated therein one or more photonics device. Horizontally extending wires defined by metallization layer 220 can be electrically connected to one or more of vertically extending vias 226 and/or vertically extending via 224 for distribution of one or more of electrical control, logic and/or power signals vertically and horizontally between different areas of photonics device dielectric stack 206. Wires defined by metallization layer 222 can be electrically connected to one or more of vertically extending vias 226 for distribution of one or more of electrical control, logic and/or power signals vertically and horizontally between different areas of photonics device dielectric stack 206.

[0043] In Fig. 4 there is shown the photonics structure built as described in reference to Fig. 3, aligned to the interposer base structure built as described in reference to Fig. 2. Referring to Fig. 4, an oxide bonding thermal process is described. Low temperature oxide fusion bonding can be utilized. Low temperature oxide fusion bonding can be performed at lower temperatures e.g. 300° C or lower. For performance of low temperature oxide fusion bonding, dielectric layers formed of silicon dioxide can be deposited as shown in Fig. 4. Dielectric layer 302 formed of silicon dioxide can be deposited on interposer base dielectric stack 126 and dielectric layer 304 formed of silicon dioxide can be deposited on photonics device dielectric stack 206. Prior to depositing of layers 302 and 304, their respective under surfaces can be polished, e.g. using chemical mechanical planarization (CMP) to define smooth surfaces to facilitate quality contact for promotion activation of van der waals forces The surfaces of layers 302 and 304 after their deposition and smoothing, can be treated to define appropriate surface chemistry to promote bonding between the two layers on an atomic level.

[0044] Referring to Fig. 5, Fig. 5 illustrates bonding between the photonics interposer base structure as shown in Fig. 2 and the photonics structure as shown in Fig. 3. On bonding of the structures using low temperature oxide fusion bonding as set forth in Fig. 4 the respective structures can be integrally formed together and can define a bond layer 306 between interposer base dielectric stack 126 and photonics device dielectric stack 206. Bonding of the

base interposer structure of Fig. 2 and the photonics structure of Fig. 3 and use of dielectric layers 302 and 304 can be completed by an annealing process for annealing of the layers 302 and 304 to form bond layer 306 which in one embodiment can be regarded as a bond dielectric layer and in one embodiment can be provided by a low temperature oxide fusion bond dielectric layer. In one embodiment, substrate 100 can be provided by a substrate of a bulk silicon wafer and substrate 200 can be provided by a substrate of a SOI wafer and in one embodiment each wafer can be provided by a 300 millimeter wafer, a wafer bonder such as a 300 millimeter wafer bonder can be used for completion of bonding of a base interposer structure to a photonics structure as illustrated in Fig. 5.

[0045] Bonding as described in reference to Fig. 5 can be performed with the thicknesses of base interposer substrate 100 (which can be provided by a bulk wafer) and substrate 200 (which can be provided by a SOI wafer substrate) preserved to their full thickness e.g. having a thickness of about 775 microns. Thus, the bonding set forth in reference to Fig. 5 can be performed with low risk of wafer breakage and can be carried out without use of handle wafers.

[0046] Fig. 6 illustrates the optoelectrical system as shown in Fig. 5 after removal of substrate 200 to define in interposer 300 having substrate 100 and interposer dielectric stack 320, which interposer dielectric stack 320 can include interposer base dielectric stack 126, bond layer 306, and photonics device dielectric stack 206. For removal of substrate 200, various processes can be used. For example, a majority of an original thickness of substrate 200 can be eliminated with use of a grinding process which can stop at a predetermined distance e.g. about 10 microns from top elevation of photonics device dielectric stack 206. With a relatively thin e.g. 10 micron thickness portion of substrate 200 remaining, where substrate 200 is formed of silicon. The remaining portion of substrate 200 can be removed e.g. via reactive ion etching (RIE). The reactive ion etching (RIE) can be selective of silicon (where substrate 200 is formed of silicon) so that silicon material of substrate 200 can be removed without removal of dielectric material of photonics device dielectric stack 206.

[0047] Fig. 7 illustrates the optoelectrical system of Fig. 6 after patterning to form vertically extending through vias 332 and metallization layer 334. For fabrication of vertically extending vias 332 and metallization layer 334 dielectric layer 324 can be formed using a damascene fabrication process on photonics device dielectric stack 206. Trench features can be formed in dielectric layer 324 and photonics device dielectric stack 206 using

e.g. reactive ion etching (RIE) that is selective to certain dielectric, polymer masking films, or underlying metal materials so that material is removed by the reactive ion etching (RIE) to form a dimensionally desired feature. The formed trenches can then be filled with conductive material e.g. copper for formation of vertically extending through vias 332 and metallization layer 334. Vertically extending through vias 116 which can extend entirely through or substantially entirely through substrate 100 can be regarded as through vias and can be regarded as through silicon vias (TSVs) where substrate 100 is formed of silicon. Vertically extending through vias 332 which can extend entirely through or substantially entirely through photonics device dielectric stack 206 can be regarded as through vias and can be regarded as through oxide vias (TOVs) where photonics device dielectric stack 206 includes one or more oxide based dielectric layer. Vias 122, vias 224 and vias 226 which can be smaller diametered than through vias 116 or through vias 332 can be regarded as contact vias or in the case that they commence and terminate at elevations within elevations of dielectric stack 126 or 206, intra stack vias.

[0048] Regarding left side through vias 332 as shown in Fig. 3 left side through vias 332 can extend through bond layer 306 and can be electrically connected to metallization layer 140 fabricated in interposer base dielectric stack 126. Regarding left side through vias 332 as shown in Fig. 3 left side through vias 332 can extend from metallization layer 140 fabricated in interposer base dielectric stack 126 through bond layer 306 through a plurality of layers of photonic device dielectric stack 206 and can terminate at metallization layer 334 fabricated at a top layer of photonic device dielectric stack 206. Left side through vias 332 can extend through multiple layers of photonic device dielectric stack 206. Left side through vias 332 can extend through multiple layers of photonic device dielectric stack 206 and thereby can extend through top and bottom elevations of a plurality of photonics devices fabricated at various elevations of the photonic device dielectric stack 206 e.g. through the top and bottom elevations of waveguides 212, photodetector 240 and waveguide 210. Regarding right side through vias 332 as shown in Fig. 3 right side through vias 332 can extend from metallization layer 222 fabricated in photonics device dielectric stack 206 through a plurality of layers of photonic device dielectric stack 206 and can terminate at metallization layer 334 fabricated at a top layer of photonic device dielectric stack 206. Metallization layer 334 which can define a strap (hook) connection in the embodiment as shown in Fig. 7 can provide a conductive path from a backside of interposer 300 e.g. the area below the backside being defined below

substrate 100 as shown in Fig. 7 to any device defined within photonics device dielectric stack 206.

[0049] As shown in the intermediary fabrication stage view of Fig. 7, a conductive path providing a strap (hook) connection can be defined so that an input voltage from a backside of interposer 300 can be input into photodetector 240 by way of the conductive path defined by redistribution layer 508 (backside) connected to through via 116 extending through substrate 100 connected to an associated vertically extending through via 332 extending through photonic device dielectric stack 206 connected metallization layer 334 (frontside) connected to vertically extending through via 332 connected to metallization layer 222 connected to via 226 connected to metallization layer 220 which can provide an input voltage to photodetector 240. A bridge connection that connects vertically extending through via 116 and vertically extending through via 332 can be provided by metallization layer 118 connected to vertically extending through via 116 which connects to via 122 which connects to metallization layer 120 which connects to via vertically extending through via 332. Optoelectrical system 100 can include multiple ones of such bridge connections, e.g. in one embodiment individual through vias 116 of a plurality of vertically extending through via 116 can include respective bridge connections, each respective bridge connection connecting a vertically extending through viae 116 to a respective vertically extending through via 332 extending through photonics device dielectric stack 206. Metallization layer 118, vertically extending via 122, and metallization layer 120 can be fabricated and defined integrally with interposer base dielectric stack 126. Where through vias 332 extend through the bottom and top elevations of one or more photonics device e.g. a waveguide 214 a waveguide 210 or a photodetector 240 as shown in Fig. 7 through vias 332 can be regarded as photonics structure through vias.

[0050] Referring to photonics device dielectric stack 206, dielectric layers defining stack 206 can include differentiated materials. For example, layer 202 can be provided by the thermal oxide layer of a starting SOI wafer as set forth herein. Dielectric layers of photonics device dielectric stack 206 can be selected for optimization of waveguide performance e.g. in one embodiment, cladding layers around waveguides can be provided by silane oxide. Dielectric layers of photonics device dielectric stack 206 that are deposited on metallization layers can be selected to resist migration of conductive material. Remaining layers of

photonics device dielectric stack 206 can be formed of such material such as e.g. tetraethyl orthosilicate (TEOS) or other appropriate SiOx derivatives.

[0051] Fig. 8 illustrates the optoelectrical system 10 of Fig. 7 after patterning to define under bump metallization formations 336. Under bump metallization formations 336 provided by pads in the embodiment shown can be fabricated by way of a process including depositing of dielectric layer 326, and further patterning to define under bump metallization formations 336. In a stage depicted in Fig. 8 interposer dielectric stack 320 encompasses dielectric layer 326, which in one embodiment can be formed of TEOS.

[0052] Fig. 9 illustrates optoelectrical system 10 after attachment of integrated circuit chip 400, which in one embodiment can be provided by a CMOS logic chip. CMOS logic chip 400 can include under bump metallization formations corresponding to metallization formations 336 as set forth in reference to Fig. 8. Integrated circuit chip 400 can be attached to under bump metallization formations 336 by way of flip chip bonding of integrated circuit chip 400 to under bump metallization formations 336 which formations 336 can be fabricated using dielectric layer 326. Attachment of integrated circuit chip 400 can be supplemented by applying an epoxy underfill (not shown) at an interface between integrated circuit chip 400 and dielectric layer 326.

[0053] Fig. 10 illustrates the optoelectrical system 10 as shown in Fig. 9 after attachment of a handle wafer 420. Handle wafer 420 can be attached to the structure shown in Fig. 9 using an adhesive layer 410. An adhesive layer 410 can be distributed about integrated circuit chip 400 and on dielectric layer 326 as shown in Fig. 10 and handle wafer 420 can be adhered to adhesive layer 410. Handle wafer 420 permits fabrication of additional features on a backside of interposer 300 after substrate 100 is thinned and is no longer able to provide structural integrity for support of the attached device layers. Fabricating processes in one embodiment are described further in reference to Fig. 11. Adhesive layer 410 can be a permanent adhesive or a temporary adhesive. Where adhesive layer 410 is a permanent adhesive layer 410 adhesive layer 410 can remain adhered to dielectric layer 326 through to completion of a fabricated interposer 300 as shown in Fig. 1.

[0054] Fig. 11 illustrates the optoelectrical system 10 as shown in Fig. 10 with additional processing to define interposer backside features. Referring to Fig. 11, material of base interposer substrate 100 can be removed to reveal a portion of vertically extending through

vias 116, which vertically extending through vias 116 prior to the reveal depicted in Fig. 11 terminate within substrate 100. Removal of material of substrate 100 can be performed e.g. by way of grinding to a predetermined elevation above a designated final elevation and then further removal can be performed using reactive ion etching (RIE) which can be selective to the material of substrate 100 so that the material of substrate 100 is selectively removed.

[0055] Fig. 12 illustrates the optoelectrical system 10 as shown in Fig. 11 after depositing of dielectric layer 502 which in one embodiment can be formed of TEOS. Dielectric layer 502 can be deposited and then planarized to define a smooth surface as shown in Fig. 12.

[0056] Fig. 13 illustrates the optoelectrical system 10 as shown in Fig. 12 after further patterning to fabricate a conductive backside redistribution layer 508. Redistribution layer 508 which can define horizontally extending redistribution wiring can be provided to fan out the contacts defined by vertically extending through vias 116. Redistribution layer 508 can be fabricated by using a damascene process, e.g., by etching of dielectric layer 502 using RIE selective to material of dielectric layer 502 to selectively remove material of dielectric layer 502 and then filling a defined trench with conductive material that defines redistribution layer 508. Referring to Figs. 11-13 substrate 100 can be grinded to reveal conductive material of through vias 116 and additional patterning can be performed for formation of redistribution layer 508 (Fig. 13). For example a dielectric layer 502 can be deposited on substrate 100 after grinding of substrate planarized to a bottom elevation of through vias 116 in the stage shown in Fig. 12, followed by depositing of redistribution layer 508, masking and etching to remove unwanted material of redistribution layer 508 to define redistribution layer wiring. In one embodiment, a photoresist stencil can be applied and filled with conductive material for formation of redistribution layer 508.

[0057] Fig. 14 illustrates optoelectrical system 10 as shown in Fig. 13 after depositing a dielectric layer 504 which can be a dielectric passivation layer and then patterning of dielectric layer 504 to define trenches to expose redistribution layer 508 in preparation for, and facilitating the selective application under bump metallization pads. Referring to Fig. 14 there is illustrated depositing of dielectric layer 504, then recessing that dielectric layer 504 in areas for accommodated of under bump metallization formations provided by under bump metallization pads as are set forth in Fig. 15.

[0058] Fig. 15 illustrates the optoelectrical system 10 as shown in Fig. 14 after further patterning to define under bump metallization formation 510 specifically in exposed areas of dielectric layer 504 to provide electrical connectivity to redistribution layer 508. On fabrication of under bump metallization formations 510 solder bumps 512 can be formed within respective under bump metallization formations 510.

[0059] For the fabrication of the fabricated interposer 300 as shown in Fig. 1, an interposer base structure (Fig. 2) can be separately fabricated relative to a photonics structure (Fig. 3). The interposer base structure can be fabricated using a first wafer having a first substrate 100 and a photonics structure (Fig. 3) can be fabricated using a second wafer having a second substrate 200. After separate fabrication of an interposer base structure (Fig. 2) and a photonics structure (Fig. 3), the two wafer built structures can be bonded together using a low temperature oxide fusion bonding process. On the performing of a low temperature oxide bond process a bond layer 306 can be defined between an interposer base structure and a photonics structure, and specifically in one embodiment between an interposer base dielectric stack 126 and a photonic device dielectric stack 206. The resulting interposer 300 as shown in Fig. 1 resulting after further fabrication processing, can feature backside to frontside electrical connectivity e.g. as provided by through vias 116 extending through base interposer substrate 100 being associated to respective through vias 332 extending through photonics device dielectric stack 206.

[0060] The optoelectrical system 10 as shown in Fig. 1 having interposer 300 can be connected to an understructure e.g. by way of connection of solder bumps 512 of interposer 300 to UBM formations of the understructure (not shown). The understructure to which the optoelectrical system 10 of Fig. 1 can be attached can be provided e.g. by a printed circuit board or can alternatively be provided e.g. by a ball grid array or an interposer.

[0061] In an alternative embodiment, interposer 300 can be entirely fabricated using a single wafer. For example a structure having the components of an interposer base structure as shown in Fig. 2 can be fabricated. Then, a structure having one or more photonics device components can be built on top of the structure as shown in Fig. 2. Finally, large scale through vias can be fabricated to extend through an interposer having photonics features e.g. one or more photonics device to provide backside to frontside electrical connectivity. While the described alternative approach can feature advantages, embodiment herein recognize problems with the approach of the described alternative embodiment. For example, large

scale through vias which would extend through a base interposer substrate such as substrate 100 and through elevations of photonics devices according to the alternative embodiment would be expected to consume significant real estate of a photonics device build area thereby limiting a number and size of photonics devices that can be fabricated.

[0062] In one aspect as set forth herein referring to Fig. 1, vertically extending through vias 332 which can be provided as photonics structure through vias can be proportioned to have sizes in one embodiment that are a fraction of the size of corresponding vertically extending through vias 116 extending though base interposer substrate 100. In one embodiment vertically extending through vias 332 which can be provided as photonics structure through vias can be proportioned to have a size that is 0.5 or less the size of corresponding through vias 116 extending though base interposer substrate 100. In one embodiment, vertically extending through vias 332 which can be provided as photonics structure through vias can be proportioned to have a size that is 0.25 or less the size of corresponding through vias 116 extending though base interposer substrate 100. In one embodiment, vertically extending through vias 332 which can be provided as photonics structure through vias can be proportioned to have a size that is 0.10 or less the size of corresponding through vias 116 extending though base interposer substrate 100. Size as set forth hereinabove in this paragraph refers to one or more of a diameter, a height, or a volume.

[0063] In one example, through vias 332 can have dimensions of about 1.0 microns diameter by 7.0 microns height and through vias 116 can have dimensions of about 10 micron diameter by 100 microns height. In one embodiment vertically extending through vias 116 and vertically extending through via 332 can be differently dimensioned but can have common aspect ratios, e.g. each can have a 10x1 aspect ratio, e.g. vertically extending through vias 332 can be sized to a dimensions of about 0.7 microns x 7.0 microns and vertically extending through vias 116 can be sized to dimensions of about 10.0 microns x 100 microns. Providing through vias 332 to be dimensionally smaller facilitates fabrication of additional and larger scale photonics devices within photonics device dielectric stack 206. Providing through vias 332 to carry one or more of control, logic and/or power signals rather than contact vias such a vias 226 can help avoid various electrical problems such as involving unwanted voltage drops and stray capacitance generation.

[0064] Fabrication methods set forth herein can facilitate providing of sets of interposers 300 having differentiated substrates. Using methods herein a first set of one or more

interposers can be fabricated having substrates of a first material and a second set of one or more interposers can fabricated having substrates. There is set forth herein building an interposer base structure on a first wafer defining a first substrate; building a photonics structure on a second wafer defining a second substrate; and bonding the photonics structure to the interposer base structure to define an interposer having the interposer base structure and one or more photonics device fabricated within the photonics device dielectric stack. In one embodiment the method can be modified so that the building interposer base structure can be repeated to build a second base structure using a second first wafer having a substrate of a material different from a substrate material of the first wafer. The method can be further modified by repeating the building a photonics structure to build a second photonics structure using an additional second wafer. The method can be further modified by bonding the second photonics structure to the second base interposer structure.

[0065] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting. As used herein, the singular forms “a,” “an,” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprise” (and any form of comprise, such as “comprises” and “comprising”), “have” (and any form of have, such as “has” and “having”), “include” (and any form of include, such as “includes” and “including”), and “contain” (and any form contain, such as “contains” and “containing”) are open-ended linking verbs. As a result, a method or device that “comprises,” “has,” “includes,” or “contains” one or more steps or elements possesses those one or more steps or elements, but is not limited to possessing only those one or more steps or elements. Likewise, a step of a method or an element of a device that “comprises,” “has,” “includes,” or “contains” one or more features possesses those one or more features, but is not limited to possessing only those one or more features. Forms of the term "defined by" encompass relationships where an element is partially defined by as well relationships where an element is entirely defined by. Numerical identifiers herein, e.g. "first" and "second" are arbitrary terms to designate different elements without designating an ordering of elements. Furthermore, a system method or apparatus that is configured in a certain way is configured in at least that way, but may also be configured in ways that are not listed. Furthermore, a system method or apparatus set forth as having a certain number of elements can be practiced with less than or greater than the certain number of elements.

[0066] The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below, if any, are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiment was chosen and described in order to best explain the principles of one or more aspects of the invention and the practical application, and to enable others of ordinary skill in the art to understand one or more aspects of the invention for various embodiments with various modifications as are suited to the particular use contemplated.

* * * * *

CLAIMS

What is claimed is:

1. A method comprising:

building an interposer base structure on a first wafer having a first substrate, wherein the building an interposer base structure includes fabricating a plurality of through vias that extend through the first substrate and fabricating within an interposer base dielectric stack formed on the first substrate one or more metallization layer;

building a photonics structure on a second wafer having a second substrate, wherein the building a photonics structure includes fabricating within a photonics device dielectric stack formed on the second substrate one or more photonics device; and

bonding the photonics structure to the interposer base structure to define an interposer having the interposer base structure and one or more photonics device fabricated within the photonics device dielectric stack.

2. The method of claim 1, wherein the bonding includes using a low temperature oxide bond process.

3. The method of claim 1, wherein the bonding includes using a low temperature oxide fusion bond process that includes a polishing stage, an activation stage and an anneal stage.

4. The method of claim 1, wherein the first wafer is a wafer with semiconducting or insulating properties.

5. The method of claim 1, wherein the second wafer is a silicon on insulator (SOI) wafer.

6. The method of claim 1, wherein the first wafer is a bulk silicon wafer and wherein the second wafer is a SOI wafer.

7. The method of claim 1, wherein the method includes subsequent to the bonding removing material from the first substrate to reveal through vias of the plurality of through vias so that the through vias extend entirely through the first substrate.

8. The method of claim 1, wherein the fabricating a plurality of through vias that extend through the first substrate includes performing the fabricating so that though vias of the plurality of through vias to extend to such depth within the first substrate so that the through vias extend entirely through the first substrate on performing removal of material of the first substrate to reveal the plurality of through vias.

9. The method of claim 1, wherein the building a photonics structure on a second wafer includes fabricating within a photonics device dielectric stack one or more photonics device selected from the group consisting of a waveguide and a photodetector.

10. The method of claim 1, wherein the building a photonics structure on a second wafer includes fabricating within a photonics device a first waveguide of a first material and a second waveguide of a second material.

11. The method of claim 1, wherein the building a photonics structure on a second wafer includes fabricating within a photonics device dielectric stack one or more photonics device selected from the group consisting of a waveguide, a photodetector, a grating coupler, a modulator, a polarizer, a splitter, and a resonator.

12. The method of claim 1, wherein the building a photonics structure on a second wafer includes fabricating within a photonics device dielectric stack a first waveguide of a first material and a second waveguide of a second material, wherein the building a photonics structure on a second wafer includes fabricating within a photonics device dielectric stack the first waveguide at a first elevation, and the second waveguide at a second elevation.

13. The method of claim 1, wherein the method includes forming a plurality of photonics structure through vias through the photonics device dielectric stack.

14. The method of claim 1, wherein the method includes forming a plurality of photonics structure through vias through the photonics device dielectric stack, and connecting photonics structure through vias of the plurality of photonics structure through vias to through vias of the plurality of through vias using respective bridge connections, the

respective bridge connections having features defined within the interposer base dielectric stack.

15. The method of claim 1, wherein the building a photonics structure on a second wafer includes fabricating within a photonics device dielectric stack a first waveguide of a first material and a second waveguide of a second material, wherein the building a photonics structure on a second wafer includes fabricating within a photonics device dielectric stack the first waveguide at a first elevation, and the second waveguide at a second elevation, and wherein the building a photonics structure on a second wafer includes fabricating within the photonics device dielectric stack a photodetector including light sensitive material.

16. The method of claim 1, wherein the method includes repeating the building an interposer base structure on a first wafer to build a second interposer base structure using a second first wafer having a substrate of a material different from a substrate material of the first wafer; repeating the building a photonics structure to build a second photonics structure using an additional second wafer, and bonding the second photonics structure to the second base interposer structure.

17. An optoelectrical system comprising:

a substrate;

an interposer dielectric stack formed on the substrate, the interposer dielectric stack including a base interposer dielectric stack, a photonics device dielectric stack, and a bond layer that integrally bonds the photonics device dielectric stack to the base interposer dielectric stack;

one or more through vias extending through the substrate;

one or more metallization layer fabricated in the base interposer dielectric stack; and

one or more photonics device fabricated in the photonics device dielectric stack.

18. The optoelectrical system of claim 17, wherein the one or more photonics device includes a waveguide.

19. The optoelectrical system of claim 17, wherein the one or more photonics device includes a photodetector.

20. The optoelectrical system of claim 17, wherein the one or more photonics device includes first waveguide formed of a first material and a second waveguide formed of a second material.

21. The optoelectrical system of claim 17, wherein the one or more photonics device includes a first waveguide formed at a first elevation, a second waveguide formed at a second elevation.

22. The optoelectrical system of claim 17, wherein the one or more photonics device includes first waveguide formed of a first material at a first elevation and a second waveguide formed of a second material at a second elevation.

23. The optoelectrical system of claim 17, wherein the substrate is formed of a semiconductor or insulating substrate.

24. The optoelectrical system of claim 17, wherein the optoelectrical system includes a backside metal redistribution layer formed on the substrate.

25. The optoelectrical system of claim 17, wherein the optoelectrical system wherein the optoelectrical system includes frontside formations formed above an elevation of the photonics dielectric stack, the frontside formations receiving a CMOS logic integrated circuit chip.

26. The optoelectrical system of claim 17, wherein the optoelectrical system includes backside formations formed on a backside of the interposer, the backside formations facilitating solder bonding of said interposer to an understructure selected from the group consisting of a ball grid array, a printed circuit board, and an interposer.

27. The optoelectrical system of claim 17, wherein the optoelectrical system includes a conductive path providing a strap connection, the strap connection defined by a conductive path including a redistribution layer connected to a through via extending

through the substrate, which through via is connected to an associated first vertically extending photonics structure through via extending through the photonic device dielectric stack, which first vertically extending photonics structure through via is connected to a first metallization layer, which first metallization layer is connected to a second vertically extending photonics structure through via, which second vertically extending photonics structure through via is connected to a second metallization layer, wherein the second metallization layer is at a lower elevation than the first metallization layer.

28. The optoelectrical system of claim 17, wherein a through via of the one or more through via is connected to an associated vertically extending photonics structure through via, the vertically extending photonics structure through via extending through the photonics device dielectric stack.

29. The optoelectrical system of claim 17, wherein a through via of the one or more through via is connected by a bridge connection to an associated vertically extending photonics structure through via, the vertically extending photonics structure through via extending through the photonics device dielectric stack.

30. The optoelectrical system of claim 17, wherein a through via of the one or more through via is connected by a bridge connection to an associated vertically extending photonics structure through via, the vertically extending photonics structure through via extending through the photonics device dielectric stack, the bridge connection having features fabricated in the base interposer dielectric stack, and wherein the vertically extending photonics structure through via is 0.5 times the size of the through via or smaller.

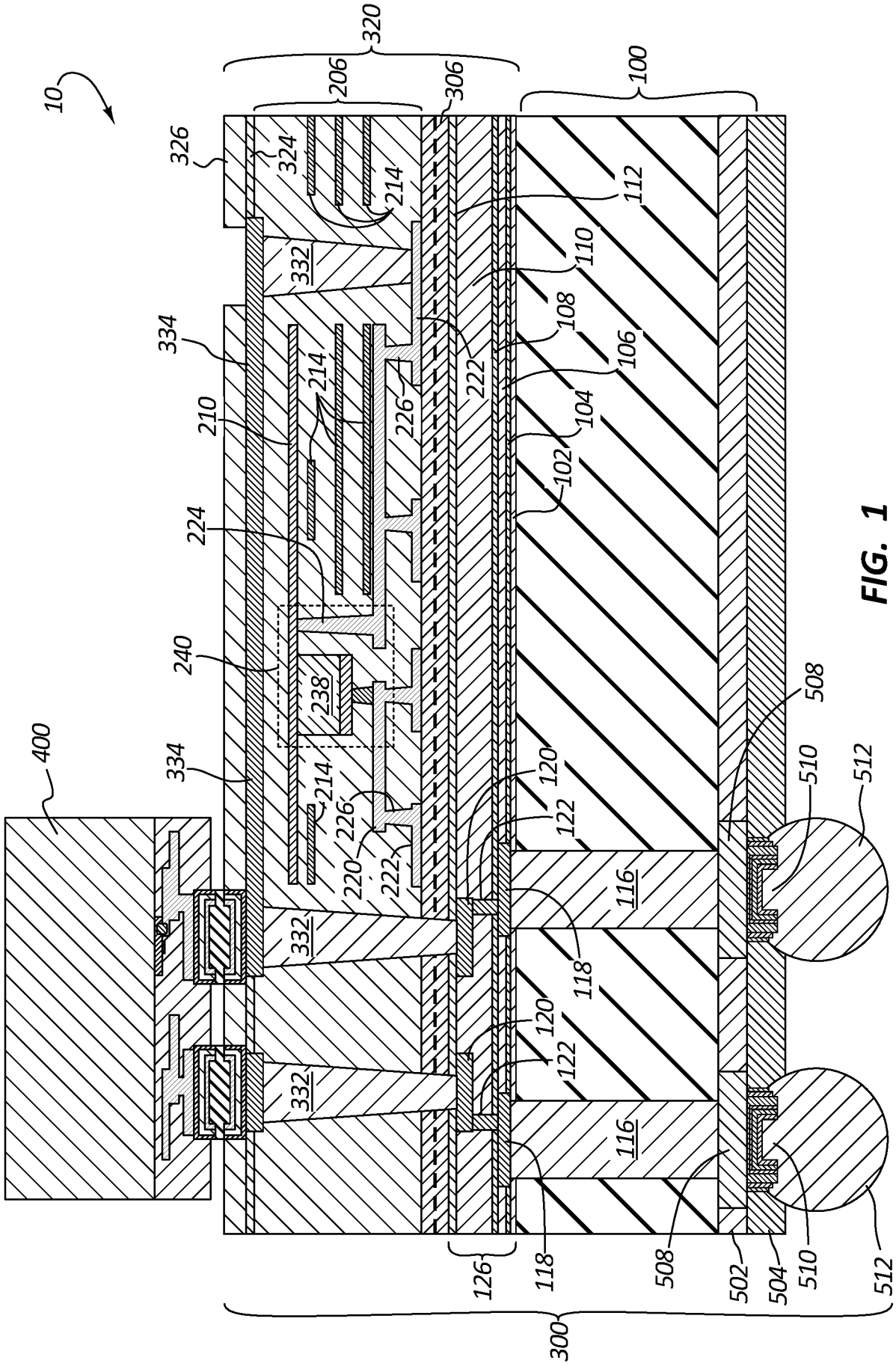
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FIG. 1

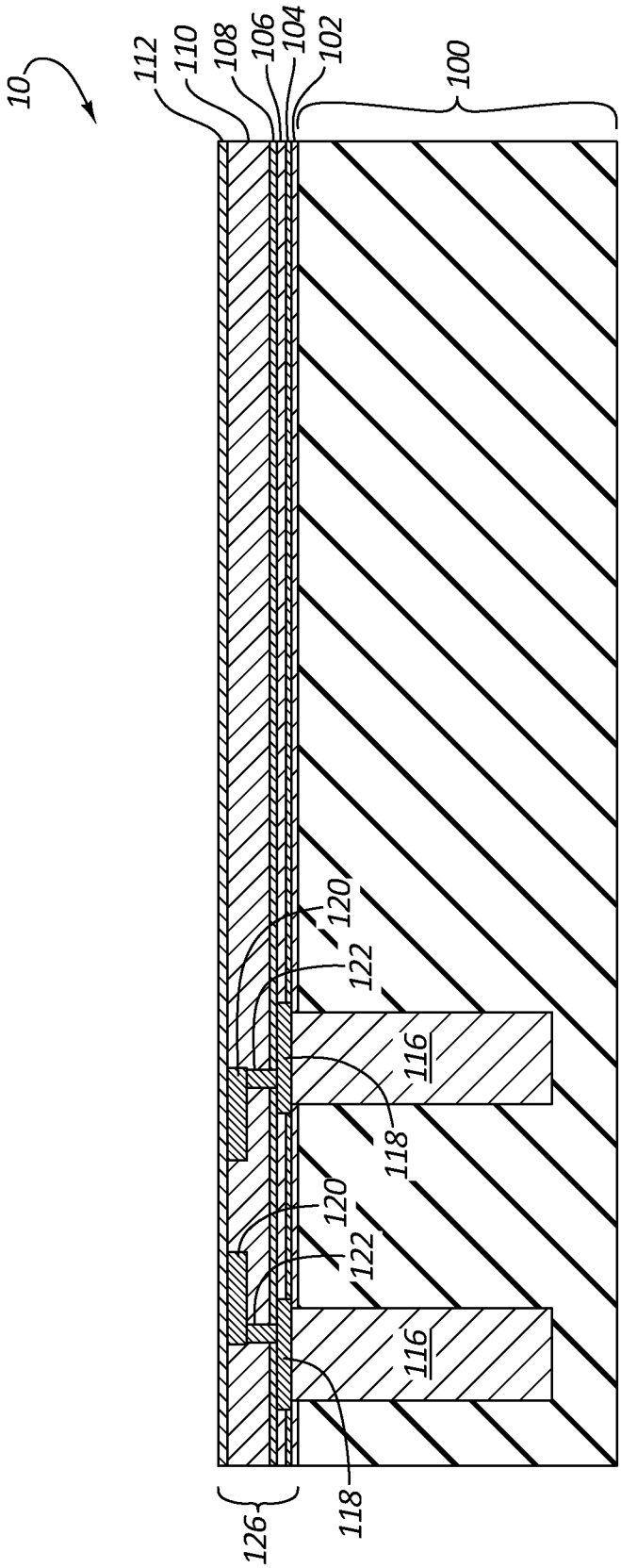
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FIG. 2

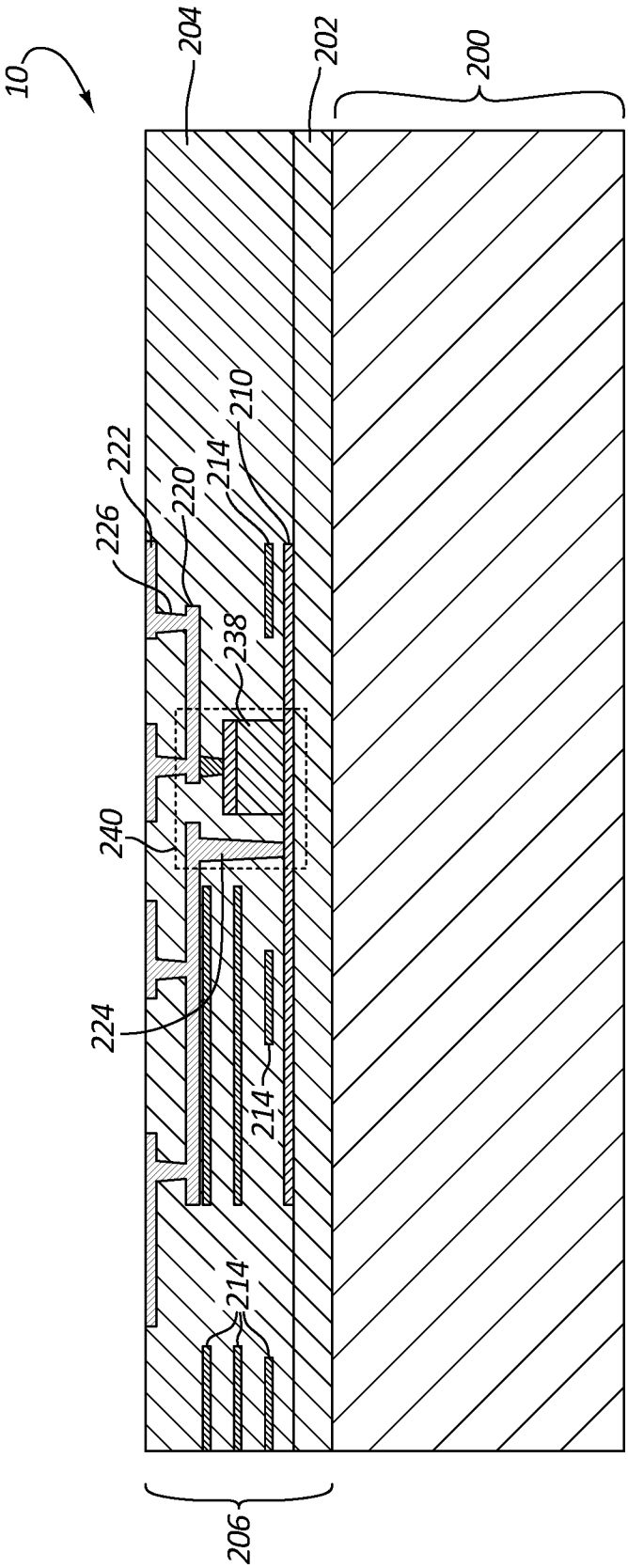

FIG. 3

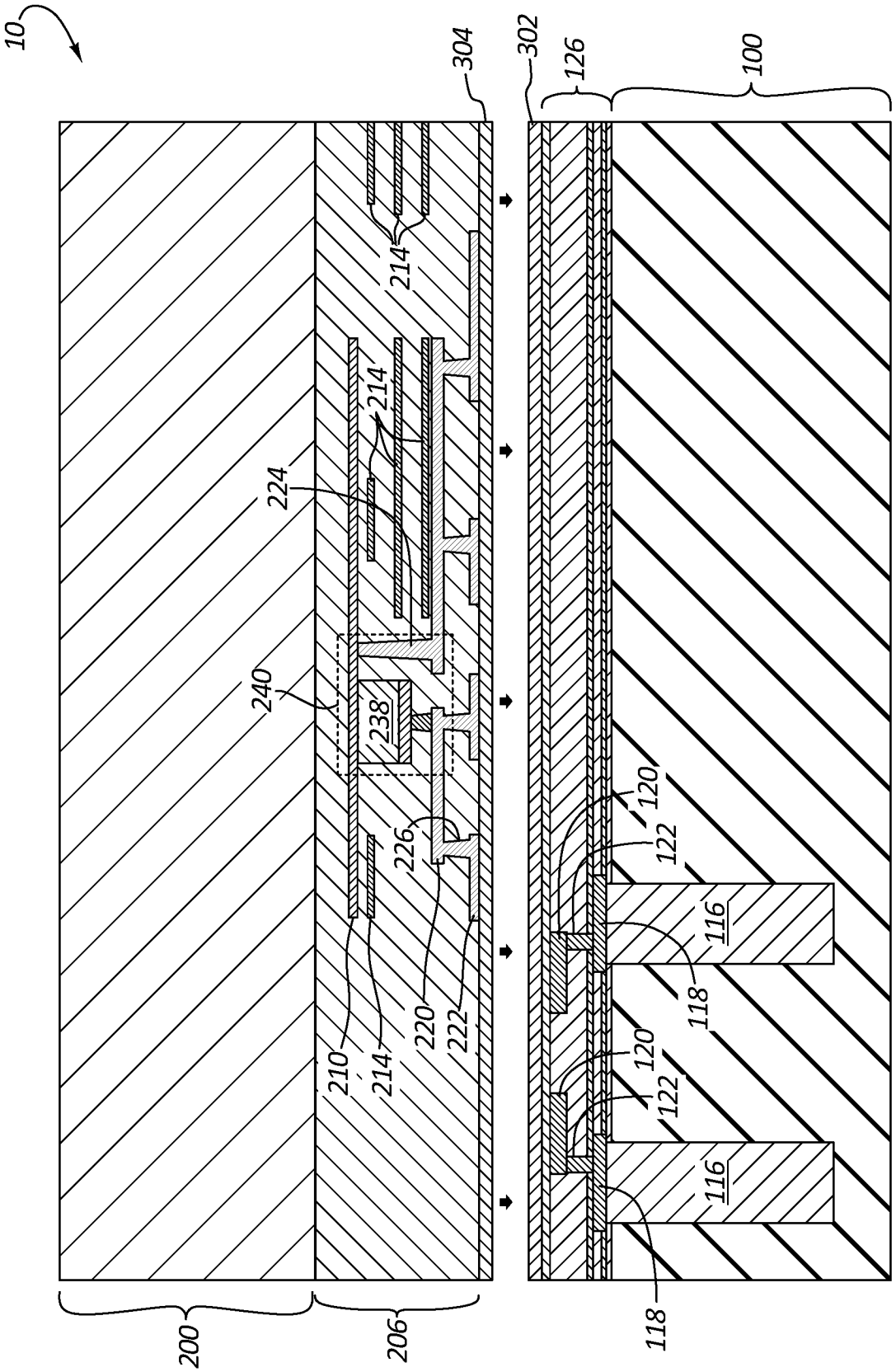
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FIG. 4

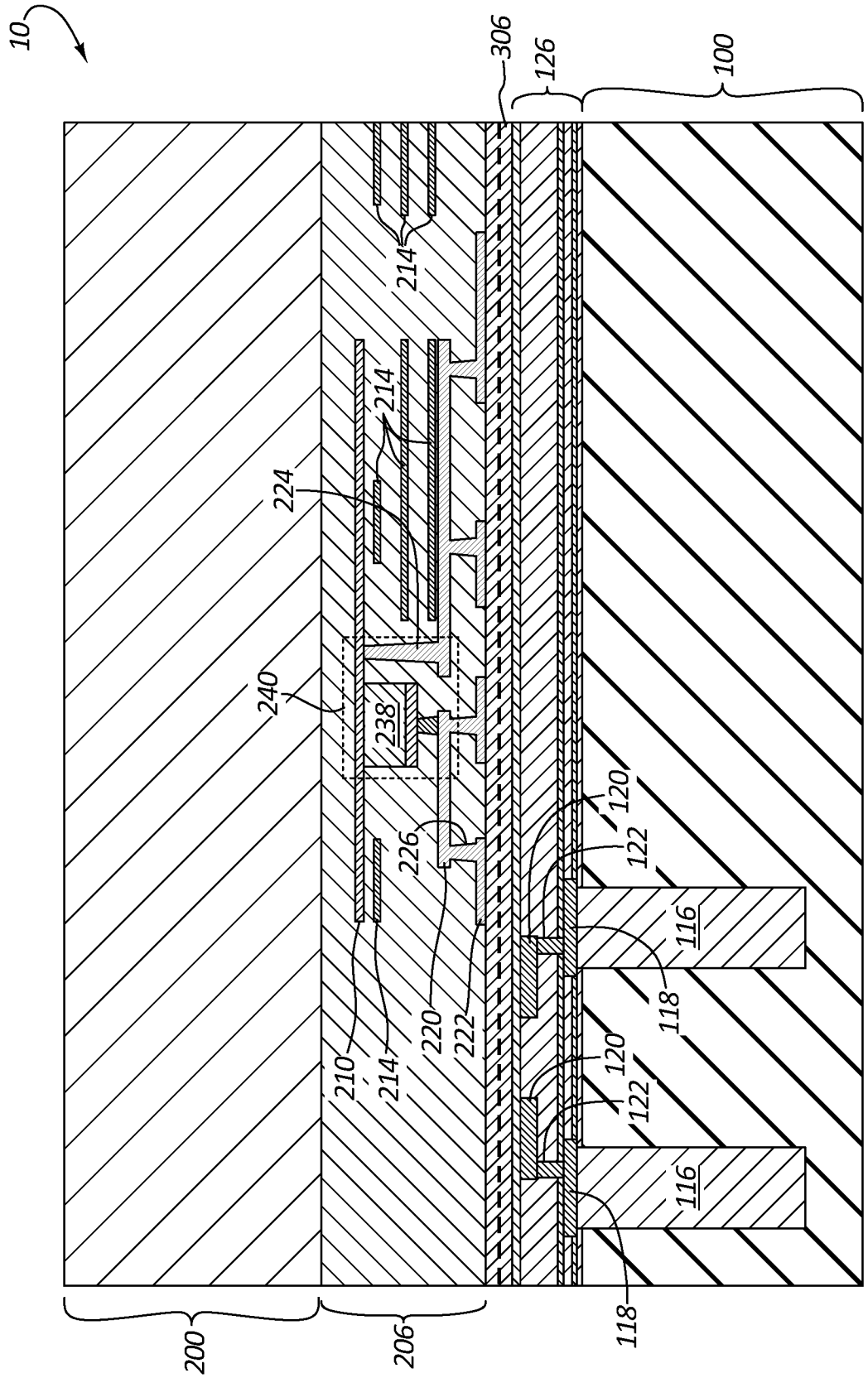
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FIG. 5

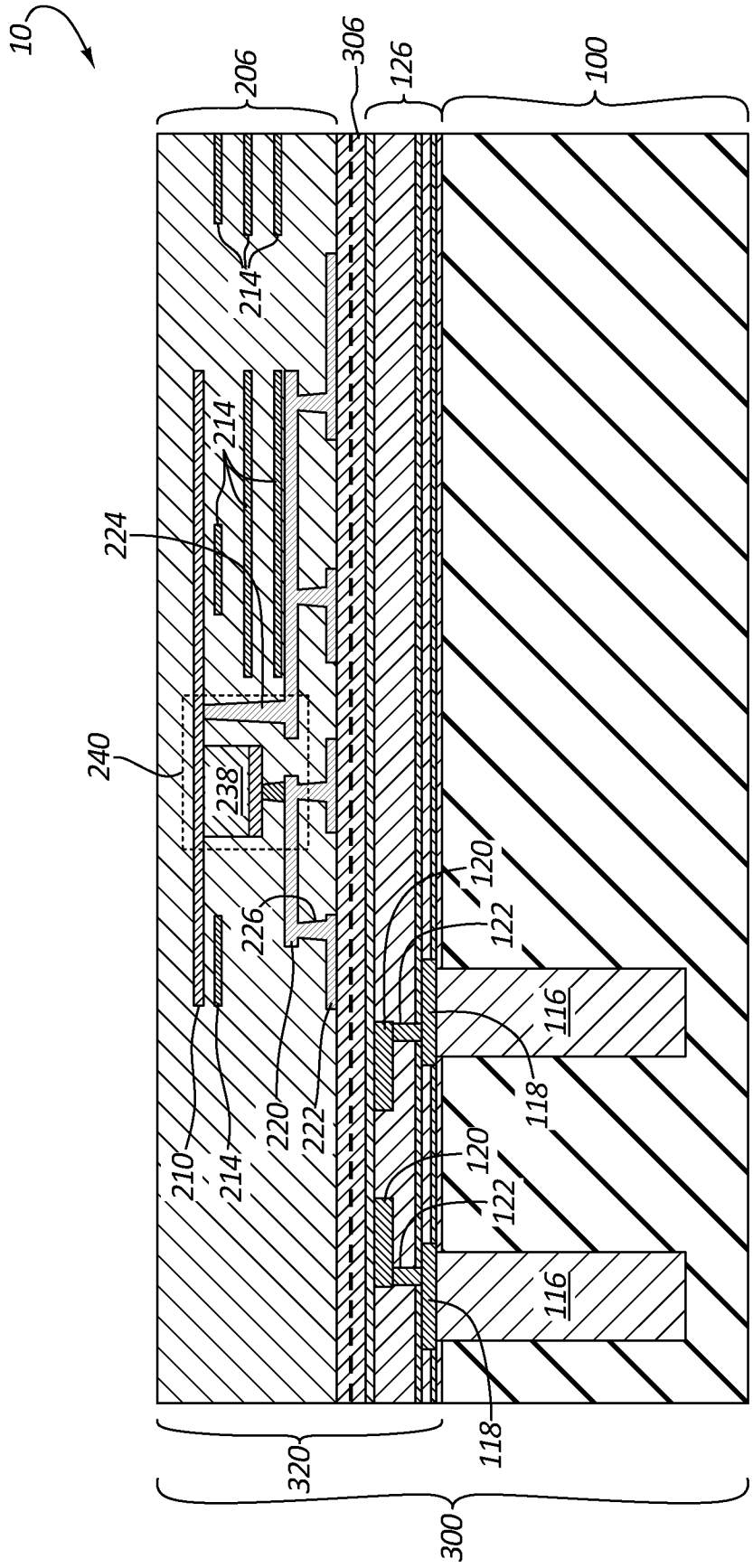
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FIG. 6

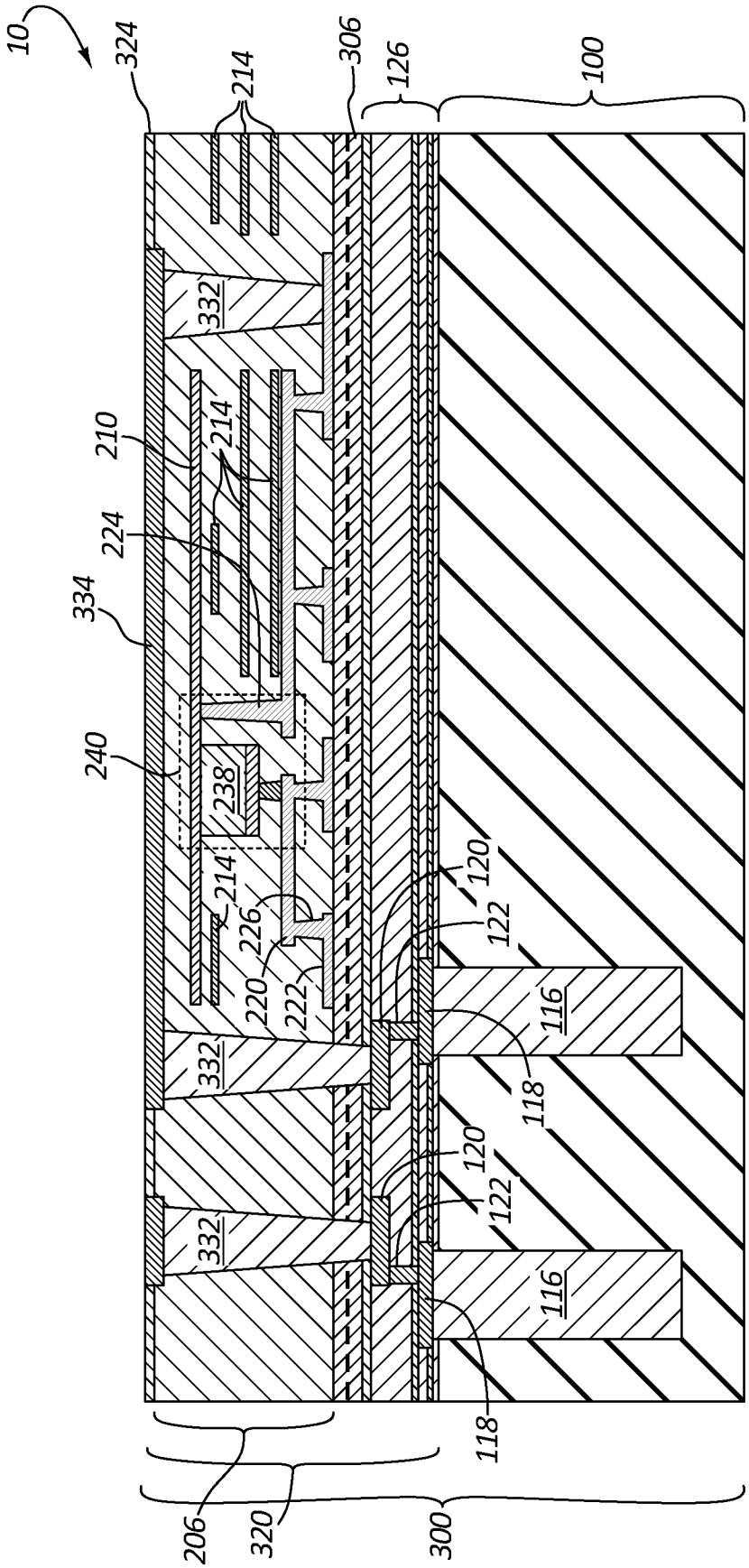
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FIG. 7

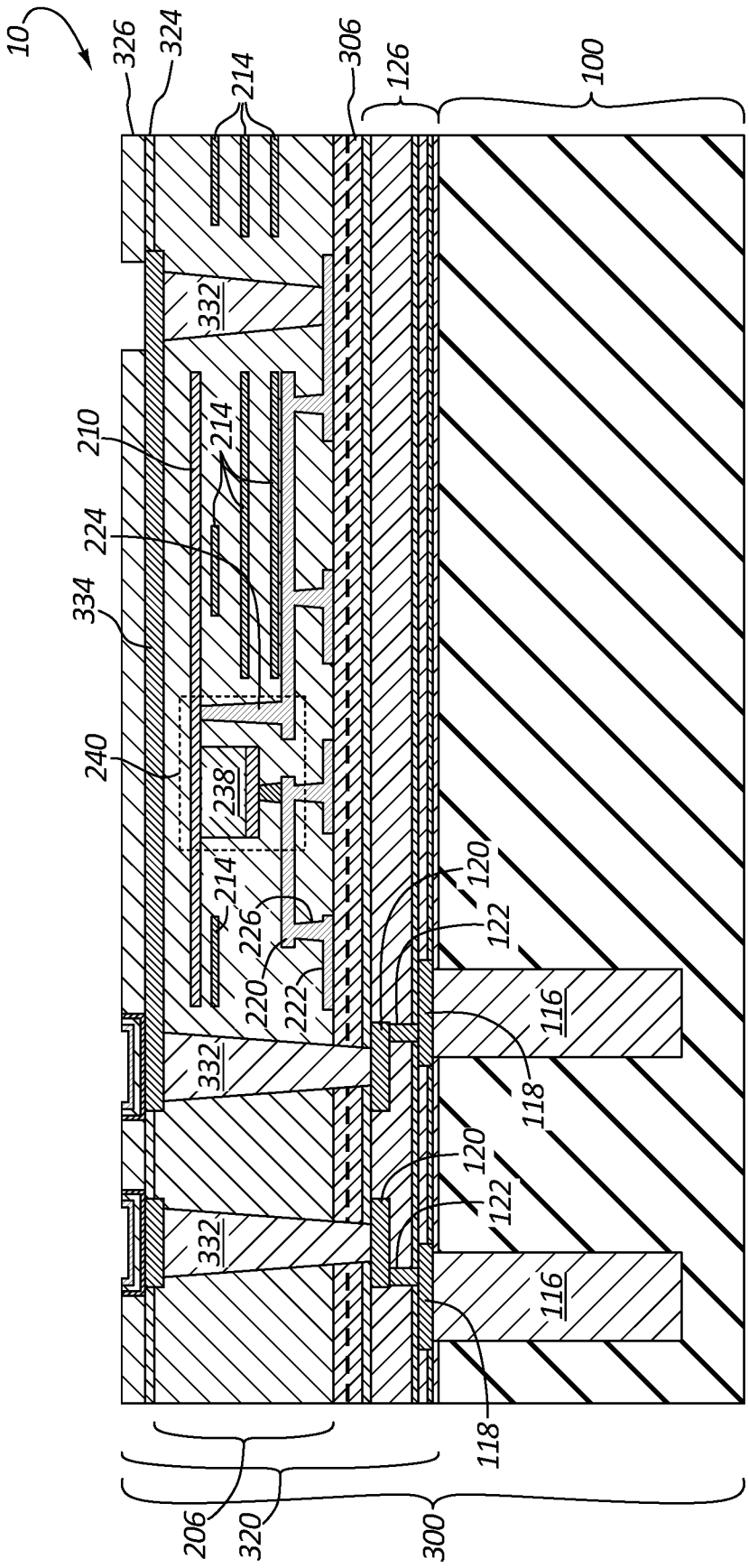
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FIG. 8

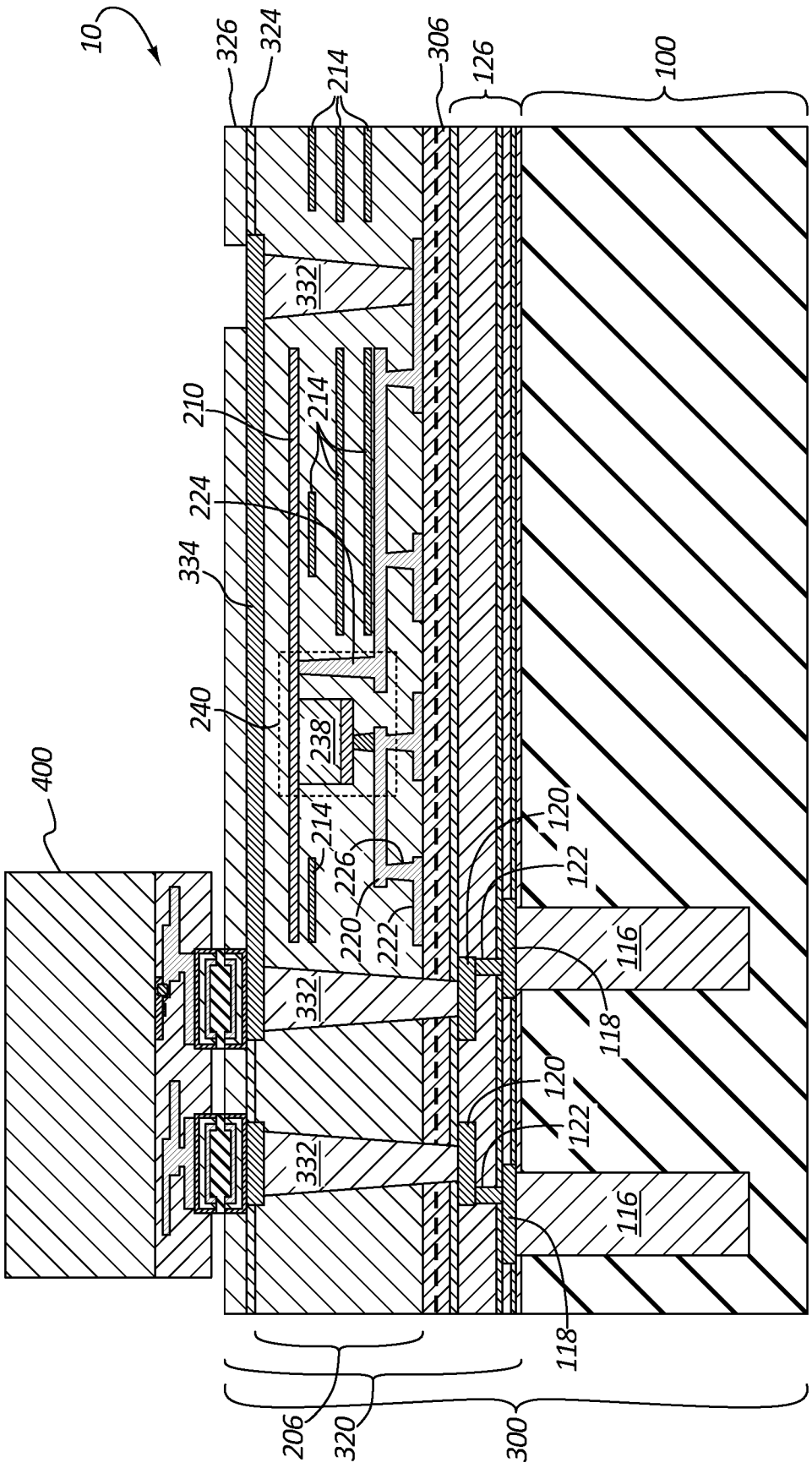
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FIG. 9

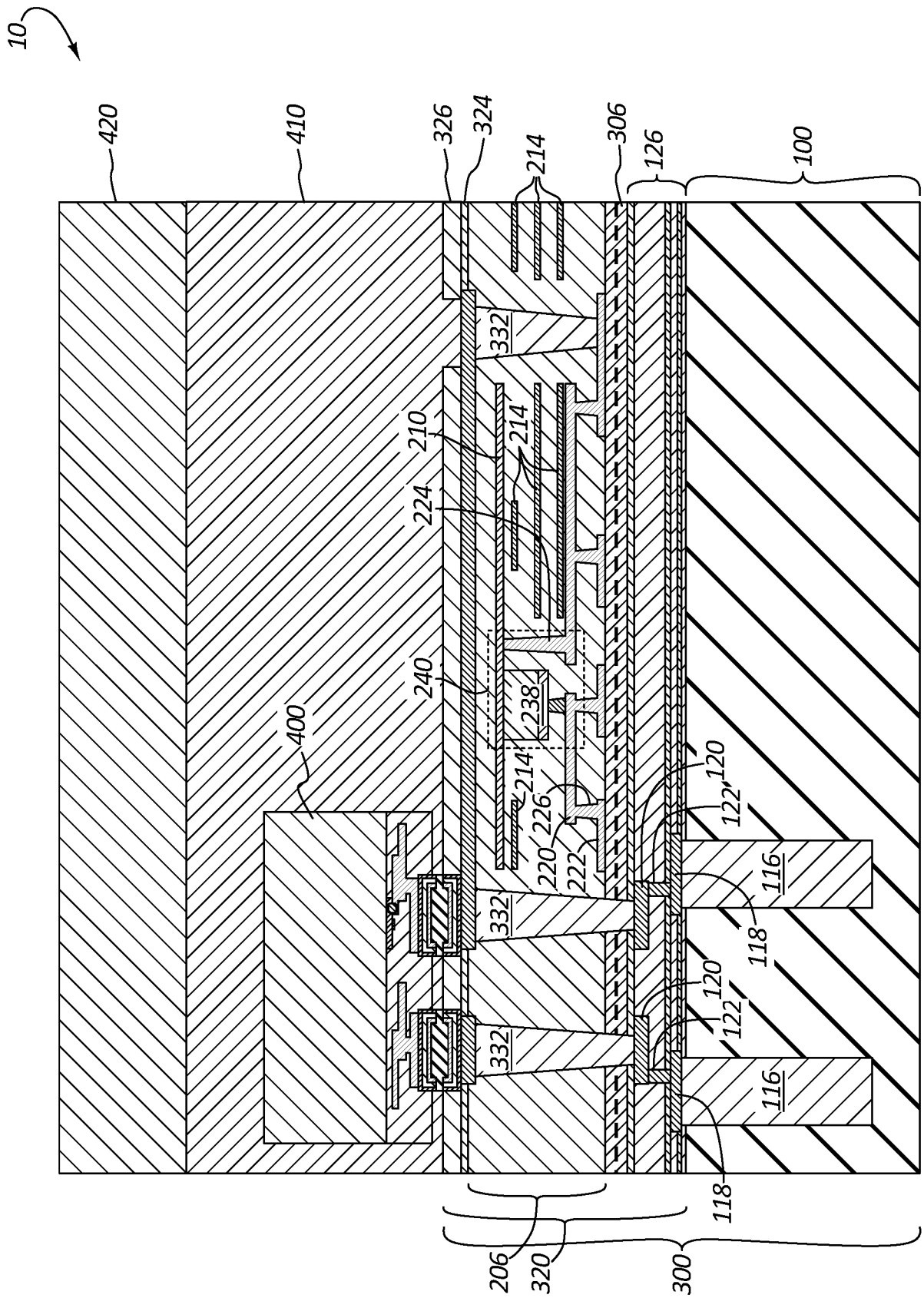
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FIG. 10

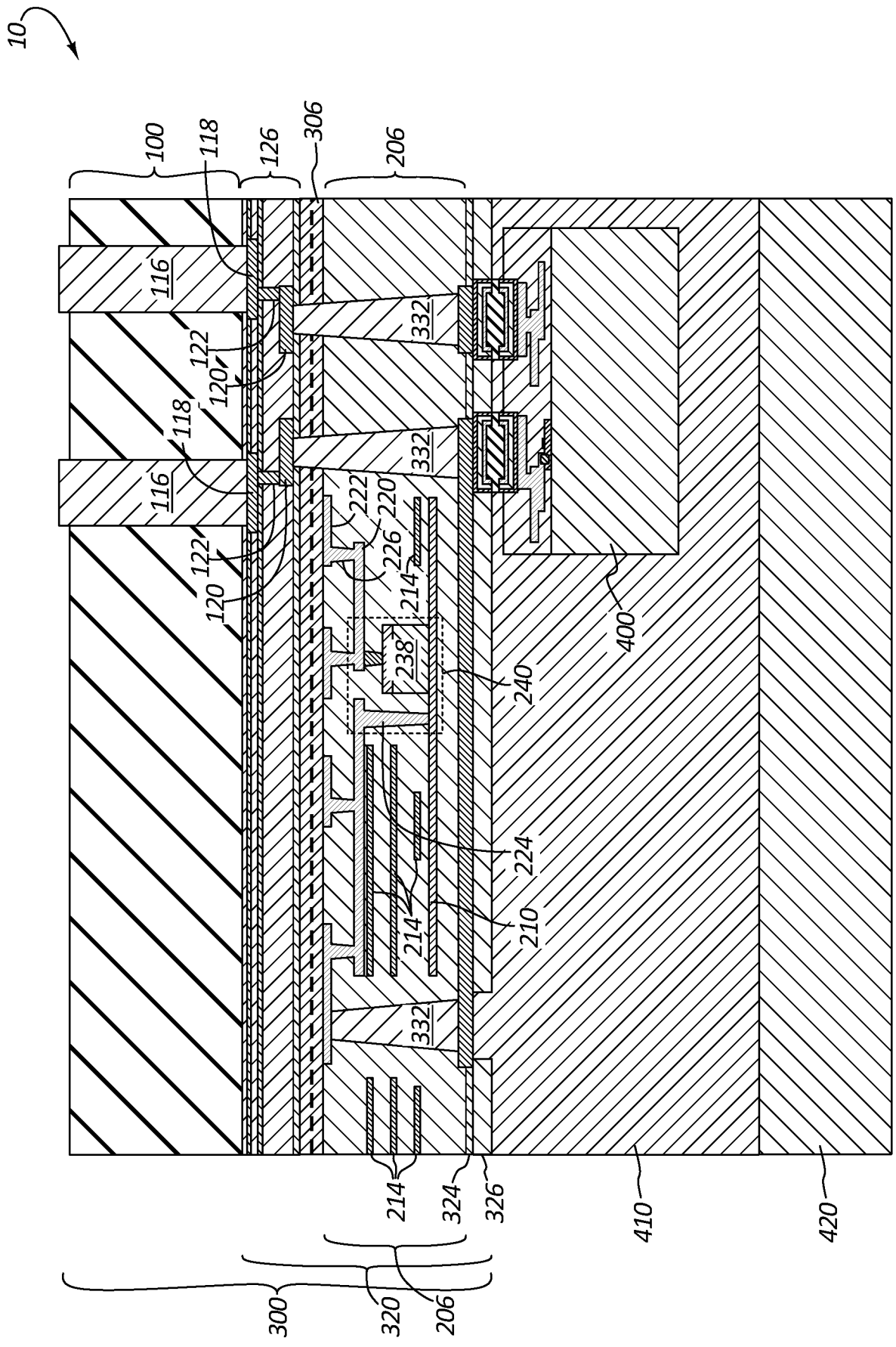
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FIG. 11

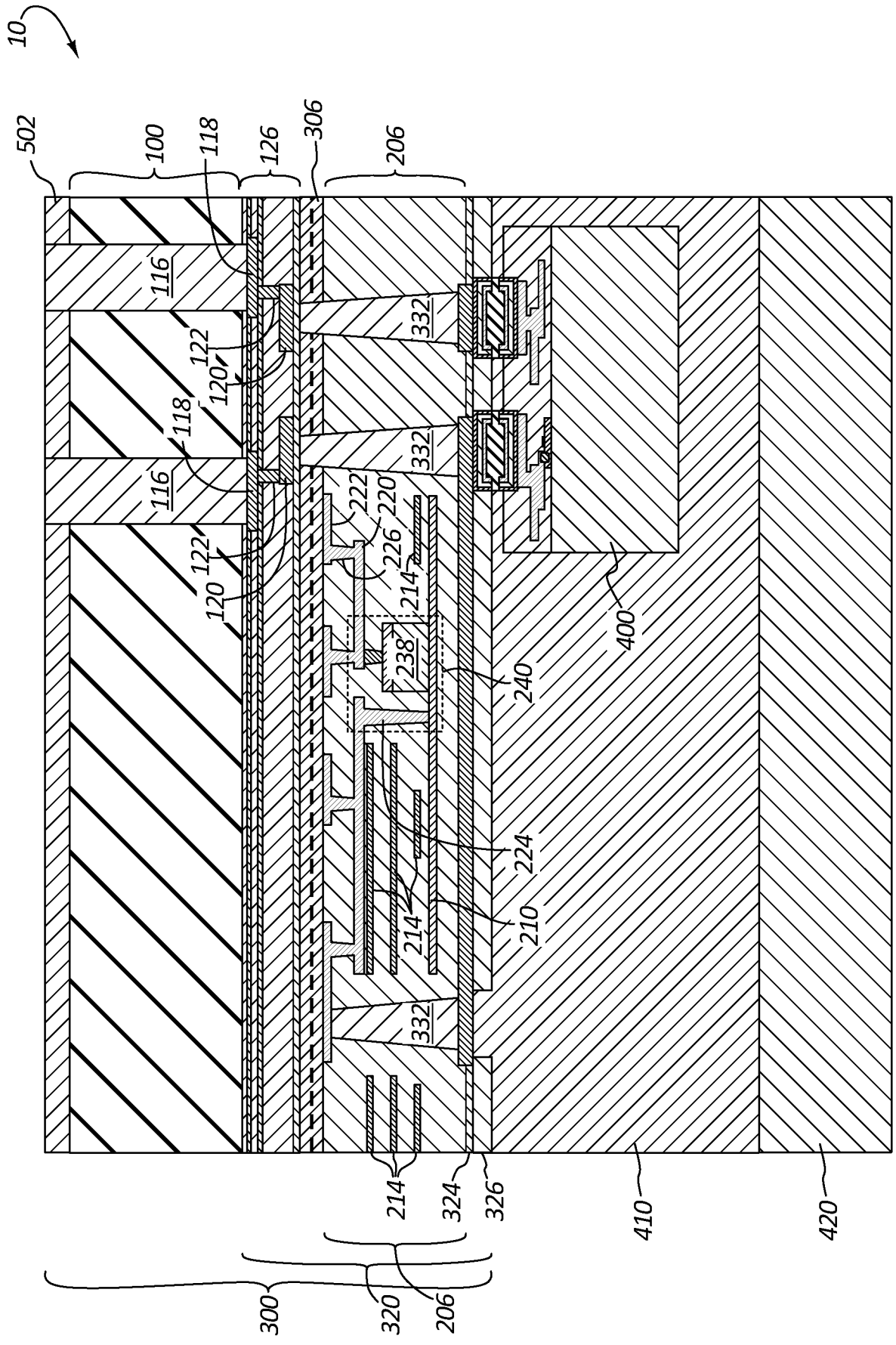
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FIG. 12

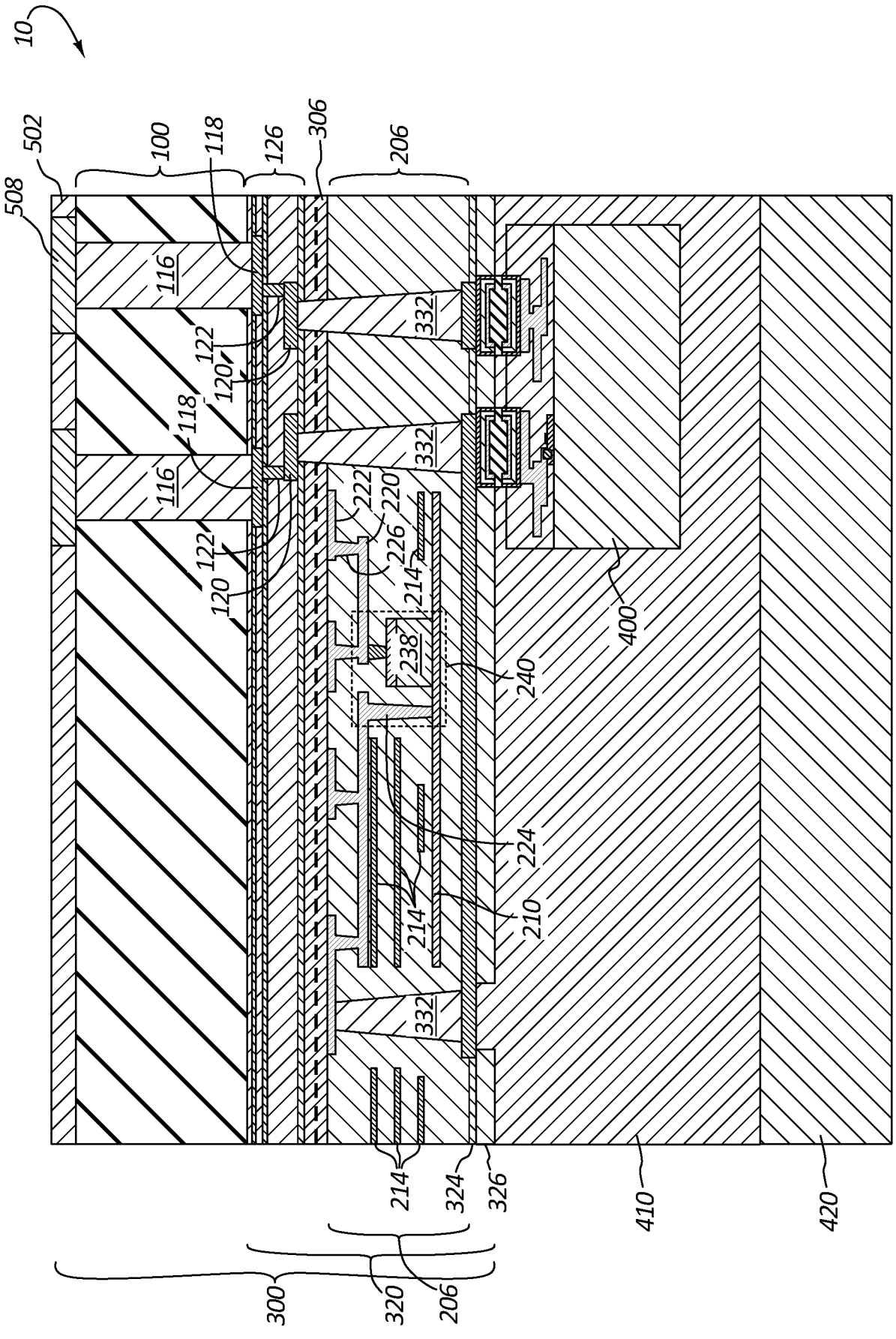
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FIG. 13

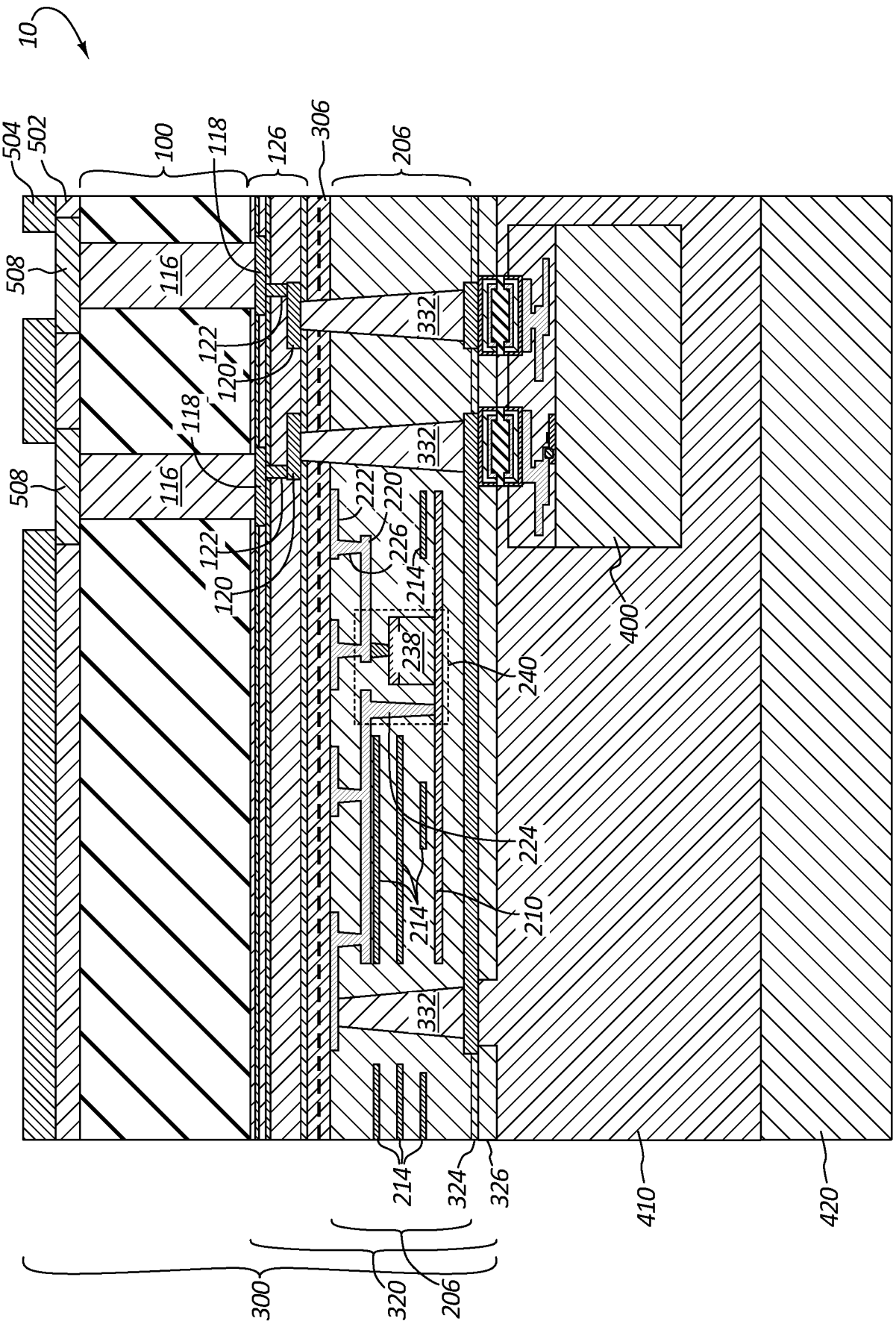
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FIG. 14

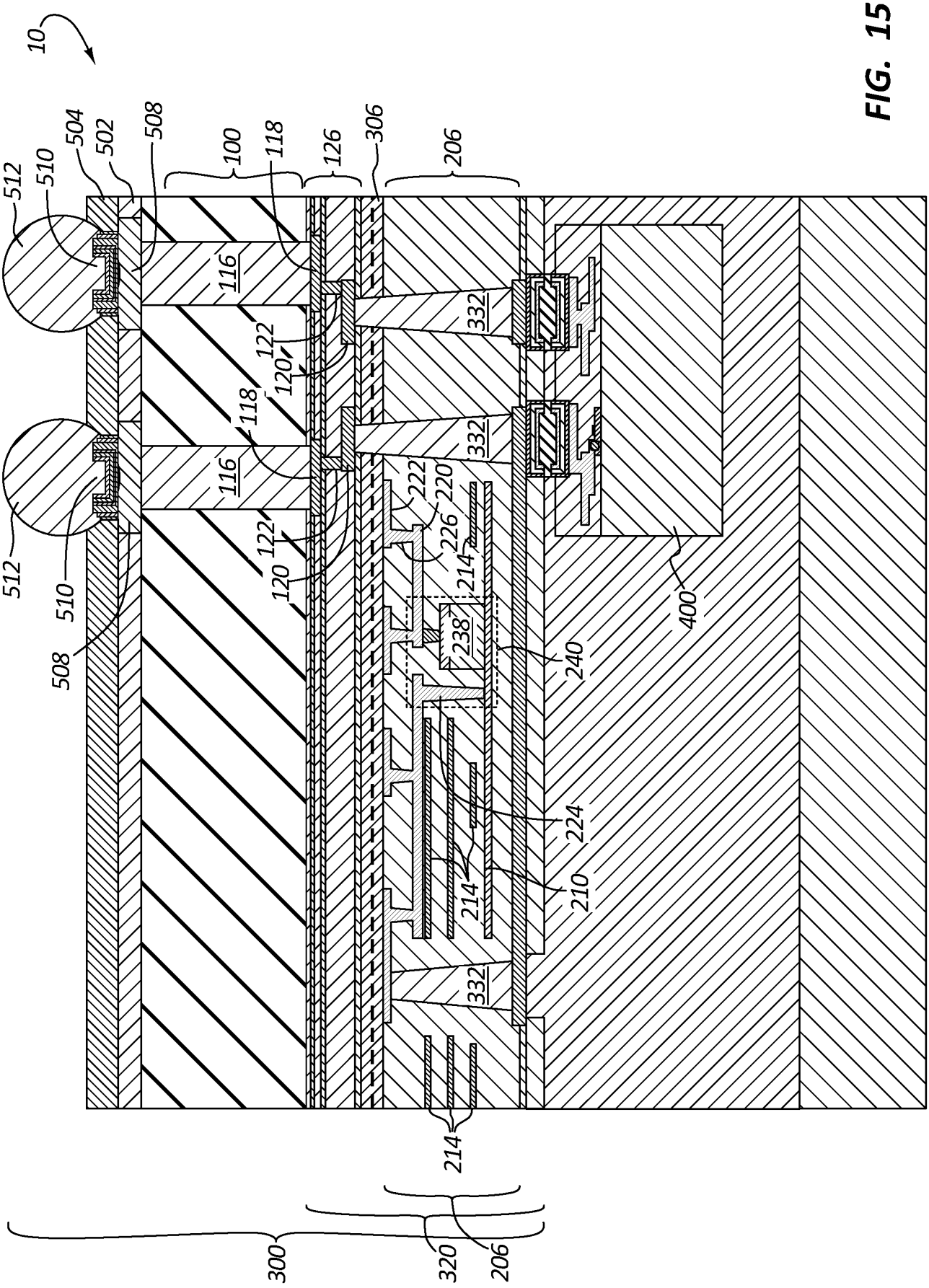
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FIG. 15

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/017558

A. CLASSIFICATION OF SUBJECT MATTER
INV. G02B6/12 H01L21/18
ADD. G02B6/42 G02B6/122 G02B6/13 G02B6/132 G02B6/134
G02B6/136 H01L23/498 H01L21/762 H01L27/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02B H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	YU MINGBIN ET AL: "3D electro-optical integration based on high-performance Si photonics TSV interposer", 2016 OPTICAL FIBER COMMUNICATIONS CONFERENCE AND EXHIBITION (OFC), OSA, 20 March 2016 (2016-03-20), pages 1-3, XP032942514, [retrieved on 2016-08-09] the whole document ----- -/--	1-30

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 April 2018	07/05/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kapsalis, Alexandros

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/017558

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CHEN C L ET AL: "Wafer-scale 3D integration of InGaAs image sensors with Si readout circuits", 3D SYSTEM INTEGRATION, 2009. 3DIC 2009. IEEE INTERNATIONAL CONFERENCE ON, IEEE, PISCATAWAY, NJ, USA, 28 September 2009 (2009-09-28), pages 1-4, XP031557983, ISBN: 978-1-4244-4511-0 the whole document ----	2
A	Ji Fan ET AL: "Low Temperature Wafer-Level Metal Thermo-Compression Bonding Technology for 3D Integration" In: "Metallurgy - Advances in Materials and Processes", 19 September 2012 (2012-09-19), InTech, XP055466841, ISBN: 978-953-51-0736-1 DOI: 10.5772/48216, paragraph [03.4] ----	3
A	US 2017/047312 A1 (BUDD RUSSELL A [US] ET AL) 16 February 2017 (2017-02-16) paragraphs [0053] - [0058]; figures 4A-4J ----	1-30
A	WO 2016/050243 A1 (TECH UNIVERSITÄT BERLIN [DE]) 7 April 2016 (2016-04-07) the whole document ----	1-30

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2018/017558

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 2017186670 A1	29-06-2017
		US 2017186739 A1	29-06-2017
		US 2018040597 A1	08-02-2018
WO 2016050243 A1	07-04-2016	CN 106716199 A	24-05-2017
		DE 102014219792 A1	31-03-2016
		DE 112015004474 A5	14-06-2017
		EP 3201663 A1	09-08-2017
		WO 2016050243 A1	07-04-2016