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[Continued on next page]

(54) Title: FREQUENCY CHANNEL COMBINER

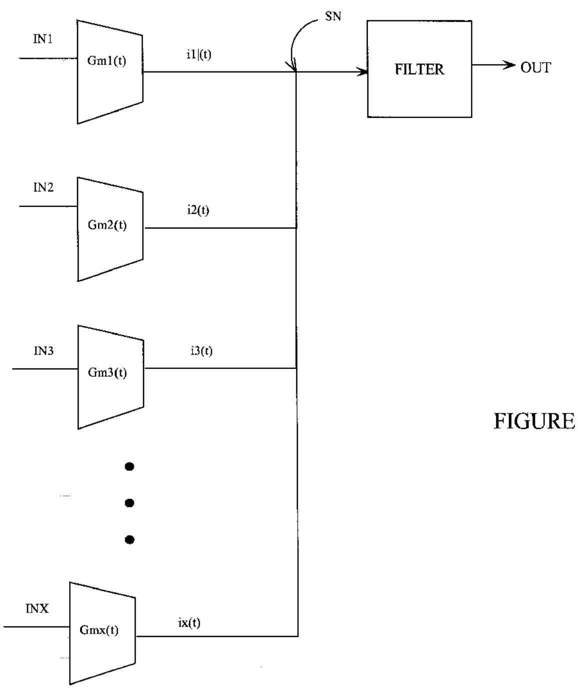

FIGURE 5

(57) Abstract: Methods and systems for processing signals wherein a plurality of signals are received at the inputs of a plurality of transconductance circuits which convert the signals into their corresponding current signals. The current signals are then multiplexed into an internal signal. The internal signal is further filtered and transmitted to an output. The transconductance circuits may be programmable in order to adjust and optimize their transconductance. Any of the input signals may result from a downconverting and filtering process.

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— *with international search report (Art. 21(3))*

Attorney Docket No. 1002P010WO02

FREQUENCY CHANNEL COMBINER

TECHNICAL FIELD

[0001] The present invention relates to electronics and, more specifically, it relates to methods and systems for processing multiple information bearing signals.

BACKGROUND OF THE INVENTION

[0002] In certain applications, it is advantageous to receive multiple signals located at different frequencies simultaneously. For example, in GPS it is useful to be able to receive the L1, L2, and L5 signals located at 1575.42 MHz, 1227.60 MHz and 1176.45 MHz simultaneously. To do so in a conventional manner, three parallel receiver chains are required, including three parallel analog to digital converters.

[0003] It would advantageous to provide a means for receiving multiple signals with a single receiver chain, and to arrange for the multiple signals to occupy a contiguous base-band spectrum just before digitizing with a single analog-to-digital converter. Such a receiver architecture can be realized with the use of the Sampling IF Filter.

[0004] The Sampling IF Filter provides filtering and downconversion functions. A time continuous signal is first sampled (at a rate above the Nyquist rate). The sampled analog signal is then delayed by different time increments, weighted, and summed to form a Finite Impulse Response (FIR) filter response. The filtered signal is then sampled at a lower rate, often less than the Nyquist rate. As a result of this second sampling, multiple frequencies from the input spectrum appear as aliases in the output. This aliasing allows the Sampling IF filter to also act as a frequency converter, and for the output to be at a different frequency than the input. In particular, the output can be extracted at a frequency band equal to the difference between the incoming signal and the Sampling IF filter clock frequency, in a manner identical to a down-conversion achieved with a mixer and a local oscillator.

[0005] The Sampling IF Filter has other properties that are advantageous. Since it is a Finite Impulse Response filter, the signal undergoes a constant group delay across all frequencies. In addition, since the weighting functions can include amplification, the filter response can provide gain.

SUMMARY OF INVENTION

[0006] The present invention provides methods and systems for filtering and downconverting input signals. Cascaded sampling IF filters are used to filter and downconvert signals at specific frequencies to simplify their processing. A first sampling IF filter with multiple passbands receives multiple signals. The multiple passbands are preferably centered around the frequencies of interest and the sampling frequency of the filter is carefully selected. Passing the signals through the first filter will downconvert the signals. Second and subsequent sampling IF filters with multiple selected passbands and sampling frequencies will perform the same function until the desired or workable frequencies result.

[0007] In a first aspect, the present invention provides a method for processing signals comprising:

a) receiving a plurality of signals at a first device which also receives a first sampling clock signal

b) filtering and downconverting said plurality of signals using said first device and based on a plurality of passbands, each passband being centered around specific predetermined frequencies, a number of passbands being equal to a number of said plurality of signals, said plurality of signals being downconverted to frequencies based on said first sampling clock signal

c) receiving outputs of said first device at a second device which also receives a second sampling clock signal

d) filtering and downconverting said plurality of signals using said second device and based on a plurality of passbands, each passband being centered around a frequency of said outputs of said first device, said outputs of said first device being downconverted to frequencies based on said second sampling clock signal.

[0008] In a second aspect, the present invention provides a method for processing at least two input signals, the method comprising:

- receiving said at least two input signals, each input signal being received at a separate transconductance circuit element;

- converting each input signal into a current signal resulting in at least two current signals;

- summing said at least two current signals into a single internal signal;

- filtering said internal signal to result in an output signal.

[0009] In a further aspect, the present invention provides a circuit for processing input signals, the circuit comprising:

- at least two transconductance circuit elements, each transconductance circuit element receiving an input signal and each transconductance circuit element converting said input signal into a current signal;

- a summing node receiving current signals from said transconductance circuit elements, said summing node adding all of said current signals into an internal signal;

- a signal filter receiving and filtering said internal signal, said signal filter outputting an output signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The drawings show features and advantages will become more apparent from a detailed consideration of the invention when taken in conjunction with the drawings in which:

FIGURE 1 is an illustration of the frequency spectrum of the input signal.

FIGURE 2 is an illustration of the frequency spectrum of the output of the first device;

FIGURE 3 is an illustration of the frequency spectrum of the final output of the second device;

FIGURE 4 is an illustration of a circuit for combining input signals while filtering the resulting combined signal; and

FIGURE 5 is an illustration of a generalized version of the circuit in Figure 4.

DETAILED DESCRIPTION OF THE INVENTION

[0011] In one aspect of the invention, two or more non-contiguous desired signals can be applied to a Sampling IF Filter which has its finite impulse response coefficients set to create two or more pass-bands, one around each of the desired signals. The Sampling IF Filter clock frequency can be selected such that its frequency or one of the harmonics of its frequency is between the frequencies of the desired signals, such that at the output the non-contiguous signals are now closer to one another in frequency so that less bandwidth is required to hold all of the desired signals.

[0012] The use of a Sampling IF Filter is also advantageous because of its ability to place zeros at arbitrary frequencies. One aspect of the invention is to place these zeros at frequencies that would also alias to the desired output frequencies.

[0013] Another feature of the Sampling IF Filter that has not been previously exploited is that effectively an LO (local oscillator) is available at all multiples of the output frequency. This allows the use of different harmonic multiples of the second sampling clock to serve as an LO for different desired frequencies.

[0014] In one implementation, as an example, the three GPS bands, L1, L2, and L5 can be applied to a first Sampling IF Filter device which has a pass-band filter response around each GPS band. (See Figure 1) If the Sampling IF Filter clock frequency is chosen to be 1299 MHz, then the three GPS bands will exit the Sampling IF Filter at the Frequencies shown in Figure 2. It should be noted that the spectrum for L2 and L5 will be inverted at this point.

[0015] This composite signal, the output of the first device, can then be passed through a second Sampling IF Filter device, again having a pass-band filter response around each of the down-converted GPS bands. If this second Sampling IF Filter clock frequency is selected to be 225

MHz, then the three GPS bands will exit the second Sampling IF Filter with equal channel separation, as shown in Figure 3. It should be noted that the spectrum for L2 and L5 have again been inverted, and as a result emerge from the second Sampling IF Filter correctly.

[0016] The three GPS channels have been filtered and down converted, and have emerged at the base-band as contiguous signals which can be digitized in a single analog-to-digital converter.

[0017] It should be noted that closer frequency spacing between the L1, L2, and L5 outputs can be achieved as long as at least one GPS band is allowed to be frequency inverted at the input to the analog-to-digital converter. For example, if the clock frequency of the first Sampling IF Filter is chosen to be 1373 MHz, then the three GPS channels will emerge from this first Sampling IF Filter at 146 MHz for a frequency inverted L2 channel, at 197 MHz for a frequency inverted L5 channel, and at 202 MHz for the L1 channel. If these signals are then applied to the second Sampling IF Filter having a clock frequency of 169 MHz, the three GPS bands will exit this second Sampling IF Filter with equal channel separation, at 23 MHz for the L2 channel, at 28 MHz for the frequency inverted L5 channel, and at 33 MHz for the L1 channel.

[0018] Alternatively, a filter with an output sampling frequency that placed an effective LO close to each desired RF channel can be used. With a sampling frequency of 42 times the chip-rate (1.023 MHz), appropriate LO frequencies can be found at the 37th , 29th, and 27th multiples of the output sampling frequency for the L1, L2 and L5 bands respectively as indicated in Table I. Thus the filter requires a sampling frequency of 42*1.023=42.966 MHz.

Table I

Name	RF (MHz)	Chip-Rate multiplier	LO (MHz)	IF (MHz)
L1	1575.42	37*42	1589.74	14.32
L2	1227.6	29*61	1246.01	18.41
L5	1176.45	27*42	1160.08	16.37

[0019] Other frequencies that those listed in Table 1 are, of course, possible. It should also be noted that the downconversion process (the process of downconverting a signal from an RF frequency to a lower IF frequency) is well-known to those skilled in the art.

[0020] After the first filter which downconverts incoming signals, the incoming signals may be combined in another manner. Another embodiment of the invention involves the use of multiple transconductance circuit elements, each of which receives a downconverted signal and each of which converts its downconverted signal into a current. The various currents (derived from the various downconverted signals) are then summed at a summing node and the resulting internal signal (a summed current signal) is filtered. Figure 4 illustrates an example configuration of such a circuit.

[0021] Referring to Fig. 4, three input signals IN1, IN2, IN3 are each received separately by three transconductance circuit elements $Gm_1(t)$, $Gm_2(t)$, and $Gm_3(t)$. Each transconductance circuit element converts the input signal into a current ($i_1(t)$), $i_2(t)$, and $i_3(t)$). The various currents are then summed into a single current signal by way of a summing node SN. The single current signal can then filtered. In the example, the signal is filtered by way of a capacitor C. Of course, any suitable filtering means or circuits or circuit elements can be used in lieu of the capacitor. A generalized version of the circuit is illustrated in Figure 5 where the filter (FILTER) is shown generally along with the various transconductance circuit elements.

[0022] The output signal (OUT), a summed, filtered version of the input signals, can be processed further if desired. The output signal can be upconverted, filtered, or can be processed in any manner desired.

[0023] It should be noted that the input signals are, preferably, downconverted versions of original signals. As an example, the original signals may be RF signals and the downconverted signals may be IF signals. Some example center frequencies for IF signals are shown as IF frequencies in Table 1 above. Some sample RF signals are also given the same Table 1.

[0024] It should further be noted that while Figure 4 illustrates 3 transconductance circuit elements, multiple (i.e. more than 2 or 3) instances of these circuit elements may be used, each one receiving an input signal and each one sending its output to a summing node.

[0025] One advantage to the above embodiment is that signals can be more easily combined in the IF sphere as opposed to the RF sphere. As is well-known, combining signals in RF can lead to issues such as handling the power of the signals. By combining the signals in the IF sphere, the RF issues are thereby avoided.

[0026] It should further be noted that the transconductance circuit elements are active devices and are programmable. Preferably, the transconductance circuit elements are programmable such that the conversion parameters from the input signal (INX) to the current signal ($i_x(t)$) are adjustable. Example methods for programmable transconductances can be found in the PCT patent application published under publication number WO2009062306, the entirety of which is hereby incorporated by reference.

[0027] Of course, the principles of the method described above may be used for other frequencies as well. Furthermore, it is to be noted that while a sampling IF filter is preferable, other devices or combinations of devices which perform the same function as the sampling IF filter may also be used.

[0028] Further information regarding sampling IF filters may be found in the following references, both of which are hereby incorporated by reference in their entirety:

Muhammad K & Staszewski RB (2004) Direct RF sampling mixer with recursive filtering in charge domain. Proceedings of the IEEE International Symposium on

Circuits and Systems (ISCAS'04), Vancouver, Canada, May 23-26 2004, 1: 577-580.

Karvonen S, Riley T & Kostamovaara J (2001) A low noise quadrature subsampling mixer. Proceedings of the International Symposium on Circuits and Systems (ISCAS'2001), Sydney, Australia, 4: 790-793.

[0029] A person understanding this invention may now conceive of alternative structures and embodiments or variations of the above all of which are intended to fall within the scope of the invention as defined in the claims that follow.

Attorney Docket No. 1002P010WO02

Having thus described the invention, what is claimed as new and secured by Letters Patent is:

1. A method for processing at least two input signals, the method comprising:

- receiving said at least two input signals, each input signal being received at a separate transconductance circuit element;
- converting each input signal into a current signal resulting in at least two current signals;
- summing said at least two current signals into a single internal signal;
- filtering said internal signal to result in an output signal.

2. A method according to claim 1 wherein at least one transconductance circuit element is programmable.

3. A method according to claim 1 wherein each input signal is a result of a downconversion process.

4. A method according to claim 1 wherein said current signals are summed at a summing node.

5. A method according to claim 1 wherein at least one of said transconductance circuit elements is an active device.

6. A method according to claim 1 wherein at least one of said at least two input signals is received from a filter and said at least one of said at least two input signals is a result of a downconversion process.

7. A method for processing signals comprising:

a) receiving a plurality of signals at a first device which also receives a first sampling clock signal

b) filtering and downconverting said plurality of signals using said first device and based on a plurality of passbands, each passband being centered around specific predetermined frequencies, a number of passbands being equal to a number of said plurality of signals, said plurality of signals being downconverted to frequencies based on said first sampling clock signal

c) receiving outputs of said first device at a second device which also receives a second sampling clock signal

d) filtering and downconverting said plurality of signals using said second device and based on a plurality of passbands, each passband being centered around a frequency of said outputs of said first device, said outputs of said first device being downconverted to frequencies based on said second sampling clock signal.

8. A method according to claim 7 wherein said first and second devices are sampling IF filters.

9. A method according to claim 7 wherein each signal in steps b) and c) are downconverted to a frequency which is a difference between an original frequency and a frequency of a sampling clock signal.

10. A method according to claim 7 wherein steps a)-b) are repeated for subsequent devices for outputs of step d)

11. A method according to claim 7 wherein said plurality of signals in step a) comprises signals at 1575.42 MHz, 1227.6 MHz, and 1176.45 MHz.

12. A method according to claim 11 wherein said first sampling clock signal has a frequency of 1299 MHz.

13. A method according to claim 12 wherein said second sampling clock signal has a frequency of 225 MHz.

14. A method according to claim 13 wherein an output of said second device comprises signals at 51 MHz, 102 MHz, and 153 MHz.

15. A circuit for processing input signals, the circuit comprising:

- at least two transconductance circuit elements, each transconductance circuit element receiving an input signal and each transconductance circuit element converting said input signal into a current signal;
- a summing node receiving current signals from said transconductance circuit elements, said summing node adding all of said current signals into an internal signal;
- a signal filter receiving and filtering said internal signal, said signal filter outputting an output signal.

16. A circuit according to claim 15 wherein each input signal is a result of a downconversion process.

17. A circuit according to claim 15 wherein at least one of said transconductance circuit elements is an active device.

18. A circuit according to claim 15 wherein at least one of said transconductance circuit elements is programmable in how said input signal is converted into a current signal.

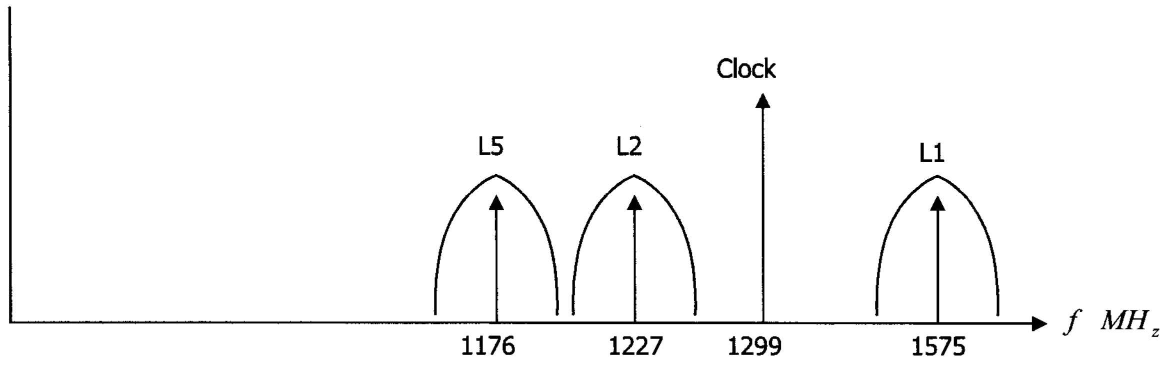

Figure 1. GPS Frequency Channels

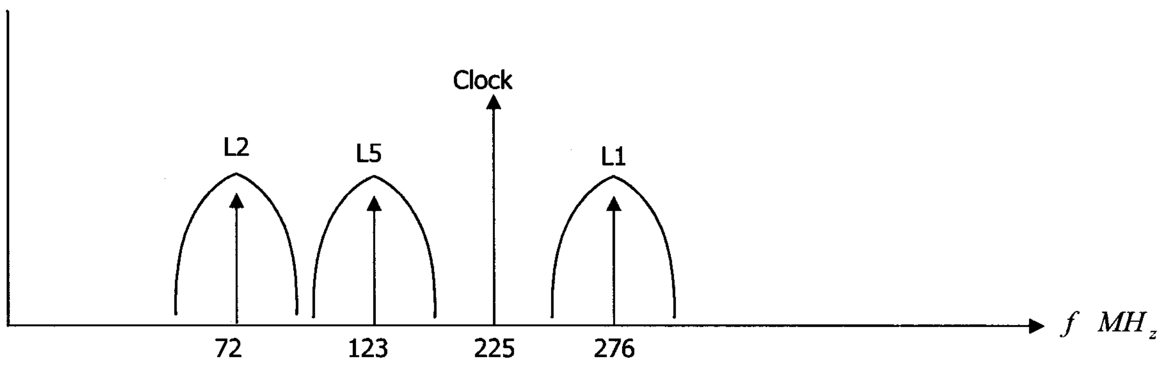

Figure 2. Down Converted GPS Frequency Channels

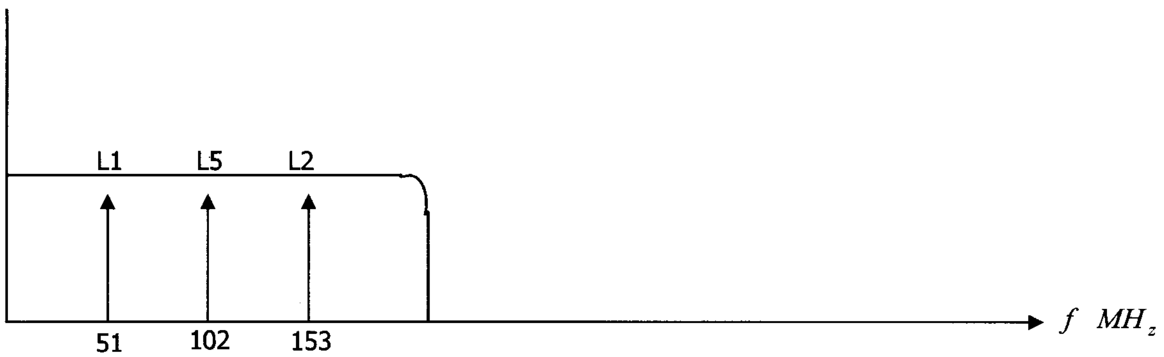

Figure 3. Contiguous Base Band Output of Second Sampling IF Filter

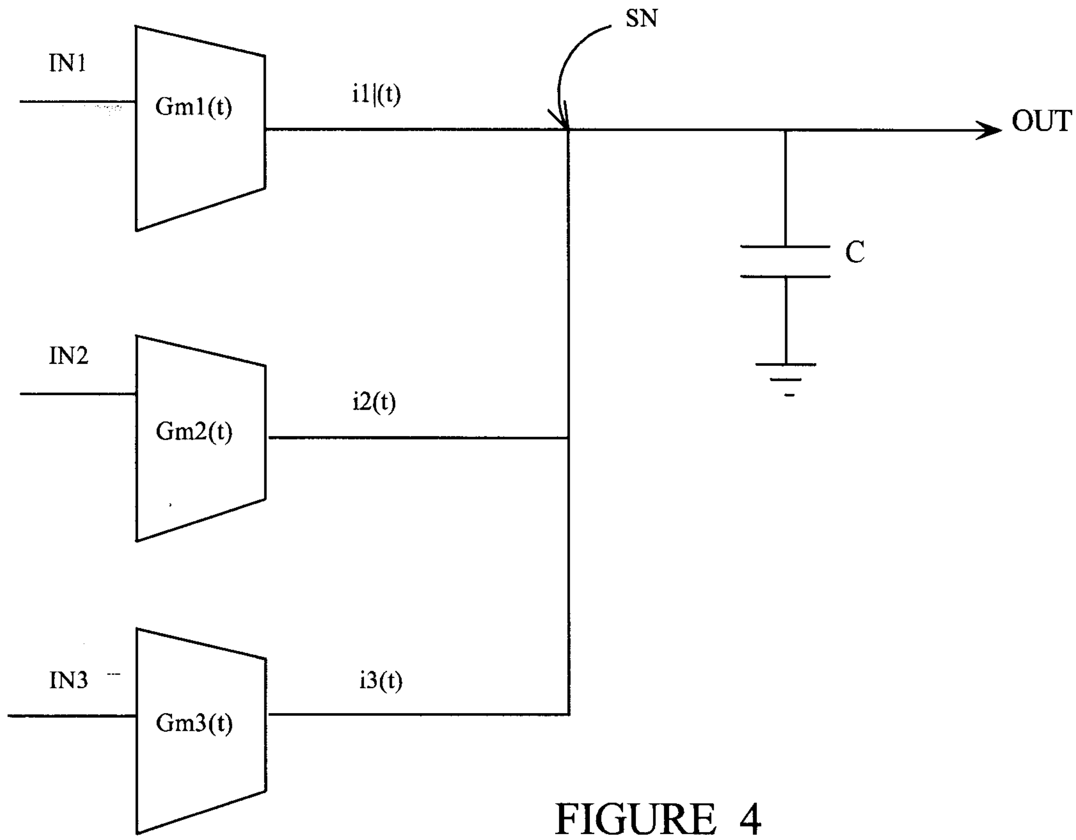

FIGURE 4

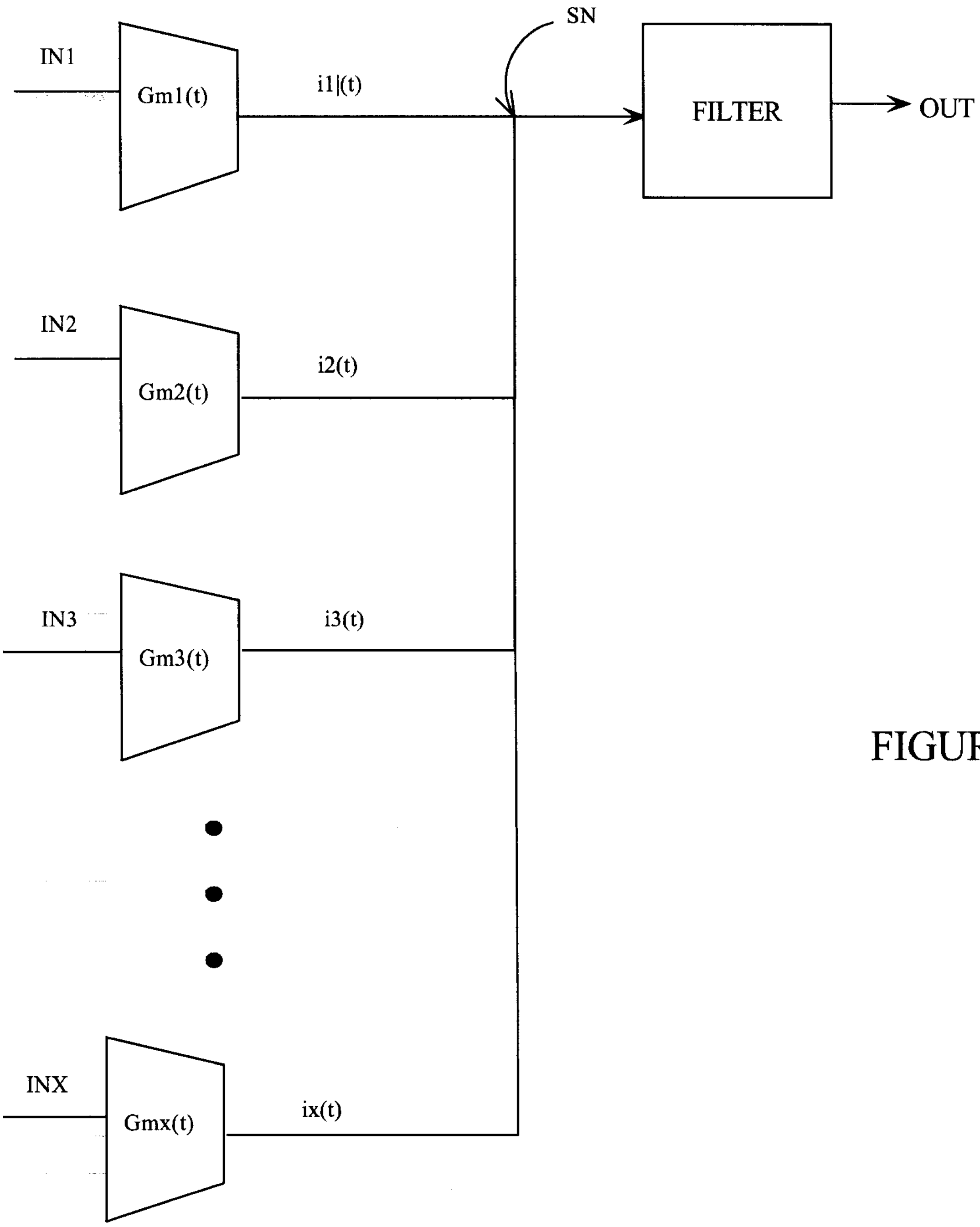
SN
IN1
Gm1(t)
i1|(t)
FILTER
OUT
IN2
Gm2(t)
i2(t)
IN3
Gm3(t)
i3(t)
INX
Gmx(t)
ix(t)

FIGURE 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2011/000008

A. CLASSIFICATION OF SUBJECT MATTER

IPC: ***H03H 2/00*** (2006.01) , **H03D 9/00** (2006.01) , **G01S 19/32** (2010.01) , **H03M 1/12** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: ***H03H*** (2006.01) , *H03D* (2006.01) , *G01S* (2010.01) , *H03M* (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)

EPOQUE, Canadian Patent Database: filter, multiplex, transconductance, current, signal, downconvert, mix, frequency, sum

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US2004017250 A1 (GIUROIU HORIA) 29 January 2004 (29-01-2004) *paragraphs 5, 49-52, 75-77, fig. 6 and fig. 13A*	1, 4, 5, 15, 17 2, 3, 6 , 16, 18
Y	WO2009062306 A1 (RILEY TOM et al.) 22 May 2009 (22-05-2009) *whole document*	2, 18
Y	US2003194984 A1 (TONCICH STANLEYet al.) 16 October 2003 (16-10-2003) * fig.2, paragraphs and paragraph 22*	3, 6, 16

[ ] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 March 2011 (03-03-2011)	20 April 2011 (20-04-2011)

Name and mailing address of the ISA/CA	Authorized officer
Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001-819-953-2476	Adrian Chitiu (819) 934-7885

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of the first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons :

1. [ ] Claim Nos. :
because they relate to subject matter not required to be searched by this Authority, namely :

2. [ ] Claim Nos. :
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically :

3. [ ] Claim Nos. :
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows :

Group A - Claims 1-6 and 15-18 are directed to a circuit and a method for processing signals comprising receiving at least two signals, converting the signals into current signals then summing these signals into an internal signal and then filtering the internal signal.

Group B - Claims 7-13 are directed to a method for processing signals comprising receiving a plurality of signals, down-converting and filtering the signals through two cascade down-converting and filtering circuits.

1. [ ] As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. [ ] As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claim Nos. :

4. [ ] No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim Nos. :

Remark on Protest
[ ] The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
[ ] The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
[ ] No protest accompanied the payment of additional search fees.

Patent document Cited in Search report	Publication Date	Patent Family Member(s)	Publication Date
US2004017250 A1	29-01-2004	US6806765 B2	19-10-2004
WO2009062306 A1	22-05-2009	US2011043256 A1	24-02-2011
		JP2011504023T T	27-01-2011
		EP2225828 A1	08-09-2010
		CN101861699 A	13-10-2010
		CA2705479 A1	22-05-2009
US2003194984 A1	16-10-2003	US2005043001 A9	24-02-2005