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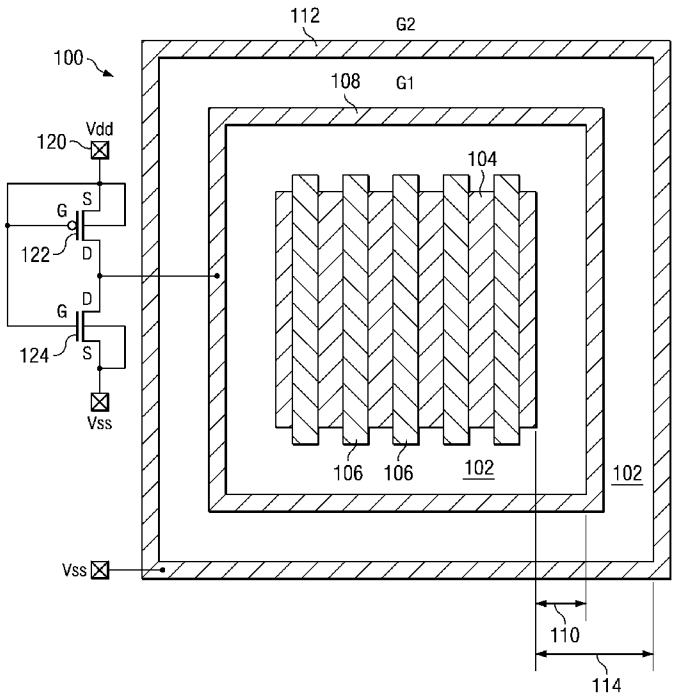
Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

[Continued on next page]

(54) **Title:** SEMICONDUCTOR DUAL GUARD RING ARRANGEMENT



(57) **Abstract:** A semiconductor dual guard ring arrangement (100) is provided which is useful during electrostatic discharge (ESD) events as well as during normal operating conditions. In particular, an inner guard that is located closer to an active area (104) provides desirable performance during normal operating conditions, while an outer guard ring located further from the active area provides desirable performance during an ESD event.

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SEMICONDUCTOR DUAL GUARD RING ARRANGEMENT

The invention relates generally to the art of semiconductor devices; and, more particularly, to a dual guard ring arrangement that is useful during both electrostatic discharge (ESD) events and normal operating conditions.

BACKGROUND

Electrostatic discharge (ESD) is a continuing problem in the design, manufacture and utilization of semiconductor devices. Integrated circuits (ICs) can be damaged by ESD events stemming from a variety of sources, in which large currents flow through the device in an uncontrolled fashion. In one such ESD event, a packaged IC acquires a charge when it is held by a human whose body is electrostatically charged. An ESD event occurs when the IC is inserted into a socket, and one or more of the pins of the IC package touch the grounded contacts of the socket. This type of event is known as a human body model (HBM) ESD stress. For example, a charge of about 0.6 μC can be induced on a body capacitance of 150 pF, leading to electrostatic potentials of 4 kV or greater. HBM ESD events can result in a discharge for about 100 nS with peak currents of several amperes to the IC. Another source of ESD is from metallic objects, known as the machine model (MM) ESD source, which is characterized by a greater capacitance and lower internal resistance than the HBM ESD source. The MM ESD model can result in ESD transients with significantly higher rise times than the HBM ESD source. A third ESD model is the charged device model (CDM), which involves situations where an IC becomes charged and discharges to ground. In this model, the ESD discharge current flows in the opposite direction in the IC than that of the HBM ESD source and the MM ESD source. CDM pulses also typically have very fast rise times compared to the HBM ESD source.

ESD events typically involve discharge of current between one or more pins or pads exposed to the outside of an integrated circuit chip. Such ESD current flows from the pad to ground through vulnerable circuitry in the IC, which may not be designed to carry such currents. Many ESD protection techniques have been thus far employed to reduce or mitigate the adverse effects of ESD events in integrated circuit devices. Many conventional ESD protection schemes for ICs employ peripheral dedicated circuits to carry the ESD currents from the pin or pad of the device to ground by providing a low impedance path thereto. In

this way, the ESD currents flow through the protection circuitry, rather than through the more susceptible circuits in the chip.

Such protection circuitry is typically connected to I/O and other pins or pads on the IC, wherein the pads further provide the normal circuit connections for which the IC was designed. Some ESD protection circuits carry ESD currents directly to ground, and others provide the ESD current to the supply rail of the IC for subsequent routing to ground. Rail-based clamping devices can be employed to provide a bypass path from the IC pad to the supply rail (e.g., VDD) of the device. Thereafter, circuitry associated with powering the chip is used to provide such ESD currents to the ground. Local clamps are more common, wherein the ESD currents are provided directly to ground from the pad or pin associated with the ESD event. Individual local clamps are typically provided at each pin on an IC, with the exception of the ground pin or pins.

SUMMARY

A semiconductor dual guard ring arrangement is provided which is useful during electrostatic discharge (ESD) events as well as during normal operating conditions. In particular, an inner guard ring that is located closer to an active area provides desirable performance during normal operating conditions, while an outer guard ring located further from the active area provides desirable performance during an ESD event.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram illustrating an example dual guard ring arrangement suitable for use with one or more NMOS transistors.

FIG. 2 is a schematic diagram illustrating an example dual guard ring arrangement suitable for use with one or more PMOS transistors.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Representative example embodiments are described.

FIG. 1 illustrates an example dual guard ring arrangement 100 that is suitable for use with one or more NMOS transistors. The illustration is a top view of the arrangement 100, which is formed on a semiconductor substrate 102, where the substrate 102 may comprise any type of semiconductor body (e.g., silicon, SiGe, SOI) such as a semiconductor wafer or one or more die on a wafer, as well as any other type of semiconductor and/or epitaxial layers grown thereon and/or otherwise associated therewith. Since the illustrated arrangement 100

has application to one or more NMOS transistors, the illustrated portion of the substrate 102 may be doped to have a p type electrical conductivity, such that the arrangement 100 can be said to be formed in a p type well in the substrate 102.

An active area 104 is centrally located in the arrangement 100. The active area 104 comprises a region of the substrate 102 wherein one or more semiconductor devices can be formed. As such, since this arrangement has application to NMOS devices, the active area 104 is doped to have an n type electrical conductivity, and can thus be said to comprise an n type well. Additionally, one or more regions of electrically conductive material 106, such as patterned polysilicon, for example, are formed over the active area 104 to serve as, at least part of, one or more NMOS transistor gates, for example.

A first guard ring 108 is formed in the substrate 102 around the active area 104 and the conductive regions 106. The first guard ring 108 is doped to have p type electrical conductivity. The guard ring 108 generally extends down to a subsurface or underlying substrate layer, such as a backgate region of the one or more NMOS transistors, for example. The first guard ring 108 is situated relatively close to the active area 104 to satisfy normal operating requirements. Although the distance 110 between the first guard ring 108 and the active area 104 may be technology dependent, the first guard ring 108 and the active area 104 are generally separated by a distance 110 of between about 0.25 and about 1.5 microns, for example.

A second guard ring 112 is formed in the substrate 102 around the first guard ring 108. Like the first guard ring 108, the second guard ring 112 comprises an area of the substrate 102 that is doped to have a p type electrical conductivity. The second guard ring 112 also generally extends down to a subsurface or underlying substrate layer, such as a backgate region of the one or more NMOS transistors, for example. The second guard ring 112 is distanced away from the active area 104 to satisfy requirements during an ESD event. The second guard ring 112 and the active area 104 are generally separated by a distance 114 of between about 2.5 and about 25 microns, for example.

A schematically illustrated inverter 120 is operatively coupled to the first guard ring 108. The inverter 120 comprises first and second transistors 122, 124, where the gates (G) of the transistors are coupled to a first voltage Vdd, which generally comprises a supply voltage. The source (S) of the first transistor 122 is also coupled to the supply voltage Vdd, while the

source (S) of the second transistor 124 is coupled to second voltage Vss, which generally corresponds to ground. The respective drains (D) of the first 122 and second 124 transistors are operatively coupled to the first guard ring 108. The second guard ring 112 is operatively coupled to the second voltage Vss.

As previously mentioned, the first or inner guard ring 108 operates during normal operating conditions, while the second or outer guard ring 112 becomes operational during an ESD event. The first guard ring 108 serves as a tap or input/output buffer for the n well active area 104 by inhibiting hot carriers and/or other undesirable particles or contaminants from entering into and exiting out of the active area 104. The distance 110 between the first guard ring 108 and the active area 104 is accordingly kept small to minimize any such adverse effects. For example, keeping the first guard ring 108 close to the one or more NMOS transistors that are touching pads mitigates well/ground bounce effects wherein well or ground voltages can be inadvertently changed. This orientation also mitigates noise injection where noise can be undesirably introduced into the circuitry. This orientation further facilitates appropriate latch up robustness whereby desired current flow is generated within and/or between devices.

The distance 114 between the first guard ring 108 and the active area 104 is kept large, on the other hand, to facilitate desired operation during ESD events. For example, during ESD conditions it is desirable to have tap guard rings placed far from the one or more NMOS transistors touching the pads. During human body model (HBM) ESD events, for example, locating the guard ring far from the devices facilitates increased resistance from the substrate 102 which is beneficial for the uniform conduction of the one or more NMOS transistors being protected. Similarly, during charged device model (CDM) ESD events the separation between the guard ring 108 and the devices facilitates enhanced gate to bulk oxide breakdown.

By way of further example, during normal operation Vdd is applied to the respective gates of the first 122 and second 124 transistors of the inverter 120. As such, the first guard ring 108 is pulled down to Vss through the connection to the respective drains of the devices 122, 124. As a result, both guard rings 108 and 112 are at Vss which is desirable for normal operating conditions. During an ESD event, however, Vdd is floating such that the respective drains of the first 122 and second 124 transistors of the inverter 120 are floating as well. As

such, the first guard ring 108 floats accordingly due to the coupling to the respective drains of the devices 122 and 124. Thus, merely the second or outer guard ring 112 is connected during an ESD event, which is desirable for the reasons described above.

Turning to FIG. 2, an example dual guard ring arrangement 200 is illustrated that is suitable for use with one or more PMOS transistors. The illustration is similar to that depicted in FIG. 1, except that electrical conductivities are reversed/opposite. Accordingly, the substrate 202 may be doped to have an n type electrical conductivity, such that the arrangement 200 can be said to be formed in an n type well in the substrate 202.

An active area 204 is centrally located in the arrangement 200. The active area 204 comprises a region of the substrate 202 wherein one or more semiconductor devices can be formed. As such, since this arrangement has application to PMOS devices, the active area 204 is doped to have a p type electrical conductivity, and can thus be said to comprise a p type well. Additionally, one or more regions of electrically conductive material 206, such as patterned polysilicon, for example, are formed over the active area 204 to serve as, at least part of, one or more PMOS transistor gates, for example.

A first guard ring 208 is formed in the substrate 202 around the active area 204 and the conductive regions 206. The first guard ring 208 is doped to have and n type electrical conductivity. The guard ring 208 generally extends down to a subsurface or underlying substrate layer, such as a backgate region of the one or more PMOS transistors, for example. As with the arrangement illustrated in FIG. 1, the first guard ring 208 is situated relatively close to the active area 204 to satisfy normal operating requirements. In particular, the first guard ring 208 and the active area 204 are generally separated by a distance 210 of between about 0.25 and about 2.5 microns, for example.

A second guard ring 212 is formed in the substrate 202 around the first guard ring 208. Like the first guard ring 208, the second guard ring 212 comprises an area of the substrate 202 that is doped to have an n type electrical conductivity. The second guard ring 212 also generally extends down to a subsurface or underlying substrate layer, such as a backgate region of the one or more PMOS transistors, for example. The second guard ring 212 and the active area 204 are generally separated by a distance 214 of between about 2.5 and about 25 microns, for example.

A schematically illustrated inverter 220 is operatively coupled to the first guard ring 208. The inverter 220 comprises first and second transistors 222, 224, where the source (S) of the first transistor 222 is coupled to a first voltage Vdd, which generally comprises a supply voltage. The source (S) of the second transistor 224 is coupled to a second voltage Vss, which generally corresponds to ground. The respective gates (G) of the transistors 222, 224 are also coupled to Vss. The respective drains (D) of the first 222 and second 224 transistors are operatively coupled to the first guard ring 208. The second guard ring 212 is operatively coupled to the source voltage Vdd.

As with the NMOS related arrangement 100 illustrated in FIG. 1, the first or inner guard ring 208 operates during normal operating conditions, while the second or outer guard ring 212 becomes operational during an ESD event. During normal operation, the application of Vss to the gates of the first 222 and second 224 transistors causes Vdd to be at the respective drains of the transistors 222, 224 such that the first guard ring 208 is pulled up to the Vdd through the connection to the drains of the devices 222, 224. As a result, both guard rings 208 and 212 are at Vdd which is desirable for normal operating conditions. During an ESD event, however, Vdd is floating such that the respective drains of the first 222 and second 224 transistors of the inverter 220 are floating as well. As such, the first guard ring 208 floats accordingly due to the coupling to the respective drains of the devices 222 and 224. Thus, merely the second or outer guard ring 212 is connected during an ESD event, which is desirable for the reasons set forth above.

Those skilled in the art to which the invention relates will appreciate that the described example embodiments are just some of the many embodiments and variations that may be implemented for the claimed invention.

CLAIMS

What is claimed is:

1. A semiconductor device including a protecting arrangement, comprising:

a first guard ring formed in a semiconductor substrate, the first guard ring having a first electrical conductivity type and surrounding an active area of the substrate that has a second electrical conductivity type;

a second guard ring formed in the substrate, the second guard ring having the first electrical conductivity type and surrounding the first guard ring, the second guard ring being coupled to a first voltage; and

an inverter operatively coupled to the first guard ring, the inverter causing the first guard ring to be at the first voltage during normal operating conditions and to float during an ESD event.

2. The device of claim 1, wherein the protecting arrangement takes the form of an NMOS dual guard ring arrangement, wherein the first guard ring is a p type first guard ring formed in a p type semiconductor substrate, the first guard ring surrounding an n type active area of the substrate, and the second guard ring is a p type second guard ring.

3. The device of claim 1, wherein the protecting arrangement takes the form of a PMOS dual guard ring arrangement, wherein the first guard ring is an n type first guard ring formed in an n type semiconductor substrate, the first guard ring surrounding a p type active area of the substrate; and the second guard ring is an n type second guard ring formed in the substrate.

4. The device of claim 1, 2 or 3, wherein at least one of:

a) the first guard ring and the active area are separated by a distance of between about 0.25 and about 2.5 microns; and

b) the second guard ring and the active area are separated by a distance of between about 2.5 and about 25 microns.2.The arrangement of claim 1, wherein the substrate has the first electrical conductivity type.

5. The device of claim 4, where the inverter comprises first and second transistors, the respective gates of the first and second transistors being coupled to a second voltage, the respective drains of the first and second transistors being coupled to the first guard ring, the source of the first transistor being coupled to one of the first and second

voltages and the source of the second transistor being coupled to the other of the first and second voltages.

6. The device of claim 5, wherein the first voltage comprises one of a ground voltage and a supply voltage, and the second voltage comprises the other of the gorund voltage and the supply voltage.

FIG. 1

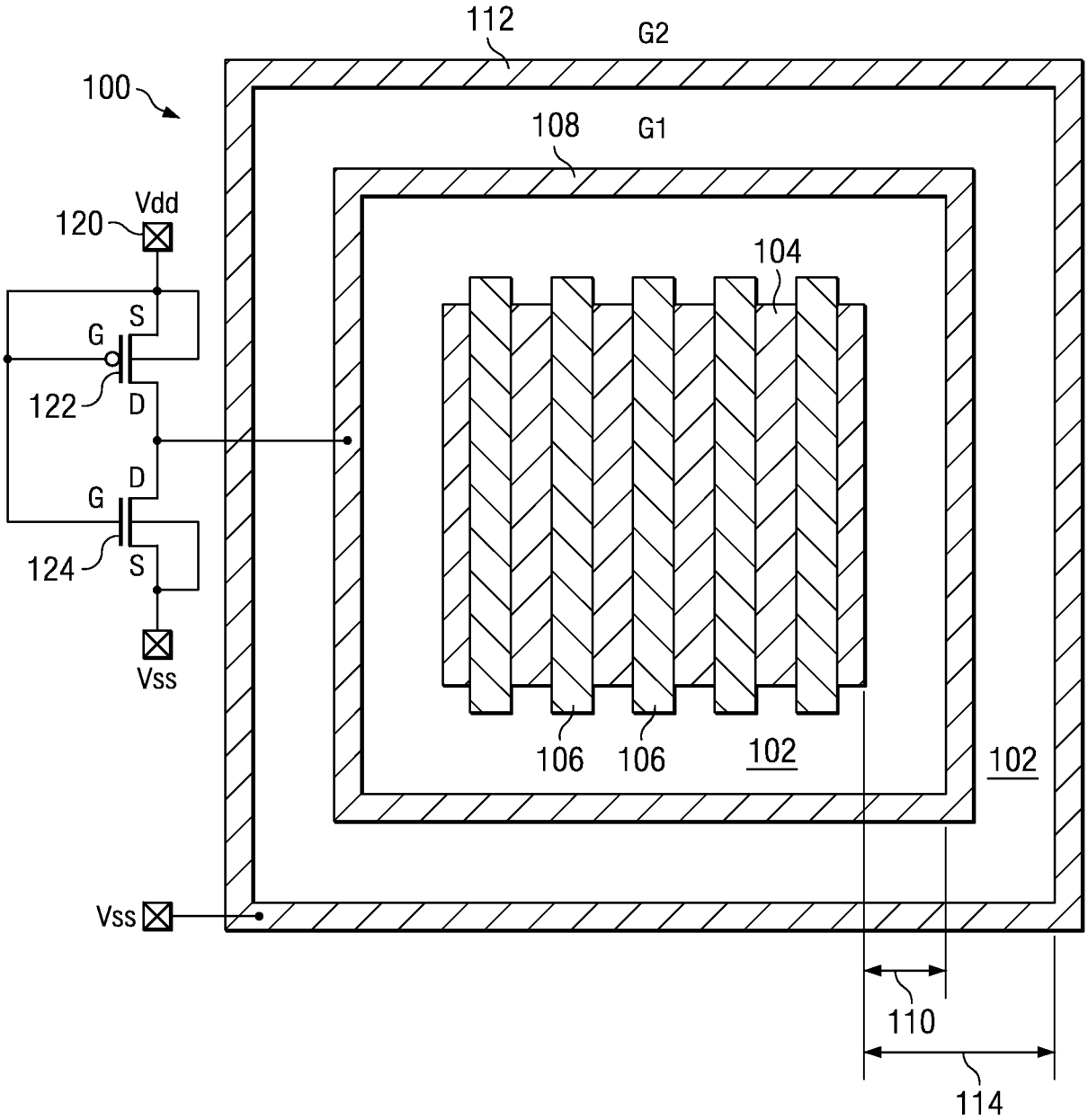
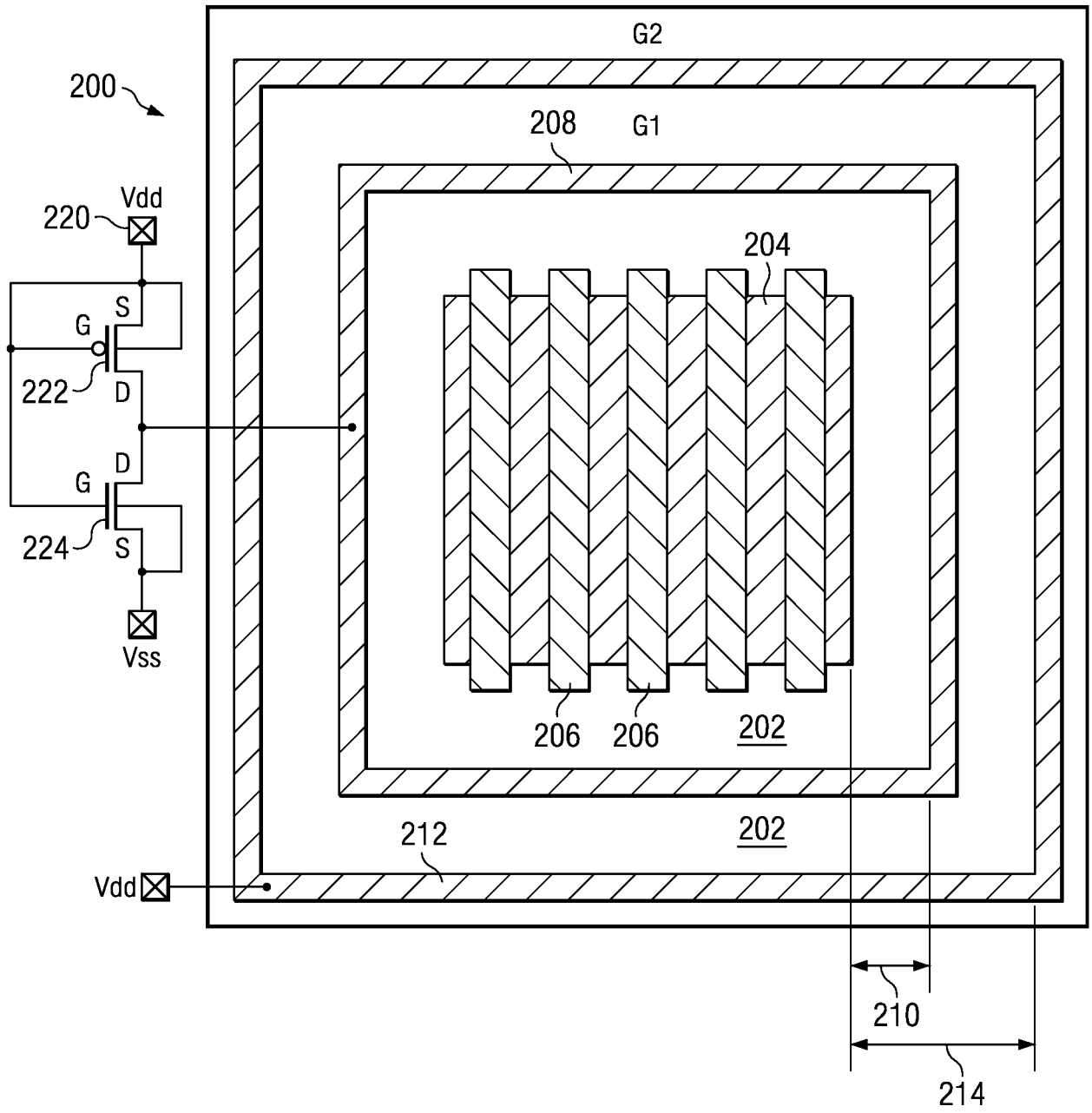

112
G2
100
108
G1
Vdd
120
104
S
G
122
D
D
G
124
S
Vss
106
106
102
102
Vss
110
114

FIG. 2


G2
200
208
G1
Vdd
220
204
S
G
222
D
D
G
224
S
Vss
206
206
202
212
202
Vdd
210
214