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(71) Applicant *(for all designated States except US)*: **VERTICAL CIRCUITS, INC.** [US/US]; 10 Victor Square, Scotts Valley, CA 95066 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **MCGRATH, Scott** [US/US]; 13 Terrace View Court, Scotts Valley, CA 95066 (US). **MCELREA, Simon, J.s.** [GB/US]; 621 Acorn Court, Scotts Valley, CA 95066 (US). **CASKEY, Terrence** [US/US]; 236 John Street, Santa Cruz, CA 95606 (US). **ANDREWS, Lawrence, Douglas** [US/US]; 22545 Old Santa Cruz Hwy., Los Gatos, CA 95033 (US). **DU, Yong** [CN/US]; 10190 N. Foothill Boulevard, Apt. F23, Cupertino, CA 95014 (US).

(74) Agent: **KENNEDY, Bill**; Haynes Beffel & Wolfeld Llp, P.o. Box 366, Half Moon Bay, CA 94019 (US).

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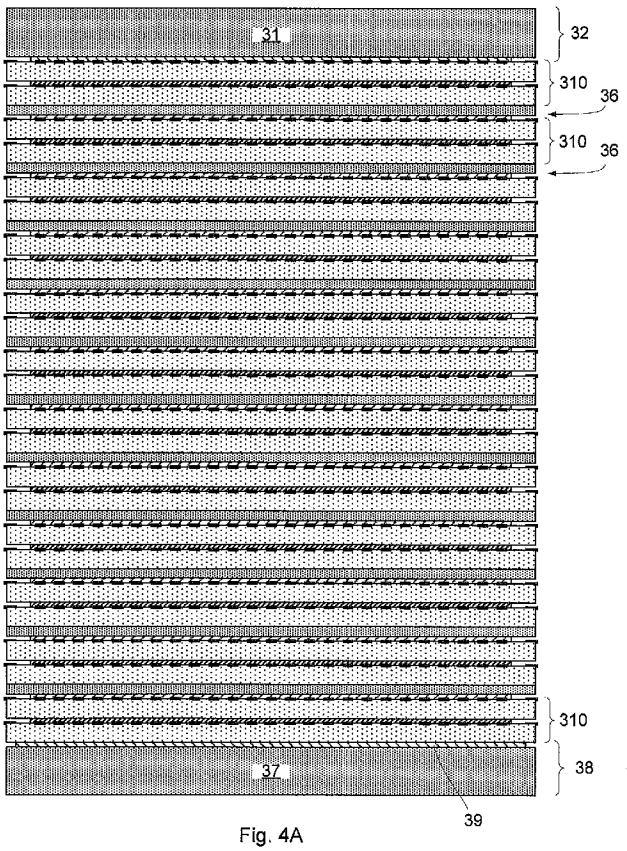

Fig. 4A

(57) Abstract: A method for forming electrical interconnection on stacked die units includes steps of arranging one or more stacked die units so that the arrangement presents die edges to be interconnected at a stack face, and applying a trace of electrical interconnect material at the presented stack face.

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METHOD FOR OPTIMIZED INTEGRATED CIRCUIT CHIP INTERCONNECTION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from S. McGrath *et al.* U.S. Provisional Application No. 60/943,252, filed June 11, 2007, titled "Coinstack method for optimized integrated circuit chip interconnection".

[0002] This application is related to S. McGrath *et al.* International Application Docket No. VCIX 1031-3, titled, "Semiconductor die coating and interconnection fixture and method", which is being filed on the same date as this application, and which claims priority from Z. Liu *et al.* U.S Provisional Application No. 60/943,211, filed June 11, 2007, titled "Semiconductor die coating and interconnection fixture method". Each application referenced herein is hereby incorporated by reference.

BACKGROUND

[0003] This invention relates to electrical interconnection of integrated circuit chips and, particularly, to interconnection of assemblies including one or more integrated circuit chips.

[0004] Interconnection of stacked die, and interconnection of die with the substrate presents a number of challenges.

[0005] Some die as provided have die pads along one or more of the die margins, and these may be referred to as peripheral pad die. Other die as provided have die pads arranged in one or two rows near the center of the die, and these may be referred to as center pad die. The die may be "rerouted" to provide a suitable arrangement of interconnect pads at or near one or more of the margins of the die.

SUMMARY

[0006] In various general aspects the invention features methods for electrical interconnection of die in a die stack, or of a die or a stack of die with underlying circuitry such as a substrate, and assemblies made by the methods.

[0007] In one general aspect the invention features a method for forming electrical interconnection on stacked die units, by arranging one or more stacked die units so that the arrangement presents die edges to be interconnected at a stack face, and applying a trace of electrical interconnect material at the presented stack face. In some embodiments corresponding die edges are presented at the stack face, and in some embodiments corresponding interconnect terminals or die pads at the stack face are aligned.

[0008] In some embodiments the interconnect material is applied using an application tool such as, for example, a syringe or a nozzle. The material exits the tool in a deposition direction generally toward the die pads or interconnect terminals, and the tool is moved over the presented stack face in a work direction. The material may be extruded from the tool in a

continuous flow, or, the material may exit the tool dropwise. In some embodiments the material exits the tool as a jet of droplets, and is deposited as dots which coalesce upon or following contact with a stack face surface. In some embodiments the deposition direction is generally perpendicular to the die edge surface, and in other embodiments the deposition direction is at an angle off perpendicular to the die edge surface. The tool may be moved in a generally linear work direction, or in a zig-zag work direction, depending upon the location on the various die of the corresponding terminals to be connected.

[0009] In some embodiments the method is carried out using a fixture to confine the stacked die units. The fixture may, for example, include first and second brackets and (optionally) separators. In such embodiments the method includes loading two or more stacked die units between the brackets in the fixture, optionally having separators between adjacent stacked die units in the fixture, and applying electrically conductive material to the stacked die units. In some such embodiments the loaded fixture generally defines a block having faces each constituting corresponding die edges, so that corresponding interconnect terminals on the die are aligned. In some such embodiments, where all corresponding aligned interconnects in all the die of the die unit are to be interconnected, a generally linear trace of conductive material contacting an interconnect terminal on one die and running generally perpendicular to the plane of the die contacts the corresponding interconnect terminal on all the die in the stacked die unit. In other embodiments fewer than all the corresponding aligned interconnects in all the die of the die unit are to be interconnected, and in such embodiments the application of interconnect material can be briefly interrupted as the deposition tool is moved in a work direction adjacent the block face.

[0010] The die units may in some embodiments be separated from one another by severing the interconnect traces. In some embodiments the die in each stacked die unit are affixed to one another by an adhesive, and in some embodiments the separators, where present, are not affixed to the die on either surface. In such embodiments the stacked die units in the block separate freely from one another when the interconnect traces are severed. Or, the deposition of interconnect material may be interrupted between the respective die stack units, so that release of the stacked die units from confinement frees the units. The deposition may be interrupted, for example, by interrupting the flow of material as the tool passes over the stack face between the respective die stack units; or, the deposition may be interrupted by preventing the material from reaching the stack face between the respective die stack units, for example by employing a mask and liftoff process.

[0011] The described methods provide for interconnection of die stacks having any desired number of die; larger stacks may be divided into smaller stacks and the smaller stacks may be subdivided into still smaller stacks, as may be desired.

[0012] In another general aspect the invention features a fixture suitable for carrying out the method.

[0013] In another general aspect the invention features stacked die assemblies and stacked die units made according to the method.

[0014] In another general aspect the invention features stacked die units or stacked die assemblies electrically interconnected with circuitry in a device for use. In some embodiments the stacked die assembly is interconnected such that the die nearest the underlying circuitry is oriented with the active side of the die facing toward the underlying circuitry; in other embodiments the stacked die assembly is interconnected such that the die nearest the underlying circuitry is oriented with the back side of the die facing toward the underlying circuitry. Not all the die in the stack need be oriented with the active side facing the same way; some die in the stack may be mounted back-to-back, or face-to-face, for example.

[0015] In another general aspect the invention features a mountable stacked die assembly, having second-level interconnects at the active side of a die at one end of the stack.

[0016] The assemblies according to the invention can be used for building computers, telecommunications equipment, and consumer and industrial electronics devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIGs. **1A** - **1F** are diagrammatic sketches in sectional view showing examples of various die edge configurations.

[0018] FIGs. **2A** - **2F** are diagrammatic sketches in sectional view showing die stack assemblies of die having die edge configurations as in FIGs. **1A** - **1F**.

[0019] FIG. **3A** is a diagrammatic sketch in elevational view showing a part of a fixture according to an embodiment of the invention.

[0020] FIG. **3B** is a diagrammatic sketch in elevational view showing a two-die stack.

[0021] FIG. **3C** is a diagrammatic sketch in elevational view showing a part of a fixture according to an embodiment of the invention.

[0022] FIGs. **4A** through **4C** are diagrammatic sketches in elevational view showing stages in a "coinstack" process according to an embodiment of the invention for electrically interconnecting two-die stacks to form two-die stack assemblies.

[0023] FIG. **5** is a diagrammatic sketch in elevational view showing a four-die stack.

[0024] FIGs. **6A** through **6C** are diagrammatic sketches in elevational view showing stages in a "coinstack" process according to an embodiment of the invention for electrically interconnecting four-die stacks to form four-die stack assemblies.

[0025] FIGs. **7A** and **7B** are diagrammatic sketches in a sectional view showing stacking of two four-die stack assemblies made as described with reference to FIGs. **6A** - **6C** to form an eight-die stack assembly according to an embodiment of the invention.

[0026] FIG. **8** is a diagrammatic sketch in a perspective view showing a four-die stack; the interconnects are omitted from this Figure to avoid obscuring certain details.

[0027] FIG. **9** is a diagrammatic sketch in a perspective view showing a four-die stack situated in relation to a substrate; the interconnects are omitted from this Figure to avoid obscuring certain details.

[0028] FIGs. **10A** and **10B** are diagrammatic sketches in a sectional view showing stages in mounting a four-die stack assembly as in FIG. **7A** on a substrate according to an embodiment of the invention.

[0029] FIGs. **11A** and **11B** are diagrammatic sketches in a sectional view showing stages in mounting a four-die stack assembly as in FIG. **7A** on a substrate according to another embodiment of the invention.

[0030] FIGs. **12** through **14** are diagrammatic sketches in sectional view showing interconnection processing of various die stacking arrangements according to embodiments of the invention.

DETAILED DESCRIPTION

[0031] The invention will now be described in further detail by reference to the drawings, which illustrate alternative embodiments of the invention. The drawings are diagrammatic, showing features of the invention and their relation to other features and structures, and are not made to scale. For improved clarity of presentation, in the FIGs. illustrating embodiments of the invention, elements corresponding to elements shown in other drawings are not all particularly renumbered, although they are all readily identifiable in all the FIGs. Also for clarity of presentation certain features are not shown in the FIGs., where not necessary for an understanding of the invention.

[0032] FIGs. **1A - 1F** show examples of various die edge configurations in die to be interconnected according to various embodiments of the invention.

[0033] FIG. **1A** shows a die having an "off-die" interconnect. The die is shown in a partial sectional view, having an active side **15** at which the integrated circuitry **11** of the die is formed, and a die edge **19**. In an off die configuration an interconnect terminal **22** is bonded to an interconnect pad (die pad) **13**. The die pad may be a peripheral die pad in the die as provided, or it may be situated at or near the die periphery as a result of rerouting of the die circuitry. The interconnect terminal may be, for example, a wire (formed for example in a wire bond operation) or a tab or ribbon (formed for example in a ribbon bond operation). The interconnect terminal **22** extends outwardly beyond the die edge **19** (hence, "off-die" terminal).

[0034] FIG. 1B shows a die having a bump or glob 23 of an electrically conductive polymer material deposited onto the die pad 13. The glob may be shaped (as in the example of FIG. 1B, so that it extends toward the die edge, and may extend to the die edge or (as in the

example shown) slightly beyond the die edge 19; it may be in the shape of a thumb, for example. Alternatively, the glob may be formed entirely above the pad, as shown in FIG. 2B. The conductive polymer material may be, for example, a curable conductive polymer such as a conductive epoxy.

[0035] FIG. **1C** shows a die having an interconnect terminal **24** formed in or at the active side of the die, at or near the margin of the die where the active side **15** of the die meets the die edge **19**. Such a marginal interconnect terminal may be an extension of a die pad, for example, and may be situated at or near the die margin as a result of rerouting of the die circuitry.

[0036] FIG. **1D** shows a die having an interconnect terminal **26** formed in the die edge **19**. The interconnect terminal may be connected to the integrated circuitry of the die by attachment of a pad of conductive material to an extension of the die pad, for example, or to rerouting circuitry.

[0037] FIG. **1E** shows a die having an interconnect terminal formed so that it wraps around a chamfer that is formed at the intersection of the die edge with active side **15** of the die. Such a wraparound terminal has a terminal portion **27** on the chamfer, and a terminal portion **28** on the die edge. A similar wraparound terminal may be formed over the intersection of the die edge with the active side of the die, where no chamfer is present.

[0038] FIG. **1F** shows a die having an interconnect terminal formed so that it wraps around a chamfer that is formed at the front side die edge (at the intersection of the die sidewall with active side **15** of the die), and further around a chamfer that is formed at the back side die edge (at the intersection of the die sidewall with back side **17** of the die). Such a wraparound terminal has a terminal portion **27** on the front edge chamfer, and a terminal portion **28** on the die sidewall, and a terminal portion **29** on the back edge chamfer.

[0039] FIGs. **2A** - **2F** show stacked die units (in these examples, each having three die in the stack), of die as in, respectively, FIGs. **1A** - **1F**. As FIG. **2A** shows, the off-die terminals project at the stack face, making them available for connection by a variety of methods. As FIGs. **2B** and **2C** show, interconnect terminals **24** in the margin of the active side of the die are beneath the margins of die stacked over them (except that the active side of one of the die is exposed and readily accessible for interconnection). As FIGs. **2D** - **2F** show, by contrast, interconnect terminals **26** formed in the die edge **19** (FIG. **1D**), and wraparound interconnect terminals **27**, **28** (FIG. **1E**) and wraparound interconnect terminals **27**, **28**, **29** (FIG. **1F**) are presented at the stack face.

[0040] FIG. **3B** shows a two-die stack **310** viewed in an edge-on elevational view. Each of the die **326**, **346** can have a number of interconnect terminals arranged along the die margins at the front side of the die, as illustrated by way of example in FIGs. **1A** - **1F** and **2A** - **2F**. For illustration, the front side **328** of die **326** has a row of interconnect terminals **329** along the die

margin adjacent the face-on die edge **312**, and a row of interconnect terminals, *e.g.*, terminal **330** along each perpendicular edge. Die **346** can also have a row of interconnect terminals along the die margin adjacent the face-on die edge **314**, and a row of interconnect terminals, *e.g.*, terminal **340** along each perpendicular edge. The die are affixed in the two-die stack **310** by an adhesive **316** between the back side of die **326** and the front side of die **346**. The adhesive may include, for example, a die attach film; or an adhesive preform such as an epoxy preform; or a liquid die attach adhesive such as a die attach epoxy. The adhesive may be a die attach film applied to the die at a wafer processing (or die array processing) stage. Where spacing between the die is required, the adhesive **316** may constitute a spacer, particularly if the adhesive includes a preform or a die attach film having a suitable thickness. Or, where an off die terminal such as, for example, a bump or glob is employed, as described above with reference to FIGs. **1B**, **2B**, the bump or glob may serve as a spacer, provided the overlying die backside is electrically insulated (such as by a thin film adhesive applied to the back of the die) and provided the bump or glob is formed to have a suitable height above the pad.

[0041] FIGs. **3A** and **3C** show elements constituting a fixture useful for application of electrical interconnects in a single operation onto a number of two-die stacks. Referring to FIGs. **3A**, **3B**, **3C**, and **4A**, the fixture includes a first (top) end bracket **32** including a top bracket body portion **31** and a spacer portion **33**; a second (bottom) end bracket **38** including a bottom bracket body portion **37** and a spacer portion **39**; and a number of (optional) separators **36** each including a separator body portion **35** and a spacer portion **37**.

[0042] The spacer portions of the end brackets and of the separator may be formed by machining the brackets or the separator.

[0043] In some embodiments the dimensions (length and width) of the top and bottom bracket body portions and of the separator body portion are the same as (or about the same as) the dimensions (length and width) of the die to be processed in the fixture. The spacer portions of the top bracket and of the separators contact the front side of the die and, accordingly, the spacer portions of the top bracket and of the separators can be smaller, so that when the die units are stacked in the fixture, the spacer portions do not impinge upon the interconnect terminals.

[0044] Spacers may not be required. In some embodiments one or both of the end brackets lack a spacer or spacer portion, or the separators (or some of them) lack a spacer or spacer portion.

[0045] FIG. **4A** shows a fixture loaded with two-die stack units for processing according to an embodiment of the invention. Loading the fixture begins by supporting the bottom bracket **38**; stacking a first die unit **310** on the bottom bracket **38** so that the back side **347** of the first die **346** contacts the surface of the spacer portion **39** of the bottom bracket **38**; stacking a

separator **36** on the first die unit **310** so that the surface of the spacer portion **37** contacts the front side **328** of the second die **326**; stacking a second die unit **310** on the first separator **36** so that the back side **347** of the first die **346** contacts the surface of the first separator body **35**; stacking a second separator **36** on the second die unit **310** so that the surface of the spacer portion **37** contacts the front side **328** of the second die **326**; and so on, alternating a separator and a die unit until a suitable number of die units have been loaded in the fixture; and then stacking a top bracket **32** onto the uppermost die unit so that the surface of the spacer portion **33** of the top bracket **32** contacts the front surface **328** of the uppermost die unit. The result is shown in FIG. **4A**. Four faces are available for interconnection, each presenting corresponding edges of all the die; one face is directed toward the viewer of the FIGs.; one (opposite) face is directed away from the viewer; a face is directed to the right side, and a face is directed to the left side. The fixture may include guides (not shown in the FIGs.) for alignment of the elements in the stack. A clamping force can then be applied to the loaded fixture to secure the stacked die units and (optional) separators during further handling.

[0046] As FIG. **4A** shows, the interconnect terminals of all the die in this embodiment are vertically aligned, so that an electrically conductive material can be applied to interconnect the die in all the die units in a single operation.

[0047] In one embodiment of the interconnect process, shown by way of example in FIG. **4B**, an electrically conductive material such as a conductive epoxy is applied using a capillary dispenser moving from a beginning point at the end of a surface of one bracket (*e.g.*, at **41** at the left end of the presenting surface of the bottom bracket **37**) in a serpentine pattern **42** across the face of the assembly to an ending point at the opposite end of a surface of the other bracket (*e.g.*, at **43** at the right end of the presenting surface of the bracket **31**). The electrically conductive material is then applied to the remaining faces in turn, as shown for example at **44** and **46**.

[0048] Then the tracts of electrically conductive material are severed at the separator elements, for example by forcing a blade through the tracts against each separator body. The clamping force is released, allowing separation of the interconnected die units **410** from the respective fixture elements **432**, **438**, **436**, as shown in FIG. **4C**. The corresponding interconnect terminals in each die unit are now interconnected, by (for example) interconnects **442** (on the presenting faces), and **446** and **444** (on faces perpendicular to the presenting face). End portions **431**, **439** of the interconnect material can then be removed from the end brackets **432**, **438**, and the fixture elements can be re-loaded for a subsequent interconnect operation.

[0049] FIGs. **5** and **6A - 6C** are similar to FIGs. **3B** and **4A - 4C**, except that these FIGs. illustrate use of a fixture to apply interconnections to a number of four-die units according to an embodiment of the invention.

[0050] FIG. **5** shows a four-die stack **510** viewed in an edge-on elevational view. Each of the die **526**, **546**, **566**, **586** has a number of interconnect terminals bonded to interconnect pads arranged along the die margins at the front side of the die.

[0051] The elements of FIGs. **3A** and **3C** can be employed in a fixture useful for application of electrical interconnects in a single operation onto a number of four-die stacks. Referring to FIG. **6A**, the fixture includes a first (top) end bracket **52** including a top bracket body portion and a spacer portion; a second (bottom) end bracket **58** including a bottom bracket body portion and an optional spacer portion; and a number of optional separators **56** each including a separator body portion and a spacer portion.

[0052] FIG. **6A** shows a fixture loaded with four-die stack units for processing according to an embodiment of the invention. Loading the fixture begins by supporting the bottom bracket **58**; stacking a first die unit **510** on the bottom bracket **58** so that the back side of the first die contacts the surface of the spacer portion of the bottom bracket **58**; and then alternately stacking separators **56** and die units **510** until a suitable number of die units have been loaded in the fixture; and then stacking a top bracket **52** onto the uppermost die unit so that the surface of the spacer portion of the top bracket **52** contacts the front surface of the uppermost die unit. The result is shown in FIG. **6A**. Four faces are available for interconnection, each presenting corresponding edges of all the die; one face is directed toward the viewer of the FIGs.; one (opposite) face is directed away from the viewer; a face is directed to the right side, and a face is directed to the left side. The fixture may include guides (not shown in the FIGs.) for alignment of the elements in the stack. A clamping force is then applied to the loaded fixture to secure the stacked die units and spacers during further handling. As FIG. **6A** shows, the interconnect terminals of all the die are vertically aligned, so that an electrically conductive material can be applied to interconnect the die in all the die units in a single operation.

[0053] In one embodiment of the interconnect process, shown by way of example in FIG. **6B**, an electrically conductive material such as a conductive epoxy is applied using a capillary dispenser moving from a beginning point at the end of a surface of one bracket (*e.g.*, at **61** at the left end of the presenting surface of the bottom bracket **67**) in a serpentine pattern **62** across the face of the assembly to an ending point at the opposite end of a surface of the other bracket (*e.g.*, at **63** at the right end of the presenting surface of the bracket **31**). The electrically conductive material is then applied to the remaining faces in turn, as shown for example at **64** and **66**.

[0054] Then the tracts of electrically conductive material are severed at the separator elements, for example by forcing a blade across the tracts against each separator body. The clamping force is released, allowing separation of the interconnected die units **610** from the respective fixture elements **652**, **658**, **636**, as shown in FIG. **6C**. The corresponding interconnect terminals in each die unit are now interconnected, by (for example)

interconnects **642** (on the presenting faces), and **646** and **644** (on faces perpendicular to the presenting face). End portions **631**, **639** of the interconnect material can then be removed from the end brackets **652**, **658**, and the fixture elements can be re-loaded for a subsequent interconnect operation.

[0055] In the embodiments shown here for illustration, the interconnect material is deposited by moving the deposition tool in a series of antiparallel lines running generally perpendicular to the active sides of the die. In other embodiments (not shown in the FIGs.) this simple pattern may be varied and, in some embodiments the deposition tool may be moved in a zig-zag or dogleg course over the stack face, to connect selected interconnect terminals. In some embodiments the deposition of material onto the stack face may be interrupted, particularly for example at one or both the top and bottom brackets, and particularly for example at the areas of separation of the respective stacked die units, so that it is not necessary to sever interconnect traces crossing the separation areas. Interruption of the deposition may be accomplished, for example, by a momentary stoppage of the flow of the material from the tool. Or, a mask may be placed over the separation areas prior to deposition and then stripped away following deposition, to remove the material from the masked areas in a lift-off process.

[0056] In some embodiments two or more deposition tools are employed at once to deposit interconnect material in the stack face. A row or an array of nozzles may be employed, for example, to deposit the interconnect material.

[0057] The method according to various embodiments of the invention can be suitable for interconnection of die having any of various interconnect terminal forms and die edge configurations, and the interconnect terminals are indicated symbolically in these FIGs. **3A - 3C**, **4A - 4C**, **5**, and **6A - 6C**. That is, they are intended to represent die having any of various die edge configurations. Some die edge configurations are discussed above with reference to FIGs. **1A - 1F**, for example. In some embodiments the interconnect material as applied (such as an electrically conductive epoxy) has some capacity to flow into the space at the margin between adjacent die, to make electrical connection with interconnect terminals in the margin at the active side of the die.

[0058] According to the invention, a number of stacked die units each made up of a selected number of die (*e.g.*, two-die stacks, four-die stacks) can be electrically interconnected in a single operation, rather than in a separate operation for each of the units. Stacks of 2^n die (*e.g.*, 2, 4, 8, 16, 32, or 64 die; or more) in a stacked die unit may be desirable for some uses, but any desired number of die may be interconnected in a stacked die unit according to various embodiments of the invention.

[0059] The die may be all of the same size, as shown in the FIGs, but die of different sizes may be stacked and interconnected according to the invention. In some embodiments for example, a smaller die may be stacked on a larger die, with the smaller die situated so that

peripheral die pads on the larger die are available for interconnection. The die may be larger in one dimension (that is, the same width but one longer than the other), or in both directions (that is, one die both wider and longer than the other). For example, a 10 x 10 mm die may be stacked over a 10 x 12 mm die having peripheral pads at the shorter edges. In such an embodiment the smaller die is situated over the larger die such that the die pads at the narrow ends of the larger die are exposed adjacent two edges of the smaller die. Or, for example, a 10 x 10 mm die may be stacked over a 12 x 12 mm die, and situated such that peripheral pads along any one or more (or all four) edges of the larger die are available for interconnection.

[0060] Additionally, or alternatively, larger stacked die assemblies may be made by constructing stacked die units in a modular design, and then stacking modules. The stackable units are robust and testable. For example, particular two-die units and four die units may constitute modules; from these modules a six-die assembly may be made by stacking a two-die unit and a four-die unit, or an eight-die assembly may be made by stacking two four-die units, for example. For illustration, FIGs. **7A** and **7B** show construction of an eight-die assembly **714** by stacking two four-die assemblies **710**, **712**. The interconnects on the assembly **710** may be connected to respective interconnects on the assembly **712** using spots of conductive epoxy. In the embodiment shown in FIGs. **7A**, **7B** an adhesive **717** contacts the active side **717** of a die in the unit **712** and the backside of a die **710** in the unit **710**, to secure the four-die units. Alternatively, the adhesive **717** may optional, as the assemblies may be secured by the conductive epoxy spots only. In this example the die have off-die interconnect terminals, and the projecting portions of the interconnect terminals are effectively embedded in the interconnect material. Die having other edge configurations can be stacked in such a manner. The interconnects of the unit **710** contact the interconnects of the unit **712** to complete the interconnection of all eight die in the assembly.

[0061] Stacked die units or assemblies constructed according to the invention can be electrically interconnected with circuitry in a device for use. For example, a stacked die unit can be mounted upon the active side of another die, and electrically interconnected by connection of all or selected ones of the interconnects of the unit with pads on the die. Or, for example, a die stack assembly can be mounted on a substrate, and electrically interconnected by connection of all or selected ones of the interconnects of the unit with leads in the substrate.

[0062] Turning now to FIG. **8**, there is shown in a perspective view a stack **10** of four semiconductor die **12**, **14**, **16**, **18**, in a die stack assembly, in which the die have off-die interconnect terminals. To avoid obscuring certain of the details, the interconnects are not shown in this Figure or in FIG. **9**. The die stack assembly may be mounted on underlying circuitry, such as on another die, or such as on a substrate, as indicated generally at **20** in

FIG. **9**. Each die has two larger generally parallel, generally rectangular (for example square) sides, and four edges. One larger side may be referred to as the front side, and the other may be referred to as the back side. The circuitry of the die is situated at or near the die surface at the front side, and so the front side may be referred to as the active side of the die. In the view presented in FIGs. **8** and **9** the die are shown with the respective active sides facing away from the substrate **20**, so that the front side **124** of die **12** is visible. Also visible in the view shown in FIGs. **8** and **9** are edges **122**, **126** of die **12**, edges **142**, **146** of die **14**, edges **162**, **166** of die **16**, and edges **182**, **186** of die **18**. Margins of the die are adjacent the edges; for example, margins **127** and **123** are adjacent the edges **126** and **122** on the back side of die **12**, and margins **125** and **121** are adjacent the edges **126** and **122** on the front side of die **12**. The die in the example shown in FIGs. **8** and **9** have off-die interconnects; other interconnect configurations are contemplated, as described for example with reference to FIGs. **1A - 1F** and **2A - 2F**. In an off-die configuration as shown in FIGs. **8** and **9**, interconnect terminals **129** are bonded to interconnect pads **128** in or near the margin **125** at the active side **124** of die **12**, interconnect terminals **149** can be optionally bonded to interconnect pads in or near the margin at the active side of die **14**, interconnect terminals **169** can be optionally bonded to interconnect pads in or near the margin at the active side of die **16**, and interconnect terminals **189** can be optionally bonded to interconnect pads in or near the margin at the active side of die **18**. The interconnect terminals, if provided, can project outward beyond the die edge as in the embodiments shown in the FIGs.

[0063] A substrate **20**, shown also in FIG. **9**, has a die attach side **224**, on which bond pads **228** are situated. A number of substrates **20** may be provided in a row or array, as suggested by the broken lines **X**; at some stage in the process, the substrates are separated, for example by sawing or punching. Each substrate has edges, of which edge **226** and **222** are visible in the view shown in FIGs. **8** and **9**; and margins of the substrate are adjacent the substrate edges; for example margins **227** and **221** are adjacent the edges **226** and **222** on the die attach side **224** of the substrate **20**, and margins **225** and **223** are adjacent the edges **226** and **222** on the obverse side of the substrate **20**. The substrate can be configured to provide for second-level interconnection to underlying circuitry in a device for use, by lands on the side of the substrate opposite the die attach side; as is well known, to form a ball grid array stacked die package, for example, the substrate may be provided with an array of solder balls on interconnect sites on the lands.

[0064] In the embodiment shown by way of example in FIGs **8** and **9**, the bond pads **228** are arranged in two rows, one generally parallel to the margin **227** and one generally parallel to the opposite margin. The locations of the bond pads correspond to the locations of the interconnect terminals on the die, when the die is mounted onto the substrate. Accordingly, the interconnect pads on the die in the examples illustrated in these examples are arranged

along two opposite margins. Other arrangements of bond pads are contemplated, according to the arrangements of pads on the particular die. In other embodiments the interconnect pads on the die may be situated along one die margin, or along three or all four margins; and the bond pads on the substrate in such embodiments are arranged correspondingly. Bond pads on the substrate may be arranged in two or more rows of pads along any one or more boundaries of the die footprint; and the bond pads may be interdigitated. In some embodiments, certain of the pads on a given die may not be connected to other die in the stack; for example, "chip select" or "chip enable" pins on a given die may be connected to underlying circuitry (on the substrate, for example), but not to other die. In such embodiments the terminals from such pads may be fanned out horizontally to interconnect pads along an edge of the die.

[0065] Die assemblies made according to embodiments of the invention, such as two-die assemblies **410**, or four-die assemblies **610**, or others, can be mounted on and electrically connected with a substrate as shown for example in FIGs. **10A** and **10B**, showing an embodiment in which the die are mounted facing away from the substrate, or for example in FIGs. **11A** and **11B**, showing an embodiment in which the die are mounted facing toward the substrate.

[0066] FIG. **10A** shows a substrate **80** having bond pads **86** exposed at a die attach side for interconnection. The four-die assembly **88** is oriented in this embodiment with the back side **81** of a die in the assembly facing toward the die attach side of the substrate. In the embodiment shown in FIGs. **10A**, **10B**, the four-die assembly **88** is affixed to the substrate using a die attach adhesive **84**, which may be applied to the substrate (as shown by way of example in FIG **10A**) or to the surface **81** of the die assembly. In some embodiments the electrical connection is secured by depositing a spot of a conductive material on the bond pad. The electrically conductive material may be a curable material such as a conductive epoxy, for example. The ends of the conductive elements on the die assembly are pressed against the spots, and then the assembly is treated to cure the spots, to complete the interconnection, as shown at **83** in FIG. **10B**. In some embodiments the adhesive **84** is omitted, and the assembly **88** is secured to the substrate **80** by the conductive epoxy spots only.

[0067] FIG. **11A** shows a substrate **90** having bond pads **96** exposed at a die attach side for interconnection. The four-die assembly **98** is oriented in this embodiment with the front side **91** of a die in the assembly facing toward the die attach side of the substrate. The four-die assembly **98** can optionally be affixed to the substrate using, for example a die attach adhesive **94**, and a spacer may optionally be situated between the die front side **91** and the adhesive **94**. The adhesive **94** may be applied to the substrate (as shown by way of example in FIG **9A**), or it may be applied to the die surface **91**. A spacer **95** may be employed and, where a spacer is employed, it may be applied to the die surface **91**, or it may be applied to an

adhesive, *e.g.* **94**, on the substrate. Or, an adhesive/spacer may be employed, including for example an adhesive containing glass or polymer spheres (for example) dimensioned to provide a suitable standoff between the die surface **91** and the die attach surface of the substrate. In some embodiments the electrical connection is secured by depositing a spot of a conductive material on the bond pad. The electrically conductive material may be a curable material such as a conductive epoxy, for example. The ends of the conductive elements on the die assembly are pressed against the spots, and then the assembly is treated to cure or reflow the spots, to complete the interconnection, as shown at **93** in FIG. **11B**.

[0068] Alternatively, an assembly may be oriented with the front side of a die in the assembly facing toward the die attach side of the substrate, as shown in FIG. **11A**, but not affixed to the substrate using an adhesive. In such embodiments, the assembly may be secured to the substrate by the electrically conductive material joining the interconnects with the bond pads. The narrow space between the die and the substrate can later be underfilled.

[0069] In some embodiments, a conformal coating of, for example, a parylene, may be employed to electrically insulate the die, to protect the die, and to provide for adhesion of adjacent die in the stack or for adhesion of the die stack to a substrate. That is, in some instances where an adhesive is called for in the description above, the adhesive may be (or include) a conformal coating of parylene; where a spacer is required, a parylene coating may be used in combination with a spacer such as a preform, or a die attach film, for example, or any other suitable spacing feature.

[0070] In the embodiments described above, the die are stacked with the respective die edges vertically aligned. Other arrangements are contemplated by the invention. For example, successive die in the stack may be offset, so that a margin of each die is exposed, as illustrated in FIGs. **12** and **13**. FIG. **12** shows a stack of offset die, in which the interconnect terminals are situated at or near the exposed margins. For the interconnect process, the stack may be supported, for example, at the back side of the lowest of the die in the stack, and the interconnect material can be deposited in a deposition direction (two possible deposition directions are shown: **D1** generally perpendicular to the surface of the interconnect terminal, and **D2** at an angle away from perpendicular) while the tool is moved in a work direction **W**. FIG. **13** shows a stack of offset die, in which the interconnect terminals are situated at the edges of the die. For the interconnect process, the stack may be supported, for example, edgewise, and the interconnect material can be deposited in a deposition direction (two possible deposition directions are shown: **D1** generally perpendicular to the surface of the interconnect terminal, and **D2** at an angle away from perpendicular) while the tool is moved in a work direction **W**. Or, for example, the die may be stacked in a staggered arrangement, as illustrated in FIG. **14**, and alternating ones of the die can be interconnected. For the interconnect process, the stack may be supported, for example, at the back side of the lowest

of the die in the stack, and the interconnect material can be deposited in a deposition direction (two possible deposition directions are shown: **D1** generally perpendicular to the surface of the interconnect terminal, and **D2** at an angle away from perpendicular) while the tool is moved in a work direction **W**.

[0071] In the various embodiments of the invention as described above, individual die are stacked and treated. In other embodiments certain of the steps can be carried out at a wafer level, or by treatment of a block or row of die, rather than of single die.

[0072] Other embodiments are within the scope of the invention. For example, an additional die may be mounted in a flip-chip manner onto a die in an assembly of die that are interconnected according to the invention.

CLAIMS

We claim:

1. A method for forming electrical interconnection on stacked die units, comprising arranging one or more stacked die units so that the arrangement presents die edges to be interconnected at a stack face, and applying a trace of electrical interconnect material at the presented stack face.

2. The method of claim 1 wherein corresponding die edges are presented at the stack face.

3. The method of claim 1 wherein corresponding interconnect terminals or die pads at the stack face are aligned.

4. The method of claim 1 wherein applying a trace comprises dispensing the material using an application tool.

5. The method of claim 4 wherein using an application tool comprises dispensing the material through a syringe.

6. The method of claim 4 wherein using an application tool comprises dispensing the material through a needle.

7. The method of claim 4 wherein using an application tool comprises dispensing the material through a nozzle.

8. The method of claim 4 wherein applying a trace comprises dispensing the material in a continuous flow.

9. The method of claim 4 wherein applying a trace comprises dispensing the material in a dropwise manner.

10. The method of claim 4 wherein applying a trace comprises dispensing the material in a pulsed flow.

11. The method of claim 4 wherein applying a trace comprises dispensing the material in a selectively interrupted flow.

12. The method of claim 4 wherein the material exits the tool in a deposition direction generally toward the die pads or interconnect terminals, and the tool is moved over the presented stack face in a work direction.

13. The method of claim 12 wherein the tool is moved over the presented stack face in a generally linear work direction.

14. The method of claim 12 wherein the tool is moved over the presented stack face in a zig-zag work direction.

15. The method of claim 1, further comprising providing a fixture comprising first and second brackets configured and dimensioned to hold arranged stacked die units, loading the arranged stacked die units in the fixture, and applying electrically conductive material to the stacked die units.

16. The method of claim 15, the loaded fixture generally defining a block having faces each constituting corresponding die edges, so that corresponding interconnect terminals on the die are aligned.

17. The method of claim 16 wherein corresponding aligned interconnects in all the die of the die unit are to be interconnected, and wherein applying interconnect material comprises forming a generally linear trace of conductive material contacting an interconnect terminal on one die and running generally perpendicular to the plane of the die and contacting the corresponding interconnect terminal on all the die in the stacked die unit.

18. The method of claim 16 wherein corresponding aligned interconnects in fewer than all the corresponding aligned interconnects in all the die of the die unit are to be interconnected, and wherein applying interconnect material comprises forming a generally linear trace of conductive material contacting an interconnect terminal on one die and running generally perpendicular to the plane of the die and contacting a corresponding interconnect terminal on another die to be

interconnected, the trace being interrupted where its trajectory passes over an interconnect terminal on a die that is not to be interconnected.

19. The method of claim 18 wherein the trace is interrupted by interrupting deposition of the material.

20. A fixture for interconnecting stacked die units, comprising first and second brackets configured and dimensioned to hold the stacked die units in a selected arrangement.

21. The fixture of claim 16, further comprising a separator interposable between adjacent stacked die units.

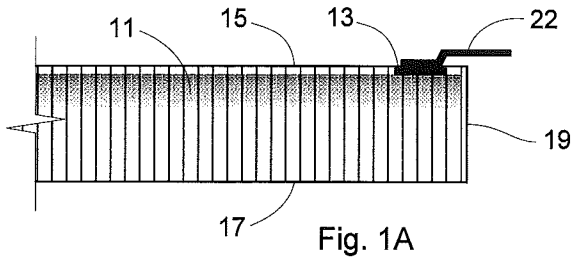

Fig. 1A

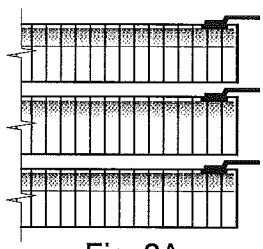

Fig. 2A

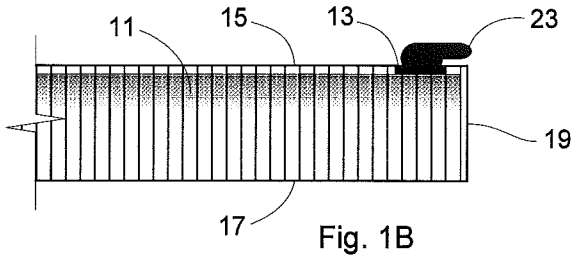

Fig. 1B

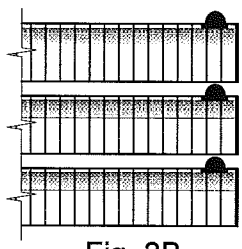

Fig. 2B

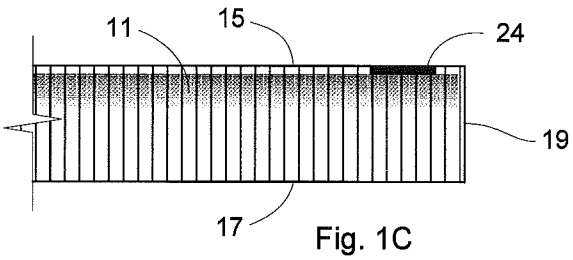

Fig. 1C

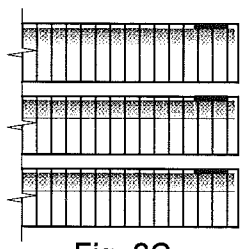

Fig. 2C

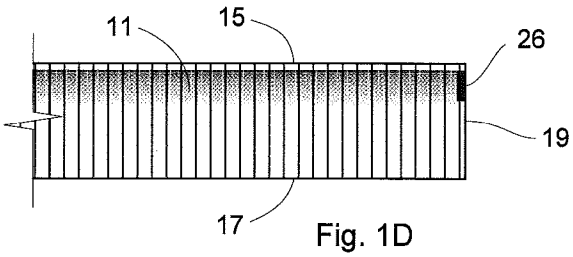

Fig. 1D

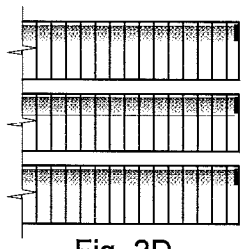

Fig. 2D

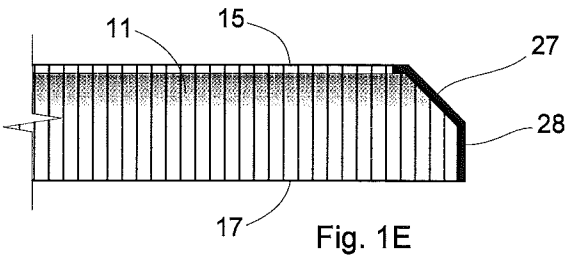

Fig. 1E

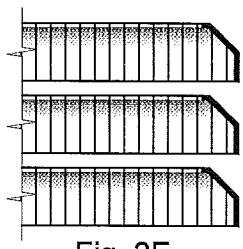

Fig. 2E

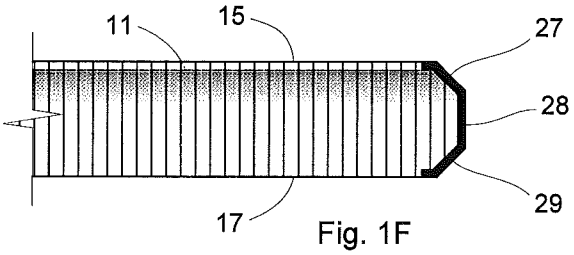

Fig. 1F

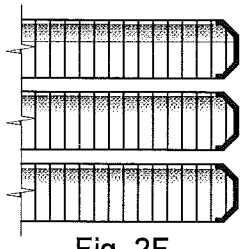

Fig. 2F

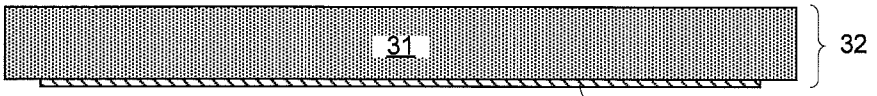

Fig. 3A

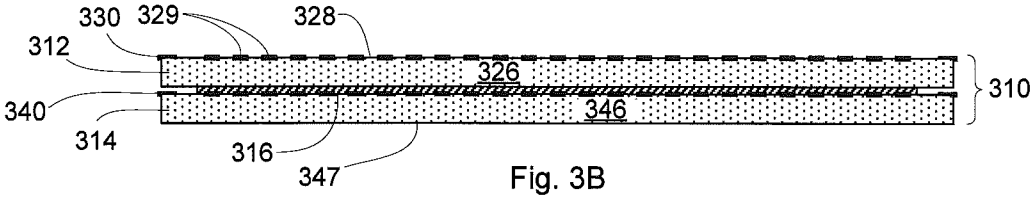

Fig. 3B

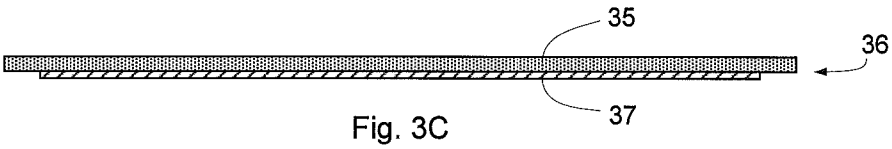

Fig. 3C

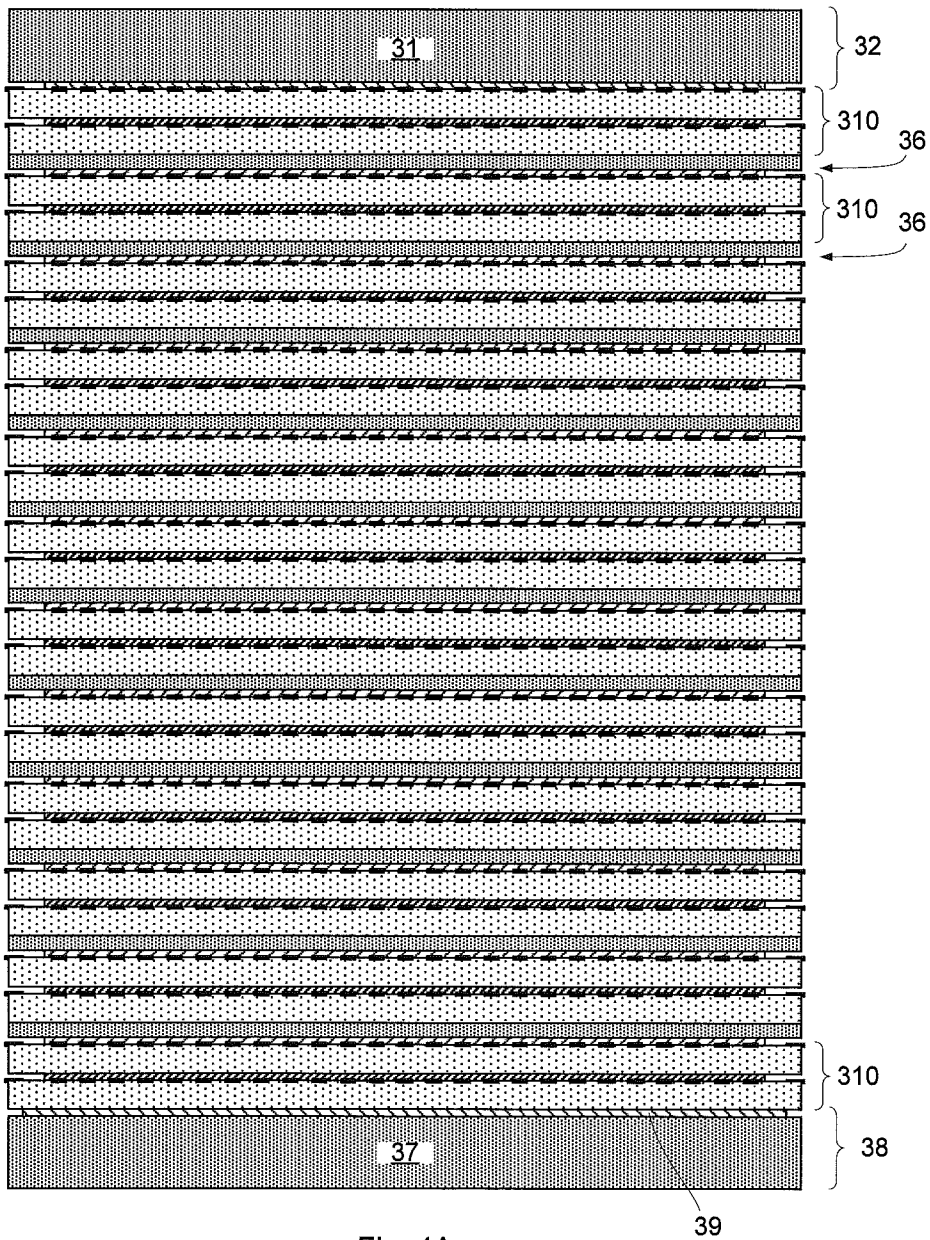

Fig. 4A

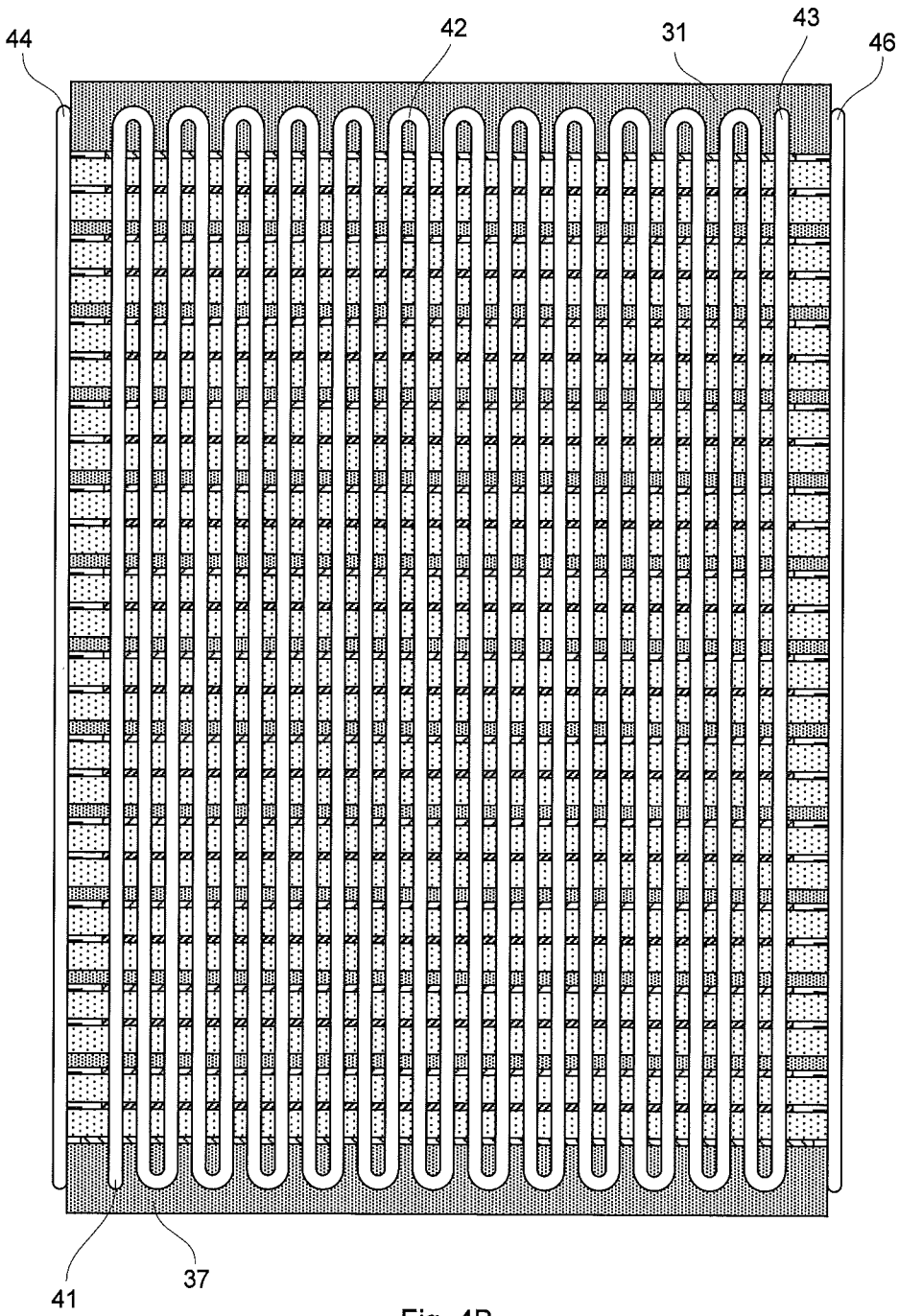

Fig. 4B

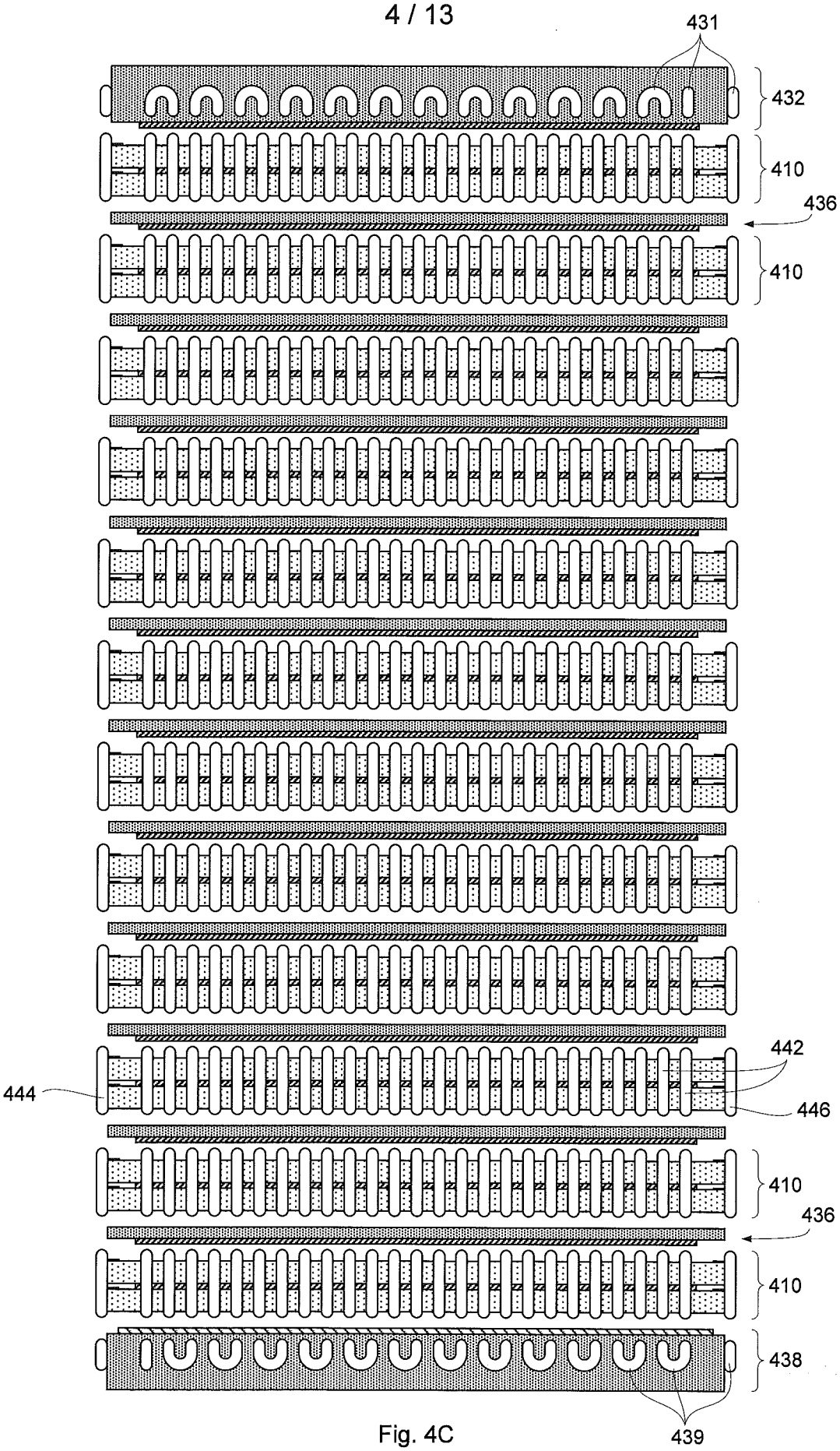

Fig. 4C

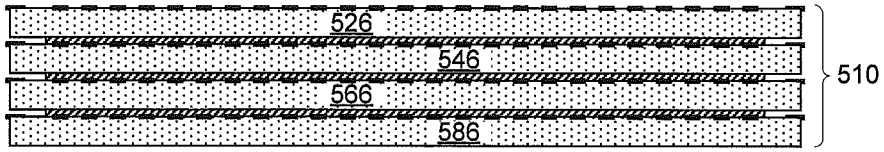

Fig. 5

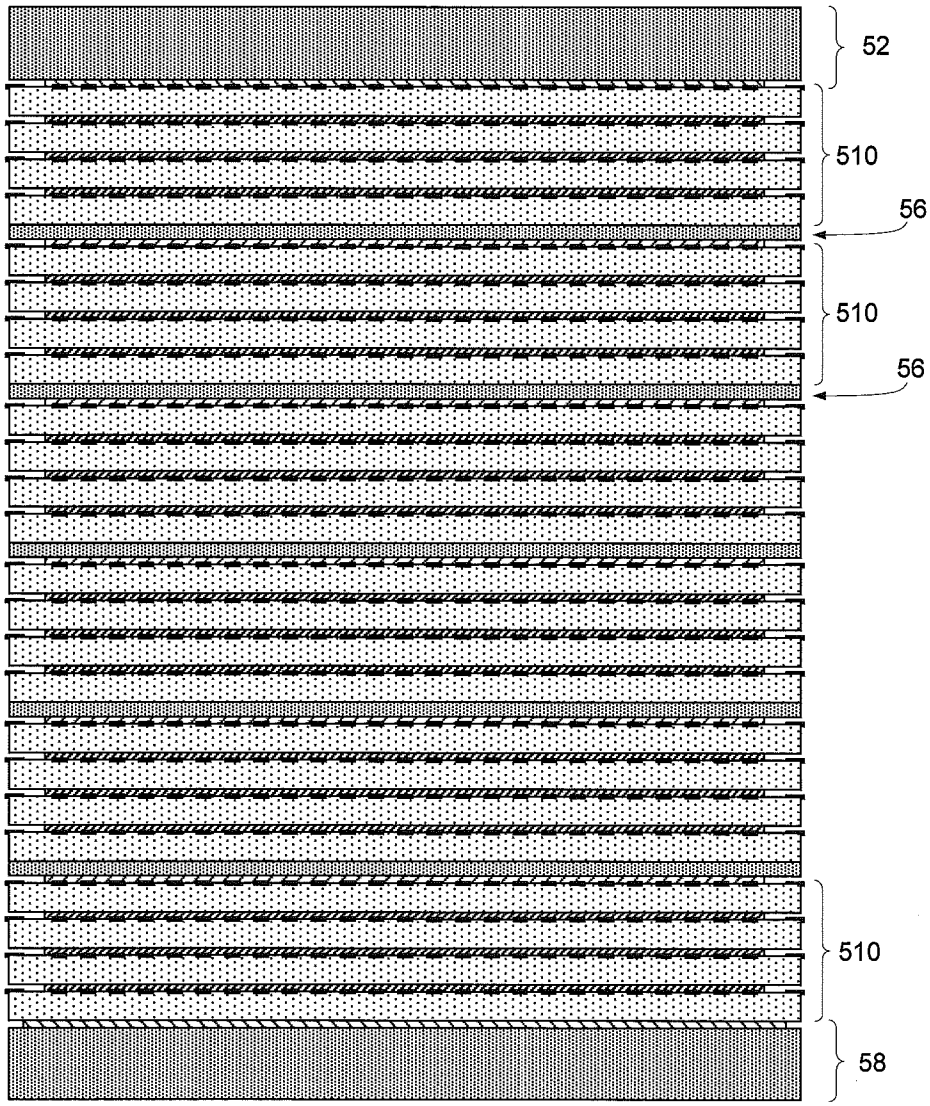

Fig. 6A

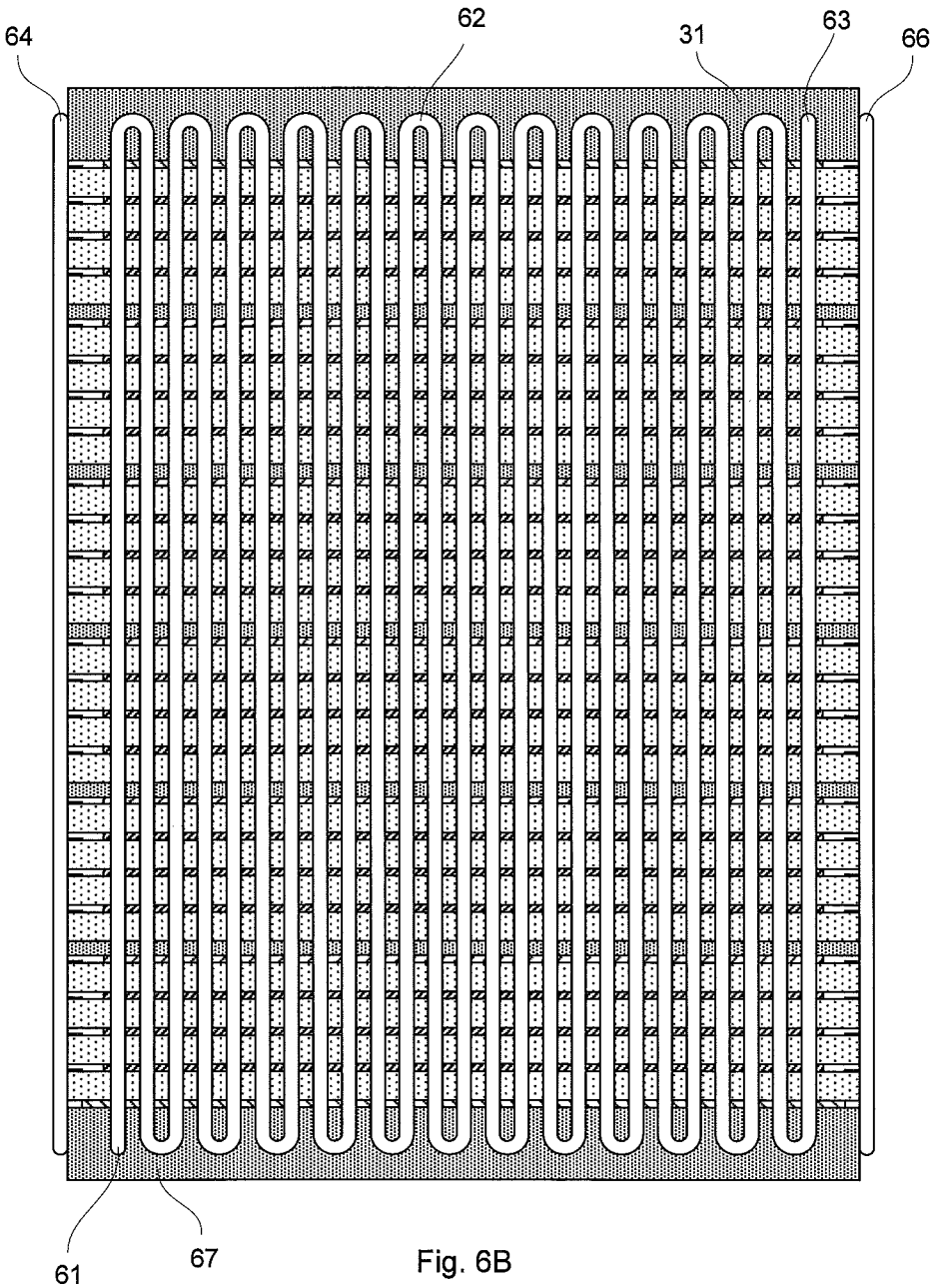

Fig. 6B

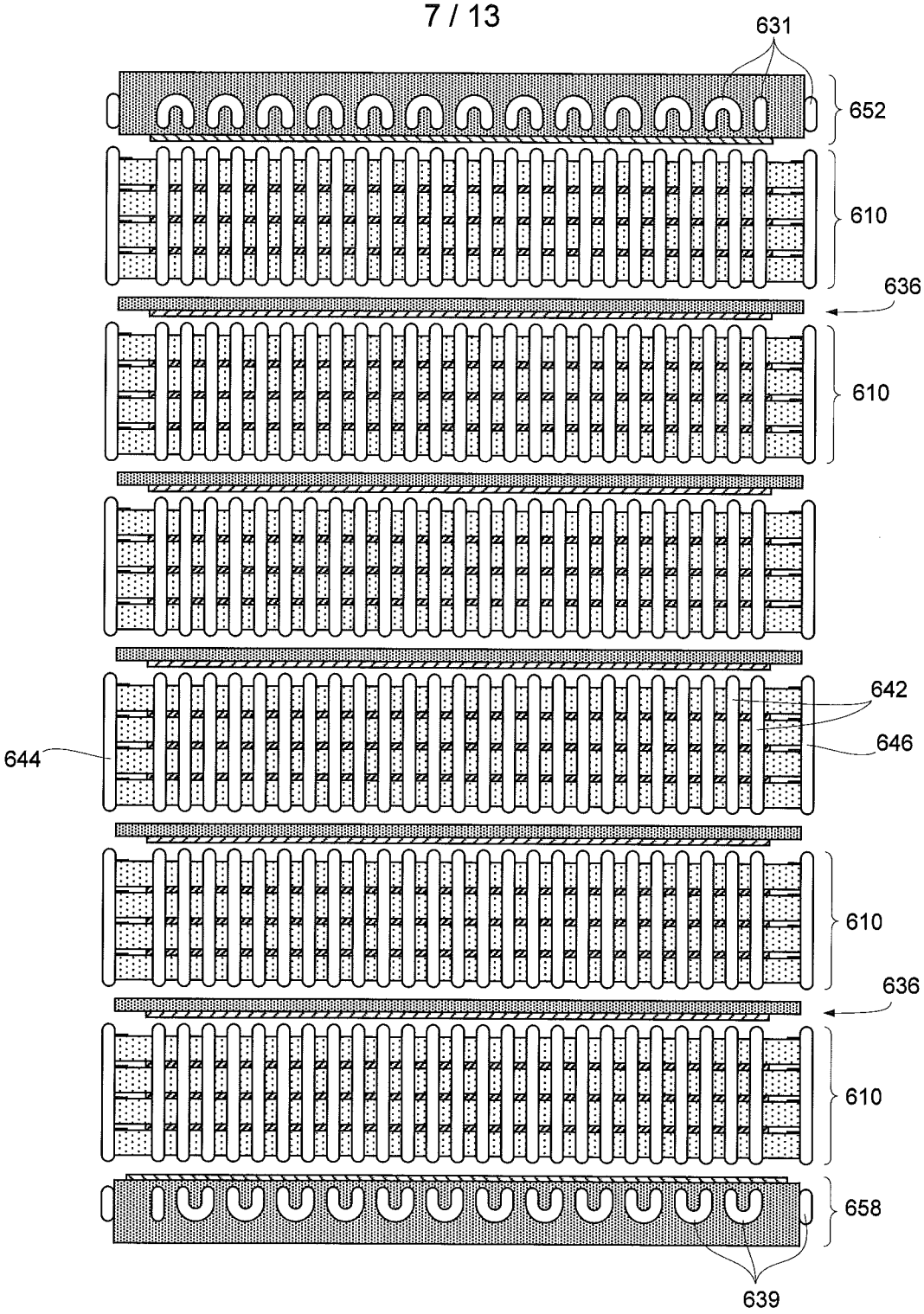

Fig. 6C

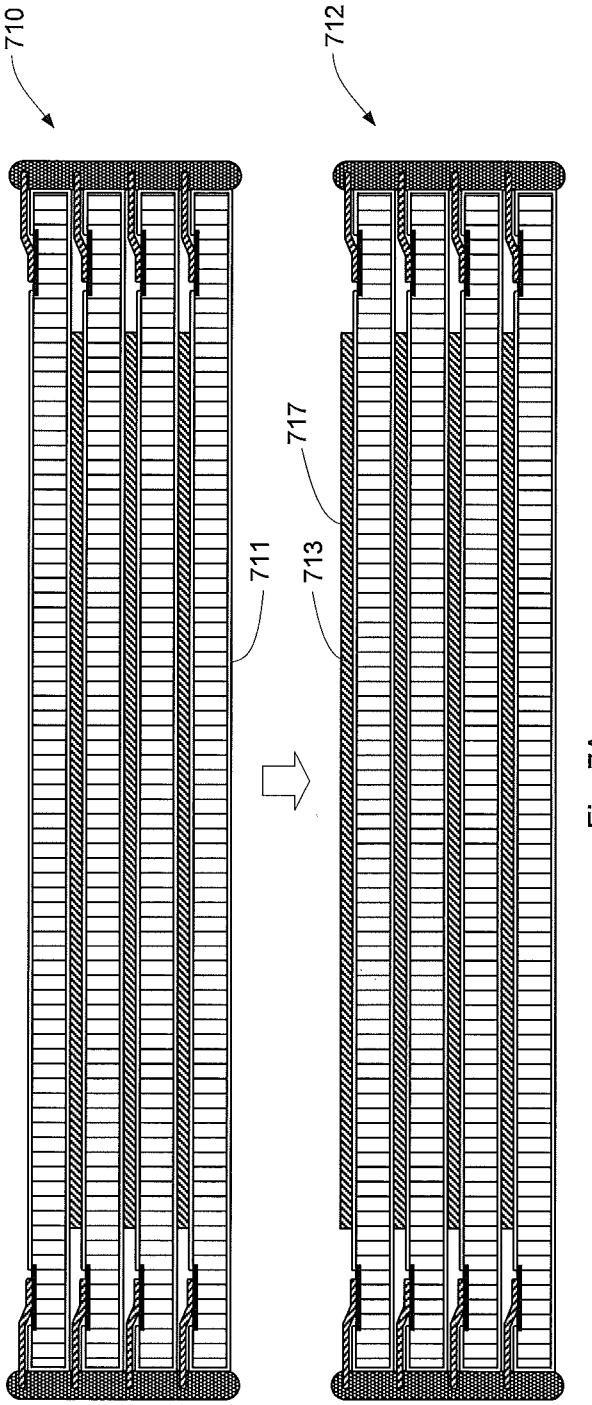

Fig. 7A

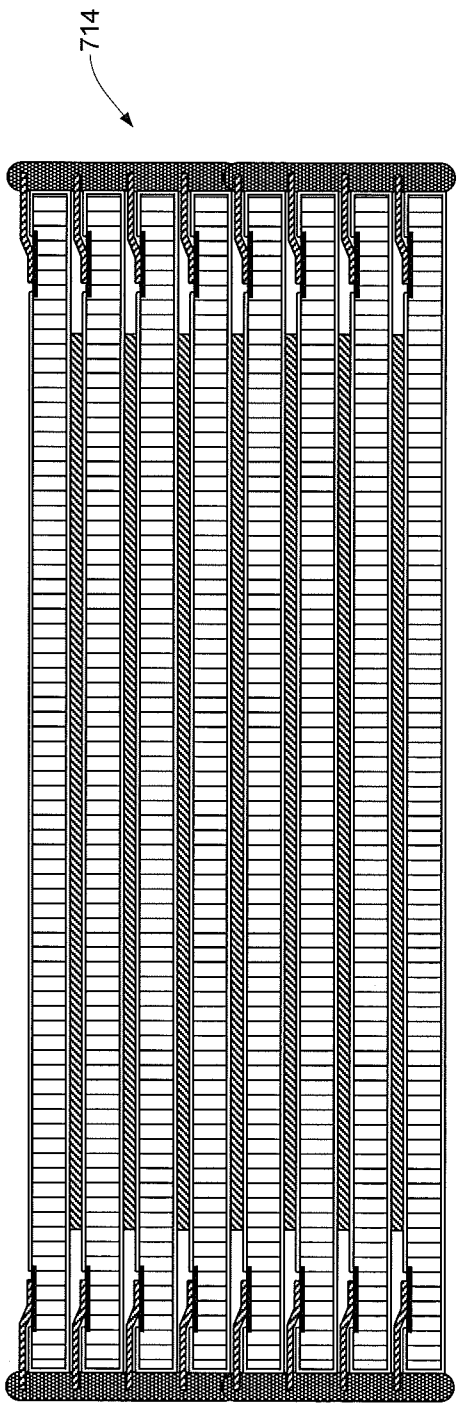

Fig. 7B

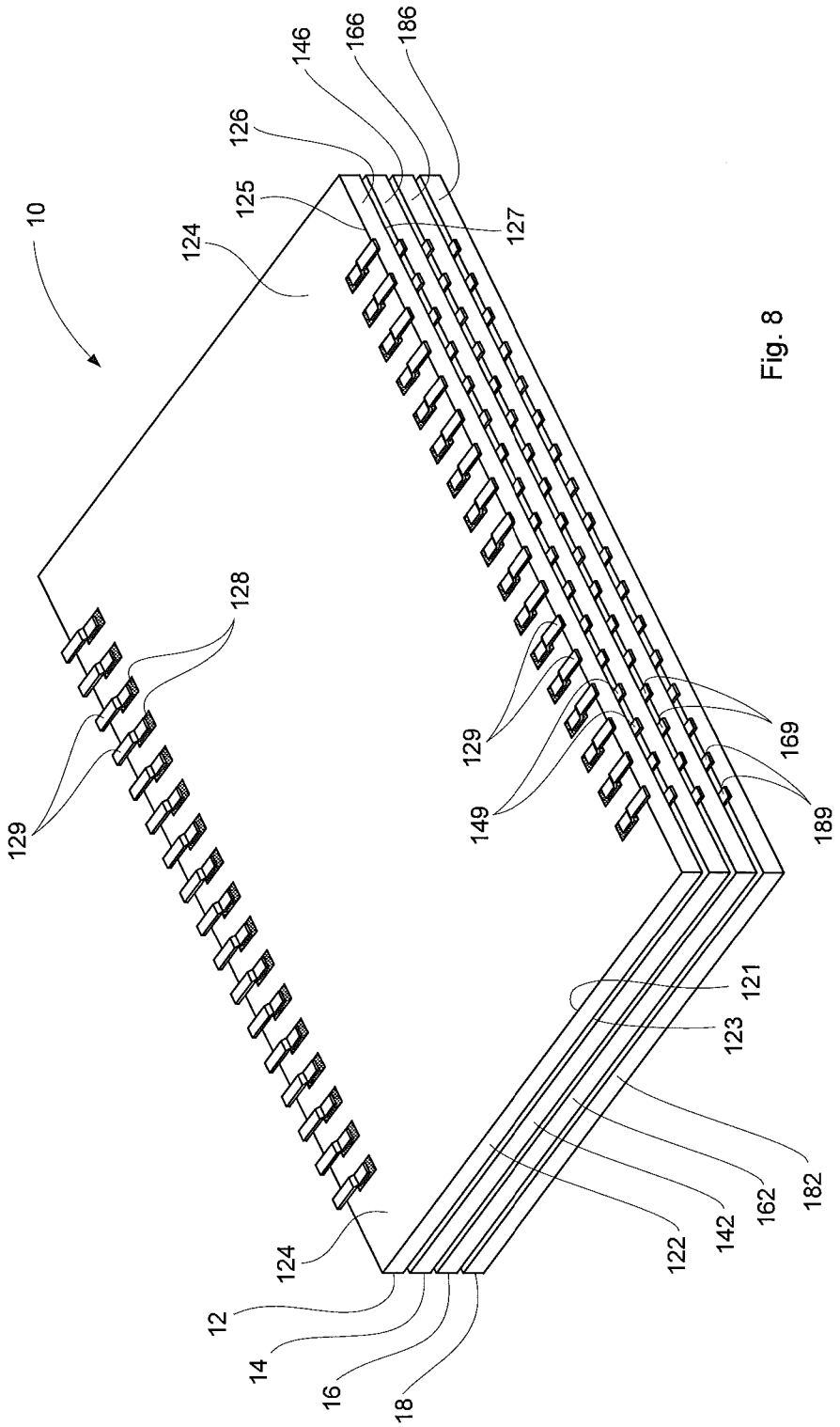
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Fig. 8

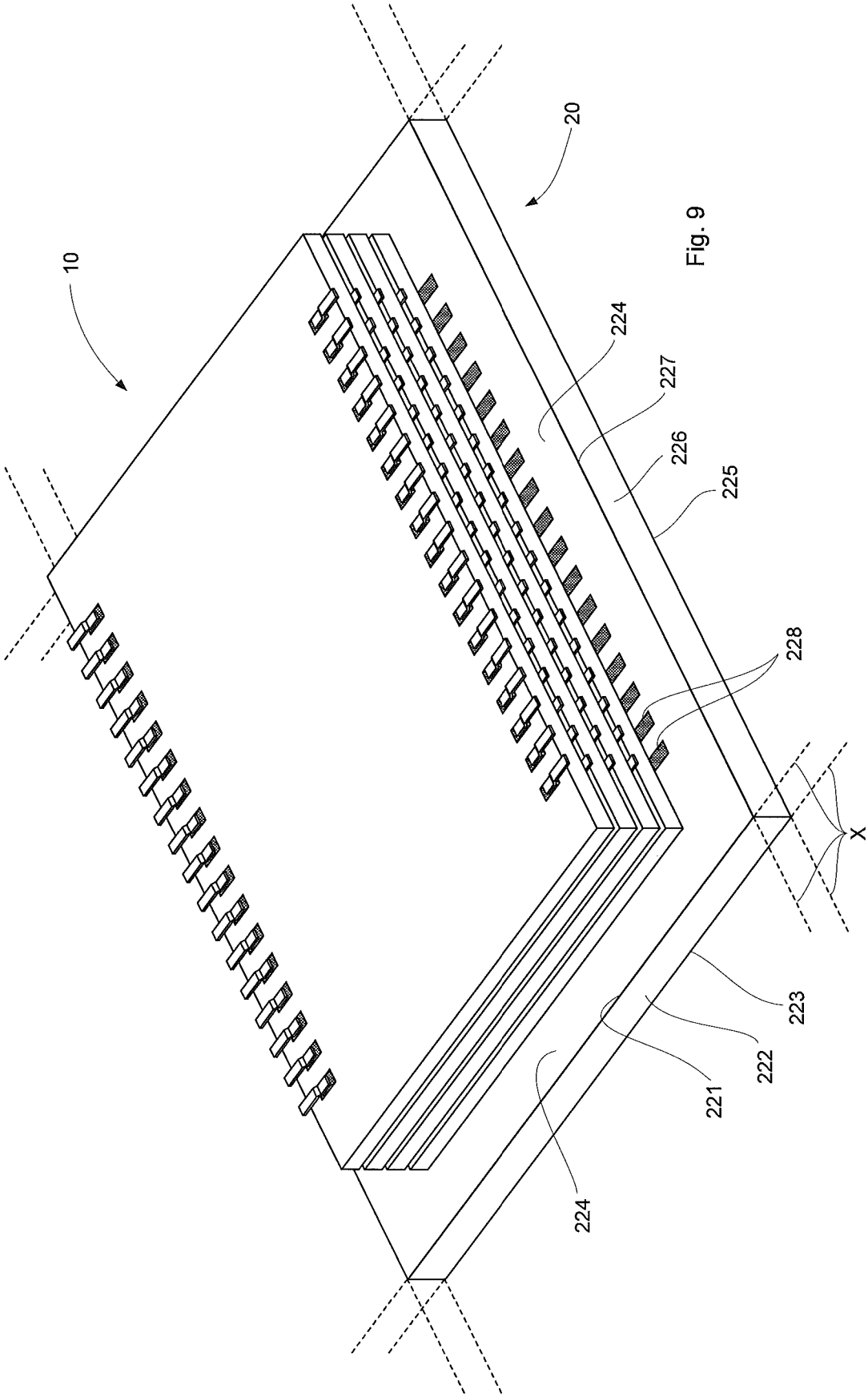

Fig. 9

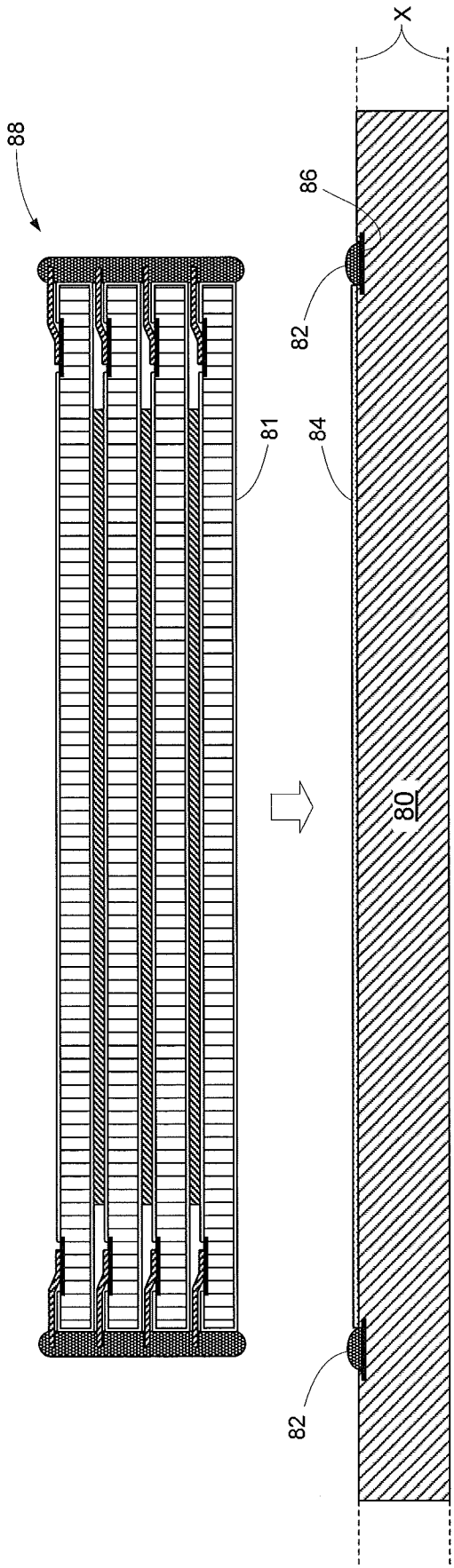

Fig. 10A

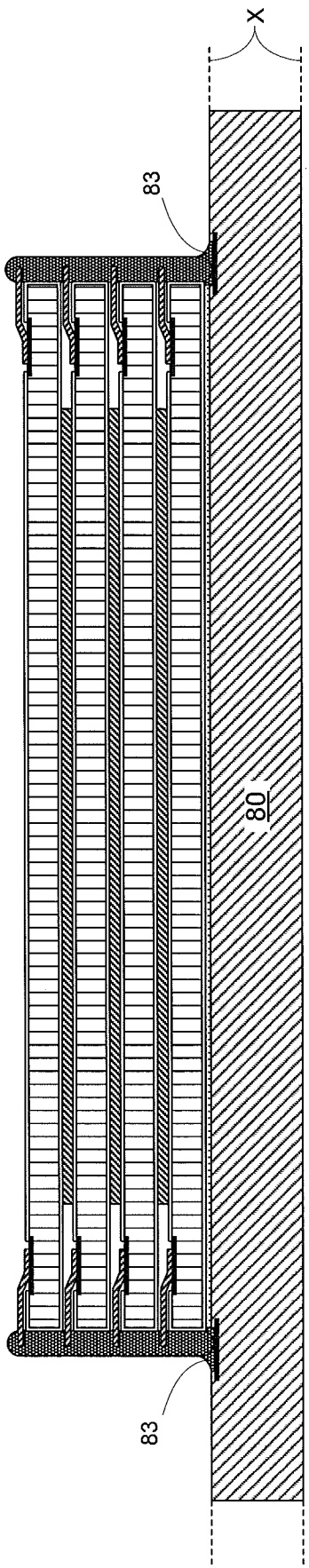

Fig. 10B

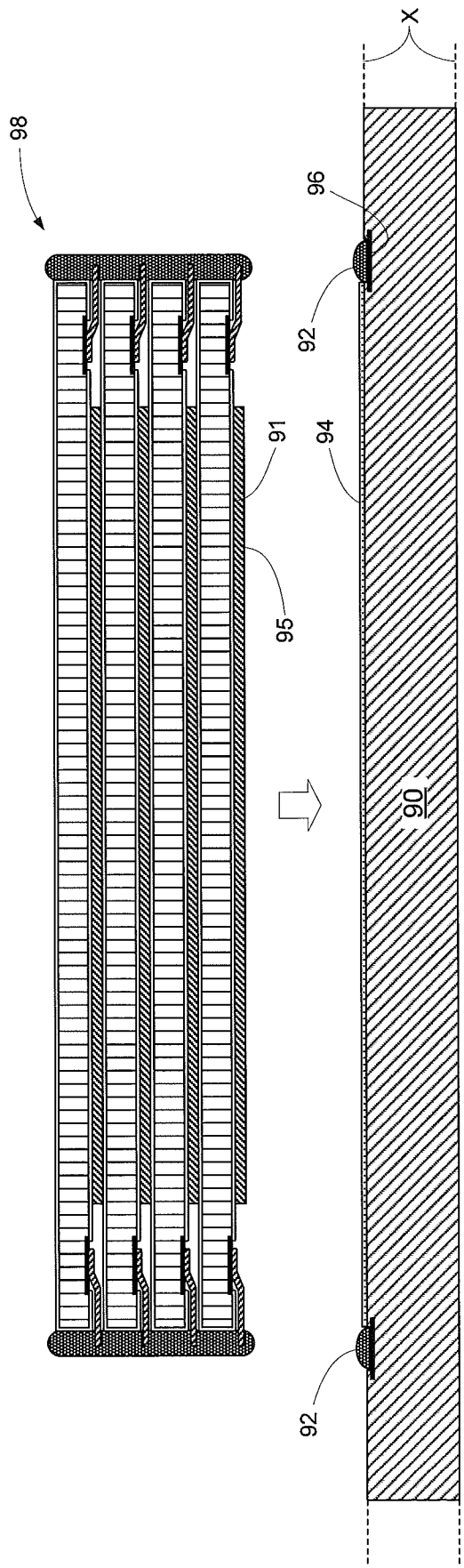

Fig. 11A

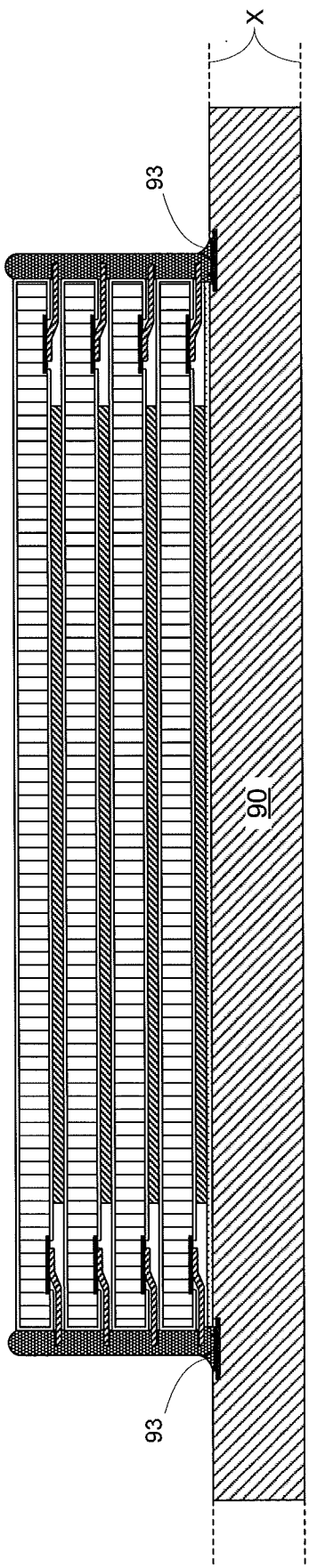

Fig. 11B

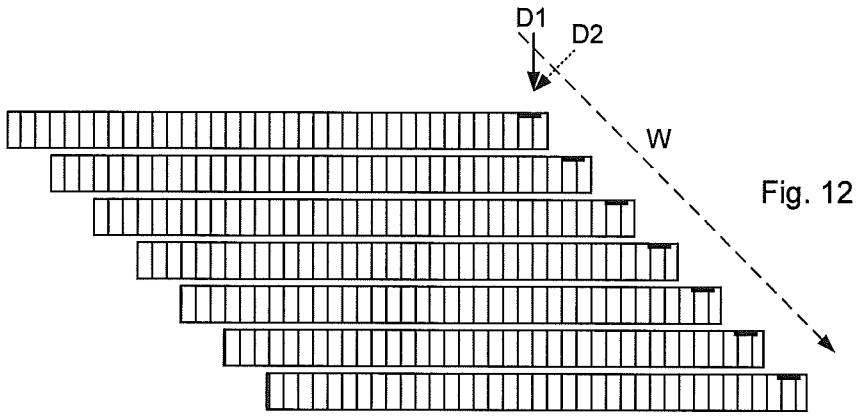

Fig. 12

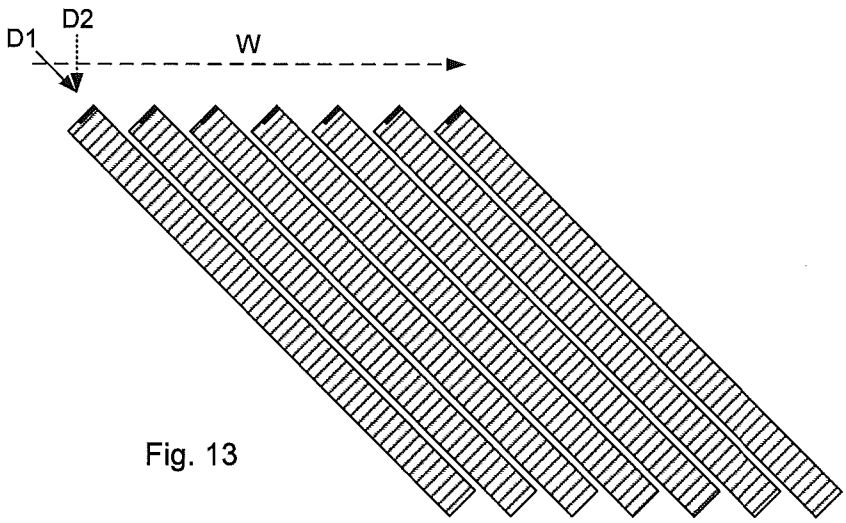

Fig. 13

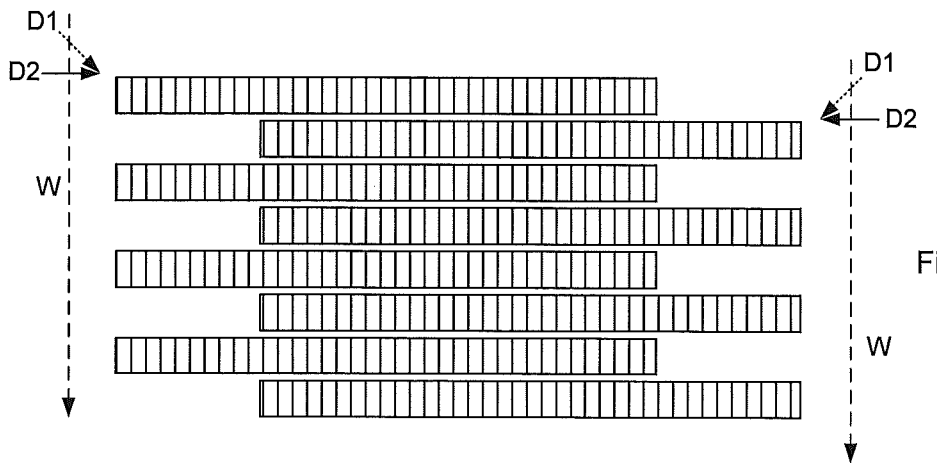

Fig. 14