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(71) **Applicant** *(for all designated States except US):* **ST-Ericsson (Grenoble) SAS** [FR/FR]; 12 Rue Jules Horowitz, F-38000 Grenoble (FR).

(72) **Inventor; and**

(75) **Inventor/Applicant** *(for US only):* **BERTHOLOM, Cedric** [FR/FR]; Les Ayes, F-38470 Vinay (FR).

(74) **Agents: VERDURE, Stephane** et al; Cabinet Plasseraud, 52 rue de la Victoire, F-75440 Paris Cedex 09 (FR).

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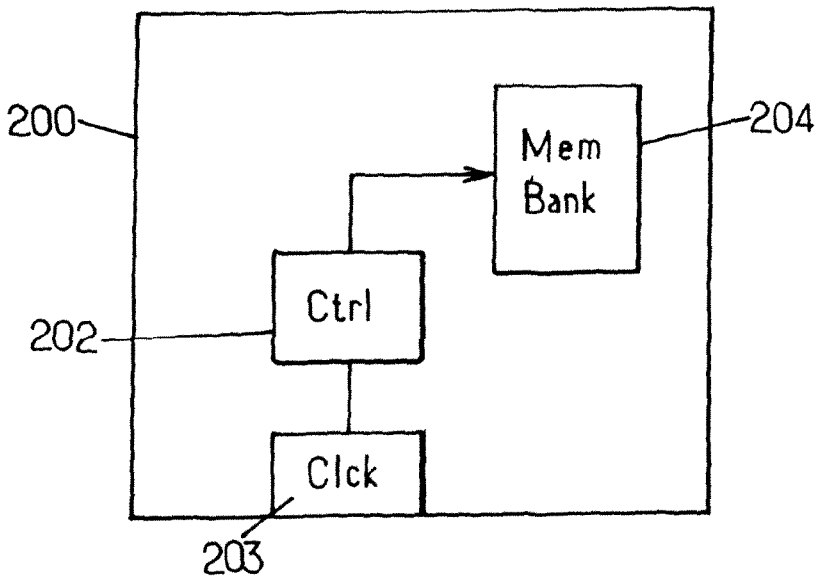

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(57) Abstract: A memory (200) is handled through a plurality of control operations which are performed according to respective timing characteristics. This memory has an autonomous clocking unit and comprises at least one memory bank (204). One of said plurality of control operations is triggered locally on the memory bank, according to a timing determined on the basis of the respective timing characteristics and the autonomous clocking unit.

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AUTONOMOUS CONTROL OF A MEMORY

The present invention is relative to control operations to be carried out inside a SDRAM (for 'Synchronous Dynamic Random Access Memory'), and more particularly to trigger some control operations, like refresh or precharge operations inside a synchronous dynamic memory.

Classically, a SDRAM memory, which is a dynamic memory with a synchronous interface, contains several independent memory banks. Each memory bank can be an array of a plurality of rows. A given memory bank can be in different states, like idle state, active state, or changing state from one state to the other.

According to a prior art, a SDRAM is associated with a memory controller, placed in a processor, which is in charge of managing data stored inside the SDRAM. The memory controller is adapted to trigger some operations to be performed inside the SDRAM, like refresh operation or precharge operation. Figure 1 illustrates an architecture of a system comprising a SDRAM and a memory controller inside a processor according to this prior art.

In such a SDRAM, data are stored in capacitors as electric charges. The electric charges stored in capacitors may be lost over time and therefore it is needed to restore periodically these electric charges by triggering refresh operations. Stated otherwise, a refresh operation corresponds to a process of recharging some capacitors in the memory. When a refresh operation is applied on a row of a memory bank, this row is opened, and some other actions can be performed on this opened row, like data read and write command.

When the memory controller wants to read or write data in a row, it is required to set this row into an idle state. This idle state is reached by performing a precharge operation used to close the row of the memory bank. A precharge operation can occur on all memory banks at the end of each data read or write operation.

The figure 1 illustrates a system 100 comprising a processor 11 and a memory 12 (SDRAM) linked by an interface 13. The processor 11 includes a memory controller 102, an interface unit 103 and a clocking system 104. The memory SDRAM 12 includes an interface unit 105 and a memory bank 106.

There are two different main types of exchange through the interface 13, between the processor 11 and the SDRAM 12: data command messages which correspond to read or write command notably, and control messages which correspond to manage the SDRAM in order to make it usable.

The processor 11 is in charge of triggering control operations to be performed on the memory 12. For that purpose, the memory controller 102 sends to the SDRAM different control messages like refresh, or precharge messages. Consequently, sometimes the bandwidth of the interface 13 between the processor and the memory is not available for transferring data command messages, because these different control messages are transferred through this interface.

Moreover, these different control operations are triggered according to a timing which depends on characteristics relative to the memory itself. A standard specifies a length of a time period required to perform a control operation like a refresh operation. However, all memories do not require the same length of time period to perform a refresh or a precharge operation. Consequently, to make the memory controller able to trigger correctly these types of operation on the SDRAM, some characteristics of the memory must be configured on the memory controller, like timing characteristics relative to any control operations, like refresh or precharge operation. Then, each time this memory controller is in charge of a new memory, it is required to perform a new configuration on it, specifying the time period required to carry out refresh or precharge operation on the basis of a standard definition.

Besides, control messages sent to trigger refresh or precharge operation on the dynamic memory cannot be sent simultaneously with a data command message. Consequently, the memory controller 11 is in charge to manage a priority conflict between sending a data command message and sending a control message. Such priority conflicts are handled at the processor level, where the timing characteristics specific to each memory are taken into

account, in the respect of a standard, notably in order to be able to manage correctly the interactions between transferring data command messages and transferring control messages.

Consequently, in such an architecture according to the prior art, on one hand, the bandwidth is reduced for transferring data command messages because the control messages are transferred through the same interface, and on the other hand, the priority conflict management can be complex at the processor level because it depends on timing characteristics which are specific to each memory to be controlled. Timing characteristics can be specified in standard.

In view of the foregoing, there is a need for enhancing such a method for handling a dynamic synchronous memory.

A first aspect of the present invention proposes a method for handling a memory through a plurality of control operations which are performed according to respective timing characteristics;

said memory having an autonomous clocking unit and comprising at least one memory bank ;

wherein one of said plurality of control operations is triggered locally on said memory bank, according to a timing determined on the basis of said respective timing characteristics and said autonomous clocking unit.

In the present context, the terms 'timing characteristics' correspond to different lengths of time period required for performing the different control operations respectively. Preferably, all these different time periods are respectively inferior than corresponding time periods defined by a standard.

The terms 'autonomous clocking unit' mean a unit able to provide a clock locally to the memory, such a clock being independent of any other component in relation with the memory, and notably independent of a processor in relation with this memory. In one embodiment, the memory can receive a clock provided by quartz, which is not used by the processor. Thanks to this autonomous or independent clocking unit, the memory is able to determine a timing to trigger any control operations in an optimal way.

The terms 'control operations' correspond to any operation to be carried out on a memory in order to allow its use, like a refresh operation or a

precharge operation for instance. In one embodiment of the present invention, a refresh operation is performed on a line after a defined time period without any action on this line, for instance without any read or write operation or refresh operation. A precharge operation is performed before any data read or write action.

In this context, control operations are different from data command which are relative to handling data in the memory, like read or write command for instance. Data command could include a type of command of configuration, which can be referred as configuration control command.

In this context, a memory is able to trigger locally itself all its control operations, without waiting for a control message sent by a processor. Stated otherwise, such a memory is advantageously able to manage itself all control operations, like for instance refresh, or precharge control operation.

Such a method according to one embodiment of the present invention can be applied advantageously in a synchronous dynamic memory. In next section ,for illustrative purpose only, the considered memory is a synchronous dynamic memory.

Here, on one hand, the synchronous dynamic memory knows all its own timing characteristics corresponding to all control operations, and on the other hand, the synchronous dynamic memory has an autonomous clocking unit. Thus, this memory can advantageously determine a timing which is adapted to trigger all control operations itself in an optimal way. Consequently, such a dynamic synchronous memory is autonomous to handle its own control operations and then it is easy to optimize such control operations based on its own specific timing characteristics.

Such optimisation is not easy to perform at a processor level, notably when such processor is in charge of controlling a plurality of dynamic synchronous memories having different timing characteristics for a given control operation.

It is important to note that it is easy to make a memory able to manage itself its timing characteristics corresponding to perform all control operations. Each constructor of a memory can set, inside the memory, all time values required to carry out the control operations on this memory.

Besides, a memory according to one embodiment of the present invention has its own independent clocking unit. Based on the independent clocking unit and the timing characteristics, such a synchronous dynamic memory can handle all its control operations itself in an optimal way.

According to the prior art, the processor is in charge of triggering control operations by sending control messages to different memories taking into account different timing characteristics respectively configured for these memories at the processor level. This management of different timings is complex to be done at a processor level. Thanks to an autonomous management at the memory level, this complexity can be avoided advantageously according to one embodiment of the present invention. The processor in charge of controlling this type of synchronous dynamic memory can be designed easily, without taking into account memory specifications relative to control operations.

Indeed, in a system comprising such a synchronous dynamic memory with an autonomous clocking unit, a processor could be advantageously autonomous regarding timing memory standards because the memory handles itself all timing characteristics regarding its control operations.

Moreover, thanks to such a memory, a processor does not need to manage conflicts between sending control message and sending data command message to the memory. Consequently, a memory controller of a processor for a synchronous dynamic memory, according to one embodiment of the present invention, can be less complex and smaller than a memory controller for a dynamic memory according to the prior art. More precisely, a memory controller adapted to a synchronous dynamic memory according to one embodiment of the present invention can be designed to manage only the data command message through the interface between the memory and the processor.

Besides, as such a memory handles itself all control operations, in one embodiment of the present invention, it would be possible to avoid receiving any external control messages regarding such operations as precharge or refresh operation. Of course, it could be useful to continue to receive and handle other type of control messages like configuration control messages.

Consequently, the interface between a processor using the memory and the memory itself can be used for data command messages exclusively. Then, the interface memory can be improved regarding the latency aspect and the size of bandwidth used for data command messages.

In one embodiment of the present invention, thanks to these characteristics, it is advantageously possible to handle a serial interface instead of a parallel interface between the memory and the processor.

In one embodiment of the present invention, a refresh operation of a dynamic random access memory standard can be a RAS-only-refresh (for 'Row Address Strobe) or an automatic refresh (CAS (for 'Column Address Strobe)-before-RAS).

The RAS-only-refresh can be executed, after applying a refresh address, in one cycle in which a RAS signal falls. In the automatic refresh, an address counter installed in the memory can generate a predetermined internal address instead of applying the refresh address. The refresh operation of such a memory as well as the automatic refresh can be set under the JEDEC standard (for 'Joint Electron Device Engineering Council').

In one embodiment of the present invention, the synchronous dynamic memory being able to receive a data command message, handling such a data command message and triggering a control operation are prioritized at the memory level.

Such a characteristic allows handling a priority conflict between handling a data command received from a memory controller and triggering a control operation on the synchronous dynamic memory. Such a priority conflict can occur on reception of a data command message when the timing determined at the memory level indicates that a control operation is required on the memory. In this case, there is a conflict between handling the received data command message and triggering the control operation. In one embodiment of the present invention, the synchronous dynamic memory is adapted to handle itself this conflict. It is important to note that it is easier to handle this type of conflict at the memory level than at a memory controller level.

In one embodiment of the present invention, a control operation is triggered in priority to a data command, and the data command is stored into a buffer until said control operation is performed.

The data command can be a data write command, and, in this case, a data to be written is stored into a buffer until the control operation is performed.

The control operation can a refresh or precharge operation.

For instance, a refresh operation can be triggered in priority to a data command, and a data to be read or written can be stored into a buffer until the refresh operation is performed. Here, the refresh operation is considered as a priority regarding a data read or write command. Advantageously, this memory knows when the refresh operation will be finished and then, it is able to handle the data read or write command in an optimal way, without any latency.

In one embodiment, a precharge operation can be triggered in priority to a data read or write command, and the data read or write command can be stored into a buffer until the precharge operation is performed. The memory knows the time period required by a precharge operation and it knows exactly when this control operation is triggered. Consequently, in these conditions, the memory can handle a data read or write command as soon as the precharge operation is finished.

A second aspect of the present invention proposes a synchronous dynamic memory comprising means adapted to carry out a method according to the first aspect of one embodiment of the present invention.

A third aspect of the present invention proposes a system comprising a synchronous dynamic memory according to the first aspect of the present invention, and a processor adapted to send data command messages to the synchronous dynamic memory.

Further features and advantages of the present invention will become more apparent from the description below. The latter is given purely by way of illustration and should be read in conjunction with the appended drawings, of which:

- Figure 1, already described, illustrates a dynamic memory system according to a prior art;

- Figure 2 illustrates a dynamic synchronous memory according to one embodiment of the present invention;
- Figure 3 illustrates a dynamic synchronous memory according to one embodiment of the present invention, comprising a priority controller; and
- Figure 4 illustrates a management of priority conflict in a system according to one embodiment of the present invention.

Figure 2 illustrates a dynamic synchronous memory according to one embodiment of the present invention. Such a dynamic synchronous memory 200 comprises at least:

- one memory bank 204;
- an autonomous clocking unit 203 adapted to provide an autonomous clock inside the memory 200 locally; and
- a control unit 202 adapted to trigger at least one control operation on the memory bank, based on the clock provided by the autonomous clocking unit locally.

Advantageously, this dynamic memory 200 is adapted to perform main steps of a method according to one embodiment of the present invention.

Some operations are required in order to allow using such a synchronous dynamic memory. Indeed, during the use of such a dynamic memory, the memory-cell capacitors impose the regular triggering of control operations, like refresh, precharge or auto-precharge operations.

In one embodiment of the present invention, a plurality of time values associated to the plurality of control operations is set on the control unit. Each time value associated to a given control operation indicates the time period length required to perform the given control operation inside the synchronous dynamic memory.

Some control operations are required to allow handling data command messages received from a processor. These data command messages can correspond to either a data write command or a data read command, these messages indicating an address into the memory, where the data must be written or must be read.

In some conditions, a control operation is required in the memory in the same time as the reception of a data command message from an external memory controller. Then, there is a potential conflict because it is necessary to choose between a data command and a control operation. In this case, a priority controller can be in charge of handling such a priority conflict.

Figure 3 illustrates a synchronous dynamic memory according to one embodiment of the present invention, comprising a priority controller 201 . This priority controller manages priorities between both different operations required in the same time.

Thus, the memory can receive a data write command, indicating an address inside the memory and a data to be written at this address, when a refresh operation is required by the control unit 202. The priority controller 201 triggers the refresh operation and, until the end of this refresh operation, it stores the data to be written into an elastic buffer 220. The control unit 202 can determine which address of the memory bank requires a refresh operation and a refresh operation is performed on this address.

Once the refresh is done, the control unit transfers the data stored in the buffer into the memory bank at the address indicated into the data write command.

The memory can receive a data read command, indicating an address inside the memory and a data to be read at this address, when a refresh operation is required by the control unit 202. In this case, the priority controller 201 can trigger the refresh operation and, until the end of this refresh operation, it stores the address to be read into an elastic buffer. The control unit 202 can determine which address of the memory bank requires a refresh operation and a refresh operation can be performed on this address.

Once the refresh is carried out the requested data is read at the address indicated into the elastic buffer and send back to the processor.

In one embodiment of the present invention, the synchronous dynamic memory receives from a processor a read command message indicating an address into the memory, then a precharge operation is locally required by the control unit 202. Then, there is a conflict between a read operation and a

precharge operation. In this case, the priority controller 201 is in charge of handling such a priority conflict too.

In one embodiment, this priority controller 201 triggers the precharge operation and, until the end of this precharge operation, the received data read command is stored. At the end of the precharge operation, the requested data is read at the address indicated into the data read command. This read data is stored into an elastic buffer. The data stored into the elastic buffer can be transmitted to the processor through the interface unit 21, once the elastic buffer is full, for instance.

Then, the dynamic synchronous memory can refresh the address where the read operation took place, while the interface unit 21 transfers the data from elastic buffer.

Figure 4 illustrates a system according to one embodiment of the present invention.

Such a system 400 comprises a memory 200 and a processor 401, which is adapted to send data command messages to the synchronous dynamic memory 200 according to one embodiment of the present invention. The processor 401 comprises a clock 406, and a command unit adapted to send a data command message to the memory 200 through an interface unit 403. The memory 200, which can be a synchronous dynamic memory, comprises at least one memory bank, an autonomous clocking unit 203 adapted to provide a clock to the memory and a control unit 202. It can include an interface unit 21.

It is important to note that the priority conflict can be handled either at the processor level or at the memory level, even if it is more advantageous to handle it at the memory level as stated above and as illustrated by Figure 3. However, the priority conflict could be handled at the processor level, for instance, when a synchronous dynamic memory, according to one embodiment of the present invention, is in relation with a processor adapted to handle the priority conflict according to the prior art as illustrated on Figure 1.

In one embodiment of the present invention, the priority conflict is handled at the memory level in such a system 400, and the memory comprises the priority controller 201. In this case, the command unit 402 of the processor

can transfer a data command message to the synchronous dynamic memory 200 at any time, without it having to take into account any timing characteristics of this memory 200. Consequently, such a processor 401 is easier to design.

The priority controller is adapted to trigger a control operation in priority to a data command, the data command being stored into a buffer until said control operation is performed. When the data command is a data write command, a data to be written can be stored into a buffer until the operation is performed. The control operation can be a refresh or precharge operation.

CLAIMS

1. Method for handling a memory (200) through a plurality of control operations which are performed according to respective timing characteristics;
said memory having an autonomous clocking unit and comprising at least one memory bank (204);
wherein one of said plurality of control operations is triggered locally on said memory bank, according to a timing determined on the basis of said respective timing characteristics and said autonomous clocking unit.

2. Method for handling a memory (200) according to claim 1, wherein, said memory being able to receive a data command message, handling said data command message and triggering a control operation are prioritized at the memory level.

3. Method for handling a memory according to claim 2, wherein a control operation is triggered in priority to a data command, and wherein said data command is stored into a buffer until said control operation is performed.

4. Method for handling a memory according to claim 3, wherein the data command is a data write command, and wherein a data to be written is stored into a buffer until the control operation is performed.

5. Method for handling a memory according to claim 3 or 4, wherein the control operation is a refresh or precharge operation.

6. Memory (200) adapted to perform a plurality of control operations performed according to respective timing characteristics;
said memory comprising:

- at least one memory bank (204);

- an autonomous clocking unit (203) adapted to provide a clock to the memory;
- a control unit (202) adapted to determine a timing to trigger a control operation on the memory bank, based on said clocking unit.

7. Memory (200) as claimed in claim 6, further comprising:

- an interface unit (21) adapted to receive data command message from a processor;

- a priority controller (201) adapted to prioritize handling of said data command message and triggering of one control operation.

8. Memory (200) as claimed in claim 7, wherein the priority controller is adapted to trigger a control operation in priority to a data command, said data command being stored into a buffer until said control operation is performed.

9. Memory (200) as claimed in claim 8, wherein the data command is a data write command, and wherein a data to be written is stored into a buffer until the operation is performed.

10. Memory (200) as claimed in claim 8 or 9, wherein the control operation is a refresh or precharge operation.

11. System comprising a memory as claimed in any one of claims 6 to 10, and a processor adapted to send data command messages to said memory.

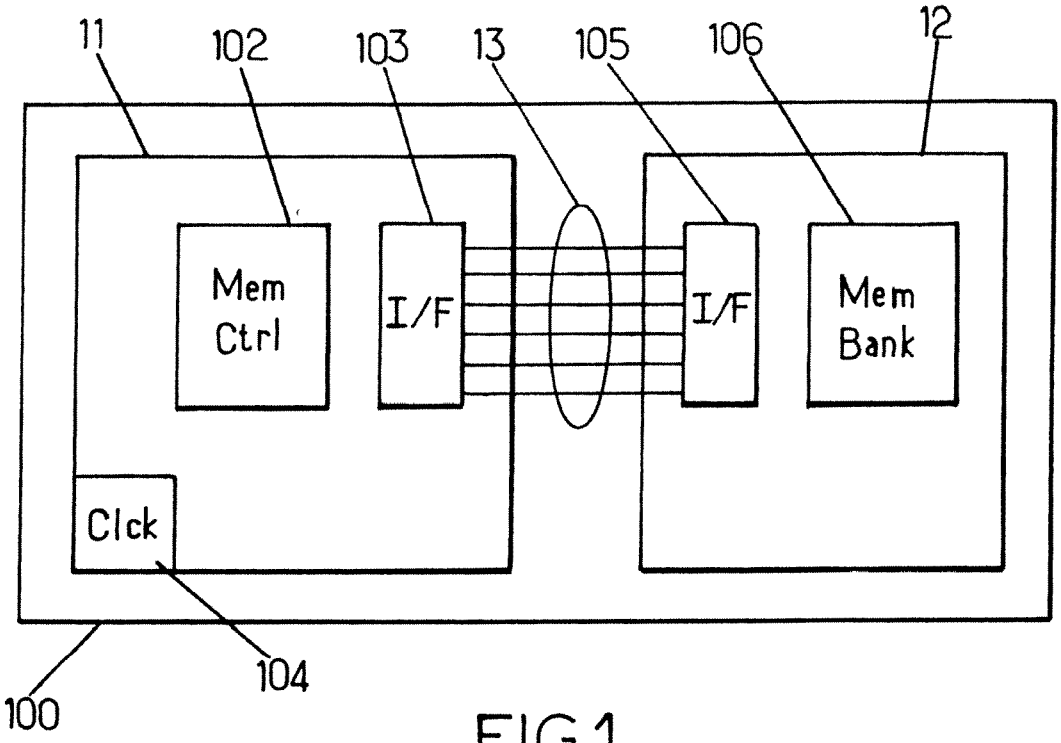

FIG.1.
PRIOR ART

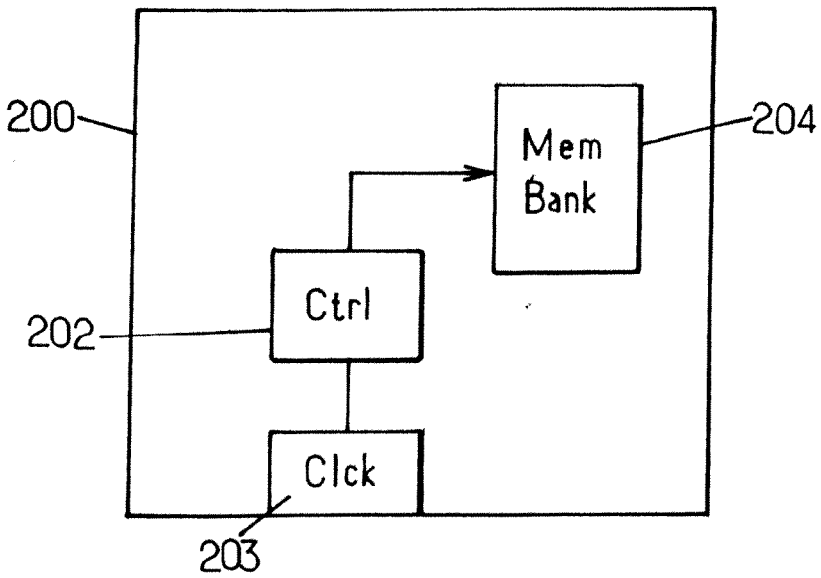

FIG.2.

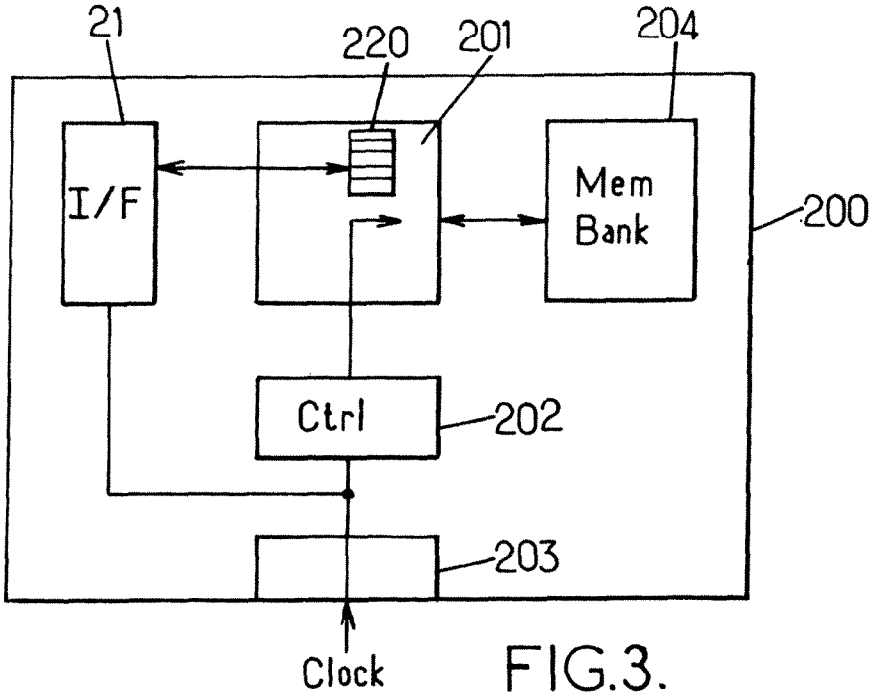
21
220
201
204
I/F
Mem
Bank
200
Ctrl
202
203
Clock

FIG.3.

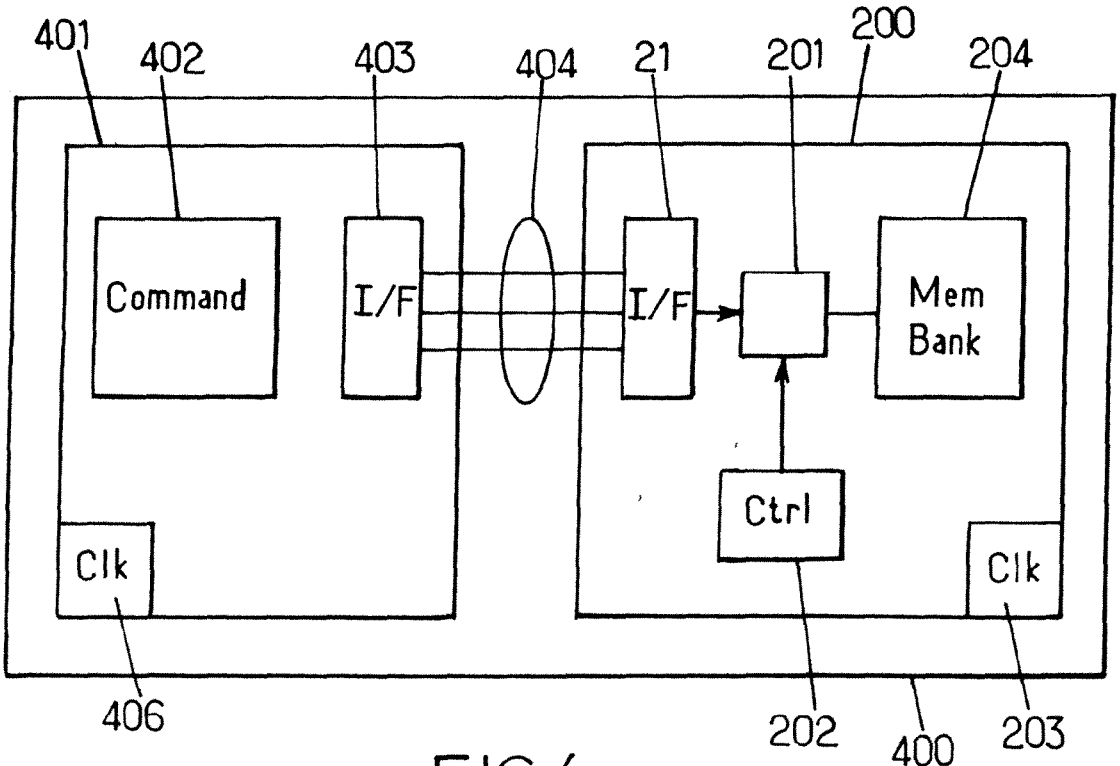
401
402
403
404
21
201
200
204
Command
I/F
I/F
Mem
Bank
Ctrl
Clk
Clk
406
202
400
203

FIG.4.

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/053228

A. CLASSIRCATION OF SUBJECT MATTER
INV. G11C11/406

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 215 678 A2 (FUJITSU LTD [JP]) 19 June 2002 (2002-06-19) paragraphs [0011] - [0014]; figure 1	1-11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 November 2009	13/11/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax (+31-70) 340-3016	**Czarik, Damien**

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2009/053228

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1215678 A2	19-06-2002	CN 1357891 A	10-07-2002
		JP 3938842 B2	27-06-2007
		JP 2002170384 A	14-06-2002
		KR 20020044045 A	14-06-2002
		TW 512343 B	01-12-2002
		US 2002067649 A1	06-06-2002