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(54) Electron source device

(57) A self-aligned electron device (10) includes emitter (13), extraction electrode (17), and focus electrode (21) separated by dielectric layers, (11, 15, 19). A single cavity (23) extending through the electrodes and the dielectric layers and terminating at the emitter electrode (13) is formed by a single photolithography step and an etching process. A composite emitter (1) including a base (3) disposed on the emitter electrode (13) and a conical tip (5) disposed on the base (3) and terminating at a vertex V is formed in the cavity (23). The base (3) can be made from materials including titanium, chromium, or doped silicon. The tip (5) can be made from a wide variety of materials including a refractory metal, a metal alloy, a silicon alloy, a carbide, a nitride, or an electroformable metal. The cavity (23) and the composite emitter (1) are self-aligned relative to each other. The dielectric layers can be etched back to reduce or eliminate charge accumulation on cavity-facing portions (43, 45) of the dielectric layers. A composite layer including a dielectric and mechanical strength enhancement layer (15a, 19a) of silicon nitride or silicon carbide and a pull-back layer (15b, 19b) of silicon oxide on top of the etch stop layer can be used to form the dielectric layers.

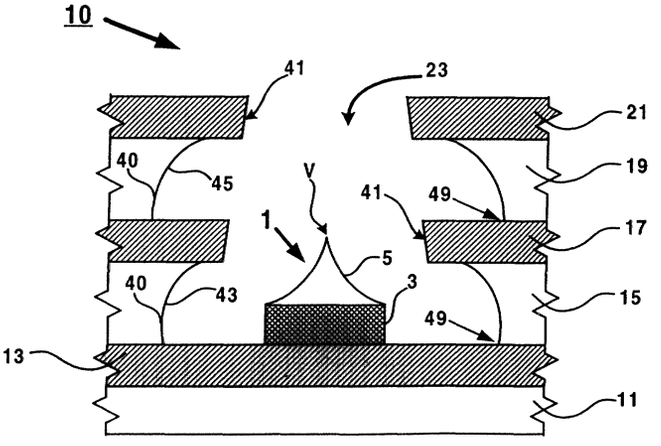

FIG. 6

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Description

[0001] The present invention relates generally to production of an electron beam using an electron source device. More specifically, the present invention relates to new structures and new materials for a self-aligned electron source device that produces a beam of electrons from a composite emitter that is co-axially surrounded by a cavity that includes extractor and focus electrodes separated by dielectric layers.

[0002] Articles and publications set forth herein are presented for the information contained therein: none of the information is admitted to be statutory "prior art" and we reserve the right to establish prior inventorship with respect to any such information.

[0003] It is well known in the art to use an array of Spindt emitters as an electron source in a flat panel display. For instance, Spindt type emitters are one type of emitter used in a field emission display (FED). An analogous technology to the FED is the cathode ray tube (CRT) used as a display in television sets and computer monitors. The FED is one type of device that incorporates an electron field emitter. Typically, in a FED, an emitter electrode has a plurality of Spindt emitters formed thereon. A Spindt emitter is a conical cathode connected to the emitter electrode at its base and having a sharp tip (needlelike point) at its vertex. A extractor electrode having a circular aperture therein is positioned proximate to the tip and is electrically biased relative to the emitter electrode so that electron emission is induced from the tip. Basically, when a sufficient voltage differential is applied between the extractor electrode and the tip of the Spindt emitter, electrons quantum mechanically tunnel out of the tip. The emitted electrons are accelerated towards a positively biased anode spaced approximately 100 μm to 200 μm away from the tip of the Spindt emitter. It is commonplace to use a glass substrate coated with a conductive material such as indium tin oxide (ITO) for the anode of the FED. The voltage potentials between the emitter electrode and the extractor electrode can be on the order of 10 V to 150 V, and the voltage potentials between the emitter electrode and the anode can be on the order of a few hundred volts to several kilovolts or more. A variety of methods are known in the art that are suitable for making the electron field emitters described above. By way of example, a general discussion of one method is disclosed in "Physical Properties of Thin-Film Field Emission Cathodes with Molybdenum Cones," by Spindt et al, published in the Journal of Applied Physics, Vol. 47, No. 12, December 1976. Additionally, another method for making electron field emitters is disclosed in "Fabrication and Characteristics of Si Field Emitter Arrays," by Betsui, published in Tech. Digest 4th Int. Vacuum Microelectronics Conf., Nagahama, Japan, page 26, 1991.

[0004] Although the Spindt type field emitters (field emitters hereinafter) have been applied to technologies, such as flat panel displays, there are several disadvantages to conventional implementations of field emitters when applied to other technologies, such as high density storage technologies, for example.

[0005] In a typical FED, each image pixel in the display is serviced by an array, usually a very large group, of individual field emitters connected to a common emitter electrode. Each pixel includes a phosphor coating that is operative to emit visible light in response to the electron beams incident on that pixel. The electron beam from a single emitter will diverge (spread out) in the direction of the pixel. However, the area of the pixel is larger than the width of the electron beam from a single emitter. Accordingly, an array of emitters is required to produce light of sufficient intensity from the pixel. Moreover, the array of emitters provides for emitter redundancy in case one or more of the field emitters is inoperative. On the other hand, high density storage technologies require a narrowly focused electron beam capable of storing data on and retrieving data from a small, bit sized area of a storage medium. Consequently, the shotgun (wide beam) approach used in FED's is not desirable in high density storage applications. A general discussion of field emitters and their use in high density storage devices can be found in the following issued U.S. Patent: 5,447,596.

[0006] Electrostatically focusing an electron beam is a technique that is well understood in the art. For instance, a negatively biased focus electrode can be used to electrostatically deflect the electron beam towards an axis of the beam. Resulting is an electron beam that converges into a narrower beam. Another example of electrostatic focusing is the use of a dielectric layer that co-axially encircles the path taken by the electron beam. The natural divergence of the beam allows the beam to impinge on the dielectric layer thereby inducing a negative electrostatic charge in the dielectric layer. Eventually, the induced charge reaches the potential of the emitter electrode. Consequently, the electrostatic charge causes the width of the beam to contract inward towards the axis of the beam. Finally, another method for focusing the beam includes the use of focusing ridges that are positioned on opposing sides of an array of emitters. The ridges are biased to a potential that is close to or equal the voltage of the emitters. The ridges electrostatically influence the trajectories of the electron beams from the array so that the phosphor in the target pixel is substantially struck by all of the emitted electrons. A general discussion of collimating electron beams in FED's can be found in the following issued U.S. Patents: 5,070,282; 5,235,244; and 5,528,103. The above mentioned focusing techniques are intended to sufficiently narrow the beam so that it strikes the target pixel with a beam width that is adequate to produce light of a desired intensity. Although the beam is narrowed by those focusing techniques, the beam is still too wide for use in high density storage applications. Furthermore, misalignment between the focusing element and the beam axis of the emitter will result in some deflection of the beam, but that deflection will not defeat proper operation of the FED. On the other hand, in a high density storage device it is desirable to have a very narrow and precisely aligned electron

beam that can be accurately directed towards the storage media.

[0007] It is also well known in the art to reduce the voltage potentials required to induce electron emission from the tip of the emitter by using microelectronic fabrication techniques to form a very sharp tip on the field emitter and/or by using a low work function material for the entire field emitter or just for the tip of the field emitter. Depending on the application, the work function of the materials used for field emitters can range from about 0.3 eV to about 6.0 eV. Work functions below 1.0 eV can be obtained by using materials, such as various types of carbon coatings, for example. A general discussion of FED field emitter materials and their work functions can be found in the following issued U.S. Patent: 5,702,281. Because FED's can be used in portable display applications, it is desirable to reduce power consumption by using low work function materials to reduce the bias voltages between electrodes. However, one disadvantage to low work function materials is that the microelectronic fabrication processes used in making the display can cause variations in the work function of the emitter material. Usually, the work function increases from its known value to a higher value. Consequently, the work function can vary from emitter to emitter, resulting in variations in electron beam current among the emitters of the FED.

[0008] Accordingly, there is a need for an electron source device that is adapted to emit a single, narrowly focused, electron beam, that includes an emitter structure having a uniform cone shape and a very sharp tip, that has an emitter made from a combination of materials having a work function that does not change during the course of microelectronic fabrication of the device, and that has an emitter that is self-aligned with the electrodes of the device.

[0009] The present invention is an improvement in the design of electron source devices. Particularly, the present invention includes improvements in the materials and structure used for an emitter of an electron source device.

[0010] The aforementioned disadvantages associated with focusing the electron bean are addressed by providing a cavity that is self-aligned with a vertex of the emitter so that the electrodes of the device are co-axially aligned with the beam axis of the emitter. The problems associated with an unstable work function for the emitter are addressed by using new combinations of materials that yield a stable work function. A uniform cone shape and a sharp tip for the emitter are addressed by using a composite of materials to form the emitter.

[0011] Broadly, the present invention is embodied in a self-aligned electron source device for generating a beam of electrons. The device includes a first dielectric layer upon which an emitter electrode is formed. A second dielectric layer is formed on the emitter electrode followed by forming an extractor electrode on the second dielectric layer. Next, a third dielectric layer is formed on the extractor electrode followed by forming a focus electrode on the third dielectric layer. A cavity is formed by a single photolithography step followed by a single etch step. The cavity extends through the focus electrode, the third dielectric layer, the extractor electrode, and the second dielectric layer. The cavity terminates at the emitter electrode. Finally, a composite emitter is formed on the emitter electrode. The composite emitter includes a base that is formed on the emitter electrode and a substantially conical tip that is formed on the base. The tip terminates at a vertex to form a sharp point. The cavity is disposed symmetrically about the composite emitter and is co-axially aligned with the vertex of the tip so that the cavity is centered about a beam axis through the vertex of the tip and the cavity and the composite emitter are substantially self-aligned relative to each other, resulting in an electrostatic lens assembly (including the extractor and focus electrodes) that is symmetric with respect to the beam axis of the composite emitter.

[0012] By applying application specific bias voltages between the electrodes of the device, electrons disposed proximate to the vertex of the tip can be extracted by the extractor electrode and focused into a smaller beam of electrons by the focus electrode. The electron beam can be used to write data to and to read data from advanced data storage systems including ultra-high density storage devices.

[0013] In embodiments of the present invention, to be described in detail below, the tip of the composite emitter can be made from a variety of electrically conductive materials including a refractory metal, a metal alloy, a silicon alloy, an electroformable metal, a carbide, or a nitride.

[0014] In one embodiment of the present invention, the first dielectric layer is formed on a substrate.

[0015] In another embodiment of the present invention, any one of the electrodes can be made from an electrically conductive composite material comprising a fine-grained amorphous layer formed on top of an adhesion layer.

[0016] In one embodiment of the present invention, the emitter electrode is made from a heavily doped semiconductor material.

[0017] In another embodiment of the present invention, the base of the composite emitter is made from titanium, chromium, or doped silicon.

[0018] In one embodiment of the present invention, any one of the second and third dielectric layers comprises an etch stop dielectric layer and a pull-back dielectric layer formed on top of the etch stop dielectric. The pull back dielectric layer includes a pull-back surface profile that is operative to reduce charge accumulation on cavity-facing portions of the dielectric layers.

[0019] In another embodiment of the present invention, the tip is made from an electroformable metal so that the vertex of the tip forms an atomically sharp point.

[0020] Other aspects and advantages of the present invention will become apparent from the following detailed

description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the present invention.

[0021] **FIG. 1** is a cross-sectional view of the self-aligned electron emission device according to the present invention.

[0022] **FIG. 2** is a cross-sectional view illustrating the position of the vertex relative to an upper surface and a lower surface of the extractor electrode according to the present invention.

[0023] **FIG. 3** is a cross-sectional view illustrating an atomically sharp vertex of an electroformed tip according to the present invention.

[0024] **FIG. 4** is a cross-sectional view of the device illustrating the cavity having a negative slope in the direction of the focus electrode according to the present invention.

[0025] **FIG. 5** and **FIG. 6** are cross-sectional views illustrating a dielectric layer having a pull-back surface profile according to the present invention.

[0026] **FIG. 7** is a cross-sectional view illustrating second and third dielectric layers having an etch stop dielectric layer and a pull-back dielectric layer according to the present invention.

[0027] **FIG. 8** is a cross-sectional view illustrating a pull-back surface profile etched into the dielectric layer of **FIG. 7.**

[0028] **FIG. 9** is a cross-sectional view illustrating electrodes made from an electrically conductive composite material according to the present invention.

[0029] **FIG. 10** is a cross-sectional view illustrating the relationship between the height of the composite emitter to the diameter of the cavity at the focus electrode and the height of the second dielectric layer according to the present invention.

[0030] **FIG. 11** is a top plan view of an array of self-aligned electron emission devices electrically configured to be enabled individually or in groups according to the present invention.

[0031] **FIG. 12** is a table illustrating metal alloys and silicon alloys for the tip according to the present invention.

[0032] In the following detailed description and in the several figures of the drawings, like elements are identified with like reference numerals.

[0033] As shown in the drawings for purpose of illustration, the present invention is embodied in a self-aligned electron source device that includes a first dielectric layer having an emitter electrode formed thereon, a second dielectric layer formed on the emitter electrode, an extractor electrode formed on the second dielectric layer, a third dielectric layer formed on the extractor electrode, and a focus electrode formed on the third dielectric layer. A cavity extending through the focus electrode, the third dielectric layer, the extractor electrode, and the second dielectric layer is formed in the device and terminates at the emitter electrode. A composite emitter is formed in the cavity and comprises a base formed on the emitter electrode and a substantially conical tip formed on the base and terminating at a vertex. The cavity is centered about the composite emitter and is co-axially aligned with a beam axis through the vertex so that the composite emitter and the cavity are substantially self-aligned with each other. The extractor electrode and the focus electrode form an electrostatic lens assembly that is adapted to extract electrons from the tip of the composite emitter and to focus the electrons into a narrow beam along the beam axis of the composite emitter.

[0034] The cavity is formed by a single photolithography step and a single dry etching step, thereby eliminating multiple patterning and etching steps that can increase manufacturing complexity, cost, and can introduce defects or contamination that reduce manufacturing yield. Furthermore, subsequent deposition of the materials for the base and tip of the composite emitter results in self-alignment between the cavity and the emitter.

[0035] The composite emitter, particularly the tip, can be made from materials selected to produce a stable work function that does not change during fabrication of the device. Additionally, the base and the tip are made from different materials that can be selected to yield a smooth conical tip having a sharp point at its vertex.

[0036] In **FIG. 1**, a self-aligned electron source device **10** includes a first dielectric layer **11.** An electrically conductive emitter electrode **13** is formed on the first dielectric layer **11.** A second dielectric layer **15** is formed on the emitter electrode **13**. An extractor electrode **17** is formed on the second dielectric layer **15.** A third dielectric layer **19** is formed on the extractor electrode **17**. A focus electrode **21** is formed on the third dielectric layer **19.** A cavity **23** is formed by etching thorough all of the above electrodes and dielectric layers except the emitter electrode **13** so that the cavity **23** terminates at the emitter electrode **13**. After forming the cavity **23,** a composite emitter **1** is formed in the cavity **23.** The composite emitter **1** includes a base **3** that is formed on the emitter electrode **13** and a substantially conical tip **5** that is formed on the base **3.** The tip **5** terminates at a vertex **V.** Preferably, the tip **5** has a sharp point at the vertex **V.** A sharp point at the vertex **V** increases the field strength at the vertex **V** thereby enhancing electron emission from the tip **5.**

[0037] The cavity **23** symmetrically surrounds the composite emitter **1** (i.e. the cavity **23** is centered about the composite emitter **1**) as shown by arrows $\mathbf{S_1}$ and $\mathbf{S_2}$ and is co-axially aligned with a beam axis **B** (shown as a dashed arrow) through the vertex **V** so that the cavity **23** and the composite emitter **1** are substantially self-aligned with each other. The cavity **23** can have substantially vertical sidewall surfaces **47** so that the cavity **23** has a substantially cylindrical shape.

[0038] The self-aligned electron source device **10** can be installed in an enclosure (not shown) having a partial

vacuum therein so that the cavity **23** is under a partial vacuum. Typically, the cavity **23** is under a partial vacuum of at least 10^{-5} torr or less.

[0039] One advantage of the self-aligned relationship between the cavity **23** and the composite emitter **1** is that electrons (not shown) extracted from the vertex **V** by the extractor electrode **17** are focused by the focus electrode **21** into a focused beam of electrons (not shown) substantially along the beam axis **B.** In essence, the focus electrode **21** narrows the cross-sectional width of the electron beam. Those electrons can impinge on a predetermined target location on a storage media (not shown) positioned opposite the focus electrode. For example, the electron beam can be used to store and access information on the storage media. The distance between the vertex **V** of the tip **5** and the storage media and the width of the electron beam at the target location will be application specific.

[0040] The cavity **23** can be formed by a single photolithography step and a single dry etching step. For instance, a conventional reactive ion etching (RIE) process in the semiconductor industry can be used to form the cavity **23.**

[0041] In one embodiment of the present invention, the first dielectric layer **11** can be formed on a substrate **25**. The substrate **25** can be a semiconductor substrate. For instance, the substrate **25** can be silicon. One advantage to using a semiconductor for the substrate **25** is that active circuits for addressing the composite emitter **1** can be formed in the substrate **25.** Other suitable materials for the substrate **25** include glass and quartz.

[0042] In another embodiment of the present invention, as illustrated in **FIG. 2,** the vertex **V** of the tip **5** is positioned intermediate between an upper surface **31** and a lower surface **33** (both shown in dashed line) of the extractor electrode **17.** Although the vertex **V** can be positioned above the upper surface **31** or below the lower surface **33,** in a preferred embodiment, the most efficacious extraction of electrons from the tip **5** results from positioning the vertex **V** intermediate between the upper surface **31** and the lower surface **33** of the extractor electrode **17.**

[0043] The base **3** of the composite emitter **1** need not have a substantially cylindrical shape as shown in **FIG. 1.** The base **3** can have an arcuate shape or a cone shape as illustrated in **FIG. 2.** The actual shape of the base **3** will depend on the material selected for the base **3** and the deposition process used to form the base **3.**

[0044] Conventional semiconductor integrated circuit fabrication processes that are well known in the art can be used to fabricate the device **10.** For instance, conventional photolithography and etching techniques can be used to form the cavity **23.** The cavity **23,** can be etched using RIE, for example. The dielectric layers and the electrodes can be formed using conventional thin-film deposition techniques. The composite emitter **1** can be formed by using evaporation techniques to deposit the base **3** and the tip **5**.

[0045] Materials for the base **3** of the composite emitter **1** include titanium (**Ti**), chromium **(Cr),** niobium **(Nb),** and resistive materials such as doped silicon **(Si).**

[0046] In one embodiment of the present invention, the tip **5** of the composite emitter **1** can be made from a refractory metal. The refractory metal for the tip **5** includes but is not limited to those shown in **Table 1** below.

Refractory Metals for the Tip 5
molybdenum (**Mo**)
niobium (**Nb**)
hafnium (**Hf**)
zirconium (**Zr**)
tantalum (**Ta**)
tungsten (**W**)
vanadium (**V**)

Table 1

[0047] In another embodiment of the present invention, the tip **5** of the composite emitter **1** can be made from a metal alloy or a silicon alloy. The alloys for the tip **5** include but are not limited to the alloys listed in **Table 2** below.

Metal Alloys and Silicon Alloys for the Tip 5
titanium molybdenum (**TiMo**)
titanium niobium (**TiNb**)
titanium hafnium (**TiHf**)
titanium zirconium (**TiZr**)
molybdenum niobium (**MoNb**)
molybdenum hafnium (**MoHf**)
molybdenum zirconium (**MoZr**)
titanium tungsten (**TiW**)
tungsten chromium (**WCr**)
silicon titanium (**SiTi**)
silicon tungsten (**SiW**)

Table 2

[0048] **FIG. 12** illustrates a matrix of alloys for the tip **5** and includes the metal and silicon alloys of **Table 2.** In **FIG. 12,** a suitable alloy for the tip **5** is indicated by a check ✓ at an intersection of a row with a column. Column numbers increase from left to right as shown by arrow **C** and row numbers increase from top to bottom as shown by arrow **R** in **FIG. 12.** For instance, silicon **(Si)** in row 10 can be combined with zirconium **(Zr)** in column 5 to form a silicon zirconium **(SiZr)** alloy for the tip **5.** Similarly, tungsten **(W)** in row 7 can be combined with chromium **(Cr)** in column 8 to form a tungsten chromium **(WCr)** alloy. As can be seen in **FIG. 12,** the metal alloys for the tip **5** include the refractory metals listed in **Table 1** above. Accordingly, a metal alloy can be made from any two different materials (excluding silicon (**Si**)) listed in **FIG. 12.** Furthermore, a silicon alloy can be made from any two different materials listed in **FIG. 12.**

[0049] One method for forming the tip **5** from the alloys of **FIG. 12** is to use a coevaporation process. For example, to form a silicon titanium **(SiTi)** alloy as indicated by the check ✓ at row 10, column 1, a silicon **(Si)** source and a titanium source **(Ti)** can be evaporated at the same time to form the tip **5**. On the other hand, a source comprising both silicon **(Si)** and titanium **(Ti)** can be evaporated to form the tip **5**.

[0050] In one embodiment of the present invention, as illustrated in **FIG. 3,** the tip **5** of the composite emitter **1** is made from an electroformable metal. The process for low temperature electroforming of the tip **5** is well known in the art. For instance, the tip **5** can be electroformed by first depositing the material for the tip **5** on the base **3.** Next, the device **10** is heated to a temperature of about half the melting point of the metal used for the tip **5.** An extraction field is applied to the extraction electrode **17** at a field strength below that necessary to extract electrons from the tip **5.** The material used for the tip **5** begins to flow under the force of the extraction field. Resulting is an atomically sharp point at the vertex **V** of the tip **5.**

[0051] Suitable materials for the electroformable metal include but are not limited to those listed in **Table 3** below.

Electroformable Metals for the Tip 5
tin (**Sn**)
indium (**In**)
magnesium (**Mg**)
tin alloy
indium alloy
magnesium alloy

Table 3

[0052] In another embodiment of the present invention, the tip **5** of the composite emitter **1** can be made from a carbide **(C).** The carbide **(C)** for the tip **5** includes but is not limited to the electrically conductive carbides shown in **Table 4** below.

Carbides for the Tip 5
silicon carbide (**SiC**)
titanium carbide (**TiC**)
tungsten carbide (**WC**)
tantalum carbide (**TaC**)
niobium carbide (**NbC**)
hafnium carbide (**HfC**)
zirconium carbide (**ZrC**)
molybdenum carbide (**MoC**)

Table 4

[0053] In another embodiment of the present invention, the tip **5** of the composite emitter **1** can be made from a nitride (**N**). The nitride (**N**) for the tip **5** includes but is not limited to the electrically conductive nitrides shown in **Table 5** below.

Nitrides for the Tip 5
silicon nitride (**SiN**)
titanium nitride (**TiN**)
tungsten nitride (**WN**)
tantalum nitride (**TaN**)
niobium nitride (**NbN**)
hafnium nitride (**HfN**)
zirconium nitride (**ZrN**)
molybdenum nitride (**MoN**)

Table 5

[0054] The first dielectric layer **11**, the second dielectric layer **15,** and the third dielectric layer **19** can be made from a dielectric material that includes but is not limited to silicon oxide, silicon nitride, silicon carbide, silicon oxide on top of silicon carbide, and silicon oxide on top of silicon nitride.

[0055] The emitter electrode **13,** the extractor electrode **17,** and the focus electrode **21** can be made from an electrically conductive material that includes but is not limited to aluminum **(Al),** tungsten **(W),** gold **(Au),** platinum **(Pt),** copper **(Cu),** chromium **(Cr),** titanium **(Ti),** tantalum **(Ta),** tantalum aluminum **(TaAl),** titanium nitride (**TiN**), tungsten nitride **(WN),** tantalum nitride **(TaN),** tantalum tungsten nitride **(TaWN),** titanium carbide **(TiC),** aluminum carbide **(AlC),** tantalum carbide **(TaC),** and tungsten carbide **(WC).**

[0056] In one embodiment of the present invention, the emitter electrode **13** is made from an electrically conductive material comprising a heavily doped semiconductor. The heavily doped semiconductor can be silicon **(Si).**

[0057] In another embodiment of the present invention, as illustrated in **FIG. 4,** at least a portion of the cavity **23** has a negative slope **41** in a direction towards the focus electrode **21** (i.e. the cavity narrows in the direction of the focus electrode **21).** The negative slope **41** is operative to reduce charge accumulation on surfaces of the second **15** and third **19** dielectric layers that face the cavity **23.**

[0058] In one embodiment of the present invention, as illustrated in **FIG. 5,** the second dielectric layer **15** and/or the third dielectric layer **19** includes a cavity facing portion **43** and **45** respectively, having a pull-back surface profile **40** that is operative to reduce charge accumulation on the cavity facing portions **43** and **45** respectively by positioning those portions away from the bore of the cavity **23.** The emitter electrode **13** and the extractor electrode **17** serve as etch stops for the second dielectric layer **15** and/or the third dielectric layer **19** as shown by arrows **49.**

[0059] The pull-back surface profile **40** can be an arcuate shape as illustrated in **FIG. 5** or the pull-back surface profile **40** can be a sloped shape (not shown). The cavity **23** can have the substantially vertical sidewall surfaces **47** as illustrated in **FIG. 5** or the cavity **23** can have the negative slope **41** as illustrated in **FIG. 6** and discussed above in reference to **FIG. 4.** The cavity **23** can also have a positive slope (not shown) in a direction toward the focus electrode **21.** Other shapes for the pull-back surface profile **40** are possible and the shape of the pull-back surface profile **40** will depend on the etching process used.

[0060] In another embodiment of the present invention, as illustrated in **FIG. 7,** the second and third dielectric layers **15** and **19** respectively can include a dielectric and mechanical strength enhancement layer **15a** and **19a** of silicon nitride (**SiN**) or silicon carbide **(SiC)** and a pull-back dielectric layer **15b** and **19b** of silicon oxide (SiO_2) formed on top of the dielectric and mechanical strength enhancement layers **15a** and **19a.**

[0061] The dielectric and mechanical strength enhancement layers **15a** and **19a** enhance the resistance to dielectric breakdown in high voltage operation of the device**10**. Additionally, the dielectric and mechanical strength enhancement layers **15a** and **19a** mechanically strengthen the adjacent metal layers that form the emitter electrode **13** and the extractor electrode **17.**

[0062] The pull-back dielectric layers **15b** and **19b** can include the pull-back surface profile **40,** as illustrated in **FIG. 8.** The thickness of the pull-back dielectric layers **15b** and **19b** can be from about 100 nanometers to about 2000

nanometers. The etch stop dielectric layers **15a** and **19a** can have a thickness from about 50 nanometers to about 200 nanometers. The pull-back surface profile **40** can be an arcuate shape as illustrated in **FIG. 8** or the pull-back surface profile **40** can be a sloped shape. For example, the arcuate shape or the sloped shape can have a positive or a negative slope in the direction of the focus electrode **21.** Other shapes for the pull-back surface profile **40** are possible and the shape of the pull-back surface profile **40** will depend on the etching process used.

[0063] In one embodiment of the present invention, as illustrated in **FIG. 9,** the emitter electrode **13,** the extractor electrode **17,** and the focus electrode **21** can be made from an electrically conductive composite material including a fine-grained amorphous layer **13b, 17b,** and **21b** respectively, formed on top of an adhesion layer **13a, 17a,** and **21a** respectively. The fine-grained amorphous layers **13b, 17b,** and **21b** can be a metal with a small grain structure, i.e. an amorphous structure like that of a metallic glass. In particular, by using a fine-grained or amorphous layer for the emitter electrode **13,** the base **3** can be deposited onto the fine-grained or amorphous layer **13b** with no preferred crystal orientation. Resulting is a smooth surface upon which the tip **5** can be grown. The smooth surface of the base **3** allows the tip **5** to grow with a smooth, uniform, and symmetrical cone shape that terminates at a sharp point at the vertex **V.**

[0064] Materials for the fine-grained amorphous layer **13b**, **17b,** and **21b** include but are not limited to titanium nitride (**TiN**), tantalum nitride (TaN), and tungsten nitride **(WN)** on top of any one of the following materials for the adhesion layer **13a, 17a,** and **21a**: titanium **(Ti);** aluminum (**Al**); tantalum **(Ta);** tungsten **(W);** and chromium **(Cr).**

[0065] In another embodiment of the present invention, as illustrated in **FIG. 2,** an electrode abutting surface **22** of any one of the first dielectric layer **11,** the second dielectric layer **15** and the third dielectric layer **19** can be planarized to form a substantially flat surface. A planarization process such as chemical mechanical polishing (CMP) can be used to planarize the dielectric layers. Planarization results in a smooth and flat surface upon which to deposit the electrodes.

[0066] In one embodiment of the present invention, the emitter electrode **13,** the extractor electrode **17,** and the focus electrode **21** have a thickness of about 50 nanometers to about 200 nanometers.

[0067] In another embodiment of the present invention, as illustrated in **FIG. 10,** the second dielectric layer **15** has a thickness that is substantially equal to a height **H** of the composite emitter **1** at the vertex **V** of the tip **5.**

[0068] In one embodiment of the present invention, as illustrated in **FIG. 10,** the cavity **23** has a diameter **W** at the focus electrode **21** that is substantially equal to the height **H** of the composite emitter **1** at the vertex **V** of the tip **5.**

[0069] The thickness of the second dielectric layer **15** and the diameter **W** of the cavity **23** will be determined by application specific parameters for the device **10** and can be controlled through the photolithography, deposition and etching steps used to fabricate the device **10.**

[0070] **FIG. 11** illustrates a top plan view of an array **20.** The device **10** is replicated four times **(10a, 10b, 10c,** and **10d)** in the array **20**. However, **FIG. 11** is not to be construed as limiting the number of devices **10** that can be arrayed as shown. For instance, the array **20** can include but is not limited to a 10 * 10 array of devices **10**. The array **20** includes two emitter electrodes **13** arranged into rows $\mathbf{R_n}$ and $\mathbf{R_{n+1}}$ and two extractor electrodes **17** arranged into two columns $\mathbf{C_n}$ and $\mathbf{C_{n+1}}$**.** Although only two rows and two columns are illustrated, the array **20** can include any combination of rows and columns. To activate one or more of the devices **10,** appropriate bias voltages can be applied to the emitter electrodes **13** and the extractor electrodes **17**. For instance, to activate the device **10b** so that electrons (not shown) are extracted from its composite emitter **1,** the emitter electrode **13** in row $\mathbf{R_n}$ can be connected to a low voltage relative to the extractor electrode **17** in column $\mathbf{C_{n+1}}$ to create an extraction field that will induce electrons to quantum tunnel off of the vertex **V** of the tip **5.** For example, the emitter electrode **13** in row $\mathbf{R_n}$ can be connected to a **GND** terminal (not shown) of a power source and the extractor electrode **17** in column $\mathbf{C_{n+1}}$ can be connected to a positive terminal (not shown) of a power source. The focus electrode can be connected to the **GND** terminal or some other negative voltage source. In **FIG. 11,** the composite emitter **1** and a portion of the emitter electrode **13** are visible through the cavity **23** in the focus electrode **21.** The symmetry between the composite emitter **1** and the cavity **23** is also illustrated in **FIG. 11.**

[0071] Additionally, FIG. **11** illustrates the relationship between the various metal layers used to implement the electrodes **13, 17,** and **21.** For instance, the emitter electrode **13** can be implemented in a metal one layer **m1**, the extractor electrode **17** can be implemented in a metal two layer **m2,** and the focus electrode **21** can be implemented in a metal three layer **m3.** The number of metal layers will be determined by the semiconductor process used to fabricate the device **10** and the layout design rules for that process.

[0072] Additionally, the devices **10a, 10b, 10c,** and **10d** can have their respective electrodes individually connected to (i.e. in electrical communication with) active switching elements (not shown) such as a field-effect transistor (FET) that allow the devices in the array **20** to be switched "On" (emit electrons) or "Off" (no electron emission) by using digital logic gates to control the gate nodes of their respective FET's. The FET can be a metal-oxide-semiconductor field-effect transistor (MOSFET), for example.

[0073] For instance, the device **10b** can have its emitter electrode **13** formed directly on a drain node of a FET. A gate node of the FET can be connected to a digital signal source adapted to turn the FET "On" or "Off". A source node of the FET can be connected to a **GND** node of a power supply. An appropriate digital signal on the gate node of the FET can be used to turn the device **10b** "On" or "Off". When the device **10b** is "On", the emitter electrode **13** is sub-

stantially at **GND.** Electron emission from the emitter **1** of the device **10b** can be initiated by biasing the extractor electrode **17** to a positive potential relative to the emitter electrode **13** so that electrons quantum mechanically tunnel out of the tip **5** of the emitter **1.** The drain node of the FET can be connected to the emitter electrode using a tungsten (**W**) plug, for example. Conversely, the electrode **13** can be formed directly on a source node of a FET and the drain node of the FET can be connected to a **GND** node of a power supply.

[0074] Although several embodiments of the present invention have been disclosed and illustrated, the invention is not limited to the specific forms or arrangements of parts so described and illustrated. The invention is only limited by the claims.

Claims

1. An electron source device 10 comprising:

a first dielectric layer 11;
an emiter electrode 13 formed on the first dielectric layer 11;
a composite emitter 1 including a base 3 formed on the emitter electrode 13 and a substantially conical tip 5 formed on the base 3 and terminating at a vertex V;
a second dielectric layer 15 formed on the emitter electrode 13;
an extracter electrode 17 formed on the second dielectric layer 15;
a third dielectric layer 19 formed on the extractor electrode 17; and
a focus electrode 21 formed on the third dielectric layer 19;
the focus and extractor electrodes (21, 17) and the second and third dielectric layers (15, 19) include a cavity 23 extending from the focus electrode 21 and terminating at the emitter electrode 13, the cavity 23 symmetrically surrounds the composite emitter 1 and is co-axially aligned with the vertex V of the tip 5 so that the cavity 23 and the composite emitter 1 are substantially self-aligned relative to each other.

2. The device of Claim 1, wherein the tip 5 of the composite emitter 1 is made from a refractory metal and the refractory metal includes a material selected from the group consisting of molybdenum, niobium, hafnium, zirconium, tantalum, tungsten, and vanadium.

3. The device of Claim 1, wherein the tip 5 of the composite emitter 1 is made from a metal alloy and the metal alloy includes a combination of any two dissimilar materials selected from the group consisting of titanium, molybdenum, niobium, hafnium, zirconium, vanadium, tungsten, chromium, and tantalum.

4. The device of Claim 1, wherein the tip **5** of the composite emitter **1** is made from an electroformable metal and the vertex **V** forms an atomically sharp point and the electroformable metal includes a material selected from the group consisting of tin, tin alloy, indium, indium alloy, magnesium, and magnesium alloy.

5. The device of Claim 1, wherein the tip **5** of the composite emitter **1** is made from an electrically conductive carbide and the electrically conductive carbide includes a material selected from the group consisting of silicon carbide, titanium carbide, tungsten carbide, tantalum carbide, niobium carbide, hafnium carbide, zirconium carbide, and molybdenum carbide.

6. The device of Claim 1, wherein the tip **5** of the composite emitter **1** is made from an electrically conductive nitride and the electrically conductive nitride includes a material selected from the group consisting of silicon nitride, titanium nitride, tungsten nitride, tantalum nitride, hafnium nitride, niobium nitride, zirconium nitride, and molybdenum nitride.

7. The device of Claim 1, wherein the base **3** of the composite emitter **1** is a material selected from the group consisting of titanium, chromium, niobium, and doped silicon.

8. The device of Claim 1, wherein any one of the dielectric layers (**11**, **15**, **19**) is made from a dielectric material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, silicon oxide on top of silicon carbide, and silicon oxide on top of silicon nitride.

9. The device of Claim 1, wherein any one of the electrodes (**13, 17, 21)** is made from an electrically conductive material selected from the group consisting of aluminum, tungsten, gold, platinum, copper, chromium, titanium,

tantalum, tantalum aluminum, titanium nitride, tungsten nitride, tantalum nitride, tantalum, tungsten nitride, titanium carbide, tantalum carbide, tungsten carbide, and aluminum carbide.

10. The device of Claim 1, wherein any one of the electrodes (**13**, **17**, **21**) is made from an electrically conductive composite material comprising a fine-grained amorphous layer **(13b, 17b, 21b**) formed on top of an adhesion layer **(13a, 17a, 21a),**

the fine-grained amorphous layer **(13b, 17b, 21b**) is a material selected from the group consisting of titanium nitride, tantalum nitride, and tungsten nitride, and

the adhesion layer **(13a, 17a, 21a)** is a material selected from the group consisting of titanium, aluminum, tantalum, tungsten, and chromium.

11. The device of Claim 1, wherein the emitter electrode **13** is made from an electrically conductive material comprising a heavily doped semiconductor.

12. The device of Claim 1, wherein any one of the second and third dielectric layers (**15, 19**) comprises a cavity-facing portion **(43, 45)** having a pull-back surface profile **40** that is operative to reduce electrical charge accumulation on the cavity-facing portion **(43, 45)** and the pull-back surface profile **40** includes a shape selected from the group consisting of a sloped shape and an arcuate shape.

13. The device of Claim 12, wherein any one of the second and third dielectric layers (**15, 19**) comprises a dielectric and mechanical strength enhancement layer (**15a, 19a)** and a pull-back dielectric layer **(15b, 19b)** of silicon oxide formed on top of the dielectric and mechanical strength enhancement layer **(15a, 19a),**

the pull-back dielectric layer **(15b, 19b)** includes the pull-back surface profile **40,** and

the dielectric and mechanical strength enhancement layer **(15a, 19a)** is made from a material selected from the group consisting of silicon nitride and silicon carbide.

14. The device of Claim 1, wherein at least a portion of the cavity **23** has a negative slope **41** in a direction towards the focus electrode **21.**

15. The device of Claim 1, wherein the tip **5** of the composite emitter **1** is made from a silicon alloy.

16. The device of Claim 15, wherein the silicon alloy is a combination of silicon and a material selected from the group consisting of titanium, molybdenum, niobium, hafnium, zirconium, vanadium, tungsten, chromium, and tantalum.

17. The device of Claim 1, wherein the emitter electrode **13** is formed directly on a node of a field-effect transistor selected from the group consisting of a drain node and a source node.

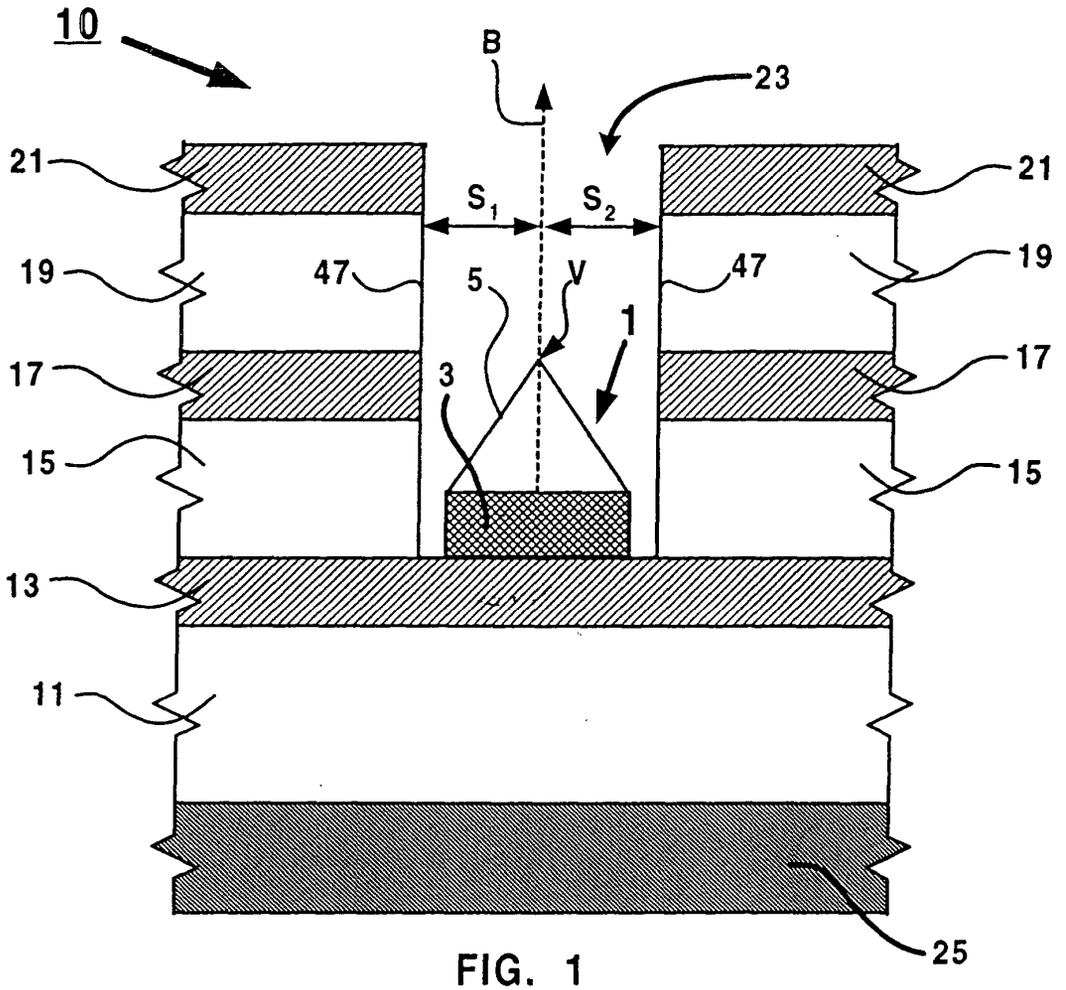
10
B
23
21
21
S_1
S_2
19
47
5
V
47
19
1
17
3
17
15
15
13
11
25

FIG. 1

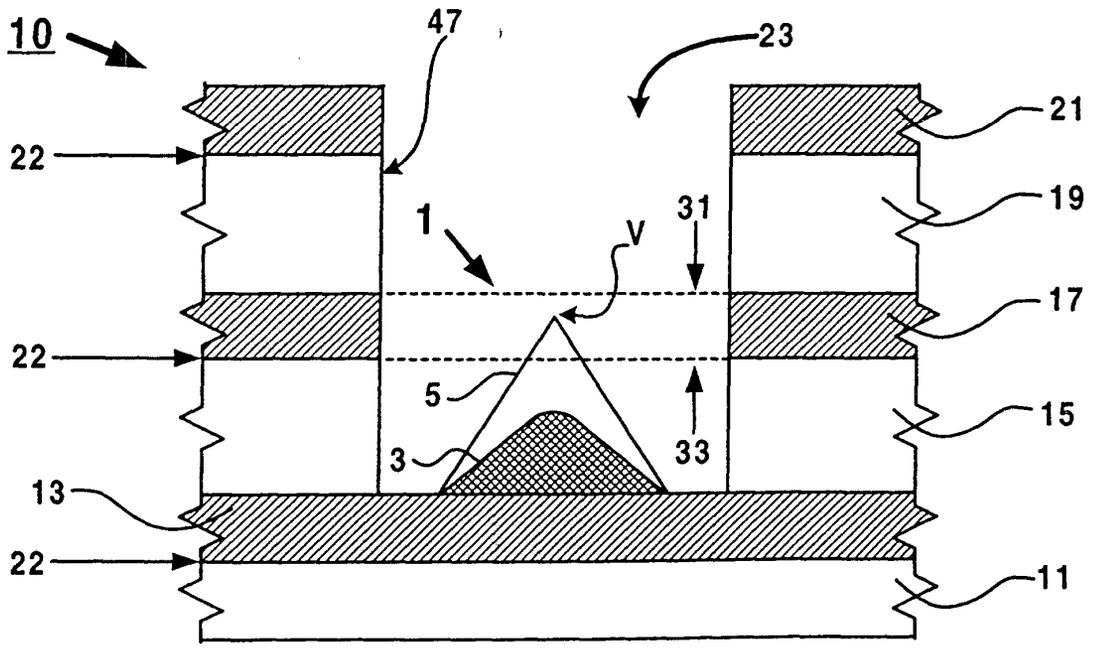
10
47
23
21
22
1
V
31
19
17
22
5
15
3
33
13
22
11

FIG. 2

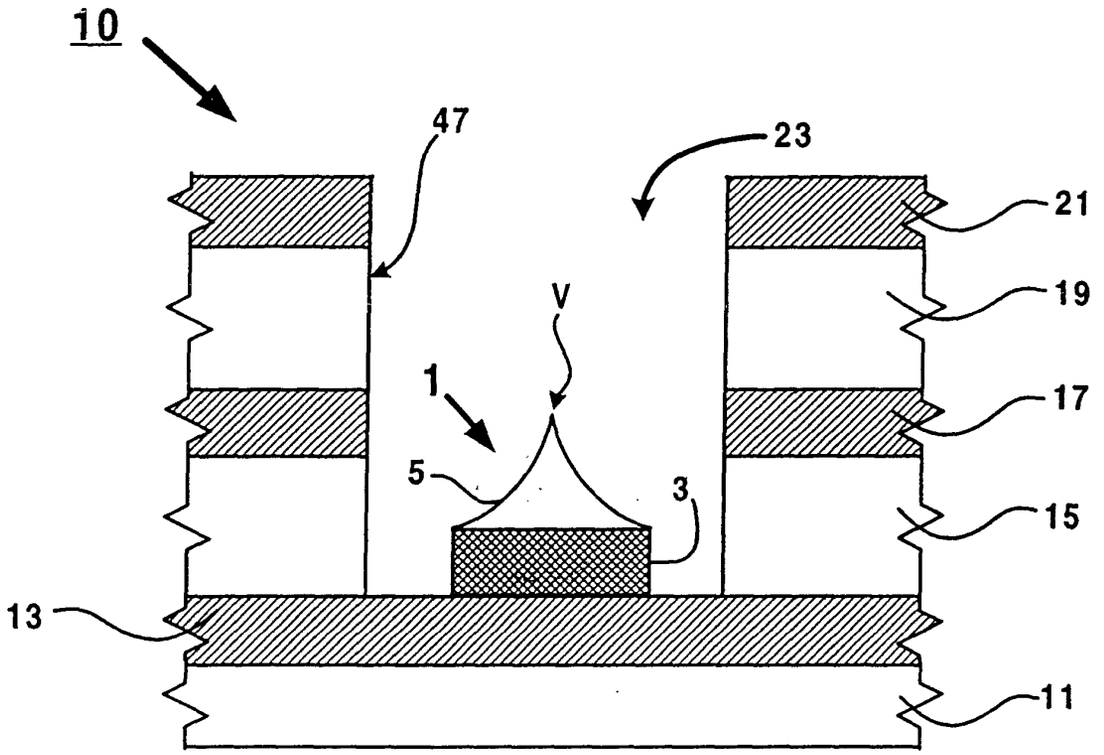

FIG. 3

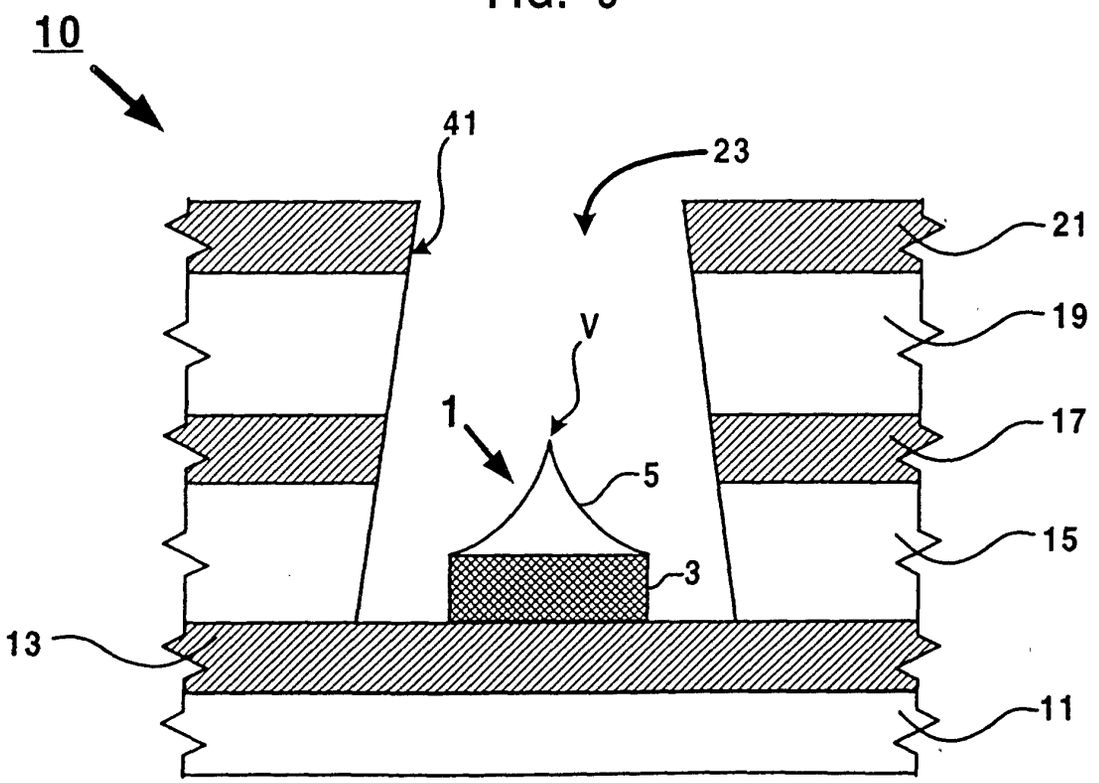

FIG. 4

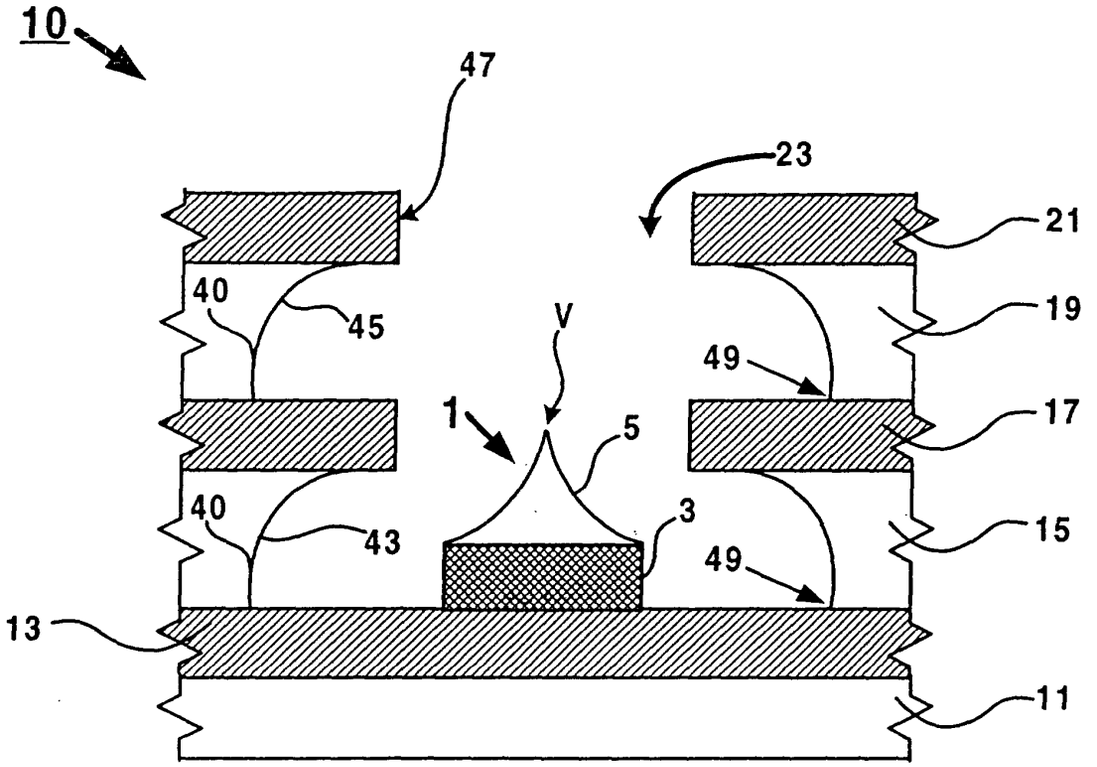
10
47
23
21
40
45
V
19
49
1
5
17
40
43
3
15
49
13
11

FIG. 5

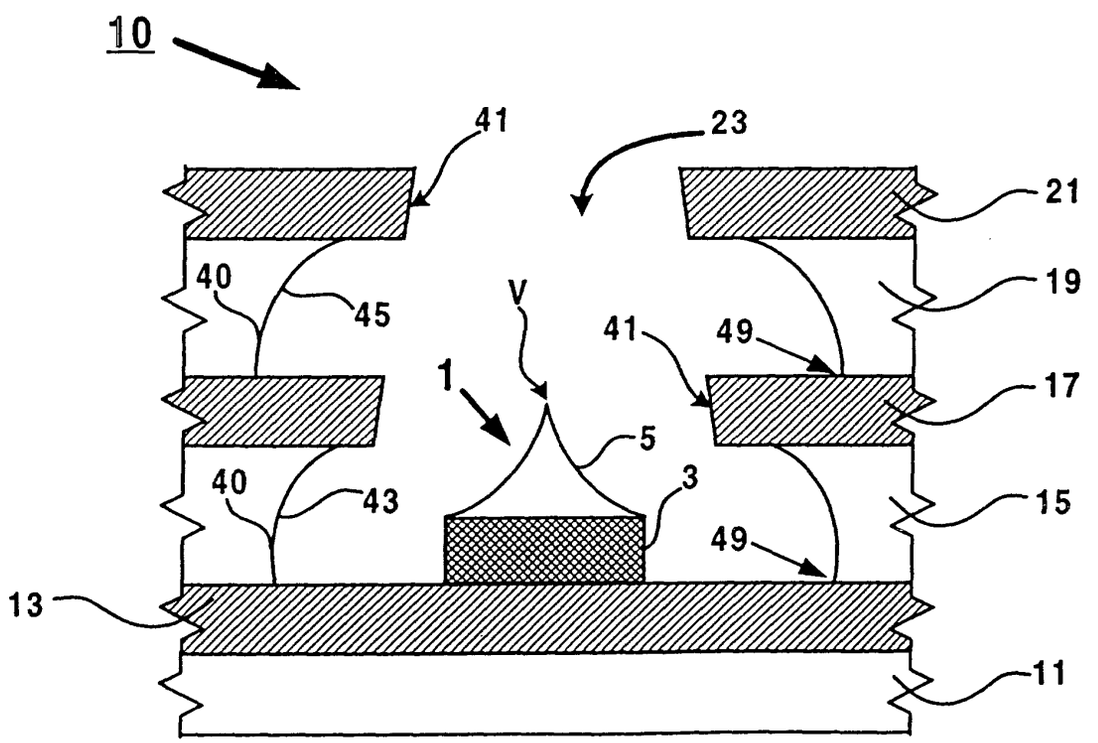
10
41
23
21
40
45
V
19
41
49
1
17
5
40
43
3
15
49
13
11

FIG. 6

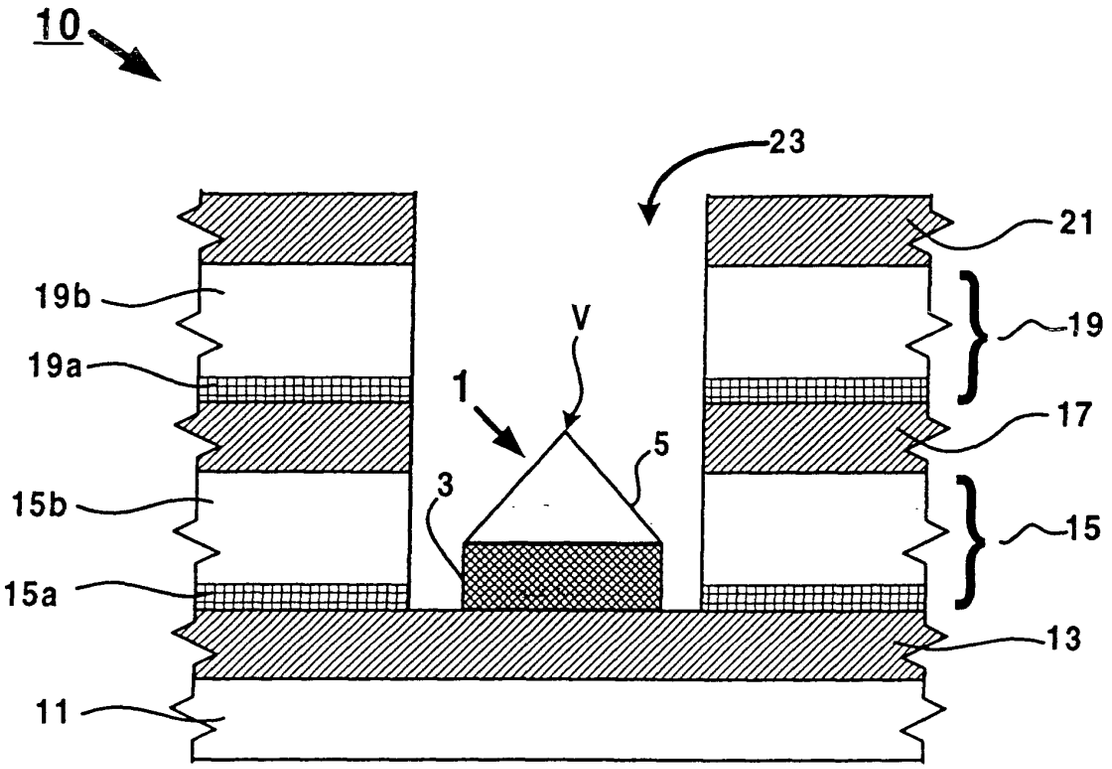
10
23
21
19b
19
V
19a
1
17
5
3
15b
15
15a
13
11

FIG. 7

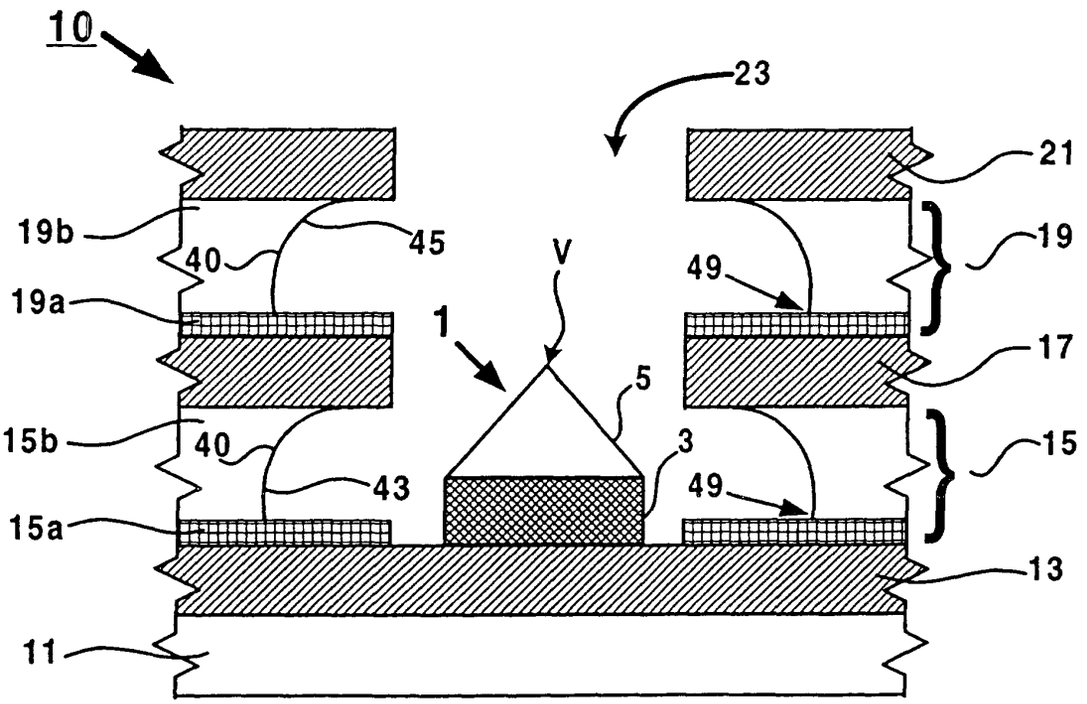
10
23
21
19b
45
19
40
V
49
19a
1
17
5
15b
40
3
15
43
49
15a
13
11

FIG. 8

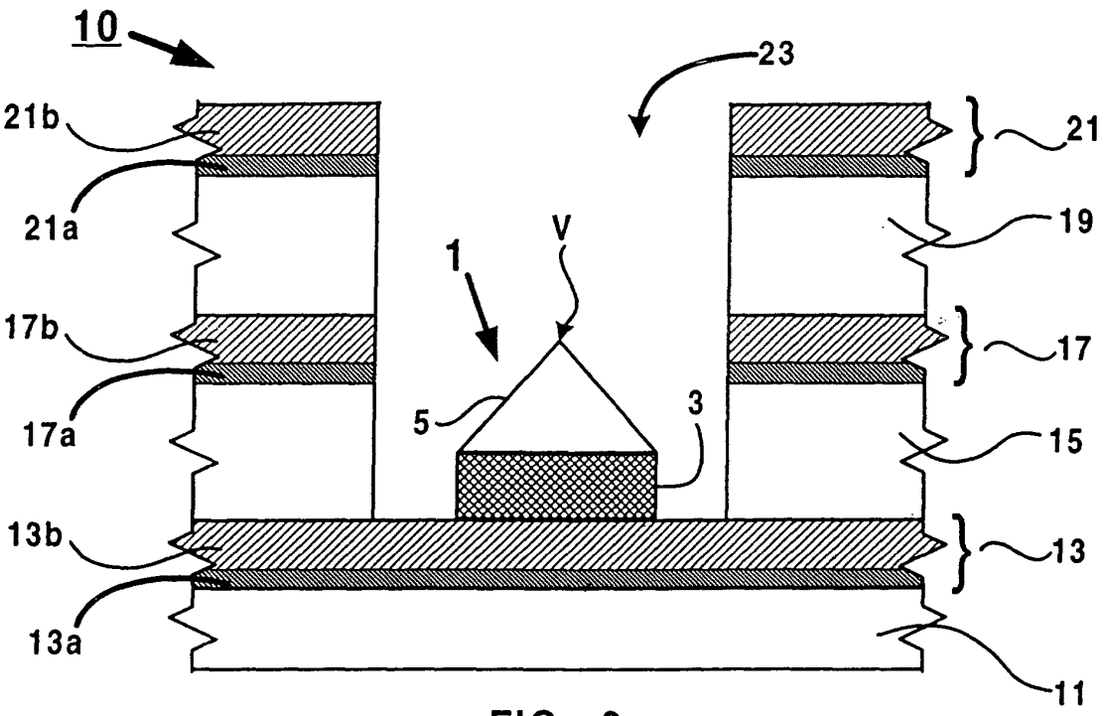
10
23
21b
21a
21
19
V
1
17b
17a
17
5
3
15
13b
13a
13
11

FIG. 9

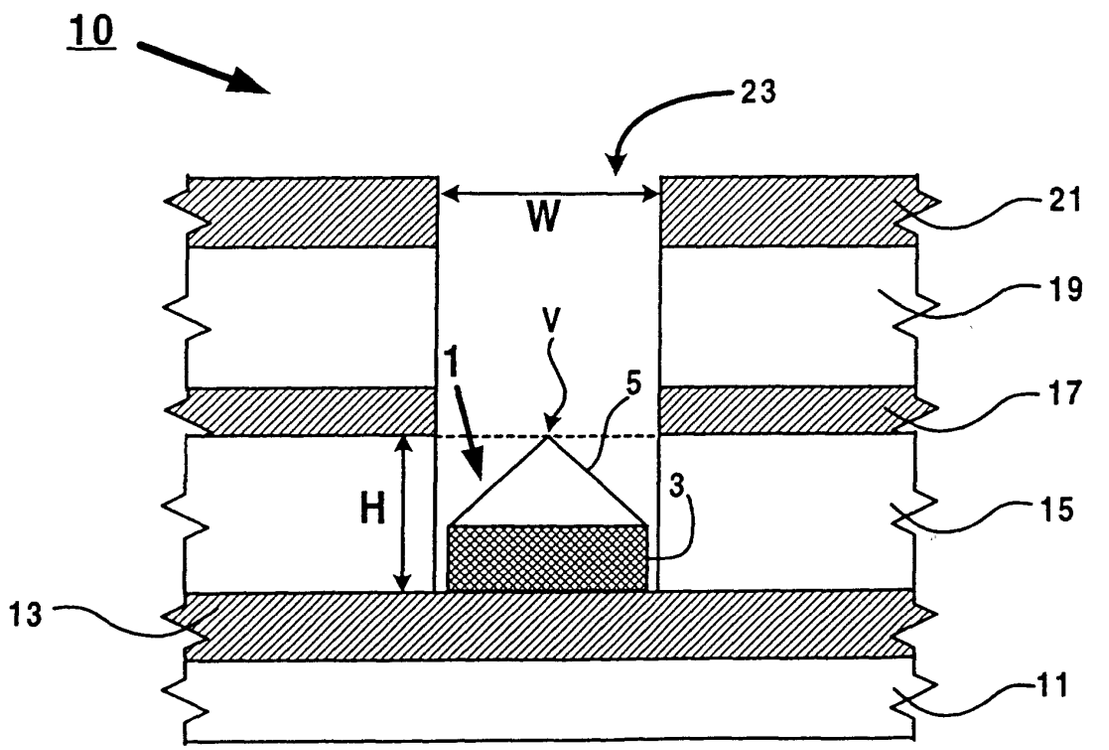
10
23
W
21
19
V
1
5
17
H
3
15
13
11

FIG. 10

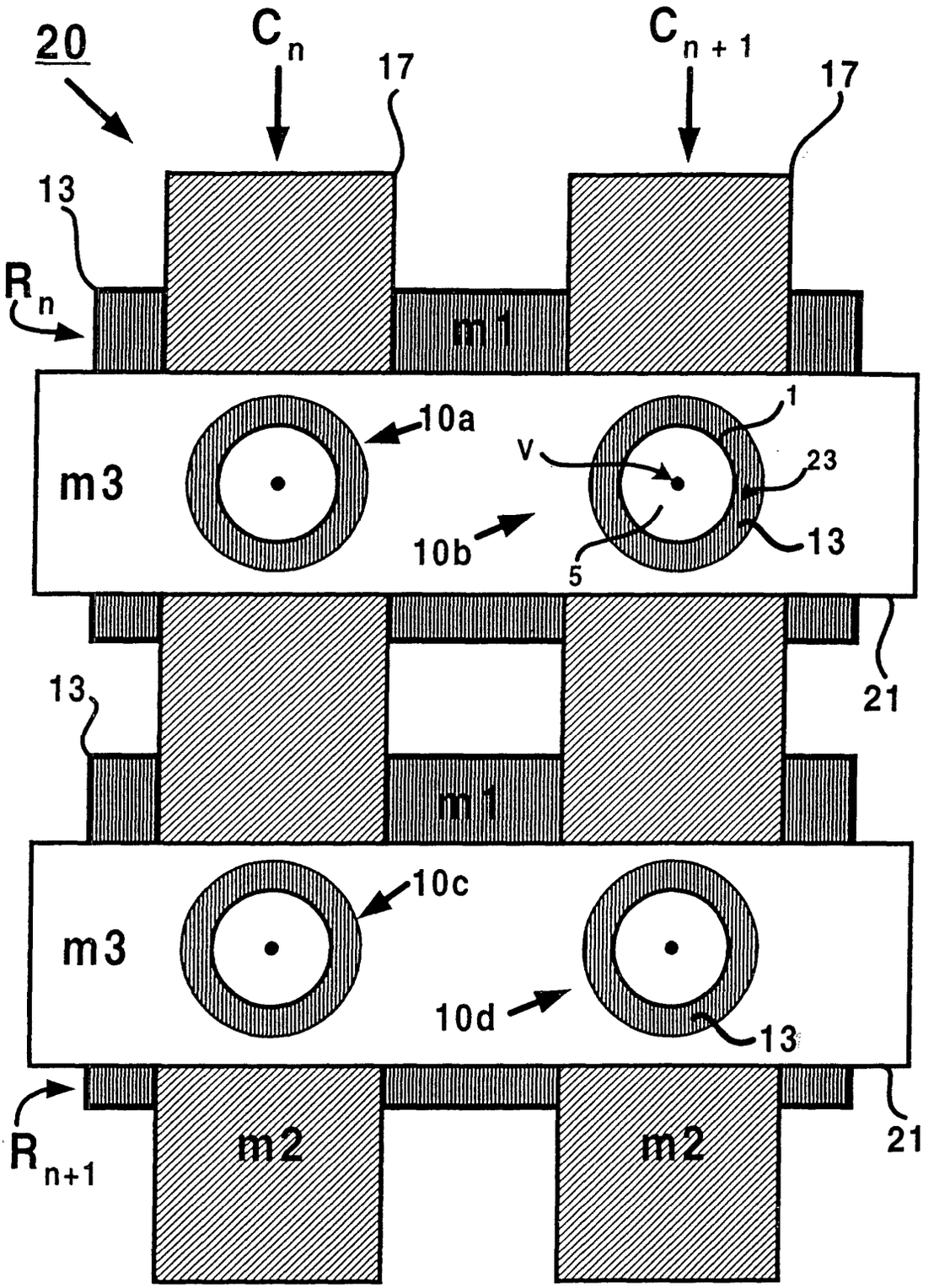
20
C_n
C_{n+1}
17
17
13
R_n
m1
m3
10a
1
V
23
10b
13
5
21
13
m1
m3
10c
10d
13
21
R_{n+1}
m2
m2

FIG. 11

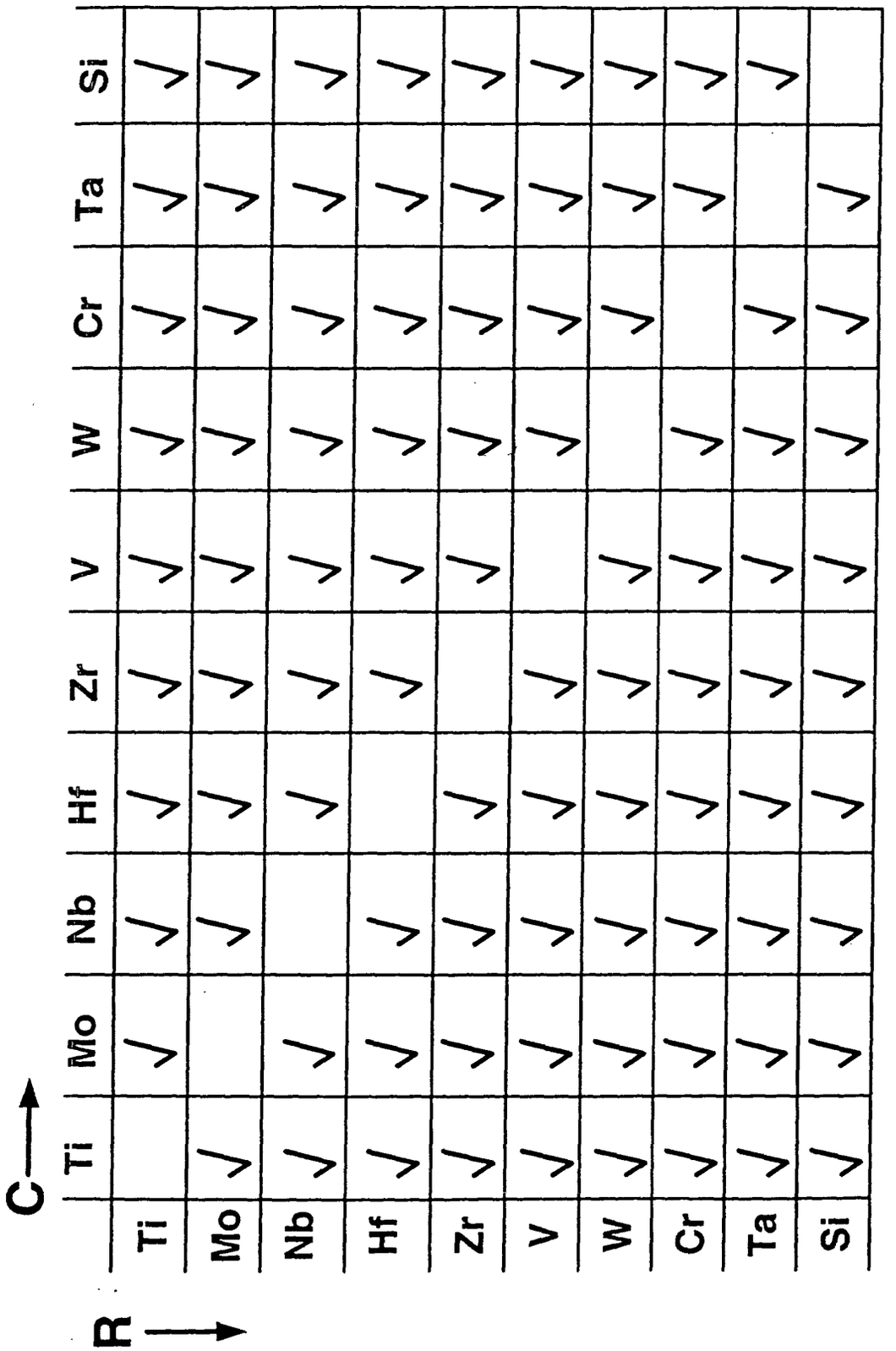

FIG. 12