

[54] **COMPUTER TYPE FLASH APPARATUS
WITH NOISE INHIBITING QUENCH
CIRCUIT**

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Related U.S. Application Data

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1971, abandoned.

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315/239, 315/241 R, 315/274

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[58] Field of Search 315/241 P, 57, 239,
315/262, 267, 274, 275, 344, 241 R, 241 S, 151

[56] **References Cited**

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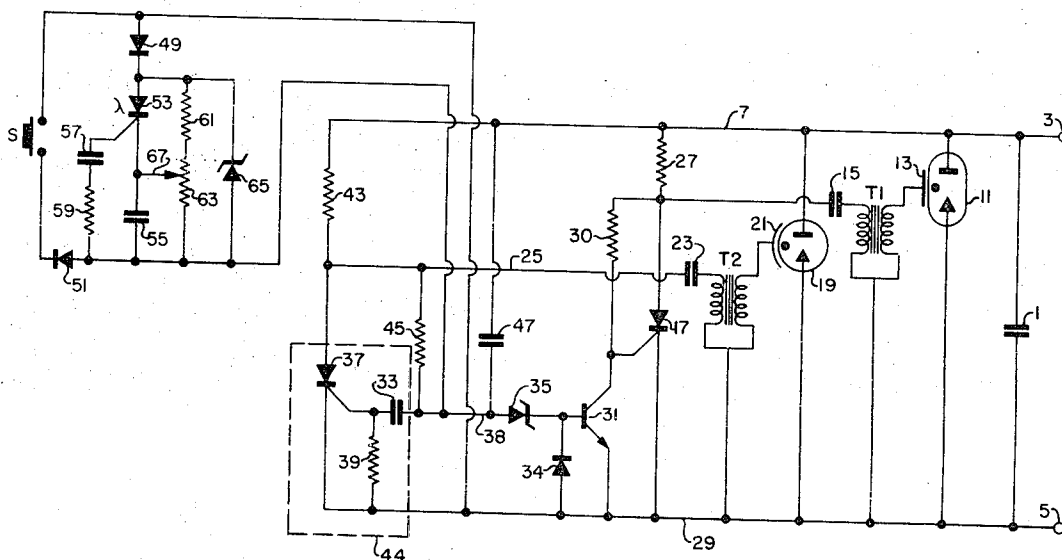
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[57] **ABSTRACT**

A computer type flash apparatus includes a switching device, a sensing transmitter and a flash device. The switching device is selectively operable for providing a contact closure to fire the flash device, which, in turn, produces light for the illumination of a scene to be photographed. The sensing transmitter provides a quench signal upon receipt of a predetermined amount of light from the scene. The quench signal is applied through a capacitor to the gate terminal of a silicon controlled rectifier (SCR) to trigger the SCR thereby actuating a quench circuit in the flash device. The operation of the quench circuit terminates the production of light by the flash device. A resistor is connected between the gate and cathode terminals of the SCR. When the flash device is fired, a signal representative thereof effects the appearance of a voltage across the resistor to inhibit noise signals from falsely triggering the SCR until the quench signal is generated by the sensing transmitter.

5 Claims, 2 Drawing Figures



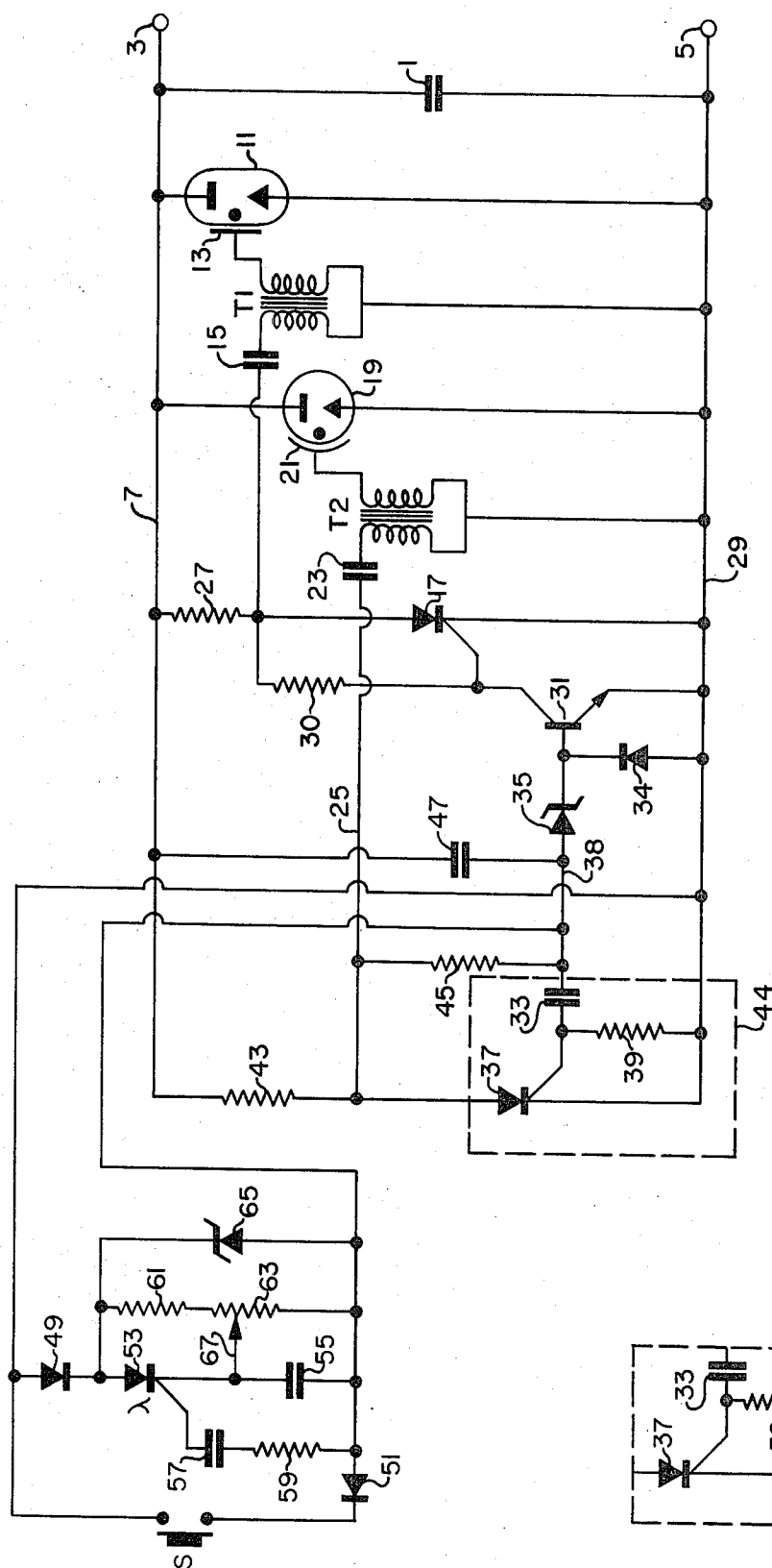


FIG. 1

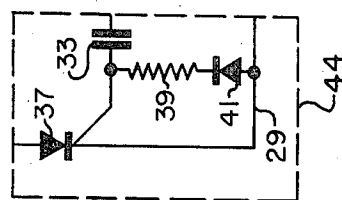


FIG. 2

COMPUTER TYPE FLASH APPARATUS WITH NOISE INHIBITING QUENCH CIRCUIT

This is a continuation-in-part of my copending application, Ser. No. 108,897 filed on Jan. 22, 1971, now abandoned.

Subject matter disclosed but not claimed herein is disclosed and claimed in copending applications by Francis T. Ogawa, Ser. Nos. 108,876, now U.S. Pat. No. 3,714,443, and 108,878, both filed on Jan. 22, 1971.

The present invention relates generally to computer-type flash devices and more specifically to computer-type flash devices with noise inhibiting quench control circuits.

In computer-type flash units, a light producing means is selectively operable to provide a flash of light to illuminate a scene to be photographed. When a predetermined amount of light has been received from the scene by a light sensing means, a quench signal is generated which is effective to terminate the production of light by the light producing means. When the quench signal is in the form of a change in the magnitude of a control signal, difficulty has heretofore been encountered in precluding spurious changes in the control signal from triggering the quenching operation of the flash device. Therefore, there exists a need for an improved quench control circuit which provides a greater measure of insensitivity to spurious changes in the control signal, caused, for example, by noise, while maintaining sufficient sensitivity to detect an expected change in the control signal.

Accordingly, it is an object of the present invention to provide an improved quench control circuit which fulfills the foregoing need.

It is another object of the present invention to provide an improved quench control circuit which is simple in design.

It is a further object of the present invention to provide an improved quench control circuit which is sensitive to anticipated control signal changes while being substantially insensitive to spurious noise signals.

In accomplishing these and other objects, there has been provided, in accordance with the present invention, an improved computer-type flash device including a novel quench control circuit. A flash tube in the flash device is selectively actuated to provide light for the illumination of a scene. An associated light sensing means generates a quench signal upon receipt of a predetermined amount of light received from the scene. A signal conditioning means responds to a signal representative of a firing of the flash tube to condition an SCR to be substantially insensitive to subsequent noise signals while maintaining sufficient sensitivity to be triggered by the quench signal. When the SCR is triggered, a quench tube is fired, thereby effectively terminating the light given off by the flash tube.

A better understanding of the present invention may be had from the following detailed description, when read in connection with the accompanying drawings in which:

FIG. 1 shows a schematic diagram embodying the present invention; and

FIG. 2 shows an alternate arrangement of a portion of the diagram of FIG. 1.

Referring to FIG. 1 in detail, there is shown a computer type flash unit including a capacitor 1 connected

between two terminals 3 and 5. The two terminals 3 and 5 are connected to the usual capacitor charging means which are not shown in the drawing. Such capacitor charging means are well known in the art and it is sufficient to say that the capacitor 1 is normally maintained in the charged state by the aforementioned capacitor charging means whereby a relatively high voltage is maintained across the capacitor 1. The high voltage terminal 3 is connected to a high voltage bus 7; the reference terminal 5 is connected to a common bus 29. A flash tube 11 is shown with its anode terminal connected to the bus 7 and its cathode terminal connected to the common bus 29. A triggering electrode 13 of the flash tube 11 is coupled through a transformer T1 to one terminal of a capacitor 15. The other terminal of the capacitor 15 is connected to the anode terminal of a silicon controlled rectifier (SCR) 17. The common terminal of the transformer T1 is connected to the common bus 29. A light terminating or quench tube 19 is shown connected between the common bus 29 and the high voltage bus 7. The quench tube triggering electrode 21 is connected through a transformer T2 to one terminal of a capacitor 23. The other terminal of the capacitor 23 is connected by a lead 25 to the anode terminal of a second SCR 37. The common terminal of the transformer T2 is connected to the common bus 29.

The anode terminal of the SCR 17 is connected through a resistor 27 to the high voltage bus 7. A resistor 30 connects the gate terminal of the SCR 17 with its anode terminal. The cathode terminal of the SCR 17 is connected to the common bus 29. The collector to emitter path of an NPN transistor 31 connects the gate terminal of the SCR 17 to the common bus 29. The base terminal of the transistor 31 is connected to a junction between the cathode terminals of a diode 34 and a zener diode 35. The anode terminal of the diode 34 is connected to the common bus 29; the anode terminal of the zener diode 35 is connected through a control signal bus 38 to one terminal of a capacitor 33. The other terminal of the capacitor 33 is connected to the gate terminal of the SCR 37. The gate terminal of the SCR 37 is also connected through a resistor 39 to the common bus 29. The capacitor 33, resistor 39 and SCR 37 comprise a quench initiation circuit 44. The cathode terminal of the SCR 37 is connected to the common bus 29; its anode terminal is connected through a resistor 43 to the high voltage bus 7. A resistor 45 connects the anode terminal of the SCR 37 to the control signal bus 38. A capacitor 47 is connected between the high voltage bus 7 and the control signal bus 38.

The common bus 29 is connected to the anode terminal of a diode 49 and also, through a selectively operable first switching means S, to the cathode terminal of another diode 51. The first switching means S may be coupled to the shutter switch actuating mechanism of an associated camera for synchronized operation therewith. The cathode terminal of the diode 49 is connected, through the anode to cathode path of a light activated silicon controlled rectifier (LASCR) 53, to one terminal of a capacitor 55. The other terminal of the capacitor 55 is connected to the anode terminal of the diode 51. The gate terminal of the LASCR 53 is connected, through a series circuit comprising a capacitor 57 and a resistor 59, to the anode terminal of the diode 51. The anode terminal of the diode 51 is also connected to the control signal bus 38. The anode terminal of the LASCR 53 is connected, through two serially

connected resistors 61 and 63, to the anode terminal of the diode 51. The anode to cathode path of a zener diode 65 connects the anode terminal of the diode 51 with the anode terminal of the LASCR 53 in shunt with the resistors 61 and 63. A slider 67 on the resistor 63 is connected to the cathode terminal of the LASCR 53.

In explaining the operation of the computer-type flash apparatus shown in FIG. 1, it is initially assumed that the capacitor 1 has been charged to a relatively high potential and maintain a relatively high potential difference between the high voltage bus 7 and the common bus 29. Capacitors 15 and 23 will have also been charged through resistors 27 and 43 respectively. The transistor 31 is normally conducting, in the steady state condition, and a current flows from the high voltage bus 7 through resistors 43 and 45, the control signal bus 38, the zener diode 35, and the base to emitter junction of the transistor 31 to the common bus 29. The aforementioned current path is part of a control signal generating means which establishes a control signal reference potential at the control signal bus 38. When an operator actuates the first switching means S, a lower resistance path is presented between the control signal bus 38 and the common bus 29, (the diode 51 and the switch S) than was present before the actuation of the switch S (the zener diode 35 and the base to emitter junction of the transistor 31). When the resistance between the control signal bus 38 and the common bus 29 decreases, the potential on the control signal bus 38 will decrease toward the reference potential on the common bus 29. That decrease in potential will render the transistor 31 non-conductive, thereby allowing a current to flow from the high voltage bus 7 through the resistors 27 and 30 into the gate terminal of the SCR 17. The SCR 17 will then become conductive and dump the charge on the capacitor 15 therethrough. The capacitor 15 then rapidly discharges through the SCR 17 and the transformer T1. The dumping of the capacitor 15 produces a ringing signal which is coupled through the transformer T1 to the triggering electrode 13 of the flash tube 11; the flash tube or light producing means 11 is actuated; i.e., the flash tube 11 is triggered and begins to conduct heavily thereby emitting light. Therefore, the transistor 31, resistors 27 and 30, SCR 17, capacitor 15, and transformer T1, may be considered as a flash actuation means, connected to the control signal bus 38, and responsive to the decrease in potential on the control signal bus 38 for actuating the light producing means or flash tube 11. The flash tube 11, in turn, provides light for the illumination of a scene to be photographed.

When the flash tube 11 begins to conduct, the potential on the high voltage bus 7 will suddenly decrease. That sudden decrease in potential is coupled through the capacitor 47 to the control signal bus 38, thereby causing a second change, again a decrease, in the potential at the control signal bus 38. Therefore, an actuation of the light producing means or flash tube 11 causes a second change in the magnitude of the control signal present on the control signal bus 38. In the present example, that second change causes the potential of the control signal bus 38 to change polarity with respect to the reference potential on the common bus 29, i.e., the potential at the control signal bus 38 becomes more negative than the potential of the common bus 29. That change in polarity of the potential difference between the control signal bus 38 and the common bus

29, when applied to the light sensing circuit including the LASCR 53, enables the LASCR 53 to sense light by forward biasing the diode 49 and the LASCR 53, and, simultaneously, isolates the switch S from the rest of the circuit by reverse biasing the diode 51. When the LASCR 53 is enabled, a current representative of the light received from a scene illuminated by the flash tube 11 will flow in its gate terminal. That current will be integrated by the capacitor 57. When the potential at the gate terminal of the LASCR 53 exceeds that present at the cathode terminal of the LASCR 53, the LASCR 53 will become conductive. The potential at the cathode terminal of the LASCR 53 is so predetermined by the setting of the slider 67 on the resistor 63 that the triggering of the LASCR 53 is indicative of the fact that the LASCR 53 has received a predetermined amount of light from the scene being photographed. That predetermined amount of light is equal to the amount of light required by the particular photographic system to properly expose a light sensitive film in the associated camera. When the LASCR 53 becomes conductive, a third effective resistance is presented between the control signal bus 38 and the common bus 29; and consequently, a third change in the magnitude of the control signal appearing at the control signal bus 38 will occur with respect to the reference potential present on the common bus 29. That third change in magnitude of the control signal is in the form of a relative increase in magnitude of the control signal toward the reference potential present on the common bus 29. That increase in magnitude is coupled through the capacitor 33 to the gate terminal of the second switching means, i.e., SCR 37, thereby rendering the SCR 37 conductive. When the second switching means or SCR 37 becomes conductive, the capacitor 23 is dumped through the circuit comprising the SCR 37 and the transformer T2. The dumping of the capacitor 23 provides a ringing signal which is coupled through the transformer T2 to the triggering electrode 21 of the quench tube 19, and the quench tube 19 is triggered into conduction. The conducting resistance of quench tube 19 is much less than that of the flash tube 11, and when the quench tube 19 becomes conductive, the capacitor 1 is very rapidly discharged and the potential on the high voltage bus 7 substantially simultaneously decreases to a magnitude insufficient to support conduction in either the quench tube 19 or the flash tube 11; both tubes will then become extinguished. With both tubes extinguished, the capacitor charging means hereinbefore referred to, again recharges the storage capacitor 1 to its steady state condition to await the initiation of another cycle of operation by an operator actuation of the first switching means S as hereinbefore explained.

The capacitor 33 and the resistor 39 of the quench initiating circuit 44, may be considered as a signal responsive means connecting the second switching means, or SCR 37, with the control signal generating means which includes the control signal bus 38. In prior art circuits, spurious increases in the control signal were sufficient to actuate the quenching circuit. Therefore, false quenching of the light given off by a flash tube was a common but undesirable occurrence. In the present example, the inclusion of the capacitor 33 and the resistor 39 in combination with the SCR 37, substantially precludes such false or premature quenching. When the flash tube 11 is fired, the potential decrease

apparent on the high voltage bus 7 is coupled to the control signal bus 38 through the capacitor 47 and effects a second change, here a decrease, in the magnitude of the control signal on the control signal bus 38. That decrease in magnitude is coupled through the capacitor 33 to the gate terminal of the SCR 37. The potential at the gate terminal of the SCR 37 then becomes negative with respect to the reference potential on the common bus 29. Therefore, the polarity of the voltage across the resistor 39 is such that a current will flow from the common bus 29 through the resistor 39 to the capacitor 33 until the potential at the capacitor 33 is equal to the reference potential on the common bus 29. While that current is flowing, a swamping signal is applied between the gate and cathode terminals of the SCR 37. That swamping signal holds the gate terminal of the SCR 37 negative with respect to its cathode terminal until the charging current flowing through the resistor 39 terminates. That swamping signal will take the form of a typical RC curve. Spurious increases in the control signal magnitude will therefore be swamped out by the swamping signal and rendered ineffective to trigger the SCR 37 into conduction. The element values of the circuitry are so chosen that an increase in magnitude of the control signal resulting from the LASCR 53 becoming conductive, is sufficient to overcome the swamping signal and trigger the SCR 37 while spurious changes appearing in the control signal of a magnitude less than the instantaneous magnitude of the swamping signal are ineffective to trigger the SCR 37.

FIG. 2 shows an alternate quench initiating circuit 44. The alternate quench initiating circuit 44 of FIG. 2 is similar to that of FIG. 1 but includes a decoupling diode 41 as an added element. The decoupling diode 41 has its anode to cathode path connected between the common bus 29 and the resistor 39. The decoupling diode is advantageously used to decouple the resistor 39 from the gate terminal of the SCR 37 when the magnitude of the control signal increases as a result of the LASCR 53 becoming conductive, thereby allowing a more positive actuation of the quench circuit.

Thus, there has been provided, a unique quench control circuit or signal conditioning means which substantially eliminates false triggering of a quench circuit by spurious noise signals while maintaining sufficient sensitivity to respond to an expected change in the control signal to actuate the quench circuit.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. The combination comprising:

control signal generating means for providing a control signal of a predetermined magnitude;

first switching means connected to said control signal generating means, said first switching means being selectively operable for effecting a first change in

magnitude of said control signal;

light producing means operable to provide light for illuminating a scene;

flash actuation means connecting said control signal generating means and said light producing means, said actuation means being responsive to said first change in magnitude of said control signal for actuating said light producing means;

coupling means coupling said light producing means with said control signal generating means, said coupling means being responsive to an actuation of said light producing means for effecting a second change in magnitude of said control signal;

light sensing means responsive to light received from said scene for effecting a third change in magnitude of said control signal upon receipt of a predetermined amount of said light received from said scene;

quench control means operable for effectively terminating said light provided by said light producing means;

second switching means actuated by said third change in magnitude of said control signal for effecting an operation of said quench control means; and

signal responsive means connecting said second switching means with said control signal generating means, said signal responsive means being responsive to said second change in magnitude of said control signal for generating a swamping signal to effectively swamp the responsiveness of said second switching means to spurious changes in said control signal, appearing between said second and third changes, of a magnitude less than the instantaneous magnitude of said swamping signal.

2. The combination as set forth in claim 1 wherein said swamping signal is of a varying time-magnitude relationship and of a predetermined duration.

3. The combination as set forth in claim 2 wherein said second switching means comprises a silicon controlled rectifier (SCR) having anode, cathode and gate terminals, and said first and second changes in magnitude of said control signal are in the form of decreases in potential, said third change in magnitude of said control signal being in the form of an increase in potential.

4. The combination as set forth in claim 3 wherein said signal responsive means comprises a capacitor connecting said control signal generating means with said SCR gate terminal and a resistor connected between said SCR gate and cathode terminals.

5. The combination as set forth in claim 4 wherein said signal responsive means further includes a diode connected in series with said resistor, the anode to cathode path of said diode being arranged between said SCR cathode and gate terminals, respectively.

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