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(71) Applicant *(for all designated States except US)*: **SILICON GENESIS CORPORATION** [US/US]; 61 Daggett Drive, San Jose, California 95134 (US).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **HENLEY, Francois, J.** [US/US]; 525 Shadowmere Way, Aptos, California 95003 (US).

(74) Agents: **TOBIN, Kent, J.** et al.; Townsend And Townsend And Crew Llp, Two Embarcadero Center, 8th Floor, San Francisco, California 94111-3834 (US).

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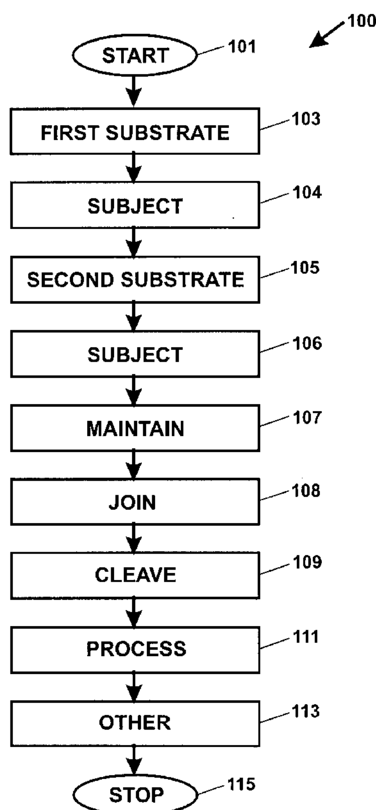

FIGURE 1

(57) Abstract: A method for manufacturing a film of material using a layer transfer process, e.g., controlled cleaving. The method includes providing a thickness of substrate material having a diameter of 200 millimeter or 300 millimeter comprising a surface region. The method includes forming a cleave region within a depth from the surface region of the substrate material to define a thickness of material to be detached. The method includes subjecting the substrate including the cleave region into a mixture of mixture of sulfuric acid and hydrogen peroxide in an unheated quartz container. In a specific embodiment, the mixture has a trace metal purity of less than 10 parts per billion. In a specific embodiment, the method includes cleaning the surface region of the substrate using at least the mixture of sulfuric acid and hydrogen peroxide, while maintaining a temperature of the mixture of at about 100 Degrees Celsius and greater and joining the surface region to a handle surface region of a handle substrate to cause the surface region to bond to the handle surface region. The method removes the thickness of material using a cleaving process.

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METHOD AND STRUCTURE FOR CLEANING SURFACES FOR BONDING LAYER TRANSFER SUBSTRATES

BACKGROUND OF THE INVENTION

[0001] The present invention relates to the manufacture of substrates. More particularly, the invention provides a technique including a method and a structure for forming multi-layered substrate structures using cleaning and bonding techniques for the fabrication of semiconductor integrated circuit devices. Such cleaning techniques use at least wet processes to reduce bonding imperfections, defects, and/or other undesirable features according to a specific embodiment. But it will be recognized that the invention has a wider range of applicability; it can also be applied to other types of substrates for three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, flat panel displays, microelectromechanical systems ("MEMS"), nano-technology structures, sensors, actuators, solar cells, biological and biomedical devices, and the like.

[0002] From the very early days, human beings have been building useful articles, tools, or devices using less useful materials for numerous years. In some cases, articles are assembled by way of smaller elements or building blocks. Alternatively, less useful articles are separated into smaller pieces to improve their utility. A common example of these articles to be separated include substrate structures, such as a glass plate, a diamond, a semiconductor substrate, a flat panel display, and others. These substrate structures are often cleaved or separated using a variety of techniques. In some cases, the substrates can be separated using a saw operation. The saw operation generally relies upon a rotating blade or tool, which cuts through the substrate material to separate the substrate material into two pieces. This technique, however, is often extremely "rough" and cannot generally be used for providing precision separations in the substrate for the manufacture of fine tools and assemblies. Additionally, the saw operation often has difficulty separating or cutting extremely hard and or brittle materials, such as diamond or glass. The saw operation also cannot be used effectively for the manufacture of microelectronic devices, including integrated circuit devices, and the like.

[0003] Accordingly, techniques have been developed to fabricate microelectronic devices, commonly called semiconductor integrated circuits. Such integrated circuits are often developed using a technique called the "planar process" developed in the early days of

semiconductor manufacturing. An example of one of the early semiconductor techniques is described in U.S. Patent No. 2,981,877, in the name of Robert Noyce, who has been recognized as one of the fathers of the integrated circuit. Such integrated circuits have evolved from a handful of electronic elements into millions and even billions of components fabricated on a small slice of silicon material. Such integrated circuits have been incorporated into and control many of today's devices, such as computers, cellular phones, toys, automobiles, and all types of medical equipment.

[0004] Conventional integrated circuits provide performance and complexity far beyond what was originally imagined. In order to achieve improvements in complexity and circuit density (i.e., the number of devices capable of being packed onto a given chip area), the size of the smallest device feature, also known as the device "geometry", has become smaller with each generation of integrated circuits. Increasing circuit density has not only improved the complexity and performance of integrated circuits but has also provided lower cost parts to the consumer.

[0005] Making devices smaller is very challenging, as each process used in integrated circuit fabrication has a limit. That is to say, a given process typically only works down to a certain feature size, and then either the process or the device layout needs to be changed. Additionally, as devices require faster and faster designs, process limitations exist with certain conventional processes and materials. An example of such a process is an ability to make the thickness of the substrate thin after the manufacture of the integrated circuit devices thereon. A conventional process often used to thin these device layers is often called "back grinding," which is often cumbersome, prone to cause device failures, and can only thin the device layer to a certain thickness. Although there have been significant improvements, such back grinding processes still have many limitations.

[0006] Accordingly, certain techniques have been developed to cleave a thin film of crystalline material from a larger donor substrate portion. These techniques are commonly known as "layer transfer" processes. Such layer transfer processes have been useful in the manufacture of specialized substrate structures, such as silicon on insulator or display substrates. As merely an example, a pioneering technique was developed by Francois J. Henley and Nathan Chung to cleave films of materials. Such technique has been described in U.S. Patent No. 6,013,563 titled Controlled Cleaving Process, assigned to Silicon Genesis Corporation of San Jose, California, and hereby incorporated by reference for all purposes.

Although such technique has been successful, there is still a desire for improved ways of manufacturing multilayered structures.

[0007] From the above, it is seen that a technique for manufacturing large substrates which is cost effective and efficient is desirable.

BRIEF SUMMARY OF THE INVENTION

[0008] According to the present invention, techniques related to the manufacture of substrates are provided. More particularly, the invention provides a technique including a method and a structure for forming multi-layered substrate structures using cleaning and bonding techniques for the fabrication of semiconductor integrated circuit devices. Such cleaning techniques use at least wet processes to reduce bonding imperfections, defects, and/or other undesirable features according to a specific embodiment. But it will be recognized that the invention has a wider range of applicability; it can also be applied to other types of substrates for three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, flat panel displays, microelectromechanical systems ("MEMS"), nano-technology structures, sensors, actuators, solar cells, biological and biomedical devices, and the like.

[0009] In a specific embodiment, the present invention provides a method for manufacturing a film of material using a layer transfer process, e.g., controlled cleaving. The method includes providing a thickness of substrate material having a diameter of 200 millimeter or 300 millimeter comprising a surface region. The method includes forming a cleave region within a depth from the surface region of the substrate material to define a thickness of material to be detached. The method includes subjecting the substrate including the cleave region into a mixture of mixture of sulfuric acid and hydrogen peroxide in an unheated quartz container. In a specific embodiment, the mixture has a trace metal purity of less than 10 parts per billion. In a specific embodiment, the method includes cleaning the surface region of the substrate using at least the mixture of sulfuric acid and hydrogen peroxide, while maintaining a temperature of the mixture of at about 100 Degrees Celsius and greater and joining the surface region to a handle surface region of a handle substrate to cause the surface region to bond to the handle surface region. The method removes the thickness of material using a cleaving process.

[0010] Numerous benefits are achieved over pre-existing techniques using the present invention. In particular, the present invention uses controlled energy and selected conditions to preferentially cleave and treat a thin film of material without a possibility of damage to such film from excessive energy release and/or thermal energy. This cleaving process selectively removes the thin film of material from the substrate while preventing a possibility of damage to the film or a remaining portion of the substrate. Additionally, the present method and structures allow for more efficient processing using a cleave layer provided in a substrate through the course of semiconductor processing, which may occur at higher temperatures, according to a specific embodiment. In a specific embodiment, the cleaved film, which is attached to a handle substrate, is subjected to a cleaning process using a wet solution having desired characteristics to firmly engage the cleaved film to the handle substrate without formation of imperfections within a vicinity of an interface region provided between the cleaved film and substrate. In a specific embodiment, the cleaved assembly can be subjected to a smoothing process as taught in U.S. Patent No. 6,287,941 issued September 11, 2001, and in the names of Kang, Sien G. and Malik, Igor J., commonly assigned (the '941 patent), or U.S. Patent Nos. 6,884,696 and 6,962,858, each of which is incorporated by reference herein. In a specific embodiment, the method can be used to prepare a clean and defect-free surface and followed by a single-wafer reactor or furnace anneal operation to effectuate the oxygen dissolution. In the case of the epi-smoothing in the '941 patent process, for example, additional cost benefits can be realized by combining the anneal as an additional treatment in-situ to the prior epi-smoothing process sequence. Depending upon the embodiment, one or more of these benefits may be achieved. These and other benefits may be described throughout the present specification and more particularly below.

[0011] The present invention achieves these benefits and others in the context of known process technology. As an example, an application of this silicon-to-silicon bonded structure can be used where one or more layers are of differing crystal orientations. For example, the base substrate can be silicon (100) orientation and the top transferred film can be silicon (110) orientation. Alternatively, the base substrate can be (110) orientation and the transferred film can be (100) orientation. Other combinations of orientation including (111) orientation with any of the above can also be included according to an embodiment of the present invention. In a specific embodiment, the multi-layer structure can also be formed onto an SOI (i.e., silicon-on-insulator) structure where the top two films are of differing orientation and mounted onto a oxide-coated base substrate. Alternatively, one or more

layers may be include global or localized strain or any combination of these, and the like. However, a further understanding of the nature and advantages of the present invention may be realized by reference to the latter portions of the specification and attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figure 1 illustrates an overall simplified method of forming silicon on silicon substrates according to embodiments of the present invention; and

[0013] Figures 2 through 8, 8A, 8B, and 9 illustrate a simplified method for manufacturing a bonded substrate structure using a layer transferred substrate according to embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0014] According to the present invention, techniques related to the manufacture of substrates are provided. More particularly, the invention provides a technique including a method and a structure for forming multi-layered substrate structures using cleaning and bonding techniques for the fabrication of semiconductor integrated circuit devices. Such cleaning techniques use at least wet processes to reduce bonding imperfections, defects, and/or other undesirable features according to a specific embodiment. But it will be recognized that the invention has a wider range of applicability; it can also be applied to other types of substrates for three-dimensional packaging of integrated semiconductor devices, photonic devices, piezoelectronic devices, flat panel displays, microelectromechanical systems ("MEMS"), nano-technology structures, sensors, actuators, solar cells, biological and biomedical devices, and the like.

[0015] Referring to Figure 1, a method 100 for cleaning and joining substrates together according to embodiments of the present invention may be outlined as follows:

1. Begin process at start, step 101;

2. Provide a first substrate (step 103), which has a first surface region, a cleave region, and a thickness of material to be removed between the first surface region and the cleave region;

3. Subject the first substrate (step 104) including the first surface region to a mixture of hydrogen peroxide and sulfuric acid;

4. Provide a second substrate (step 105), which has a second surface region;

5. Subject the second substrate (step 106) including the second surface region to a mixture of hydrogen peroxide and sulfuric acid;

6. Maintain (step 107) the second substrate and/or the first substrate in the mixture having a temperature of about 100 Degrees Celsius and greater;

7. Join (step 108) the first surface region of the first silicon substrate to the second surface region of the second silicon substrate;

8. Cleave (step 109) the thickness of material from the first silicon substrate, while the second silicon substrate remains attached to the thickness of material;

9. Process (step 111) at least a portion of one of the substrates using one or more processes to form at least one integrated circuit device onto the portion of the one of the substrates;

10. Perform other steps (step 113), as desired; and

11. Conclude process at stop, step 115;

[0016] The above sequence of steps provides a method according to an embodiment of the present invention. More particularly, the invention provides a technique including a method and a structure for forming multi-layered substrate structures using cleaning and bonding techniques for the fabrication of semiconductor integrated circuit devices. Such cleaning techniques use at least wet processes to reduce bonding imperfections, defects, and/or other undesirable features according to a specific embodiment. Other alternatives can also be provided where steps are added, one or more steps are removed, or one or more steps are provided in a different sequence without departing from the scope of the claims herein. Further details of the present method can be found throughout the present specification and more particularly below.

[0017] Figures 2 through 10 illustrate a simplified method for manufacturing integrated circuits on a layer transferred substrate according to embodiments of the present invention. These diagrams are merely illustrations that should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. As shown, the method includes providing a semiconductor substrate 200, e.g., silicon, germanium, a silicon-germanium alloy, gallium arsenide, any Group III/V materials,

and others. In a specific embodiment, the semiconductor substrate can be made of a single homogenous material, or a combination of various layers, depending upon the specific embodiment. Of course, there can be other variations, modifications, and alternatives.

[0018] In a preferred embodiment, the substrate 200 has a thickness of semiconductor material 205 and a surface region 207. In a specific embodiment, the substrate also has a cleave plane 203 (including a plurality of particles, deposited material, or any combination of these, and the like) provided within the substrate, which defines the thickness of semiconductor material. In a specific embodiment, the thickness of semiconductor material is crystalline silicon (e.g., single crystal silicon), which can include an overlying epitaxial silicon layer. In a specific embodiment, the silicon surface region 207 can have a thin layer of oxide such as silicon dioxide. The silicon dioxide has a thickness of 5 nm and less according to a specific embodiment. In other embodiments, the silicon dioxide can be fairly thick to form silicon on insulator structures and the like. Depending upon the embodiment, the silicon oxide can be silicon dioxide, silicon oxide, silicon rich oxide, or any SiOx species, combinations thereof, and the like. Of course, there can be other variations, modifications, and alternatives.

[0019] Depending upon the embodiment, the cleave region can be formed using a variety of techniques. That is, the cleave region can be formed using any suitable combination of implanted particles, deposited layers, diffused materials, patterned regions, and other techniques. In a specific embodiment, the method introduces certain energetic particles using an implant process through a top surface of the semiconductor substrate, which can be termed a donor substrate, to a selected depth, which defines the thickness of the semiconductor material region, termed the "thin film" of material. A variety of techniques can be used to implant the energetic particles into a single crystal silicon wafer according to a specific embodiment. These techniques include ion implantation using, for example, beam line ion implantation equipment manufactured from companies such as Applied Materials, Inc. and others. Alternatively, implantation occurs using a plasma immersion ion implantation ("PIII") technique, ion shower, and other non-mass specific techniques (e.g., complete mass separate, partial mass separate) can be particularly effective for larger surface regions according to a specific embodiment. Combination of such techniques may also be used. Of course, techniques used depend upon the application.

[0020] Depending upon the application, smaller mass particles are generally selected to reduce a possibility of damage to the material region according to a preferred embodiment. That is, smaller mass particles easily travel through the substrate material to the selected depth without substantially damaging the material region that the particles traverse through. For example, the smaller mass particles (or energetic particles) can be almost any charged (e.g., positive or negative) and or neutral atoms or molecules, or electrons, or the like. In a specific embodiment, the particles can be neutral and or charged particles including ions such as ions of hydrogen and its isotopes, rare gas ions such as helium and its isotopes, and neon, or others depending upon the embodiment. The particles can also be derived from compounds such as gases, e.g., hydrogen gas, water vapor, methane, and hydrogen compounds, and other light atomic mass particles. Alternatively, the particles can be any combination of the above particles, and or ions and or molecular species and or atomic species. The particles generally have sufficient kinetic energy to penetrate through the surface to the selected depth underneath the surface.

[0021] Using hydrogen as the implanted species into the silicon wafer as an example, the implantation process is performed using a specific set of conditions. Implantation dose ranges from about 1E15 to about 1E18 atoms/cm2, and preferably the dose is greater than about 1E16 atoms/cm2. Implantation energy ranges from about 1 KeV to about 1 MeV , and is generally about 50 KeV. Implantation temperature ranges from about -20 to about 600 Degrees Celsius, and is preferably less than about 400 Degrees Celsius to prevent a possibility of a substantial quantity of hydrogen ions from diffusing out of the implanted silicon wafer and annealing the implanted damage and stress. The hydrogen ions can be selectively introduced into the silicon wafer to the selected depth at an accuracy of about +/-0.03 to +/-0.05 microns. Of course, the type of ion used and process conditions depend upon the application.

[0022] Effectively, the implanted particles add stress or reduce fracture energy along a plane parallel to the top surface of the substrate at the selected depth. The energies depend, in part, upon the implantation species and conditions. These particles reduce a fracture energy level of the substrate at the selected depth. This allows for a controlled cleave along the implanted plane at the selected depth. Implantation can occur under conditions such that the energy state of the substrate at all internal locations is insufficient to initiate a non-reversible fracture (i.e., separation or cleaving) in the substrate material. It should be noted, however, that implantation does generally cause a certain amount of defects (e.g., micro-

detects) in the substrate that can typically at least partially be repaired by subsequent heat treatment, e.g., thermal annealing or rapid thermal annealing. Of course, there can be other variations, modifications, and alternatives.

[0023] Depending upon the embodiment, there may be other techniques for forming a cleave region and/or cleave layer. As merely an example, such cleave region is formed using other processes, such as those using a silicon-germanium cleave plane developed by Silicon Genesis Corporation of Santa Clara, California and processes such as the SmartCutTM process of Soitec SA of France, and the EltranTM process of Canon Inc. of Tokyo, Japan, any like processes, and others. In a specific embodiment, the cleave region can include a strained/stressed region or be substantially free of strain/stress according to a specific embodiment. The cleave region can also include a deposited region with or without an implanted region according to a specific embodiment. Of course, there may be other variations, modifications, and alternatives.

[0024] Referring now to Figure 3, the method includes joining 300 the surface region of the semiconductor substrate to a first handle substrate 301. In a specific embodiment, the handle substrate is made of a suitable material that is also substantially crystalline, e.g., single crystal silicon. That is, the handle substrate can be made of a silicon wafer, an epitaxial silicon wafer, denuded zone wafers (e.g., hydrogen annealed, argon annealed, a MDZ^{TM} Product by MEMC Electronic Materials, Inc.) or other crystalline materials (including layer transferred silicon on insulator substrates) according to a specific embodiment. Depending upon the embodiment, the handle substrate can be doped (e.g., P-type, N-type) and/or undoped, including nitrogen doped substrates and the like. Of course, there can be other handle substrate material. In a preferred embodiment, the silicon wafer has a silicon surface region 301. In a specific embodiment, the silicon surface region can have a thin layer of oxide such as silicon dioxide. The silicon dioxide has a thickness of 5 nm and less according to a specific embodiment. Depending upon the embodiment, the silicon oxide can be silicon dioxide, silicon oxide, silicon rich oxide, or any SiOx species, combinations thereof, and the like. Of course, there can be other variations, modifications, and alternatives.

[0025] In a preferred embodiment, the first handle substrate has a surface region 305, which will be joined and/or bonded with surface region 207 provided on substrate 200. Like reference numerals are used in this figure has others, but are not intended to be limiting the

scope of the claims herein. Further details of the joining process can be found throughout the present specification and more particularly below.

[0026] Before joining, the semiconductor substrate and the first handle substrate surfaces are each subjected to a cleaning solution to treat the surfaces of the substrates to clean the substrate surface regions according to a specific embodiment. An example of a solution used to clean the substrate and handle surfaces is a mixture of hydrogen peroxide and sulfuric acid, and other like solutions. In a specific embodiment, the mixture is formed using four bottles 96% Sulfuric Acid (H_2SO_4), which is CMOS grade from J.T. Baker and is often comes in 15 lb bottles. The sulfuric acid has a trace metal purity specified <10 ppb for each metal according to a specific embodiment. The four bottles of sulfuric acid is mixed with 1 bottle of 30% hydrogen peroxide (H_2O_2). The bottle of hydrogen peroxide is Fynite 1 grade from J.T. Baker, and often comes in 8 pint bottles in a specific embodiment. In preferred embodiments, the trace metal purity is <1 ppb for each metal. Of course, there can be other variations, modifications, and alternatives.

[0027] In a preferred embodiment, the mixture is performed using an unheated quartz bath but becomes heated using the exothermic reaction of the chemical mixture to cause an increase in temperature of the mixture to a desired temperature range. In a specific embodiment, the mixture life in the both is about 4 hours after mixing the solutions together. In a preferred embodiment, the bath mixture temperature is greater than about 100°C. In a specific embodiment, the temperature is measured using an optical pyrometer. After mixing the bath temperature can reach approximately 120°C - 140°C according to a specific embodiment. In a specific embodiment, multiple substrates can be immersed into the bath as long as the temperature is about 100 Degrees Celsius and greater until the temperature is reduced to below 100 Degrees Celsius, where the substrates are taken out. Optionally, the method includes chemical spiking of hydrogen peroxide using, for example, a 1/2 bottle per spike, to slightly extend bath life according to a specific embodiment. Of course, there can be variations, alternatives, and modifications. Depending upon the embodiment, reaction byproducts of the chemical mixture can include water and Caro's acid (H_2SO_5), and other species. In a preferred embodiment, the present cleaning process removes undesirable organic contaminants and/or particles caused by a preceding operation such as implanting, and the like. Such contaminants and/or particles lead to voids, imperfections, defects, etc. during the bonding process in a specific embodiment.

[0028] In a specific embodiment, a dryer dries the semiconductor substrate and handle surfaces to remove any residual liquids and/or particles from the substrate surfaces. Self-bonding occurs by placing surfaces of cleaned substrates (e.g., semiconductor substrate surface and handle substrate surface) together after an optional plasma activation process depending on the specific layer-transfer process used. If desired, such plasma activated processes clean and/or activate the surfaces of the substrates. The plasma activated processes are provided, for example, using an oxygen or nitrogen bearing plasma at 20°C to 40°C temperature. The plasma activated processes are preferably carried out in dual frequency plasma activation system manufactured by Silicon Genesis Corporation of San Jose, California. Of course, there can be other variations, modifications, and alternatives, which have been described herein, as well as outside of the present specification.

[0029] Thereafter, each of these substrates is bonded together according to a specific embodiment. As shown, the handle substrate has been bonded to the donor substrate surface region. The substrates are preferably bonded using an EVG 850 bonding tool manufactured by Electronic Vision Group or other like processes for smaller substrate sizes such as 200mm or 300mm diameter wafers. Other types of tools such as those manufactured by Karl Suss may also be used. Of course, there can be other variations, modifications, and alternatives. Preferably, bonding between the handle substrate and the donor is substantially permanent and has good reliability.

[0030] Accordingly after bonding, the bonded substrate structures are subjected to a bake treatment according to a specific embodiment. The bake treatment maintains the bonded substrate at a predetermined temperature and predetermined time. Preferably, the temperature ranges from about 200 or 250 Degrees Celsius to about 400 Degrees Celsius and is preferably about 350 Degrees Celsius for about 1 hour or so for a silicon donor substrate and the first handle substrate to attach themselves to each other permanently according to the preferred embodiment. In a specific embodiment, the bake treatment can occur using a furnace, a rapid thermal process, or a hot plate or any combination of these. Depending upon the specific application, there can be other variations, modifications, and alternatives.

[0031] In a specific embodiment, the substrates are joined or fused together using a low temperature thermal step. The low temperature thermal process generally ensures that the implanted particles do not place excessive stress on the material region, which can produce an uncontrolled cleave action. In a specific embodiment, the low temperature bonding

process occurs by a self-bonding process. Of course, there can be other variations, modifications, and alternatives.

[0032] Alternatively, an adhesive disposed on either or both surfaces of the substrates, which bond one substrate to another substrate. In a specific embodiment, the adhesive includes an epoxy, polyimide-type materials, and the like. Spin-on-glass layers can be used to bond one substrate surface onto the face of another. These spin-on-glass ("SOG") materials include, among others, siloxanes or silicates, which are often mixed with alcohol-based solvents or the like. SOG can be a desirable material because of the low temperatures (e.g., 150 to 250.degree. C.) often needed to cure the SOG after it is applied to surfaces of the wafers.

[0033] Alternatively, a variety of other low temperature techniques can be used to join the donor substrate surface regions to the handle substrate. For instance, an electro-static bonding technique can be used to join the two substrates together. In particular, one or both substrate surface(s) is charged to attract to the other substrate surface. Additionally, the donor substrate surface can be fused to the handle wafer using a variety of other commonly known techniques. Of course, the technique used depends upon the application.

[0034] Referring to Figure 4, the method includes initiating a controlled cleaving action using energy 401 provided at a selected portion of the cleave plane to detach the thickness of semiconductor material from the substrate, while the thickness of semiconductor material remains joined to the first handle substrate. Depending upon the specific embodiment, there can be certain variations. For example, the cleaving process can be a controlled cleaving process using a propagating cleave front to selectively free the thickness of material from the donor substrate attached to the handle substrate. Alternative techniques for cleaving can also be used. Such techniques, include, but are not limited to those called a NanocleaveTM process of Silicon Genesis Corporation of Santa Clara, California, a SmartCutTM process of Soitec SA of France, and an EltranTM process of Canon Inc. of Tokyo, Japan, any like processes, and others. The method then removes the remaining portion of the semiconductor donor substrate, which provided the thickness of material to the handle substrate according to a specific embodiment.

[0035] Referring to Figure 5, the method provides a resulting handle substrate 500 including an overlying thickness of material 205 according to a preferred embodiment. In a specific embodiment, the thickness of material is provided on the handle substrate using a

silicon on silicon bond, which provides electrical coupling between the two structures. As shown, the thickness of material includes a cleaved surface region 501. The bonded substrate structure is bonded together, but not suitable for integrated circuit processing. That is, the bonded substrate structure should be subjected to a permanent bond using at least a rapid thermal technique and/or furnace anneal, which will be described in more detail throughout the present specification and more particularly below. Of course, there can be other variations, modifications, and alternatives.

[0036] Referring now to Figure 6, the present method includes subjecting an interface region 601 to a thermal process to cause an increase in temperature from at least a first temperature within a first temperature range of about 100 Degrees Celsius to about 200 Degrees Celsius to at least a second temperature within a second temperature range of about 800 Degrees Celsius and greater. In a preferred embodiment, the thermal process causes the increase in temperature from the first temperature to at least the second temperature within a time period of about 2 seconds and less to form a second characteristic at the interface region. In a specific embodiment, the time period can be less than one second. Depending upon the embodiment, the thermal process can be a suitable rapid thermal process, rapid thermal anneal, rapid thermal process using laser irradiation, or the like. In a specific embodiment, the thermal process comprises irradiating the thickness of material and silicon handle substrate using a monochromatic light source. Further details of the irradiation technique can be found throughout the present specification and more particularly below.

[0037] In a specific embodiment, the irradiation can occur in a suitable processing tool. The processing tool can include a chamber of a cluster tool or suitable stand alone tool or the like. Depending upon the embodiment, the cluster tool can also include other chambers for implantation, controlled cleaving, bonding, and other process technologies. In a specific embodiment, the irradiation can occur using an increase in temperature with a suitable increase from an initial temperature to a final temperature. Such increase in temperature can be at a rate of about 1000 Degrees Celsius per minute and greater or include step increases or other variations according to a specific embodiment. Of course, there can be other variations, modifications, and alternatives.

[0038] In a preferred embodiment, the present method maintains the interface region substantially free from one or more voids of a dimension of about 10 microns and greater. In a specific embodiment, the method preferably maintains the interface region free from any

and all voids, which can cause reliability and/or processing limitations. These voids may be caused by a plurality of hydrogen species that have been introduced into the cleave region in a preceding process according to a specific embodiment. Depending upon the embodiment, the thermal processing secures bonding between the thickness of material while preventing accumulation of hydrogen species by diffusion, which can be characterized by a hydrogen diffusion characteristic in the thickness of material. Other impurities that may accumulate at the interface through diffusion include water, hydroxide species, carbon containing species, and others according to a specific embodiment.

[0039] In a preferred embodiment, the interface region is subjected to a high temperature thermal treatment process that substantially frees the interface region from oxide species. Depending upon the embodiment, the process can include or more rapid thermal and/or furnace annealing techniques. That is, the bond between the thickness of silicon material and silicon substrate is free from silicon dioxide or other oxides according to a specific embodiment. The interface preferably electrically couples the thickness of material to the silicon substrate according to a specific embodiment. Depending upon the embodiment, the interface can also have a very thin oxide layer, which is about 10 nm and less. Such thin oxide layer causes certain resistance between the thickness of silicon material and silicon substrate according to a specific embodiment. The resistivity is less than about 10 times a resistivity of the surrounding bulk substrates (e.g., crystalline silicon) according to a specific embodiment. Of course, there can be other variations, modifications, and alternatives.

[0040] In a more preferred embodiment, the thermal treatment is provided using an inert gas or reducing gas maintained on the silicon on silicon substrate member. In a specific embodiment, the gas is substantially free from any oxide species. The thermal treatment includes subjecting the interface region to a thermal process to cause a change to the interface region from the first characteristic to a second characteristic, which is free from the silicon oxide material and where an epitaxial silicon material is formed by epitaxial regrowth provided between the thickness of single crystal silicon material and the handle silicon substrate. In a preferred embodiment, the method also maintains the interface region free of multiple voids during the thermal process to form the epitaxial silicon material to electrically couple the thickness of single crystal silicon material to the handle silicon substrate. In a specific embodiment, the epitaxial growth is predominantly or substantially single crystal in characterisitic. Of course, there can be other variations, modifications, and alternatives.

[0041] In a specific embodiment, the thermal process comprises subjects the joined thickness of single crystal silicon material and the handle substrate to an argon, hydrogen, or argon-hydrogen bearing environment at a temperature greater than about 1000 Degrees Celsius, although it can be slightly below depending upon the embodiment. Other types of combinations including argon, hydrogen, nitrogen, or the like can also be used according to a specific embodiment of the present invention. The thermal processes causes oxygen species in the interface region to diffuse out from the interface region, through one or more portions of the substrate member according to a specific embodiment. In a preferred embodiment, the oxygen diffuses out of the bonded substrate members. The interface region changes in characteristic from an oxide material to a crystalline silicon material, which is more effective at electrically coupling the thickness of silicon material to the handle substrate. Of course, there can be other variations, modifications, and alternatives.

[0042] Referring to Figure 7, an illustration of a silicon substrate 301 and an overlying thickness of silicon material 205 is shown. This diagram is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, modifications, and alternatives. Between the thickness of silicon material and silicon substrate is a thin oxide layer 701, which has been previously described. In a specific embodiment, the thin oxide layer has a concentration illustrated by plot 750. As shown, the vertical axis shows oxygen species concentration, which is provided against horizontal axis for spatial position. The spatial position is provided along the thickness from the surface region of the thickness of material to the backside of the silicon substrate, as shown. As shown, a high concentration of oxide material is illustrated at the interface region between the thickness of silicon material and silicon substrate. As the oxygen-rich interfacial layer is dissolved by the thermal treatment, an epitaxial regrowth of the silicon occurs that allows the interface to become of high crystalline quality and of high electrical conductivity.

[0043] Previous work by Goesele et al., "Growth, Shrinkage, and Stability of Interfacial Oxide Layers Between Directly Bonded Silicon Wafers", *Journal of Applied Physics,* A 50(1990), pp. 85-94; "Stability of Interfacial Oxide Layers During Silicon Wafer Bonding", *Journal of Applied Physics,* 65(2), 15 January 1989, pp. 561-563; and Ling et al. "Relationship Between Interfacial Native Oxide Thickness and Bonding Temperature in Directly bonded Silicon Wafer Pairs", *Journal of Applied Physics*; 71 (3), 1 Feb. 1992, pp. 1237-1241, generally show that thermal annealing of bonded silicon wafers show dissolution behavior into float-zone silicon while CZ silicon would show a net interfacial oxide growth.

In order to avoid developing defects and oxide dissolution spheroidization (uneven oxide thinning), rotated same-orientation films or the use of different crystal orientations are necessary. The work develops the concept of oxygen dissolution but its use in cleaved thin-film interface removal was not addressed.

[0044] In a specific embodiment, the method subjects the thickness of silicon material and silicon substrate, including the interface region, to a thermal treatment, as illustrated by Figure 8. This diagram is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, modifications, and alternatives. As shown, the high temperature anneal, which representatively includes an argon and/or hydrogen environment, drives out the oxide material from the substrate, as illustrated by plot 850 according to a specific embodiment. As shown, the interface region 801 is now crystalline silicon material, which couples the thickness of material to the silicon substrate according to a specific embodiment. Of course, there can be other variations, modifications, and alternatives.

[0045] As an example, certain process details associated with this example has been calculated and are illustrated by way of Figure 8A. In this example, an argon thermal treatment is used where the oxygen situated at the bond interface is moved through the surface by diffusion. The rate of diffusion is calculated by Fick's law of diffusion using the crystalline silicon oxygen diffusivity and solid solubility at 1200 C. For easy reading, Fick's law has also been reproduced below.

$$\textit{Flux (in atoms/cm}^2\textit{ second)} = Do\,(T)\,(dC/dz)$$

where *C* is the oxygen concentration;

Do(T) is an oxygen diffusivity coefficient in silicon.

Note that for purposes of the slope calculation, the oxygen concentration operating for purposes of diffusion would be the solid solubility limit *Cs(T)* at the interface boundary and zero at the crystal surface. The derivative would therefore simplify to ***Cs(T)/film thickness)***. As illustrated, the calculated flux of 7.24 E+12 Oxygen atoms per square centimeters per seconds would allow a 200 nanometers silicon film to release a 5 nanometer SiOx layer (x=0.5) of 5.5 E+15 Oxygen atoms per square centimeters within about 13 minutes. Of course, there can be other variations, modifications, and alternatives.

[0046] Referring now to Figure 8B to further illustrate the epitaxially formed interface region, substrate 301, which has single crystal characteristics, is the handle substrate. In a specific embodiment, the handle substrate is a denuded silicon substrate that is substantially free from impurities such as oxygen precipitates, voids, cops, and other imperfections. In a specific embodiment, the oxygen concentration in the denuded substrate is about 0.5 to about 3E18 atoms/cm3 and less. Overlying the handle substrate is a thickness of single crystal material 205, which has been layer transferred onto the handle substrate. Between the thickness of single crystal material, which may be silicon, and handle substrate is a first oxide bearing interface region 853 according to a specific embodiment. In a specific embodiment, the first oxide bearing interface is derived by oxide material on either or both handle or thickness of material to facilitate bonding. In a specific embodiment, the first interface region has a first thickness that may be about 5 nanometers and less in a specific embodiment. Of course, there can be other variations, modifications, and alternatives.

[0047] Upon application of the present thermal treatment process, which converts the oxide material into single crystal silicon, according to a specific embodiment. The conversion occurs from each of the two interface regions (see arrows) toward a center region according to a specific embodiment. As these two regions converge, a resulting interface 851 forms, which is crystalline silicon that may have different crystal orientations. In a specific embodiment, the resulting interface has about one to five monolayers of silicon material, which electrically couple the thickness of material to the handle substrate. Depending upon the specific embodiment, the upper interface region 855 may move faster than the lower interface region 857 since the upper interface region has a thinner solid region 255 that facilitates diffusion of oxygen species from interface region 853, through the thickness of material to an outer region (outside the solid) according to a specific embodiment. Of course, there can be other variations, modifications, and alternatives.

[0048] In a specific embodiment, the resulting handle substrate has suitable characteristics for undergoing one or more processing steps. That is, the handle substrate can be subjected to conventional semiconductor processing techniques, including but not limited to, photolithography, etching, implanting, thermal annealing, chemical mechanical polishing, diffusion, deposition, and other others, which may be known by one of ordinary skill in the art. The handle substrate can also be selectively removed while transferring the thin film of material onto another substrate structure according to a specific embodiment.

[0049] Referring to Figure 9, the present method performs other processes on portions of the thickness of material regions, which have been attached to the handle substrate, according to a specific embodiment of the present invention. The method forms 900 one or more devices on one or more portions of the thin film of material overlying the handle substrate surface. Such devices can include integrated semiconductor devices, photonic and/or optoelectronic devices (e.g., light valves), piezoelectronic devices, microelectromechanical systems ("MEMS"), nano-technology structures, sensors, actuators, solar cells, flat panel display devices (e.g., LCD, AMLCD), biological and biomedical devices, and the like. Such devices can be made using deposition, etching, implantation, photo masking processes, any combination of these, and the like. Of course, there can be other variations, modifications, and alternatives. Additionally, other steps can also be formed, as desired.

[0050] In a preferred embodiment, the processing includes high temperature semiconductor processing techniques to form conventional integrated circuits thereon. The method forms a planarized surface region overlying the thickness of semiconductor material. In a specific embodiment, the planarized surface region can be formed using one or more suitable techniques. Such techniques include deposition of a dielectric layer, which is later reflowed using thermal treatment. The planarized surface region can also be formed using a chemical mechanical polishing process including a suitable slurry, pad, and process according to a specific embodiment. The planarized surface region can also be formed using any combination of these techniques and others according to a specific embodiment. The planarized surface region preferably has a uniformity of about 0.1% to about 5% end to end, and is within about 15 Angstroms RMS in roughness as measured on a 2 micron by 2 micron atomic-force microscope scan. Of course, there can be other variations, modifications, and alternatives.

[0051] Optionally, in a specific embodiment, the method also joins the planarized surface region of the resulting processed handle substrate to a face of a second handle substrate. Before joining, the processed thickness of material and the second handle substrate surfaces are each subjected to a cleaning solution to treat the surfaces of the substrates to clean the substrate surface regions according to a specific embodiment. An example of a solution used to clean the substrate and handle surfaces is a mixture of hydrogen peroxide and sulfuric acid, and other like solutions.

[0052] In a specific embodiment, the mixture is formed using four bottles 96% Sulfuric Acid (H_2SO_4), which is CMOS grade from J.T. Baker and is often comes in 15 lb bottles. The sulfuric acid has a trace metal purity specified <10 ppb for each metal according to a specific embodiment. The four bottles of sulfuric acid is mixed with 1 bottle of 30% hydrogen peroxide (H_2O_2). The bottle of hydrogen peroxide is Fynite 1 grade from J.T. Baker, and often comes in 8 pint bottles in a specific embodiment. In preferred embodiments, the trace metal purity is <1 ppb for each metal. Of course, there can be other variations, modifications, and alternatives.

[0053] In a preferred embodiment, the mixture is performed using an unheated quartz bath but becomes heated using the exothermic reaction of the chemical mixture to cause an increase in temperature of the mixture to a desired temperature range. In a specific embodiment, the mixture life in the both is about 4 hours after mixing the solutions together. In a preferred embodiment, the bath mixture temperature is greater than about 100°C as measured. In a specific embodiment, the temperature is measured using an optical pyrometer. After mixing the bath temperature can reach approximately 120°C - 140°C according to a specific embodiment. In a specific embodiment, multiple substrates can be immersed into the bath until the temperature reduces to below 100 Degrees Celsius. Optionally, the method includes chemical spiking of hydrogen peroxide using, for example, a 1/2 bottle per spike, to slightly extend bath life according to a specific embodiment. Of course, there can be variations, alternatives, and modifications. Depending upon the embodiment, reaction byproducts of the chemical mixture can include water and Caro's acid (H_2SO_5), and other species.

[0054] A dryer dries the semiconductor substrate and handle surfaces to remove any residual liquids and/or particles from the substrate surfaces. Self-bonding occurs by placing surfaces of cleaned substrates (e.g., planarized region and handle substrate surface) together after an optional plasma activation process depending on the specific layer-transfer process used. If desired, such plasma activated processes clean and/or activate the surfaces of the processed substrates. The plasma activated processes are provided, for example, using an oxygen or nitrogen bearing plasma at 20°C to 40°C temperature. The plasma activated processes are preferably carried out in dual frequency plasma activation system manufactured by Silicon Genesis Corporation of San Jose, California. Of course, there can be other variations, modifications, and alternatives, which have been described herein, as well as outside of the present specification.

[0055] Thereafter, each of these substrates (and processed devices) is bonded together according to a specific embodiment. As shown, the handle substrate has been bonded to the planarized surface region. The substrates are preferably bonded using an EVG 850 bonding tool manufactured by Electronic Vision Group or other like processes for smaller substrate sizes such as 200mm or 300mm diameter wafers. Other types of tools such as those manufactured by Karl Suss may also be used. Of course, there can be other variations, modifications, and alternatives. Preferably, bonding between the handle substrate and the planarized surface is substantially permanent and has good reliability.

[0056] Accordingly after bonding, the bonded substrate structures are subjected to a bake treatment according to a specific embodiment. The bake treatment maintains the bonded substrate at a predetermined temperature and predetermined time. Preferably, the temperature ranges from about 200 or 250 Degrees Celsius to about 400 Degrees Celsius and is preferably about 350 Degrees Celsius for about 1 hour or so for a planarized substrate region and the second handle substrate to attach themselves to each other permanently according to the preferred embodiment. Depending upon the specific application, there can be other variations, modifications, and alternatives.

[0057] In a specific embodiment, the substrates are joined or fused together using a low temperature thermal step. The low temperature thermal process generally ensures that the implanted particles do not place excessive stress on the material region, which can produce an uncontrolled cleave action. In a specific embodiment, the low temperature bonding process occurs by a self-bonding process.

[0058] Alternatively, an adhesive disposed on either or both surfaces of the substrates, which bond one substrate to another substrate. In a specific embodiment, the adhesive includes an epoxy, polyimide-type materials, and the like. Spin-on-glass layers can be used to bond one substrate surface onto the face of another. These spin-on-glass ("SOG") materials include, among others, siloxanes or silicates, which are often mixed with alcohol-based solvents or the like. SOG can be a desirable material because of the low temperatures (e.g., 150 to 250.degree. C.) often needed to cure the SOG after it is applied to surfaces of the wafers.

[0059] Alternatively, a variety of other low temperature techniques can be used to join the substrate surface region to the handle substrate. For instance, an electro-static bonding technique can be used to join the two substrates together. In particular, one or both substrate

surface(s) is charged to attract to the other substrate surface. Additionally, the donor substrate surface can be fused to the handle wafer using a variety of other commonly known techniques. Of course, the technique used depends upon the application.

[0060] While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims. Further details of experiments performed using the present invention can be found throughout the present specification and more particularly, in U.S. Application No. ________________(18419-019600US), commonly assigned, and hereby incorporated by reference herein.

[0061] Additionally processes may include repeating the layer transfer processes to form resulting multi-layered substrate structure according to a specific embodiment. The structure includes bulk substrate. The bulk substrate includes an overlying layer, which may be a layer transferred layer. The overlying layer includes layer transferred layer, which has processed and completed device structures thereon. Overlying layer includes one or more layers, which also may be layer transferred, deposited, or any combination of these, according to a specific embodiment. Additionally, the thermal process can include a single and/or multiple thermal processes, which are the same or different according to a specific embodiment. Of course, there can be other variations, modifications, and alternatives.

[0062] While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

WHAT IS CLAIMED IS:

1 1. A method for manufacturing a film of material using a layer transfer
2 process, the method comprising.
3 providing a thickness of substrate material having a diameter of 200
4 millimeter or 300 millimeter comprising a surface region;
5 forming a cleave region within a depth from the surface region of the substrate
6 material to define a thickness of material to be detached;
7 subjecting the substrate including the cleave region into a mixture of mixture
8 of sulfuric acid and hydrogen peroxide in an unheated quartz container;
9 cleaning the surface region of the substrate using at least the mixture of
10 sulfuric acid and hydrogen peroxide, while maintaining a temperature of the mixture of at
11 about 100 Degrees Celsius and greater;
12 joining the surface region to a handle surface region of a handle substrate to
13 cause the surface region to bond to the handle surface region; and
14 remove the thickness of material using a cleaving process.

1 2. The method of claim 1 wherein the substrate is a first silicon wafer and
2 the handle substrate is a second silicon substrate.

1 3. The method of claim 1 wherein the substrate is a silicon germanium
2 material, a silicon carbide material, a gallium nitride material , or a group III/V material..

1 4. The method of claim 1 wherein the handle substrate is quartz or silicon
2 or glass.

1 5. The method of claim 1 wherein the mixture is made from a 96%
2 sulfuric acid solution and a 30% hydrogen peroxide solution.

1 6. The method of claim 1 wherein the mixture in the quartz container has
2 a lifetime of about four hours and less.

1 7. The method of claim 1 further comprising monitoring the temperature
2 using a optical pyrometer.

1 8. The method of claim 1 wherein the temperature ranges from about 120
2 Degrees Celsius to about 140 Degrees Celsius.

1 9. The method of claim 1 further comprising introducing a hydrogen
2 peroxide solution having a concentration of about 25% to about 35% to the mixture.

1 10. The method of claim 1 further comprising introducing a hydrogen
2 peroxide solution having a concentration of about 30% to extend a lifetime of the mixture.

1 11. The method of claim 1 wherein the bonding forms a silicon on silicon
2 bond interface.

1 12. The method of claim 1 wherein the bonding forms a silicon on
2 insulator bond interface.

1 13. The method of claim 1 wherein the mixture removes any organic
2 contaminants from the surface region , the removal allows for a substantially defect free
3 interface between the surface region and the handle surface.

1 14. The method of claim 1 wherein the cleave region is characterized by a
2 separation strength that is less than a bonding strength between the handle substrate and the
3 substrate.

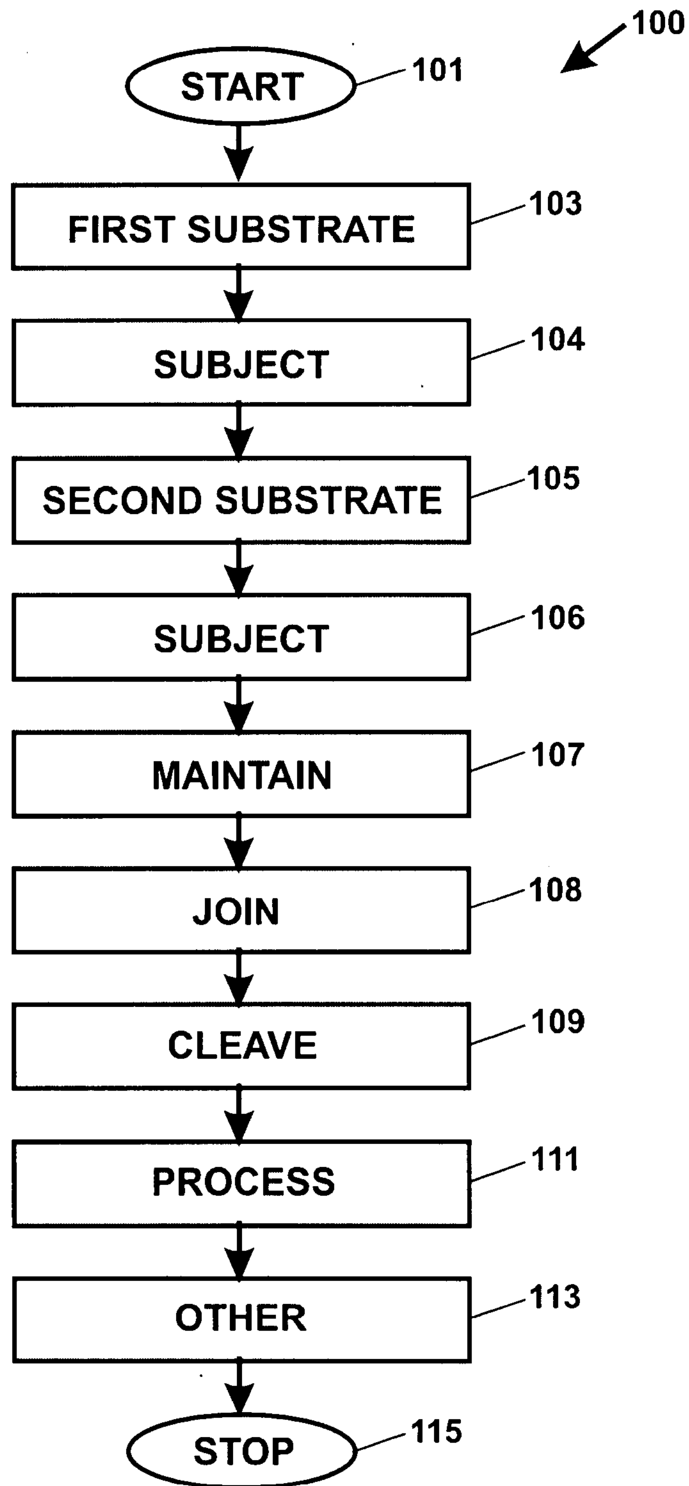

FIGURE 1

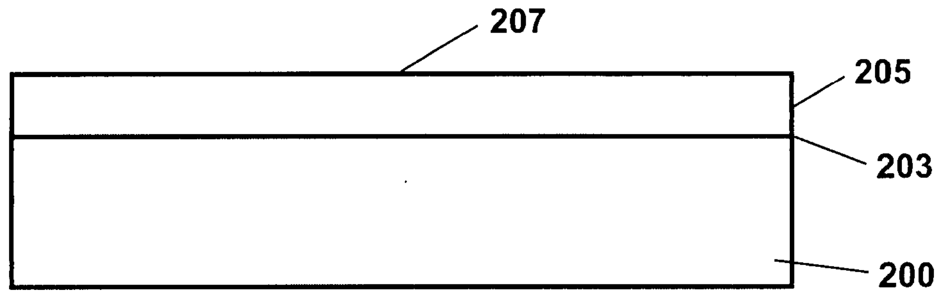

FIGURE 2

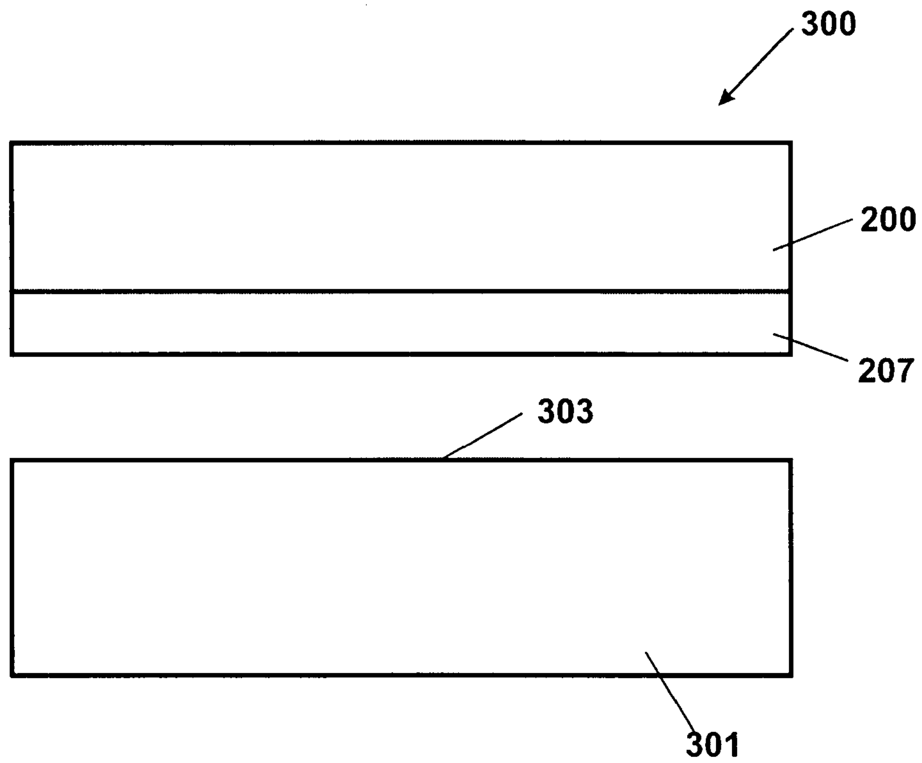

FIGURE 3

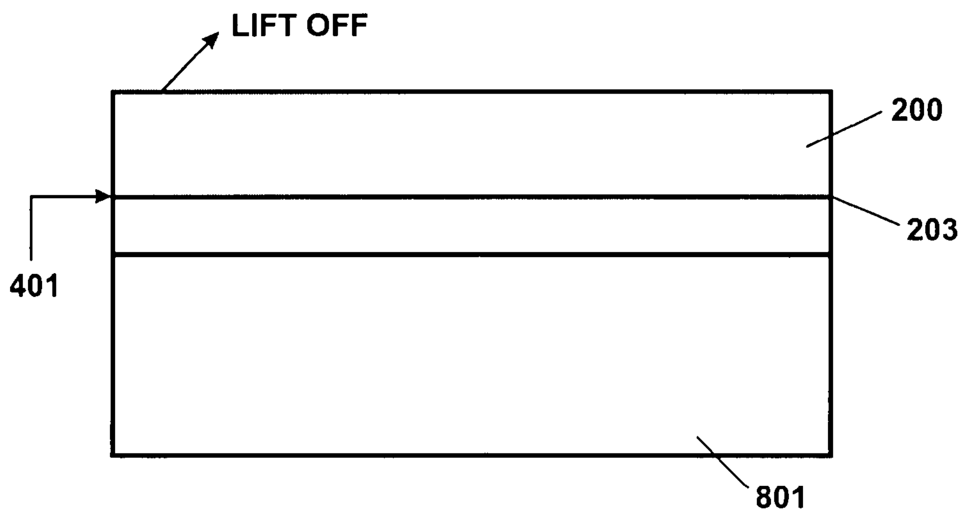

FIGURE 4

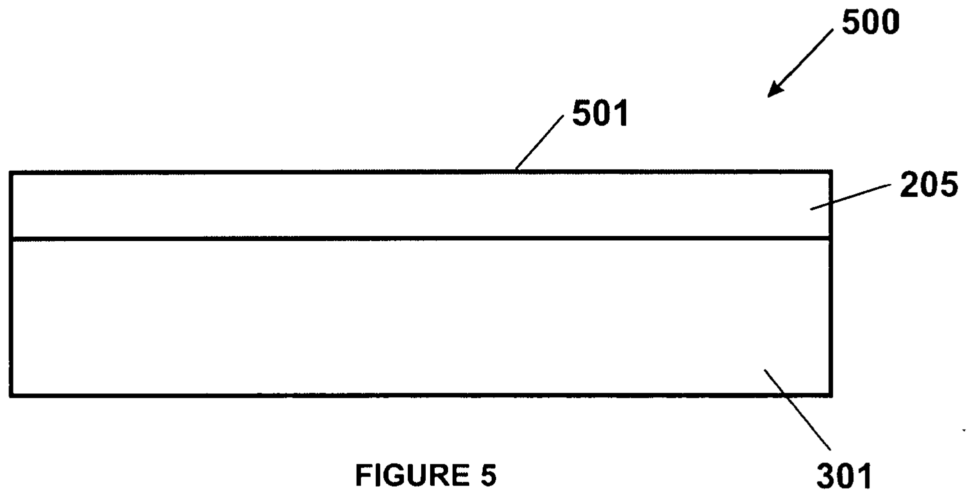

FIGURE 5

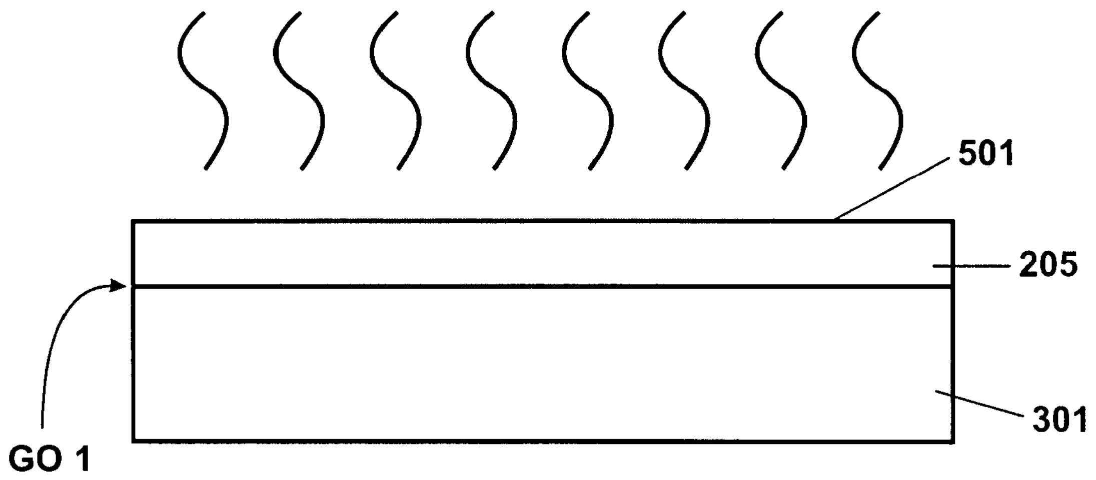

FIGURE 6

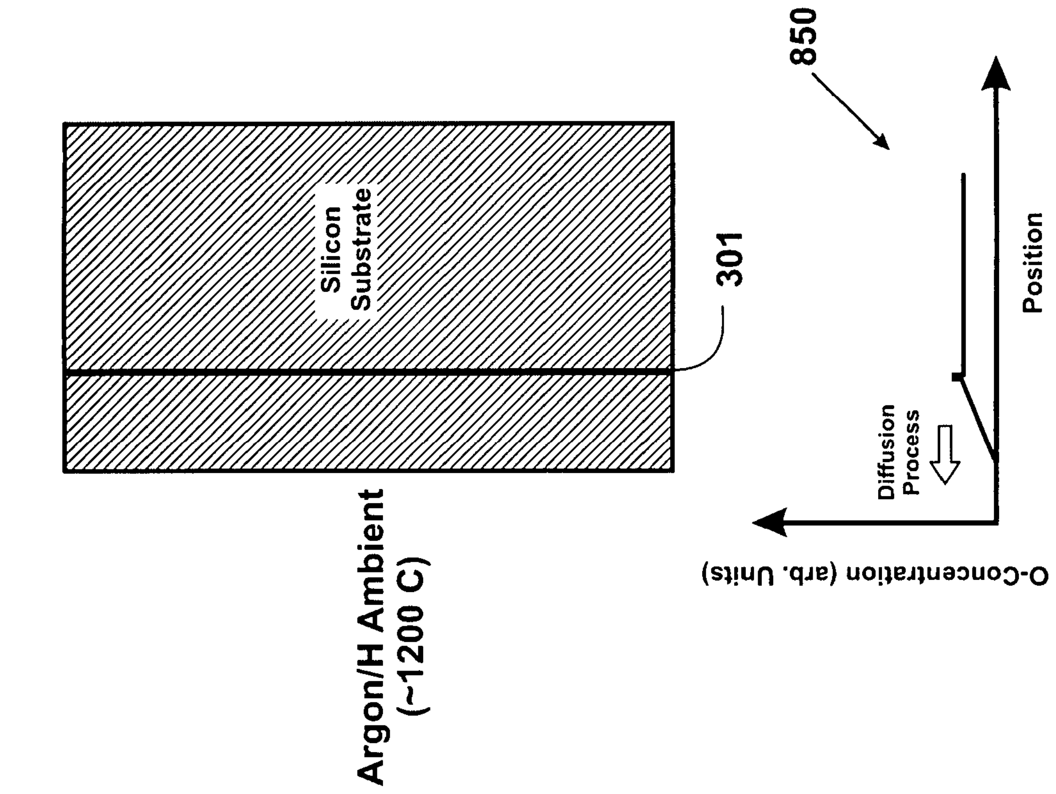

FIGURE 8

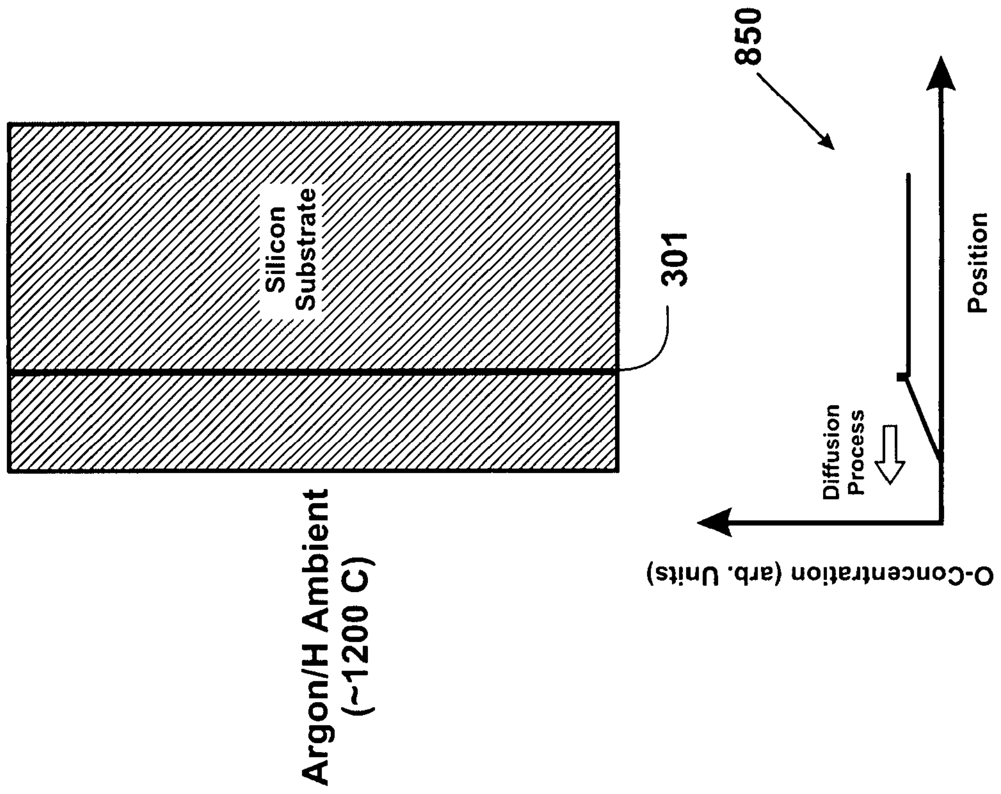

FIGURE 7

- Parameters
  - Silicon Layer thickness - 2000 Å
  - Argon Ambient, 1200 C treatment
  - 50 Å interface layer, $SiO_{0.5}$ stochiometry
- Diffusion Law (oxygen in silicon)
  - Flux (atoms/cm2-sec) = $D_o(T)$ *[$dC_S(T)$/d Z]
  - where
  - $C_S(T)$ = solid solubility limit,
  - $D_o(T)$ = Oxygen diffusion constant in silicon
- At 1200 C, $C_S(T)$ = 4.6E+17 cm^{-3}, $D_O(T)$ = 3.15E-10 cm^2/sec
  - Using surface concentration ~ 0,
  - Flux = 7.24E+12 O-atoms/cm^2-sec
- Total O-Dose = [4.4 E+22 cm^{-3}/4] * 50 E-8 cm = 5.5 E+15 atoms/cm^2
- Expected time to dissolution
  - Total o-Dose/Flux = 5.5 E+15 atoms/cm^2 / 7.24 E+12 o-atoms/cm^2-sec
- <u>TIME TO DISSOLUTION = 760 seconds</u>

FIGURE 8A

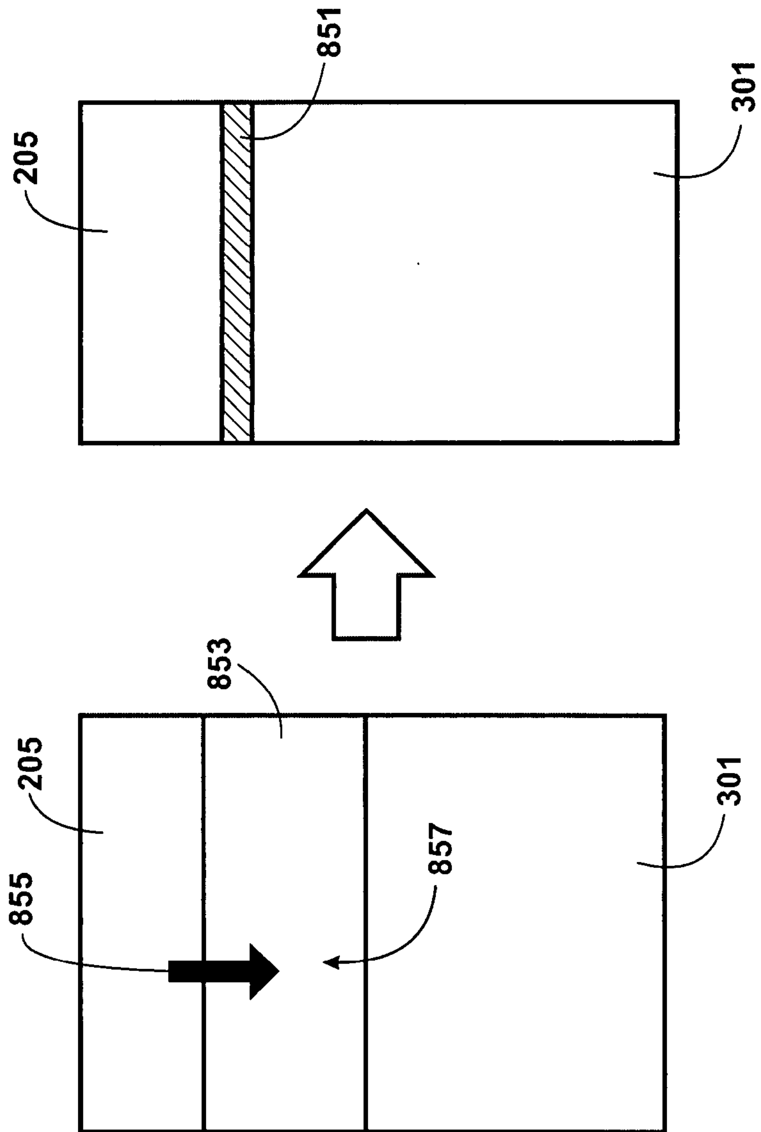

FIGURE 8B

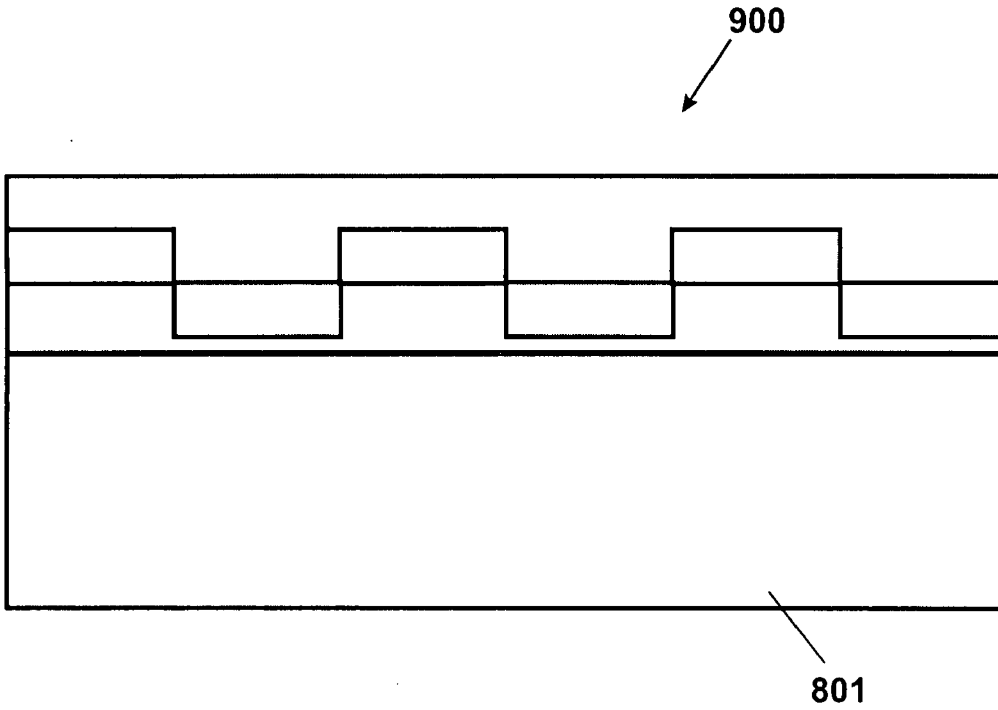

FIGURE 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/60800

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/302, 21/461 (2007.10)
USPC - 438/691, 745
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 438/691, 745

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 438/458, 459

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Google Scholar and PubWest (PGPB,USPT,USOC,EPAB,JPAB): layer, transfer, hydrogen peroxide, sulfuric acid, caro's acid, quartz, handle, optical pyrometer, piranha, silicon, genesis

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006/0211219 A1 (Henley et al.) 21 Sep 2006 (21.09.2006); entire document especially para [0011], [0014], [0041], [0042], [0061], [0067], [0076] and [0206].	1-14
Y	US 6,294,145 B1 (Hall et al.) 25 Sep 2001 (25.09.2001); entire document especially col 1, ln 13-28 and col 2, ln 1-6.	1-14
Y	US 5,300,170 A (Donohoe) 5 Apr 1994 (05.04.1994); entire document especially col 4, ln 19-20.	7
A	US 2006/0205180 A1 (Henley et al.) 14 Sep 2006 (14.09.2006); entire document.	1-14

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
6 Oct 2007 (06.10.2007)

Date of mailing of the international search report
14 NOV 2007

Name and mailing address of the ISA/US
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-3201

Authorized officer:
Lee W. Young
PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774