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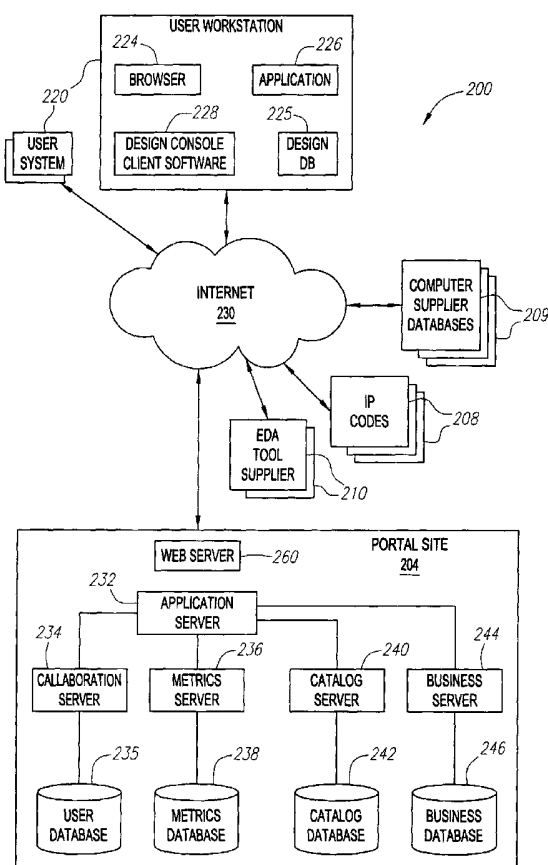
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(54) Title: METHOD AND SYSTEM FOR CHIP DESIGN USING REMOTELY LOCATED RESOURCES



(57) Abstract: A multi-faceted design platform (104) acts as a tool for front-end hardware IC designers who design complex core base System on Chip. The design platform (104) uses a network such as the Internet (230) to search and gain access to previously designed virtual core blocks. The design platform (104) provides a means to select (306) and transfer (308) all relevant information regarding the selected virtual core blocks and allows the designer to immediately incorporate the virtual core block into the new SoC design. The design platform (104) further generates the appropriate source code files (320) for immediate use with a plurality of known verification tools to verify both the integration and connectivity of the virtual core blocks as well as the basic functionalities of the SoC design.



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/18213**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(7) : G06F 17/50

US CL : 716/1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 716/1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
IEEE, EAST**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	WO 01/65422 A2 (ROBERTSON et al.) 07 September 2001 (07.09.2001), pages 1-50.	1-44
A	US 6,102,961 A (LEE et al.) 15 August 2000 (15.08.2000), see entire document	1-44
A	WILSEY, Philip A., Web-Based Analysis and Distributed IP, Proceedings of the 1999 Winter Simulation Conference, December 1999, pages 1445-1453.	1-44

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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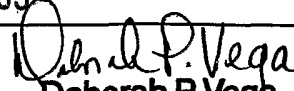
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