

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
31 December 2003 (31.12.2003)

PCT

(10) International Publication Number
WO 2004/001800 A2

(51) International Patent Classification⁷: **H01L**
(21) International Application Number:
PCT/US2003/019272
(22) International Filing Date: 19 June 2003 (19.06.2003)
(25) Filing Language: English
(26) Publication Language: English
(30) Priority Data:
60/390,011 19 June 2002 (19.06.2002) US
(71) Applicant: **FOSTER-MILLER, INC.** [US/US]; 350 Second Avenue, Waltham, MA 02451 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

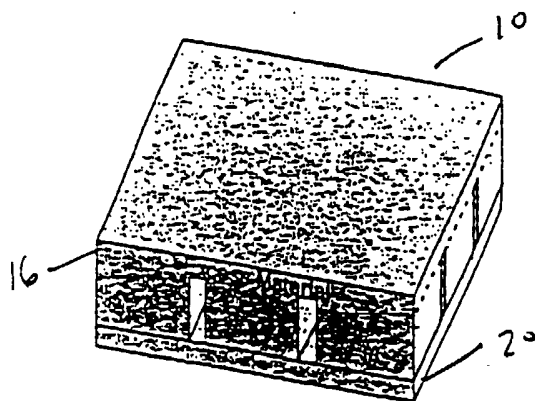
(72) Inventors: **FARRELL, Brian**; 47 Channing Street, Quincy, MA 02170 (US). **JAYNES, Paul**; 19 Summer Street, Attleboro, MA 02703 (US). **TAYLOR, Malcolm**; 30A Elm Street, Pepperell, MA 01463 (US).
(74) Agents: **SHANSKE, Jason, D.** et al.; Iandiorio & Teska, 260 Bear Hill Road, Waltham, MA 02451-1018 (US).

Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CHIP PACKAGE SEALING METHOD



(57) Abstract: A method of manufacturing a package including manufacturing a substrate to include at least one layer of LCP material, manufacturing a cover made of LCP material to include a lower lip, and sealing the cover to the substrate by heating the interface between the lower lip and the substrate.

WO 2004/001800 A2

CHIP PACKAGE SEALING METHOD

FIELD OF THE INVENTION

This invention relates to an electronic and optoelectronic component package, a unique lid assembly, and several useful package sealing techniques.

RELATED APPLICATIONS

This application claims priority from provisional application serial no. 60/390,011 filed June 19, 2002. This invention was made with U.S. Government support under Contract No. DAAH01-00-C-R070 awarded by the U.S. Army. The Government may have certain rights in the subject invention.

BACKGROUND OF THE INVENTION

Semi-conductor packaging is an active field. U.S. Patent No. 5,827,999, incorporated herein by this reference, delineates the limitations associated with numerous prior art packaging techniques including encasement, the cavity package, and various thermoplastic chip carrier packages. The basic purpose of any semi-conductor package is protection of the component(s) (e.g., electronic chips, electrooptical devices, and the like) housed by the package while at the same time providing electrical and/or optical interconnections from the component(s) through the package. Manufacturability and protection are key concerns. The applicant owns U.S. Patent No. 6,320,257 disclosing a semiconductor packaging technique comprising an interconnect substrate including at least one layer of LCP material, at least one semiconductor

component bonded to the substrate, a lid, and a hermetic seal sealing the lid to the substrate. This patent is hereby incorporated herein by this reference. The '999 patent discloses the idea of molding a casing onto the circuit substrate around a chip. The casing can be made of, among other things, liquid crystal polymer material. As recognized by the inventors hereof, LCP materials have a very low moisture permeability and can provide a hermetic seal especially if the package lid covering the chip and also the substrate which supports the chip are both made of LCP or even if the lid assembly is composed of a metal, ceramic, or glass. Other relevant art includes Patent Nos. 6,403,211; 6,538,211; 6,057,597; 6,428,650; 6,136,128; 5,761,053; 6,501,654; and 5,471,011; and Patent Publication Nos. US 2003/0002265; US 2002/0187570; US 2001/0019475; US 2003/0026556; US 2003/0044130; US 2002/0197026; US 2003/0057535; and US 2003/0045024.

This art, however, is not primarily concerned with manufacturability. In most, if not all cases, a single component is mounted to a circuit substrate and then the lid or cover is secured over the component to the substrate. Assembly of the components as single entities consumes unnecessary time, effort, and cost in the component assembly process. Also, the art listed above is not primarily concerned with feasibility studies to ascertain the most economical methods of sealing the cover over the component to the substrate.

BRIEF SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a highly efficient package lid and substrate assembly process.

It is a further object of this invention to provide such a process which results in precision alignment of the package lids to the interconnect substrate.

It is a further object of this invention to provide such a process which is versatile and can accommodate many different types of components, substrate designs, cover designs, and sealing processes.

It is a further object of this invention to provide a novel semi-conductor package lid sub-assembly.

It is a further object of this invention to provide new ways of efficiently and effectively sealing the cover over the component(s) to the substrate.

This invention results from the realization that a highly effective package lid and assembly process is effected by injection molding a number of individual covers as an integrated lid sub-assembly, mating a populated interconnect substrate with the integrated lid sub-assembly, and then singulating the individual packages. Sealing the individual covers over a component to the substrate can be accomplished before singulation or even after singulation using a variety of different efficient methods.

This invention features a method of manufacturing a package, the method comprising manufacturing a substrate to include at least one layer of LCP material, manufacturing a cover made of LCP material to include a lower lip, and sealing the cover to the substrate by heating the interface between the lower lip and the substrate. In one embodiment, a susceptor material is disposed between the lower lip of the cover and the substrate and sealing includes employing a laser to heat the interface as laser energy is absorbed by the susceptor material. In one example, susceptor material is Clearweld™ and the

laser is an infrared laser. Also, pigmentation can be added to at least the lower lip of the cover and sealing includes directing laser energy through the substrate to be absorbed by the lower lip. Or, pigmentation can be added to the substrate and sealing includes directing laser energy through the lower lip to be absorbed by the substrate.

In another embodiment, the lip includes at least one energy director extending therefrom and sealing includes directing ultrasonic energy to be focused by the energy director to melt the interface. Also, a cavity is formed in the substrate which receives the energy director. Directing ultrasonic energy may include using a plunge welding ultrasonic welding system including a frame shaped horn which engages the lower lip.

One method of manufacturing a package includes manufacturing a substrate, manufacturing a cover to include a lower lip, disposing a susceptor material between the lower lip of the cover and substrate, and employing a laser to heat the interface between the lower lip and the substrate as laser energy is absorbed by the susceptor material.

Another method of manufacturing a package includes manufacturing a substrate to include at least a top layer of pigmented material, manufacturing a cover to include a lower lip, mating the cover to the substrate, and directing laser energy through the lower lip to be absorbed by the pigmentation in the substrate to seal the cover to the substrate.

Another method of manufacturing a package includes manufacturing a substrate, manufacturing a cover including pigmented material, mating the cover to the substrate, and directing laser energy through the substrate to be absorbed

by the pigmented cover material to seal the cover to the substrate.

Still another method of manufacturing a package includes manufacturing a substrate, manufacturing a cover to include a lower lip with at least one energy director extending therefrom, mating the cover to the substrate, and directing ultrasonic energy to be focused by the energy director to melt the interface between the cover and the substrate.

Still another method of manufacturing a package includes manufacturing a substrate to include a top layer including a cavity formed therein, manufacturing a cover to include a lower lip with at least one said energy director extending therefrom, mating the cover to the substrate so that the energy director is received in the cavity, and directing ultrasonic energy to be focused by the energy director to melt the interface between the cover and the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages will occur to those skilled in the art from the following description of a preferred embodiment and the accompanying drawings, in which:

Figs. 1A-1D are schematic three-dimensional views showing various conventional package designs useful in connection with optoelectric components;

Fig. 2 is a schematic three-dimensional bottom view showing, in one example, a lid sub-assembly in accordance with the subject invention;

Fig. 3 is a schematic three-dimensional view showing a printed circuit board substrate before it is populated with components;

Fig. 4 is a schematic three-dimensional partial cross-sectional view of the lid sub-assembly shown in Fig. 1;

Fig. 5 is a schematic three-dimensional view showing the printed circuit board substrate of Fig. 2 now populated with components;

Fig. 6 is another schematic three-dimensional view showing one example of a lid sub-assembly in accordance with the subject invention;

Fig. 7 is a schematic three-dimensional view of the lid sub-assembly of Fig. 6 with a susceptor compound now in place on the bottoms of the individual covers;

Fig. 8 is a schematic three-dimensional view showing the lid sub-assembly of Fig. 7 being mated to the populated circuit board substrate using the alignment pins of the subject invention;

Fig. 9 is a schematic three-dimensional view showing how, in one embodiment, the alignment pins of the lid sub-assembly are melted to the substrate to secure the lid subassembly in place on the substrate;

Fig. 10 is a schematic three-dimensional view showing the lid sub-assembly now mated to the substrate in accordance with the subject invention just before singulation;

Fig. 11 is a schematic three-dimensional view showing the individual covers after singulation in accordance with one embodiment of the subject invention;

Fig. 12 is a schematic three-dimensional view showing singulation of the covers and the substrate at the same time in accordance with the another embodiment of the subject invention;

Fig. 13 is a schematic three-dimensional view showing another type of lid sub-assembly interconnection layer in accordance with the subject invention;

Fig. 14 is a schematic three-dimensional view showing another type of cover in accordance with the subject invention including an optical window;

Fig. 15 is a schematic cross-sectional view of the optical window type cover of Fig. 14;

Fig. 16 is a schematic view showing an array of covers each including a lower lip portion in accordance with the subject invention;

Fig. 17 is a schematic view showing a single cover of the array of covers shown in Fig. 16 just before it is sealed over a component and onto the substrate;

Fig. 18 is a schematic partial cross-sectional view showing how the lower lip assembly of a single cover is sealed with respect to the substrate in accordance with one embodiment of the subject invention;

Fig. 19 is a schematic partial cross-sectional view showing another method of sealing a cover to a substrate;

Fig. 20 is a schematic partial cross-sectional view showing still another method of sealing a cover to a substrate;

Fig. 21 is a schematic partial cross-sectional view showing still another method of sealing a cover to a substrate in accordance with the subject invention;

Fig. 22 is a schematic view showing a frame-shaped ultrasonic horn useful in connection with the subject invention for ultrasonically sealing a cover to a substrate;

Fig. 23 is a bottom view of a single cover including a metallization layer in accordance with one embodiment of the subject invention;

Figs. 24-29 are schematic views showing the steps involved in packaging electronic components in accordance with this invention and also showing another embodiment of the lid assembly in accordance with this invention; and

Fig. 30 is a schematic view showing still another lid assembly embodiment in accordance with the invention.

DISCLOSURE OF THE PREFERRED EMBODIMENT

Aside from the preferred embodiment or embodiments disclosed below, this invention is capable of other embodiments and of being practiced or being carried out in various ways. Thus, it is to be understood that the invention is not limited in its application to the details of construction and the arrangements of components set forth in the following description or illustrated in the drawings.

Figs. 1A-1D show typical packages 5A-5D for optoelectronic components. One goal of the subject invention is to provide packages for optoelectronic and other components which are more efficiently manufactured and assembled thus reducing costs.

Fig. 2 shows, in one example of the subject invention, lid assembly 10 which includes an array of individual covers 12 each cover including, typically, four side walls 14 and a covering cap or top 15 (see Fig. 4). Interconnecting layer 16, Figs. 1 and 4, in this embodiment, a continuous plate which integrates

covers 12 for placement in unison over multiple components on a substrate.

Lid assembly 10 is typically molded from filled LCP material (e.g., 30% glass filler) and may even include multi-axially oriented material as discussed in the applicant's U.S. Patent No. 6,320,257 herein incorporated by this reference.

The use of LCP in place of other thermoplastic polymers is preferred because LCP exhibits superior barrier properties, high use temperature, and dimensional stability for precision molding tolerances. Other thermoplastics, other materials, and other forming processes, however, may also be used.

In one preferred embodiment, alignment pins 18, also made of LCP material, extend outward from the molded interconnecting layer 16 in the spaces between the covers. Then, chip circuit board substrate 20, Fig. 3 includes corresponding alignment holes 22. Substrate 20 typically includes at least one layer, preferably the top layer, of multi-axially oriented LCP material as set forth in patent No. 6,320,257 (see Figs. 2b and 3 thereof). Thus, substrate 20, typically a printed circuit board, can accommodate a wide variety of different types of components (chips, optical devices, MEMs devices, and the like) and also accommodates a number of different chip mounting technologies (wire bonding, ball grid arrays, surface mount technology, and the like). Areas 24 on substrate 20 are dedicated to the components 26 as shown in Fig. 5.

In one example, a bonding agent, an adhesive, and/or a susceptor (e.g., Clearweld™) material 30, Fig. 2 may be dispensed (e.g., screened) onto the distal end of each sidewall, or onto the mating surface on the substrate, before lid assembly 10 is mated to the populated substrate 20, Fig. 8 as the alignment pins 18 are received in the alignment holes as shown at 32. Next, ultrasonic

horn 40, Fig. 9 can be used to melt the distal ends of the alignment pins to secure lid assembly 10 to substrate 20. Melting/welding of the alignment pins is not a necessary step as the subsequent lid sealing process can form a sufficient mechanical bond of the lid to the substrate. Each cover may also be hermetically sealed to substrate 20 at this stage in the assembly process using one or more of the techniques discussed below. Each cover is typically associated with one component but a cover may also be disposed over multiple components.

Singulation can be carried out in a number of different ways. In Fig. 10, integration layer 16 is removed by back lapping, for example, to separate each cover 12, Fig. 11. Then, substrate 20 is singulated in one process step using conventional techniques. Or, in other embodiments, substrate 20 may be left intact.

Alternatively, singulation of both the covers and substrate 20, Fig. 12 can be accomplished by cutting through both integration layer 16 and substrate 20 as shown in Fig. 12 along lines 50 using (a routing tool, laser, water jet, or other cutting apparatus). If the lid assembly and the substrate are manufactured in a certain way, the modules may be snapped apart rather than cut apart. For vibration or shock sensitive components this may not be feasible, but in some cases a snap-singulation may be practical. The substrate would have to be embossed, etched, or scribed to snap along a line and the mating lid assembly would also have to include a snap line.

Fig. 13 shows a different kind of interconnecting layer 16a spanning the tops 15 of each cover 12. The interconnection part of the lids depicted in Fig.

13 may be the runners used to injection mold the lid assembly. Again, this whole package lid sub-assembly can be molded in the form shown in Fig. 13. Covers 12 are singulated by removing layer 16a and/or cutting through it in the areas between the individual covers.

Figs. 14-15 show a different type of cover 12a including optical window 60 useful when the component housed in cover 12a is an optical device. Walls 14a of cover 12a include ledge 62 which supports optical window 60. Window 60 may be laser welded in place on ledges 62. The optical window 60 may be made of a number of optical materials formed into a number of shapes (e.g., flat optical window, collimating lens, micro-lens arrays, and the like).

Figs. 16 shows alternative covers 12b extending outward from integration layer 16 each including lower lip 70 useful, as described below, for securing the covers to a substrate using a variety of different sealing processes in accordance with the subject invention and interconnected by a bulk of injection molded material. This formation of the lid assembly can be locked in place or sealed and then backlapped to singulate the lids.

The subject invention also includes a wide variety of methods for hermetically sealing lip 70, Fig. 17 of cover 12 over component 24 on substrate 20 either after cover 12 is singulated as shown in Fig. 17 or even before cover 12 is singulated (i.e. when cover 12 is still interconnected to a number of similarly constructed covers). Typically, cover 12 is injection molded out of a filled LCP material and substrate 20 is made of or includes bi-axially oriented LCP material.

LCP material is somewhat transparent to near-infrared radiation. Thus,

in one example, susceptor material 100, Fig. 18 (e.g., Clearweld™, or an alternative IR absorbing material) is placed between lower lip 70 of the cover and substrate 20 and infrared laser energy 102 is used to heat the interface between cover lip 70 and substrate 20 as the laser energy is absorbed by susceptor material 100. The result is localized heating which melts and seals the LCP material at the interface between lip 70 and substrate 20. The susceptor material may be printed, jetted, screened, or painted onto the lower lip of the cover and/or onto the substrate or even plated thereto. The thickness of lip 70 should be no greater than 32 mils to achieve proper heating and a hermetic seal.

In another example, the LCP material of at least the top layer of substrate 20', Fig. 19 is pigmented with, for example, carbon resin 110 prior to injection molding or extrusion of the material. When laser energy 102 hits the pigmented substrate after passing through lip 70, heat is generated at the contact point between lip 70 and substrate 20' and a hermetic seal is created. The thickness, width, and geometry of lower lip 70 all play a part in the sealing effectiveness and can be optimized for various different designs.

Another option is to pigment at least lip portion 70', Fig. 20 of the cover and direct laser energy 102 to lip portion 70' through substrate 20. Now, the thickness of substrate 20 should be in the 2 to 20 mil range. Pigmentation of the substrate (Fig. 19) or cover (Fig. 20) can be augmented with susceptor layer 100, Fig. 18. Standard diode laser welding systems can be used as the source of laser energy.

In still another example, lower lip 70', Fig. 21 of the cover includes energy directing prongs 120 which are received in cavities 122 formed in

substrate 20'. An ultrasonic horn 140 is used to create heat at the interface between lower lip 70' and substrate 20'. Energy directors 120 are integrated into the lid design to focus the ultrasonic energy in order to induce melting at the interface and provide a hermetic seal.

In Fig. 22 a plunge welding type ultrasonic welding system is used with frame shaped horn 142 which engages all four sides of lower lip 70 of the cover simultaneously to hermetically seal cover 12 to substrate 20 in a single operation.

Finally, soldering as a sealing method can be used if LCP lip 70" or the entire cover, Fig. 23 is metallized on the bottom thereof at sealing interface 150 and if the substrate, not shown, also includes metallization which mates with the lip of the cover.

The result is a hermetically sealed package and an efficient, scalable assembly process reducing time, effort, and cost. Depending on the size of the component(s), panel level assembly as described herein can increase the manufacturing efficiency by an estimated 50% or more. Typically, the package lid assembly is manufactured by injection molding. The printed circuit board may be manufactured with a footprint for package sealing and precision alignment holes for aligned mating. The board is populated with the various components which may be electrical, optoelectronic, and the like and then the panel of package lids is mated with the component substrate. The panel lid assembly is locked to the substrate to maintain alignment and then each cover is sealed before or after singulation of the packages. The alignment and locking method described above is one of many possible mechanisms. Alternatives

include, but are not limited to, alignment fiducials formed out of etched metal, screened on chemistries, drilled, and deposited metal. These alignment fiducials will be located on both the substrate and the mating lid. As for the alignment pins, in addition to a straight pin that is ultrasonically melted to secure the assembly, a snap-fit alignment pin may also be implemented. The preferred substrate is composed of at least one layer of biaxially or multiaxially oriented LCP film and bond areas for silicon dice, integrated circuits, MEMs, MOEMs, or a variety of electronic or optoelectronic components that require packaging. One advantage of the subject invention is passive alignment via the alignment holes and the alignment pins. The dimensional stability of the package lids and the dimensional stability the circuit board are tight enough to eliminate the need for special alignment methods for panel level assembly. Passive alignment is especially important in the optoelectronic component arena, but may be useful for multimode applications where the tolerances are on the order of microns, rather than nanometers (singlemode fibers). When a component includes a glass window, a lens array, or other optical devices that require aligned mating, passive alignment within a few microns is achieved and the subject invention saves significant manufacturing time and money.

Figs. 24-29 illustrate one possible packaging technique in accordance with the subject invention. LCP substrate 200 Fig. 24 is biaxial or multiaxial or includes layers of uniaxial LCP cross-plyed. Alignment holes 202 are formed in at least the top layer of substrate 200. Areas 204 receive the various components. Molded LCP assembly 208, Fig. 25 includes integrated covers 210 and alignment pins 212. This embodiment, each cover includes sidewalls 209

terminating in lip 213. The lips of all covers are co-joined by interconnecting layer 215. After substrate 200 is populated with components 211 as shown in Fig. 26, lid assembly 208, Fig. 27 is mated with substrate 200 as alignment pins 212 are received in alignment holes 202. Laser 218, Fig. 28 is the used to seal all individual covers 210 to substrate 200. Singulate is the accomplished as shown in Fig 24 using router 220. The result is individual packages as discussed above.

Fig. 30 shows another embodiment of an array of LCP covers 250 interconnected by runners 252 which, during singulation, can be broken or cut.

Although specific features of the invention are shown in some drawings and not in others, this is for convenience only as each feature may be combined with any or all of the other features in accordance with the invention. The words “including”, “comprising”, “having”, and “with” as used herein are to be interpreted broadly and comprehensively and are not limited to any physical interconnection. Moreover, any embodiments disclosed in the subject application are not to be taken as the only possible embodiments.

Other embodiments will occur to those skilled in the art and are within the following claims:

What is claimed is:

CLAIMS

1. A method of manufacturing a package, the method comprising:
manufacturing a substrate to include at least one layer of LCP material;
manufacturing a cover made of LCP material to include a lower lip; and
sealing the cover to the substrate by heating the interface between the lower lip and the substrate.
2. The method of claim 1 further including disposing susceptor material between the lower lip of the cover and the substrate and wherein sealing includes employing a laser to heat the interface as laser energy is absorbed by the susceptor material.
3. The method of claim 2 in which the susceptor material is Clearweld™.
4. The method of claim 1 in which the laser is an infrared laser.
5. The method of claim 1 further including adding pigmentation to at least the lower lip of the cover and sealing includes directing laser energy through the substrate to be absorbed by the lower lip.
6. The method of claim 1 further including adding pigmentation to

the substrate and sealing includes directing laser energy through the lower lip to be absorbed by the substrate.

7. The method of claim 1 in which the lip includes at least one energy director extending therefrom and sealing includes directing ultrasonic energy to be focused by the energy director to melt the interface.

8. The method of claim 7 further including forming a cavity in the substrate which receives the energy director.

9. The method of claim 7 in which directing ultrasonic energy includes using a plunge welding ultrasonic welding system.

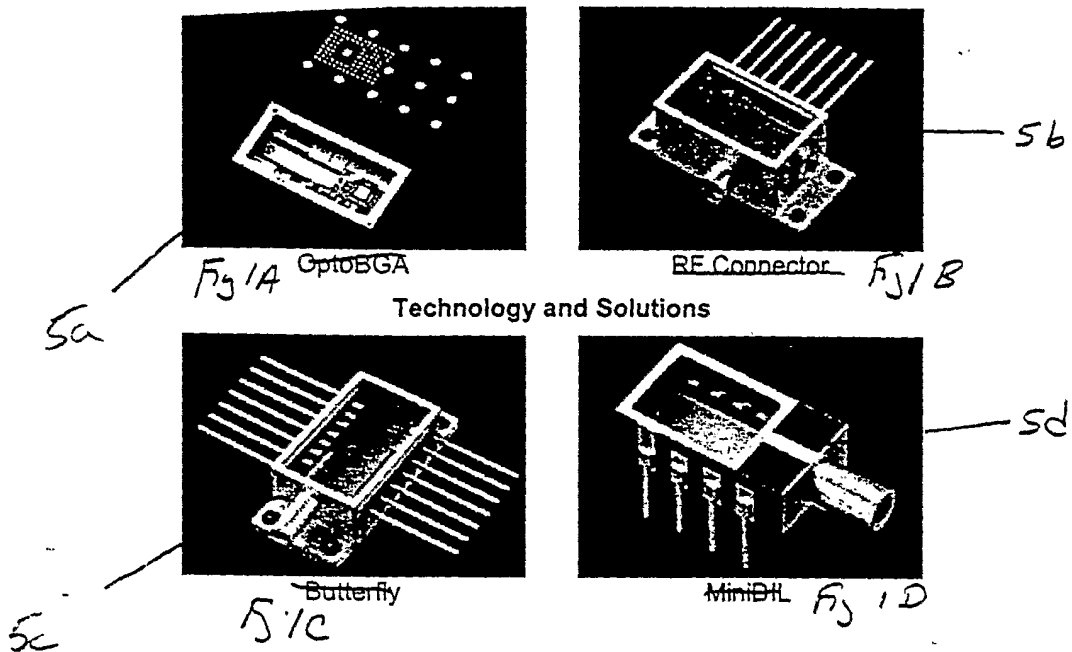
10. The method of claim 9 in which the plunge welding ultrasonic welding system includes a frame shaped horn which engages the lower lip.

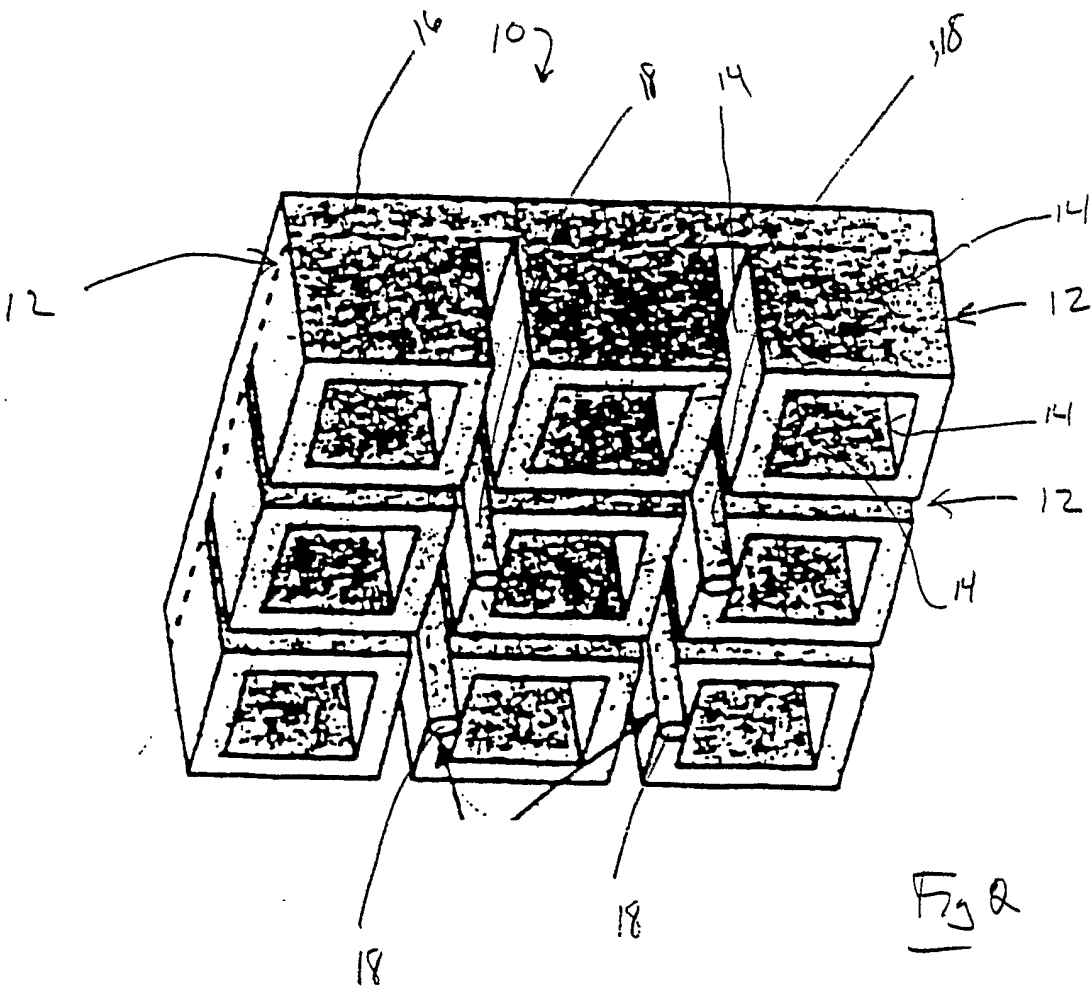
11. A method of manufacturing a package, the method comprising:
manufacturing a substrate;
manufacturing a cover to include a lower lip;
disposing a susceptor material between the lower lip of the cover and substrate; and
employing a laser to heat the interface between the lower lip and the substrate as laser energy is absorbed by the susceptor material.

12. A method of manufacturing a package, the method comprising:
manufacturing a substrate to include at least a top layer of
pigmented material;
manufacturing a cover to include a lower lip;
mating the cover to the substrate; and
directing laser energy through the lower lip to be absorbed by the
pigmentation in the substrate to seal the cover to the substrate.
13. A method of manufacturing a package, the method comprising:
manufacturing a substrate;
manufacturing a cover including pigmented material;
mating the cover to the substrate; and
directing laser energy through the substrate to be absorbed by the
pigmented cover material to seal the cover to the substrate.
14. A method of manufacturing a package, the method comprising:
manufacturing a substrate;
manufacturing a cover to include a lower lip with at least one
energy director extending therefrom;
mating the cover to the substrate; and
directing ultrasonic energy to be focused by the energy director to
melt the interface between the cover and the substrate.
15. The method of claim 14 further including forming a cavity in the

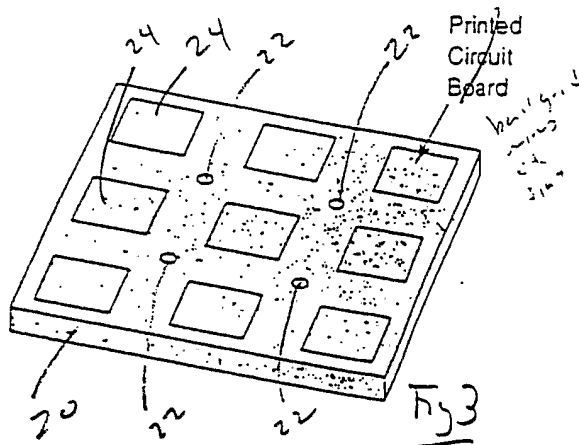
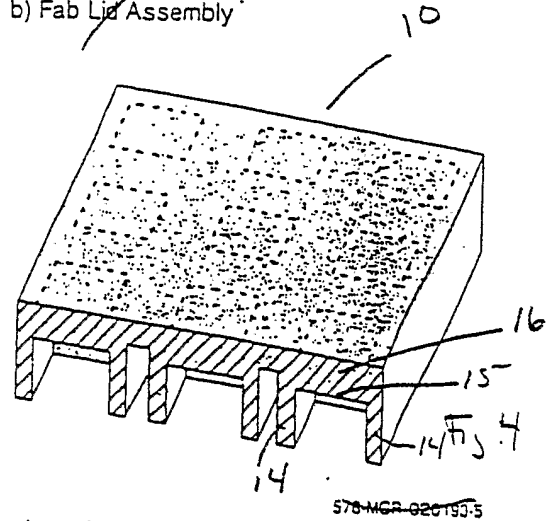
substrate which receives the energy director.

16. A method of manufacturing a package, the method comprising:
 - manufacturing a substrate to include a top layer including a cavity formed therein;
 - manufacturing a cover to include a lower lip with at least one said energy director extending therefrom;
 - mating the cover to the substrate so that the energy director is received in the cavity; and
 - directing ultrasonic energy to be focused by the energy director to melt the interface between the cover and the substrate.

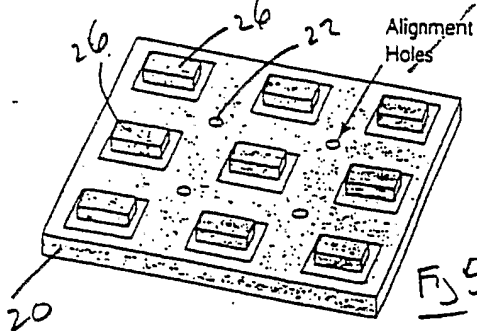
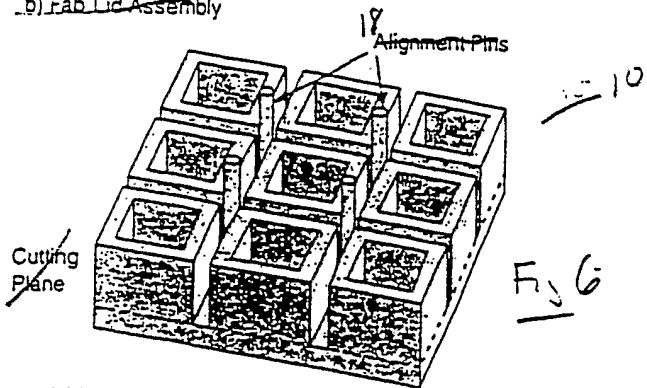
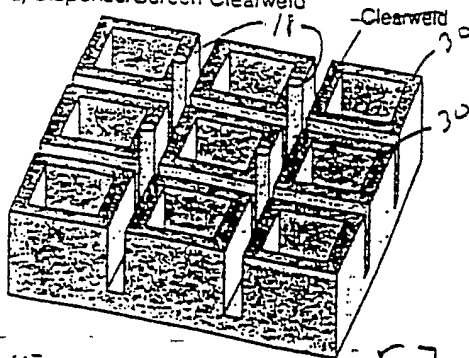
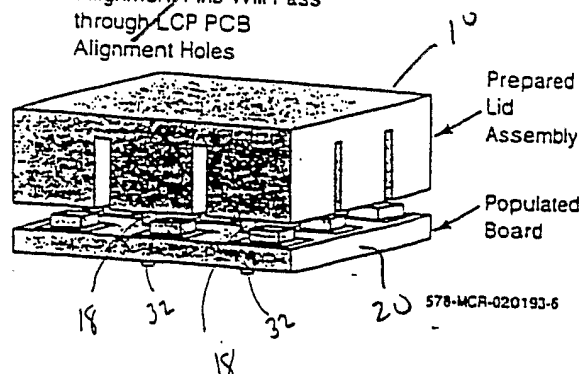




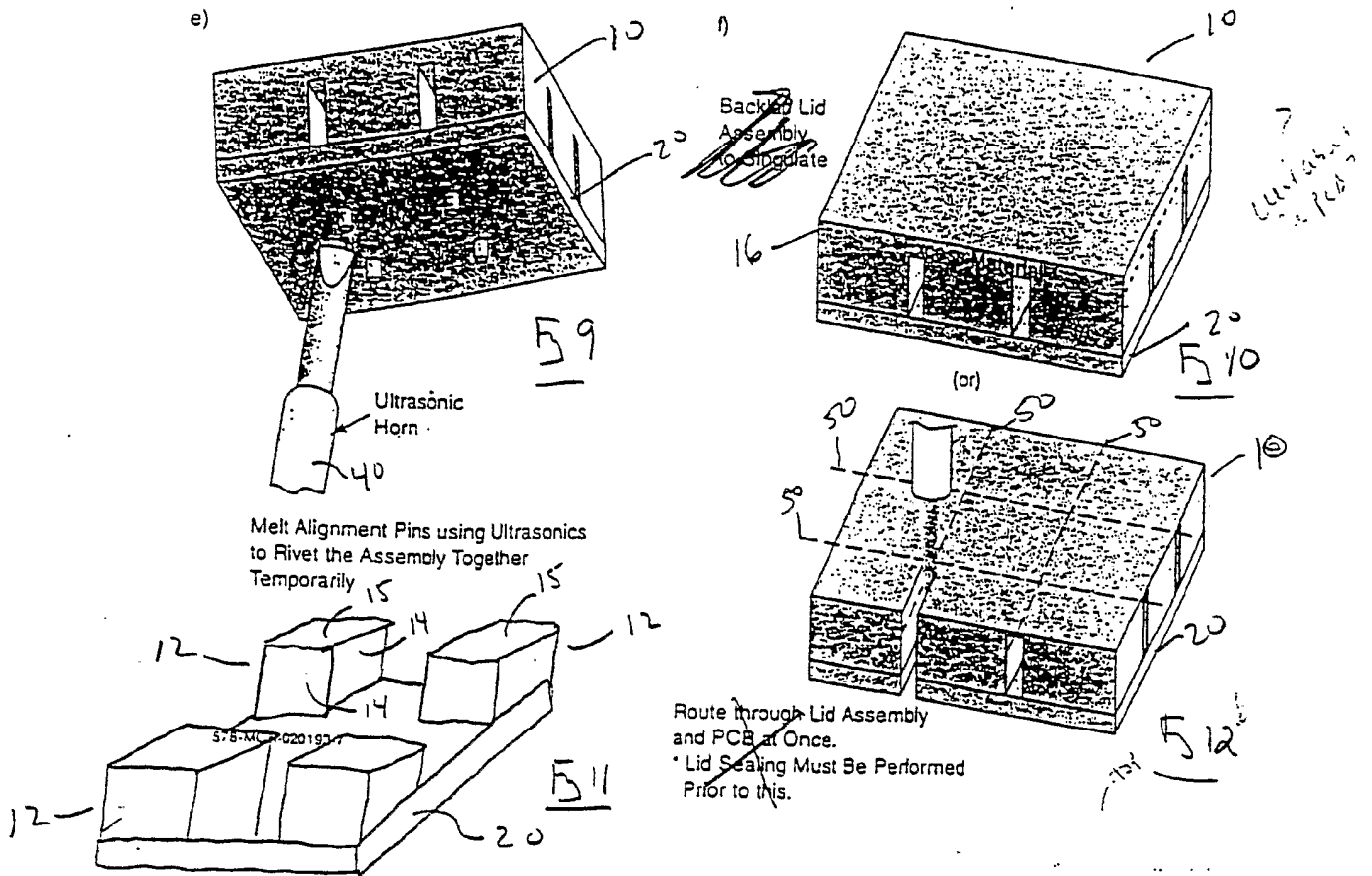
Panel Level Assembly and Packaging

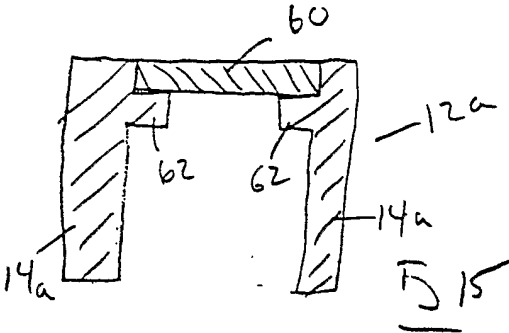
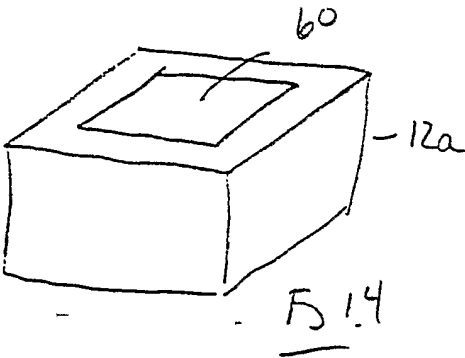
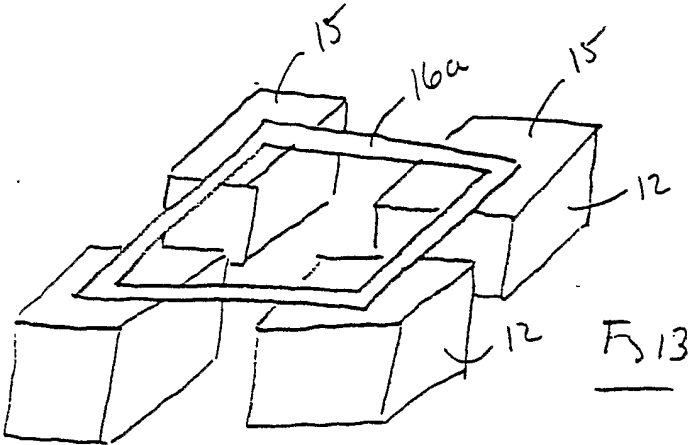
a) ~~Fab Circuit Board~~b) ~~Fab Lid Assembly~~

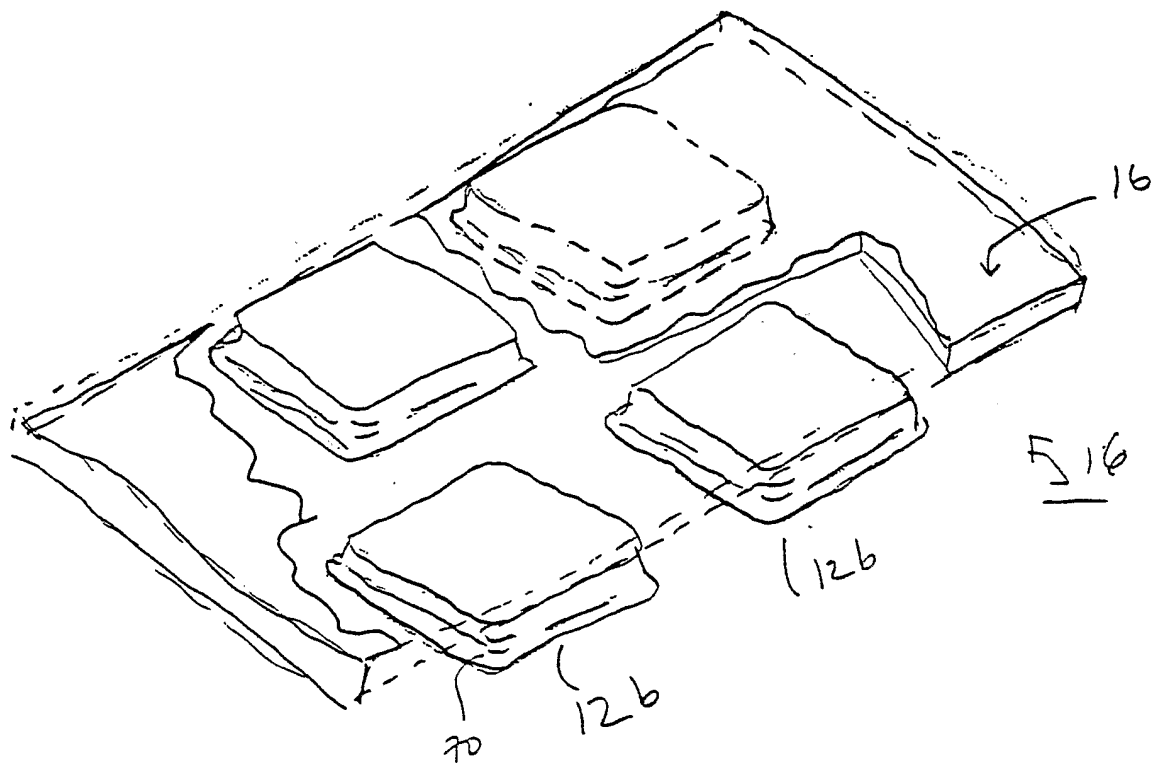
Panel Level Assembly and Packaging (continued)

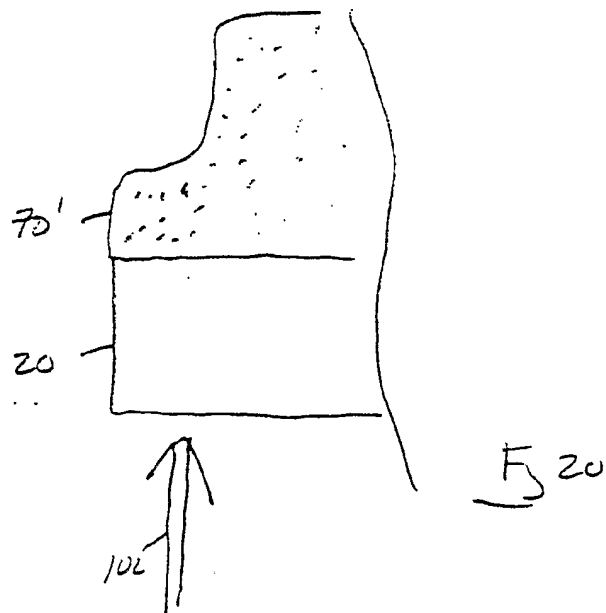
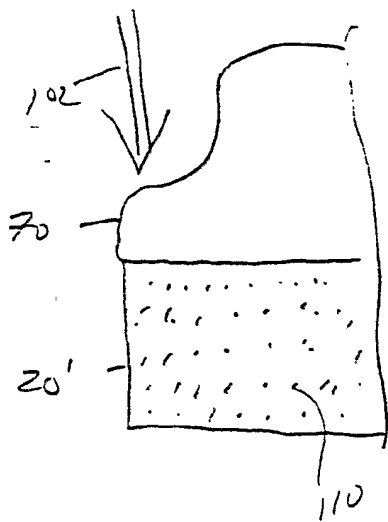
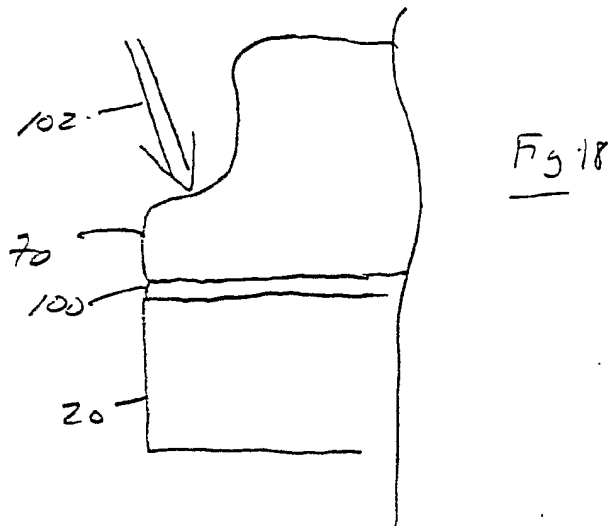
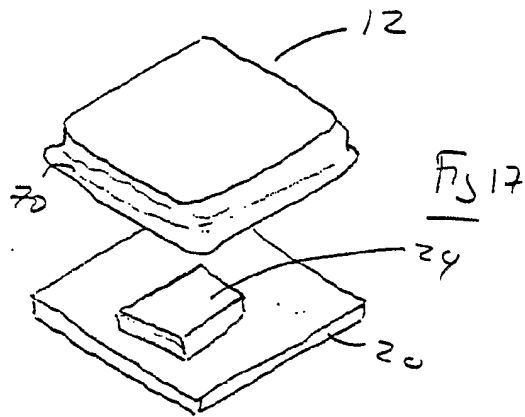
c) ~~Populate Board with Solder or Bond~~b) ~~Fab Lid Assembly~~d) ~~Dispense/Screen Clearweld~~e) ~~Mate Populated Board with Prepared Lid Assembly. Alignment Pins Will Pass through LCP PCB Alignment Holes~~

578-MCR-020193-5









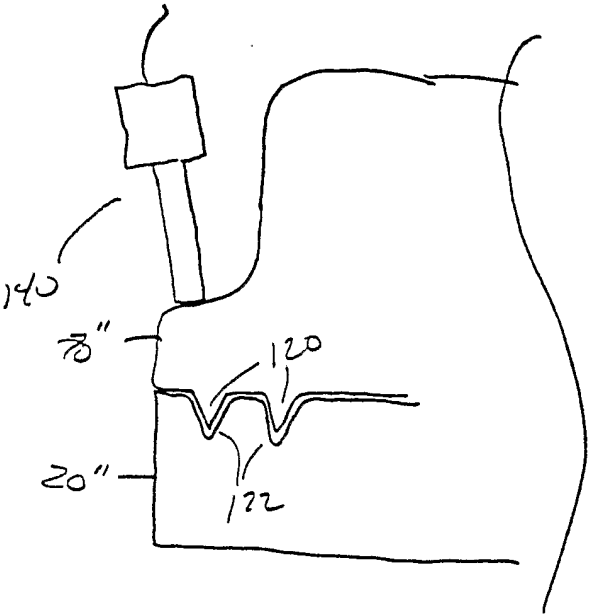


Fig 21

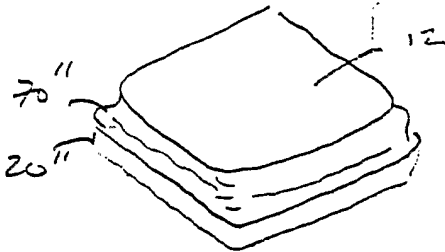
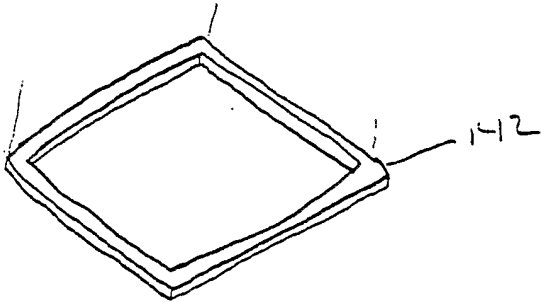


Fig 22

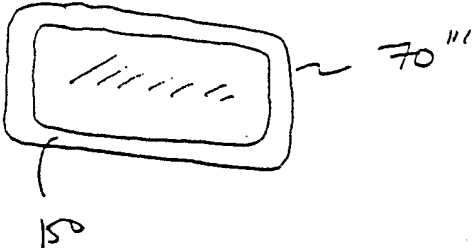
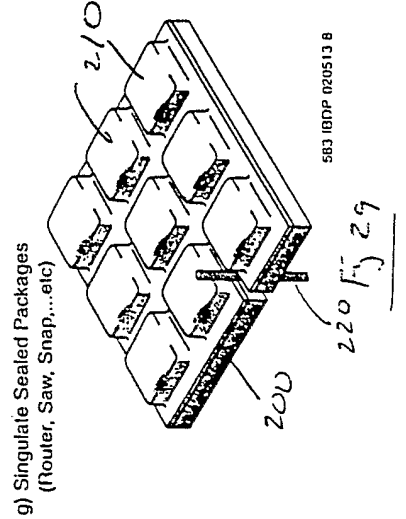
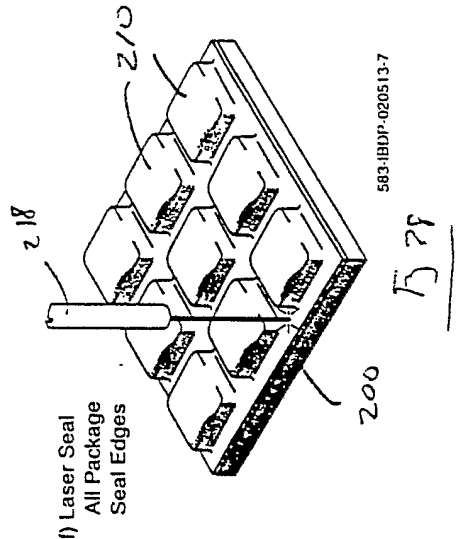
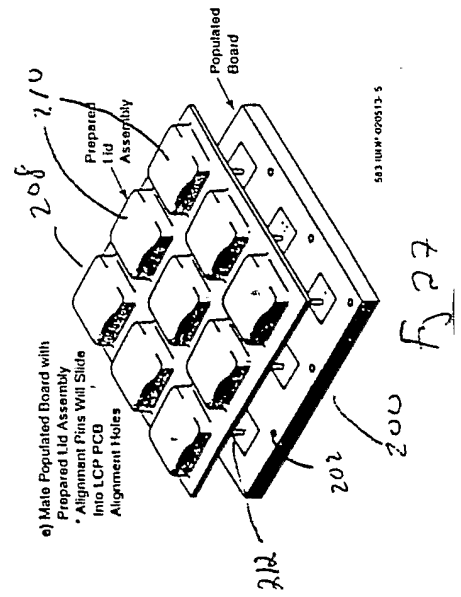
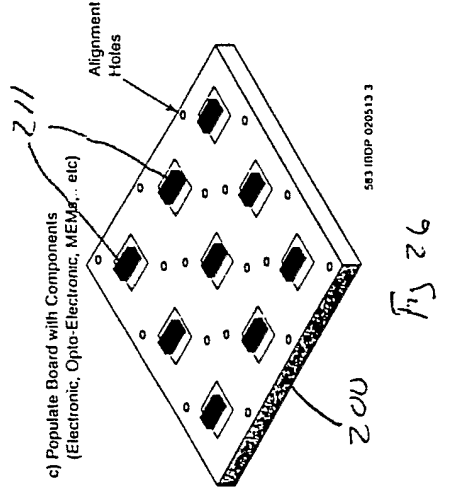
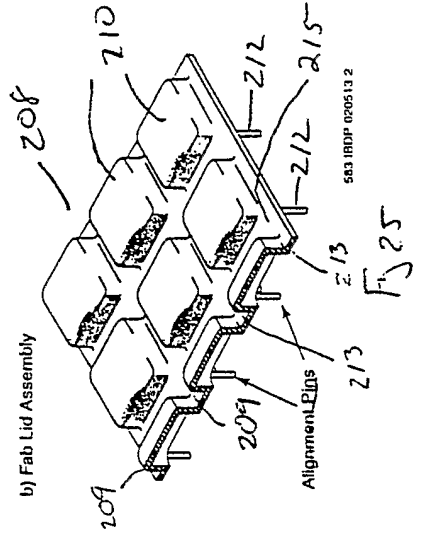
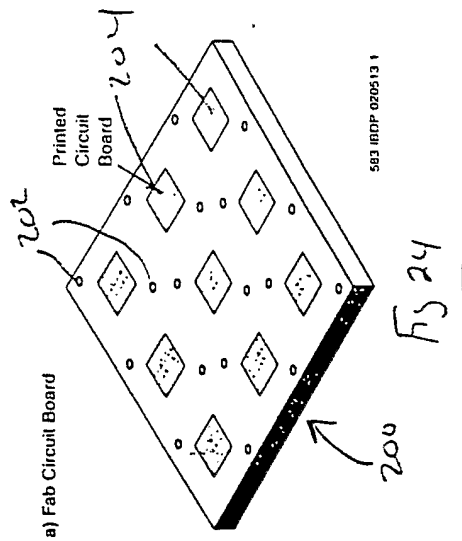


Fig 23

Scalable Manufacturing



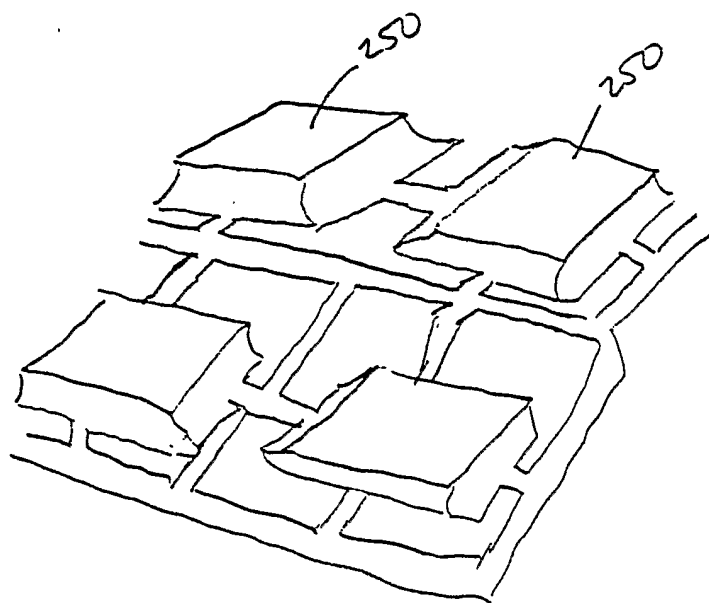


Fig 30