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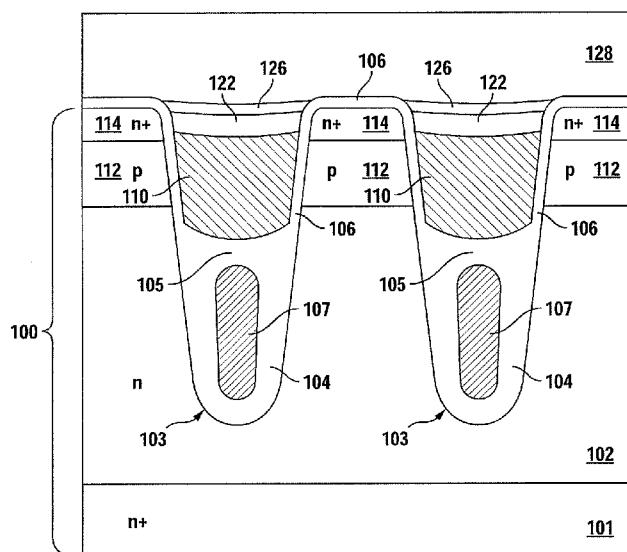


FIG. 1J

(57) Abstract: A method for forming a trench-gate FET includes the following steps. A plurality of trenches is formed extending into a semiconductor region. A gate dielectric is formed extending along opposing sidewalls of each trench and over mesa surfaces of the semiconductor region between adjacent trenches. A gate electrode is formed in each trench isolated from the semiconductor region by the gate dielectric. Well regions of a second conductivity type are formed in the semiconductor region. Source regions of the first conductivity type are formed in upper portions of the well regions. After forming the source regions, a salicide layer is formed over the gate electrode in each trench abutting portions of the gate dielectric. The gate dielectric prevents formation of the salicide layer over the mesa surfaces of the semiconductor region between adjacent trenches.

STRUCTURE AND METHOD FOR FORMING A SALICIDE ON THE GATE ELECTRODE OF A TRENCH-GATE FET

BACKGROUND OF THE INVENTION

5 [0001] The present invention relates in general to semiconductor technology, and more particularly, to a structure and method for forming a salicide on the gate electrode of a trench-gate field effect transistor (FET).

[0002] Conventional metal-oxide-semiconductor (MOS) integrated circuits often utilize a low resistance titanium silicide layer on the polysilicon gate electrode to reduce gate
10 resistance. The titanium silicide layer is generally formed using a self-aligned process. A thin layer of titanium is deposited on the wafer and the wafer is heated. The titanium reacts with exposed silicon to form a titanium silicide. Areas not exposed to silicon do not react, and the un-reacted titanium is removed during subsequent cleaning processes. A silicide formed by such a process may be referred to as a salicide, which is a term used in the art to
15 refer to a self-aligned silicide.

[0003] Conventional MOS integrated circuits utilizing a titanium salicide layer require spacers. The spacers provide a physical and electrical barrier between the titanium salicide and nearby conductive layers to prevent shorting and bridging. In a conventional trench-gate FET, spacers are formed adjacent to the gate dielectric along the trench sidewalls to isolate
20 the titanium salicide from the source regions. Without spacers, the titanium used to form titanium salicide can react with the silicon in the gate dielectric to form titanium silicide stringers that cause shorting between the titanium salicide and the source regions. Also, titanium salicide growth is isotropic, and the salicide layer can extend laterally causing bridging.

25 [0004] Using spacers, however, reduces the cross-sectional area of the salicide layer thus increasing gate resistance. Also, with trench-gate FETs the dielectric layer covering mesa surfaces adjacent to the trench is typically removed during spacer etch, thus allowing salicide to form on the mesa surfaces. Salicide formed on the mesa surfaces is difficult to remove thus impacting subsequent contact etch processes.

[0005] Thus, there is a general need for improved structures and methods for forming a salicide on the gate electrode of a trench-gate FET.

SUMMARY OF THE INVENTION

5 [0006] In accordance with an embodiment of the invention, trench-gate FET structures may be formed as follows. A plurality of trenches is formed extending into a semiconductor region. A gate dielectric is formed extending along opposing sidewalls of each trench and over mesa surfaces of the semiconductor region between adjacent trenches. A gate electrode is formed in each trench isolated from the semiconductor region by the gate dielectric. Well
10 regions of a second conductivity type are formed in the semiconductor region. Source regions of the first conductivity type are formed in upper portions of the well regions. After forming the source regions, a salicide layer is formed comprising at least one of cobalt or nickel over the gate electrode in each trench abutting portions of the gate dielectric. The gate dielectric prevents formation of the salicide layer over the mesa surfaces of the
15 semiconductor region between adjacent trenches.

[0007] In one embodiment, the salicide layer comprises at least one of cobalt, nickel, or molybdenum.

[0008] In another embodiment, forming the well regions comprises performing a thermal process substantially without oxygen to minimize oxide formation over the gate electrode.

20 [0009] In another embodiment, forming the source regions comprises performing a thermal process substantially without oxygen to minimize oxide formation over the gate electrode.

[0010] In yet another embodiment, a wet clean process is performed without HF to minimize removal of exposed portions of the gate dielectric.

[0011] In accordance with another embodiment of the invention, a trench-gate FET
25 structure comprises trenches extending into a semiconductor region with portions of the semiconductor region extending between adjacent trenches forming mesa surfaces. The semiconductor structure also comprises a continuous gate dielectric extending along sidewalls of each trench and over the mesa surfaces, and a gate electrode in each trench isolated from the semiconductor region by the gate dielectric. The semiconductor structure
30 also comprises a salicide layer comprising at least one of cobalt or nickel extending over the gate electrode in each trench and abutting portions of the gate dielectric. The semiconductor

structure also comprises a dielectric layer over the salicide layer in each trench, and an interconnect layer over the dielectric layer and over portions of the gate dielectric extending over the mesa surfaces.

[0012] In one embodiment, the semiconductor structure further comprises well regions of a second conductivity type in the semiconductor region and source regions of a first conductivity type in upper portions of the well regions. The well regions and the source regions are adjacent to the sidewalls of each trench, and the salicide layer in each trench overlaps bottom portions of adjacent source regions along a depth of the trenches.

[0013] In another embodiment, the portions of the gate dielectric extending over the mesa surfaces isolate the interconnect layer from the semiconductor region, and the dielectric layer isolates the interconnect layer from the salicide layer.

[0014] In yet another embodiment, a top surface of the salicide layer in each trench is recessed relative to the mesa surfaces.

[0015] The following detailed description and the accompanying drawings provide a better understanding of the nature and advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Figs. 1A-1J show simplified cross-sectional views at various steps of forming a trench-gate FET structure with a salicide layer on the gate electrode in accordance with embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] In accordance with embodiments of the present invention, trench-gate FET structures with reduced gate resistance are obtained using simple manufacturing processes. Some embodiments include forming a salicide layer comprising cobalt or nickel over the gate electrode. Cobalt and nickel do not react with the silicon in silicon oxide to form stringers in the same manner as titanium, and thus spacers can be eliminated. Eliminating spacers increases the cross-sectional area of the salicide layer thus reducing gate resistance. Other embodiments include forming the source and well regions prior to salicide formation. Source and well formation require high temperature processing. Salicide layers have generally low thermal stability, and forming the salicide layer after source and well formation prevents

exposure of the salicide layer to the high temperature processing. Other embodiments include forming source and well regions using thermal processes substantially without oxygen to minimize oxide formation over the gate electrode. A thin oxide over the gate electrode can be removed prior to salicide formation while minimizing removal of exposed portions of the gate dielectric. Thus, the remaining portions of the gate dielectric extending along upper trench sidewalls can prevent shorting between the salicide layer and the source region. Also, by eliminating spacers the gate dielectric extending over mesa surfaces is not removed during spacer etch. The gate dielectric prevents salicide formation on the mesa surfaces thus improving contact etch processes.

[0018] In yet other embodiments, a wet clean process without HF may be used between implant steps and thermal processes. The wet clean removes less dielectric than conventional wet clean processes using HF. The remaining portions of the gate dielectric along the upper trench sidewalls can prevent shorting between the salicide layer and the source regions. This eliminates the need for spacers, thus increasing the cross-sectional area of the salicide and reducing gate resistance. Also, the remaining portions of the gate dielectric extending over mesa surfaces prevent salicide formation on the mesa surfaces, thus improving contact etch processes. These and other embodiments of the invention, as well as other features and advantages, are described in more detail below.

[0019] Figs. 1A-1J show simplified cross-sectional views at various steps of forming a trench-gate FET structure with a salicide layer on the gate electrode in accordance with embodiments of the invention. It should be understood that the structures illustrated in Figs. 1A-1J are exemplary, and the scope of the invention is not limited to these specific examples. Also, the dimensions in the figures of this application are not to scale, and at times the relative dimensions are exaggerated or reduced in size to more clearly show various structural features. Additionally, while only two trenches are shown in each figure, it is to be understood that the structure illustrated may be replicated many times in an actual semiconductor device.

[0020] In Fig. 1A, trenches 103 are formed in semiconductor region 100 using conventional photolithography and etch techniques. In one embodiment, semiconductor region 100 includes an n-type epitaxial layer 102 extending over a highly doped n⁺ type substrate 101. In some embodiments, trenches 103 extend into and terminate within epitaxial

layer 102. In other embodiments, trenches 103 extend through epitaxial layer 102 and terminate within substrate 101.

[0021] Shield dielectric 104 and shield electrode 107 are formed in the bottom portion of trenches 103 using known techniques. In one embodiment, formation of shield dielectric 104 may include forming a dielectric layer along the sidewalls and bottom of trenches 103 using a conventional oxide deposition or thermal oxidation process. Formation of shield electrode 107 may include forming a layer of polysilicon over the dielectric layer to fill trenches 103. The dielectric and polysilicon layers may then be etched using known techniques to recess the layers in the bottom portion of trenches 103 and thus form shield dielectric 104 and shield electrode 107.

[0022] Inter-electrode dielectric (IED) 105, gate dielectric 106, and polysilicon layer 108 may also be formed in trenches 103 using known techniques. For example, formation of IED 105 may include forming a dielectric layer along the upper sidewalls of trenches 103 and over shield electrode 107 using conventional deposition or thermal oxidation processes. The dielectric layer may be etched using known techniques to recess the layer and form IED 105 extending over shield electrode 107. Gate dielectric 106 may be formed along the upper sidewalls of trenches 103 and over adjacent mesa surfaces using conventional deposition or thermal oxidation processes. The formation of polysilicon layer 108 may include depositing a polysilicon layer over IED 105 and gate dielectric 106 using a conventional polysilicon deposition process.

[0023] In Fig. 1B, one or more conventional polysilicon etch or chemical mechanical polishing (CMP) processes may be used to remove polysilicon layer 108 from over the mesa surfaces between adjacent trenches 103 and form gate electrode 110 in each trench. Also shown in Fig. 1B, well regions 112 may be formed in an upper portion of semiconductor region 100. Formation of well regions 112 may include implanting p-type dopants into an upper portion of semiconductor region 100 using a conventional well implant process. In one embodiment, a wet clean without HF is used after the implant step to clean the surface of the structure prior to high temperature processing. For example, a conventional SC1/SC2 clean without HF may be used. The clean preserves exposed portions of gate dielectric 106 along the upper sidewalls of trenches 103 and over the mesa surfaces. In another embodiment, a thermal process substantially without oxygen may be used to activate the dopants and form well regions 112. For example, the thermal process may use only inert gases such as nitrogen

or argon during a high temperature drive step. This minimizes oxide formation over the gate electrode. The length of the process and the temperature of the process may be determined according to known techniques.

[0024] In Fig. 1C, source regions 114 are formed in an upper portion of semiconductor region 100. For example, a conventional source implant process may be used to implant n-type dopants into an upper portion of semiconductor region 100. In one embodiment, a wet clean without HF may be used after the implant to clean the surface of the structure prior to high temperature processing. For example, a conventional SC1/SC2 clean without HF may be used to preserve exposed portions of gate dielectric 106. In another embodiment, a thermal process substantially without oxygen may be used to activate the dopants and form source regions 114. The thermal process may use only inert gases such as nitrogen or argon during the high temperature drive step to minimize oxide formation over the gate electrode. The length of the process and the temperature of the process may be determined according to known techniques.

[0025] In an alternative embodiment, conventional well and source implant steps may be performed as described above. After the implant steps, a wet clean without HF may be used to clean a surface of the structure prior to high temperature processing. A thermal process substantially without oxygen may then be used to activate the dopants and form well regions 112 and source regions 114.

[0026] In yet another embodiment, a conventional well implant step may be performed as described above. After the well implant step, a wet clean without HF may be used to clean the surface of the structure. A conventional source implant step may be performed as described above. After the source implant step, a wet clean without HF may be used to clean the surface of the structure. A thermal process substantially without oxygen may then be used to activate the dopants and form well regions 112 and source regions 114. Alternatively, the source implant may be performed prior to the well implant in any of the above embodiments. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0027] In Fig. 1D, metal layer 116 and cap layer 118 are formed over the structure using known techniques. In one embodiment, a cleaning process may be used prior to forming metal layer 116 to remove oxide from the surface of gate electrode 110. The cleaning process may include one or more conventional wet or dry etch processes. For example, in

one embodiment a wet etch process using a sulfuric peroxide mix (SPM) etch followed by a dilute HF etch may be used. Tests have shown that this process can enable formation a salicide layer with low sheet resistance and low resistivity. The cleaning process can be carefully designed to remove the oxide from the surface of gate electrode 110 with minimal impact on the exposed portions of gate dielectric 106.

[0028] In one embodiment, metal layer 116 is formed using a conventional metal deposition process. Metal layer 116 contacts an upper surface of gate electrode 110 and extends over gate dielectric 106 along the upper sidewalls of trenches 103 and over the mesa surfaces. Metal layer 116 may comprise titanium, cobalt, nickel, molybdenum or other metals or alloys suitable for salicide formation. Cap layer 118 may be formed over metal layer 116 to prevent oxidation of metal layer 116 during subsequent processing. In one embodiment, cap layer 118 may comprise titanium or titanium nitride and be formed over metal layer 116 using a conventional deposition process.

[0029] In one embodiment, a metal layer comprising cobalt, nickel, or molybdenum is used to form metal layer 116. The silicides of these metals do not react with the silicon in silicon oxide to form stringers in the same manner as titanium, thus reducing shorts and eliminating the need for spacers. Also, the differential etch between these metals and their respective silicides allow them to be used in self-aligned processes. This is in contrast to metals such as tungsten, which cannot be used to form a salicide because the unreacted metal cannot be removed without also removing the silicide. Thus, tungsten silicide requires separate photo and etch processing, and does not provide the device scaling of a self-aligned process.

[0030] In Fig. 1E, mono-silicide layer 120 is formed over gate electrode 110 using known techniques. For example, in one embodiment a conventional rapid thermal anneal (RTA) process at a temperature of between about 475 - 600°C for between about 20 - 40 seconds may be used to react portions of metal layer 116 with silicon from gate electrode 110 to form mono-silicide layer 120. As shown in Fig. 1E, portions of metal layer 116 extending over gate dielectric 106 and cap layer 118 remain unreacted. Portions of gate dielectric 106 extending over mesa surfaces prevent salicide formation on the mesa surfaces.

[0031] In Fig. 1F, cap layer 118 and unreacted portions of metal layer 116 are removed using known techniques. For example, in an embodiment one or more conventional wet or dry etch processes may be used to remove cap layer 118 and the unreacted portions of metal

layer 116. The etch processes are selective and do not remove mono-silicide layer 120 or the exposed portions of gate dielectric 106 extending over the mesa surfaces.

[0032] In Fig. 1G, salicide layer 122 is formed over gate electrode 110 using known techniques. For example, in one embodiment a conventional RTA process at a temperature of between about 700 - 800°C may be used to convert mono-silicide layer 120 to salicide layer 122. As shown in Fig. 1G, salicide layer 122 may abut portions of gate dielectric 106 thus increasing the cross-sectional area of salicide layer 122. In one embodiment, the thickness of mono-silicide layer 120 can be carefully designed such that a bottom surface of salicide layer 122 overlaps a bottom portion of source regions 114 along a depth of trenches 103. This can increase the volume of salicide layer 122 and further decrease gate resistance. In another embodiment, the top surface of salicide layer 122 is recessed relative to the adjacent mesa surfaces.

[0033] In Fig. 1H, dielectric layer 124 is formed over the structure using known techniques. For example, in one embodiment a conventional dielectric deposition process may be used to deposit dielectric layer 124 over salicide layer 122 and the exposed portions of gate dielectric 106 extending over the mesa surfaces. In an embodiment, one or more conventional dielectric etch or CMP processes may be used to remove dielectric layer 124 from over the mesa surfaces and form self-aligned dielectric layer 126 over salicide layer 122. In other embodiments, conventional photolithography and etch techniques may be used to remove dielectric layer 124 from over the mesa surfaces.

[0034] In Fig. 1J, interconnect layer 128 (e.g., comprising metal) is formed over the top side of the structure using known techniques. The portions of gate dielectric 106 extending over the mesa surfaces between adjacent trenches isolate source regions 114 from interconnect layer 128. The high quality gate dielectric 106 improves isolation between the mesa surfaces and interconnect layer 128. Interconnect layer 128 contacts source regions 114 at source contacts along a third dimension (e.g., the dimension into the page). This increases device density by eliminating stripe-shaped source contacts between trenches 103. A bottom-side conductive interconnect layer (not shown), e.g., comprising metal, that electrically contacts the backside of semiconductor region 100 may also be formed using known techniques.

[0035] Structures formed according to embodiments of the present invention enjoy, among other advantages and features, elimination of spacers (by forming a salicide layer comprising cobalt, nickel, or molybdenum, by minimizing oxide formation over the gate electrode during

formation of source and well regions, and/or by preserving gate dielectric thickness along upper trench sidewalls during cleaning processes), prevention of salicide formation on mesa surfaces (by preserving gate dielectric thickness over mesa surfaces), reduction in gate resistance (by increasing cross-sectional area and volume of the salicide layer), improved contact etch processes (by preventing salicide formation on mesa surfaces), increased device density and scalability (by eliminating spacers and stripe-shaped source contacts between each trench), and reduced process complexity (by eliminating spacer deposition and etch processes). Further, embodiments of the invention described herein advantageously form salicide layer 122 after formation of well regions 112 and source regions 114, thus preventing exposure of salicide layer 122 to the thermal processes associated with well and source formation. This allows the use of salicides comprising cobalt or nickel, which have a lower thermal stability than titanium salicide.

[0036] The trench-gate FET structures illustrated in Figs. 1A-1J include a shielded gate. It is to be understood that methods of the present invention can be applied to conventional non-shielded trench-gate FET devices.

[0037] Note that while the embodiments depicted in Figs. 1A-1J shows n-channel trench-gate FETs, p-channel trench-gate FETs may be obtained by reversing the polarity of the source and well regions, the epitaxial layer, and the substrate. Further, in embodiments where the semiconductor region includes an epitaxial layer extending over a substrate, MOSFETs devices are obtained when the substrate and epitaxial layer are of the same conductivity type, while IGBTs devices are obtained when the substrate has the opposite conductivity type to that of the epitaxial layer.

[0038] Furthermore, while the various embodiments described above are implemented in conventional silicon, these embodiments and their obvious variants can also be implemented in silicon carbide, gallium arsenide, gallium nitride, diamond, or other semiconductor materials. Additionally, the features of one or more embodiments of the invention may be combined with one or more features of other embodiments of the invention without departing from the scope of the invention.

[0039] Therefore, the scope of the present invention should be determined not with reference to the above description, but should instead be determined with reference to the appended claims along with their full scope of equivalents.

WHAT IS CLAIMED IS:

1 1. A method of forming a trench-gate FET structure, the method
2 comprising:
3 forming a plurality of trenches extending into a semiconductor region;
4 forming a gate dielectric extending along opposing sidewalls of each trench
5 and over mesa surfaces of the semiconductor region between adjacent trenches;
6 forming a gate electrode in each trench;
7 forming well regions of a second conductivity type in the semiconductor
8 region;
9 forming source regions of the first conductivity type in upper portions of the
10 well regions; and
11 after forming the source regions, forming a salicide layer comprising at least
12 one of cobalt or nickel over the gate electrode in each trench abutting portions of the gate
13 dielectric, wherein the gate dielectric prevents formation of the salicide layer over the mesa
14 surfaces of the semiconductor region between adjacent trenches.

1 2. The method of claim 1 wherein the salicide layer comprises at least
2 one of cobalt, nickel, or molybdenum.

1 3. The method of claim 1 wherein forming the well regions comprises
2 performing a thermal process substantially without oxygen to minimize oxide formation over
3 the gate electrode in each trench.

1 4. The method of claim 1 wherein forming the source regions comprises
2 performing a thermal process substantially without oxygen to minimize oxide formation over
3 the gate electrode in each trench.

1 5. The method of claim 1 further comprising:
2 performing a wet clean process without HF to minimize removal of exposed
3 portions of the gate dielectric.

1 6. The method of claim 1 wherein the source regions are formed adjacent
2 to the opposing sidewalls of each trench, and the salicide layer in each trench overlaps bottom
3 portions of the adjacent source regions along a depth of the plurality of trenches.

1 7. The method of claim 1 further comprising:
2 forming a dielectric layer over the salicide layer in each trench; and
3 forming an interconnect layer over the dielectric layer, the dielectric layer
4 isolating the interconnect layer from salicide layer.

1 8. The method of claim 1 wherein forming the salicide layer comprises:
2 forming a metal layer extending over exposed portions of the gate dielectric
3 and over the gate electrode in each trench;
4 performing a thermal process such that portions of the metal layer extending
5 over the gate electrode in each trench react to form the salicide layer; and
6 removing unreacted portions of the metal layer.

1 9. The method of claim 1 further comprising:
2 forming a shield electrode in each trench under the gate electrode; and
3 forming an inter-electrode dielectric in each trench extending between the
4 shield electrode and the gate electrode.

1 10. A method of forming a trench-gate FET structure, the method
2 comprising:
3 forming a trench extending into the semiconductor region;
4 forming a gate dielectric along sidewalls of the trench and over mesa surfaces
5 of the semiconductor region adjacent to the trench;
6 forming a gate electrode in the trench;
7 performing a first implant of dopants of the first conductivity type into the
8 semiconductor region;
9 performing a second implant of dopants of a second conductivity type into the
10 semiconductor region;
11 performing one or more thermal processes to thereby form a source region
12 corresponding to the first implant and a well region corresponding to the second implant, the
13 one or more thermal processes being performed substantially without oxygen to minimize
14 oxide formation over the gate electrode; and
15 after performing the thermal process, forming a salicide layer comprising at
16 least one of cobalt or nickel over the gate electrode abutting portions of the gate dielectric,

17 wherein the gate dielectric prevents formation of the salicide layer along the mesa surfaces of
18 the semiconductor region.

1 11. The method of claim 10 wherein the salicide layer comprises at least
2 one of cobalt, nickel, or molybdenum.

1 12. The method of claim 10 wherein the salicide layer overlaps a bottom
2 portion of the source region along a depth of the trench.

1 13. The method of claim 10 further comprising:
2 performing a wet clean process without HF to minimize removal of exposed
3 portions of the gate dielectric.

1 14. The method of claim 10 wherein forming the salicide layer comprises:
2 forming a metal layer extending over exposed portions of the gate dielectric
3 and the gate electrode;
4 performing a second thermal process such that portions of the metal layer
5 extending over the gate electrode react to form a mono-silicide;
6 removing unreacted portions of the metal layer; and
7 performing a third thermal process such that the mono-silicide reacts to form
8 the salicide layer.

1 15. A trench-gate FET structure comprising:
2 trenches extending into a semiconductor region, wherein portions of the
3 semiconductor region extending between adjacent trenches form mesa surfaces;
4 a continuous gate dielectric extending along sidewalls of each trench and over
5 the mesa surfaces;
6 a gate electrode in each trench;
7 a salicide layer comprising at least one of cobalt or nickel extending over the
8 gate electrode in each trench and abutting portions of the gate dielectric;
9 a dielectric layer over the salicide layer in each trench; and
10 an interconnect layer over the dielectric layer and over portions of the gate
11 dielectric extending over the mesa surfaces.

1 16. The trench-gate FET structure of claim 15 wherein the salicide layer
2 comprises at least one of cobalt, nickel, or molybdenum.

1 17. The trench-gate FET structure of claim 15 further comprising:
2 well regions of a second conductivity type in the semiconductor region; and
3 source regions of a first conductivity type in upper portions of the well
4 regions, wherein the well regions and the source regions are adjacent to the sidewalls of each
5 trench, and wherein the salicide layer in each trench overlaps bottom portions of adjacent
6 source regions along a depth of the trenches.

1 18. The trench-gate FET structure of claim 15 wherein portions of the gate
2 dielectric extending over the mesa surfaces isolate the interconnect layer from the
3 semiconductor region and the dielectric layer isolates the interconnect layer from the salicide
4 layer.

1 19. The trench-gate FET structure of claim 15 wherein a top surface of the
2 salicide layer in each trench is recessed relative to adjacent mesa surfaces.

1 20. The trench-gate FET structure of claim 15 further comprising:
2 a shield electrode in each trench under the gate electrode; and
3 an inter-electrode dielectric in each trench extending between the shield
4 electrode and the gate electrode.

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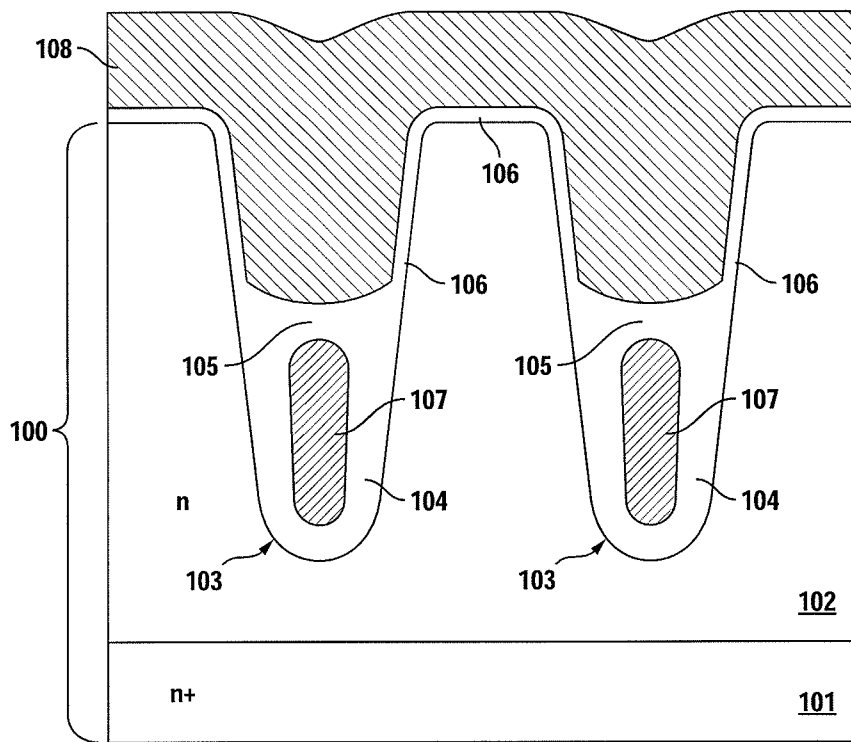


FIG. 1A

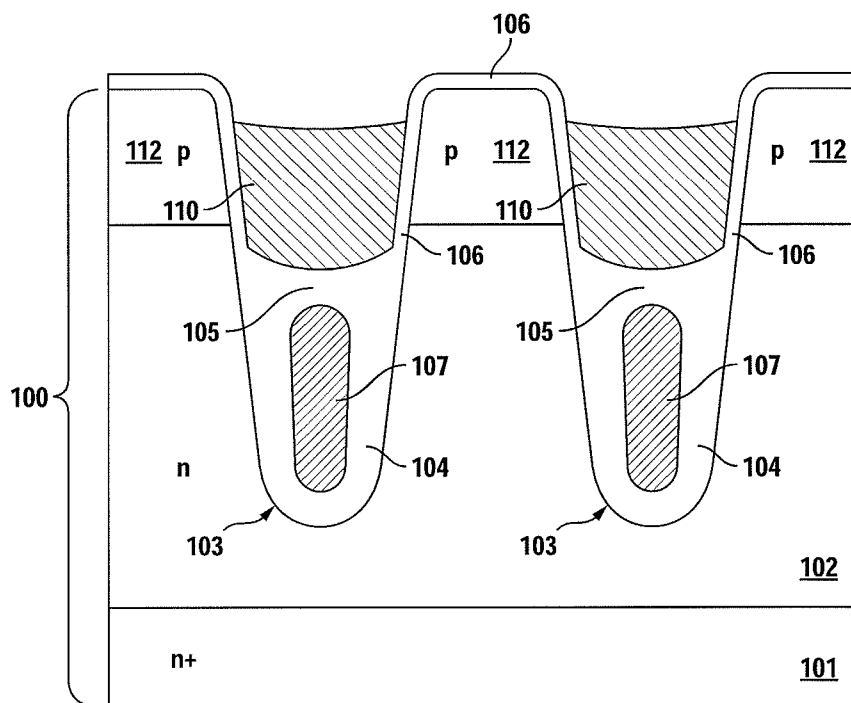


FIG. 1B

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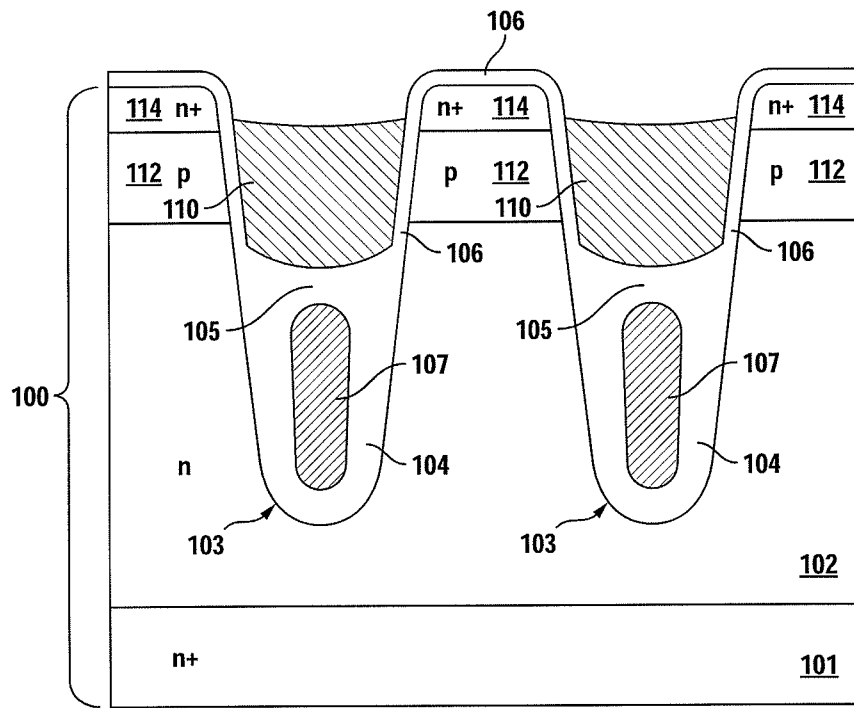


FIG. 1C

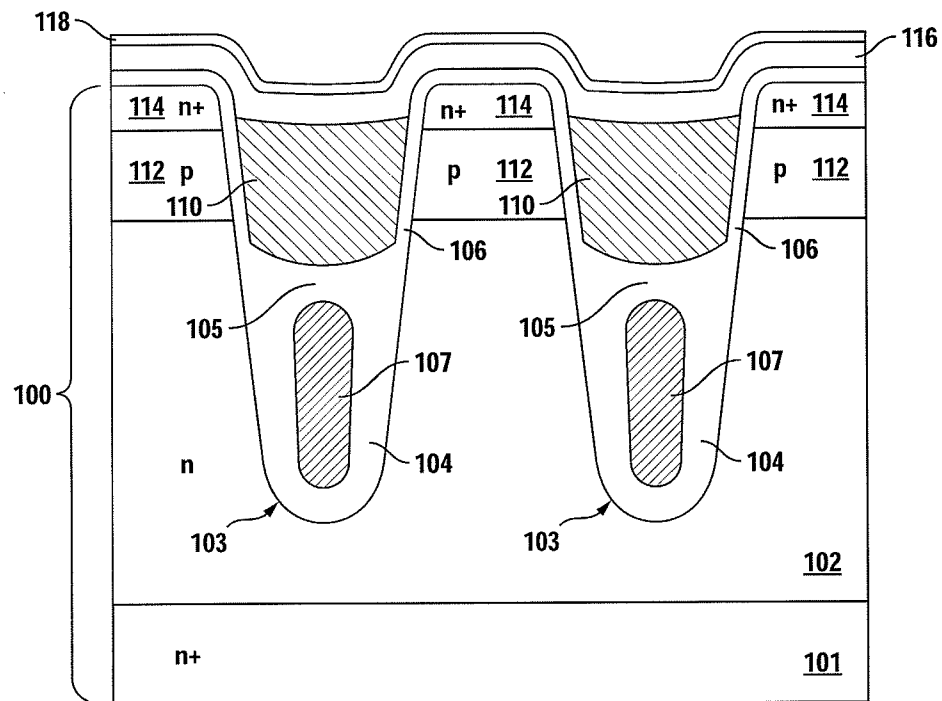


FIG. 1D

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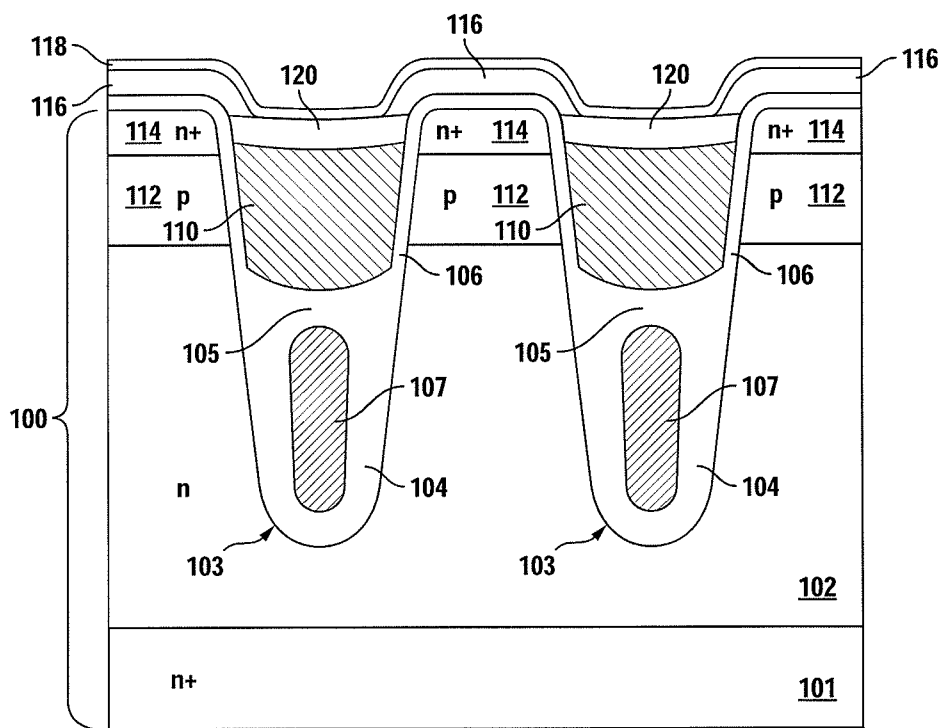


FIG. 1E

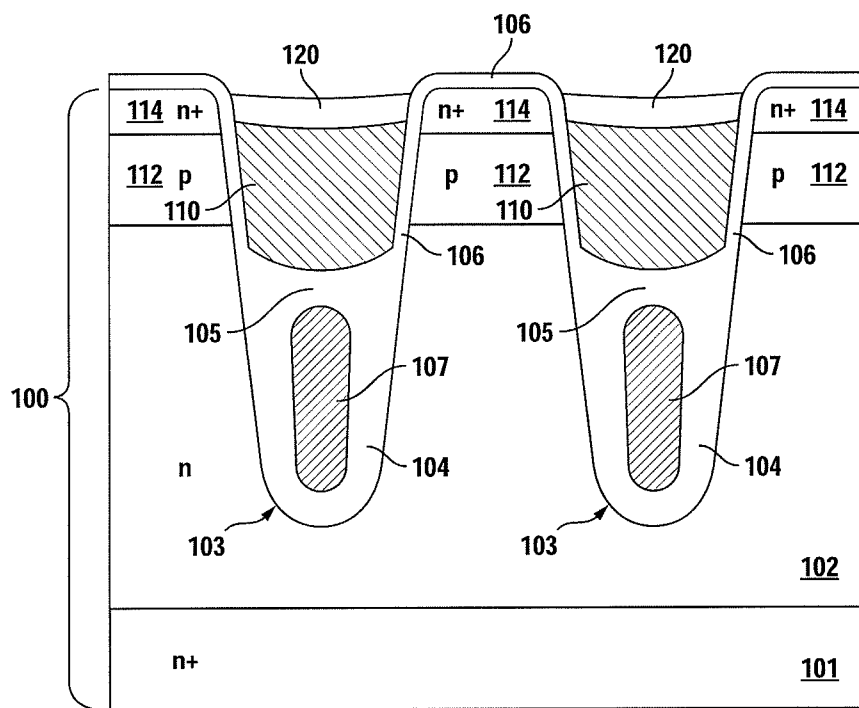


FIG. 1F

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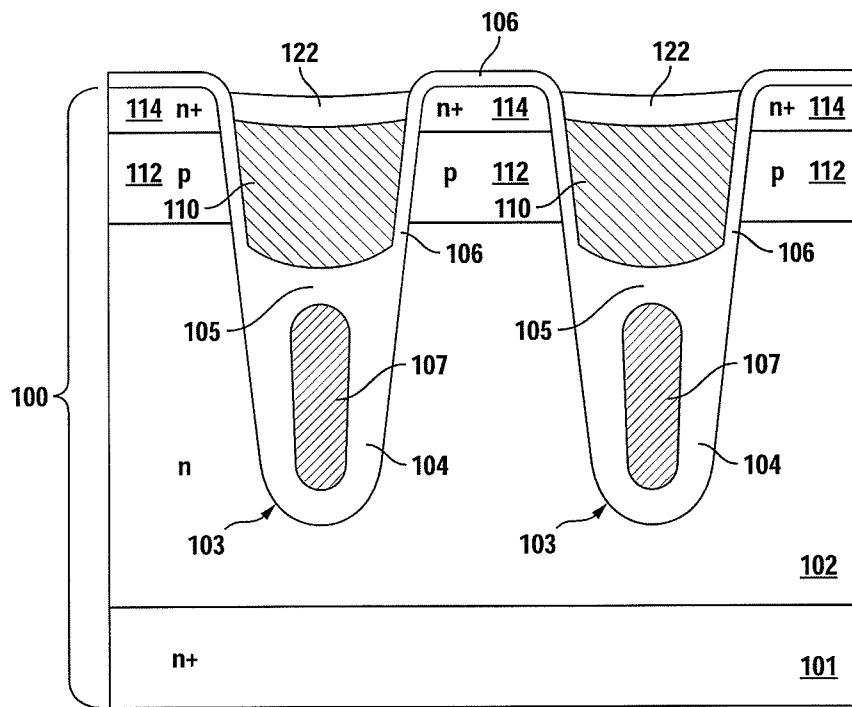


FIG. 1G

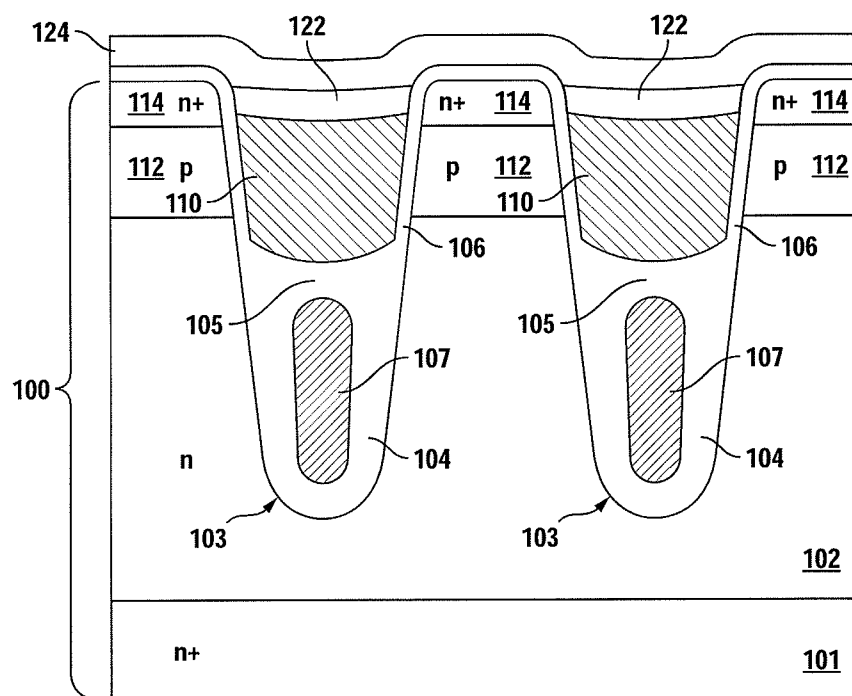


FIG. 1H

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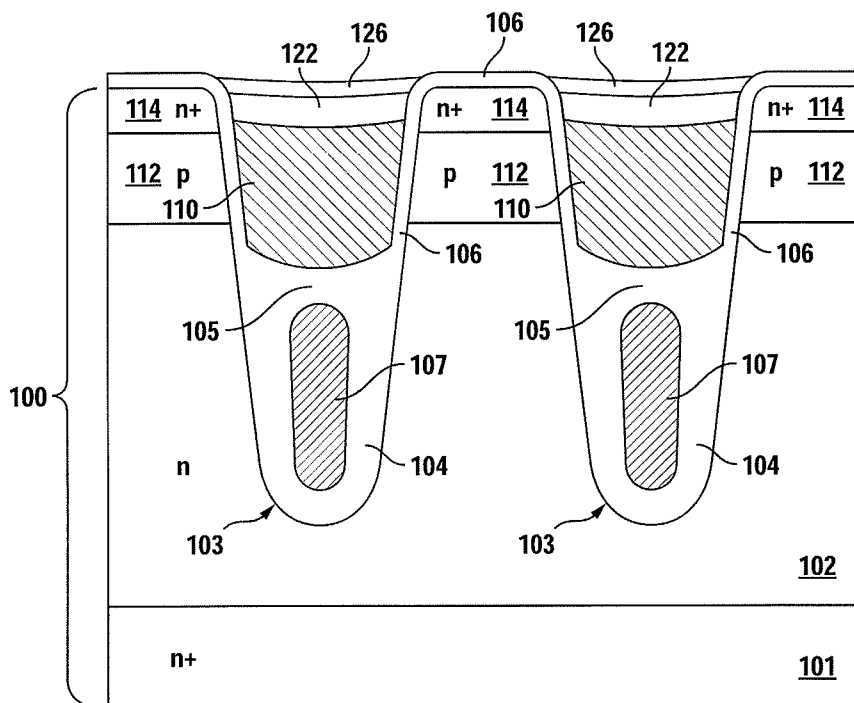


FIG. 1I

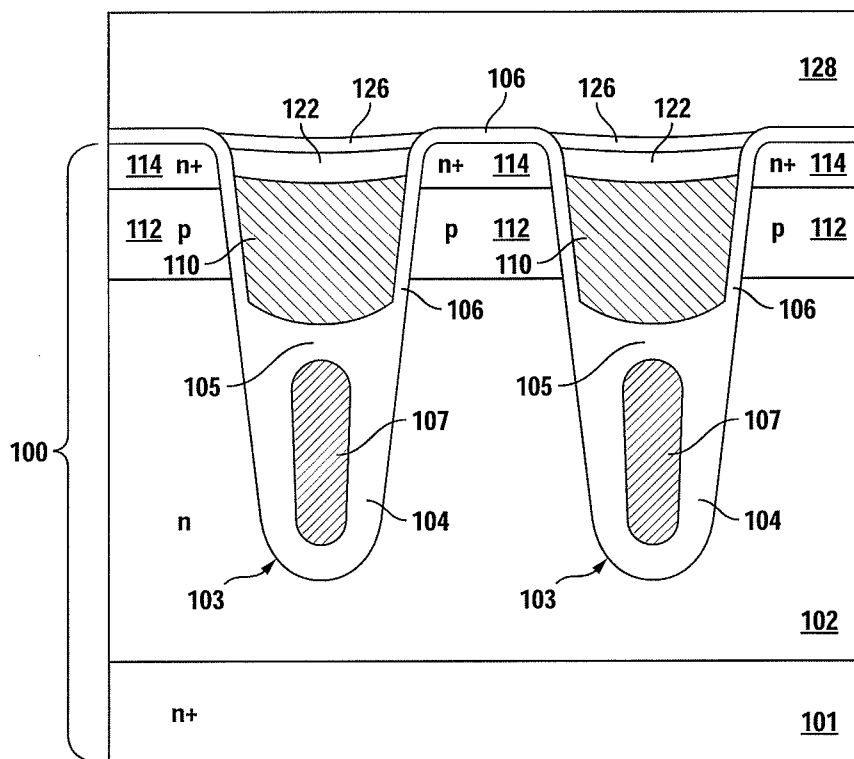


FIG. 1J