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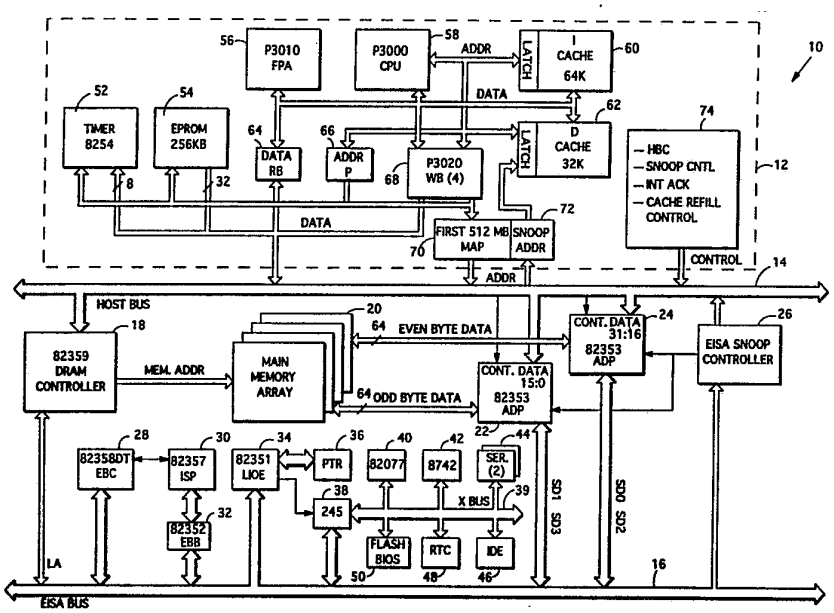

(57) Abstract

A microcomputer system, according to an embodiment of the present invention, comprises a motherboard with sockets for EISA add-on boards and a processor board. The BIOS program for the processor board is stored on the motherboard, in a flash memory. A permanent BIOS program, also on the motherboard, has program code for a routine to check if the BIOS in flash memory is appropriate for the particular type of processor board then installed. Each processor board has a code wired into its edge connector, and this code will hardwise select a portion of the permanent BIOS that is machine code correct for the CPU on the processor board. BIOS programms in flash memory can be updated or changed by downloading from a floppy disk under control of the permanent BIOS.

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BASIC INPUT/OUTPUT SYSTEM (BIOS) PROGRAM STORAGE ON A MOTHERBOARD FOR A VARIETY OF COMPUTER CPU TYPES

Background of the Invention

The present invention relates generally to microcomputer systems and more particularly to the problem of providing and updating basic input/output system (BIOS) programs in systems capable of accepting a variety of CPU types on plug-in processor boards that fit into a common motherboard.

It is the industry practice in microcomputer based systems to provide a basic input/output system (BIOS) program in some type of read only memory (ROM). BIOS programs provide the specific interfacing necessary between a particular computer system and a generalized disk operating system (DOS), such as MS-DOS. Sometimes the BIOS is copied to random access memory (RAM) for execution (because it is faster), and sometimes the BIOS is delivered in easy-to-program EPROM. A boot-up program needed to initialize the system and read-in the DOS can be, and often is, separated from the BIOS. Since the BIOS is a program, albeit firmware, it is subject to constant "improvement," in the form of updates (new versions). The BIOS must necessarily be in machine code, so different types of CPUs will each require their own tailor-made BIOS program to provide similar functionality.

The advent of computer system platforms and industry standard busses, such as EISA, have encouraged the use of plug-in boards that can be mixed and matched on a system motherboard. The rapid advancement of microcomputer technology has also caused many sizes and speeds of a single microprocessor family to be simultaneously available. For example, the Intel 286, 386, and 486 are all available on EISA type boards and come in a variety of CPU speeds ranging from 10 to 50 MHz. At one extreme this selection offers economy, and at the other extreme it offers performance. It then is an easy matter for a user to buy what is needed in the way of parts, and then to plug them together.

Of the various popular program mediums, floppy disks are the easiest for users to acquire, handle, and insert into their systems. Replacing boards and/or chips, such as BIOS ROM chips, is more difficult, and often results in system failures, especially when users without technical training try to install boards and/or chips.

What is needed in view of the low level of user technical expertise is a hardware system capable of determining which BIOS program is

appropriate and then to automatically load it in the appropriate permanent memory space from a floppy disk.

Summary of the Invention

Briefly, an embodiment of the present invention comprises a flash memory on a motherboard and means to download a BIOS program from a floppy disk. Alternatively, a means for determining the type of CPU is present on a plug-in board installed in the motherboard and can be used to select among several different BIOS programs present on the floppy for downloading to the flash memory.

An advantage of the present invention is that a flexible computer system architecture is enabled thereby that allows quick and easy field updating of the BIOS by users.

Brief Description of the Drawings

Fig. 1 is a block diagram of a computer system constructed according to one embodiment of the present invention. A block diagram of a typical processor board is shown connected to the system's motherboard;

Fig. 2 is a top view of the motherboard for the system of Fig. 1. The locations of the major active components are identified;

Fig. 3 is a top view of the motherboard for the system of Fig. 1. The locations of the various connectors and plugs are identified;

Fig. 4 is a block diagram of a simple i386DX based processor board capable of being plugged into the system of Fig. 1;

Fig. 5 is a block diagram of a high performance i486DX based processor board capable of being plugged into the system of Fig. 1;

Fig. 6 is a block diagram of the state machine interfacing the processor board of Fig. 5 to the system of Fig. 1. The PST logic in Fig. 4 is similar in purpose and implementation;

Fig. 7 is a block diagram of a i486DX based processor board capable of being plugged into the system of Fig. 1. The PST logic is shown functionally divided among five PALs U1 and U3-U6.;

Fig. 8 is a top view of a printed circuit board assembly for a i486DX based processor board capable of being plugged into the system of Fig. 1;

Fig. 9 is a top view of a printed circuit board assembly for a i486SX based processor board capable of being plugged into the system of Fig. 1;

Fig. 10 is a block diagram of a i486DX based processor board and cache that is capable of being plugged into the system of Fig. 1;

Fig. 11 is a block diagram of a computer system constructed according to a second embodiment of the present invention. Block diagrams of several typical processor boards are all shown connected to the system's

motherboard, although only one at a time is usually configured. A major difference between this system and the one in Fig. 1 is the addition of a high-speed system bus for high-performance peripherals, such as the SCSI or LAN master controller shown here;

Fig. 12 is a detailed block diagram showing schematically the interfacing of a CPU to the host system bus such that a cache write-back can be supported; and

Fig. 13 is a memory map of the address space for a MIPS type RISC CPU implementation on a processor board capable of being plugged into the system of Fig. 1 or Fig. 11.

Detailed Description of the Embodiments

A first embodiment of the present invention comprises a high-end, desktop computer 10 which is useful in several different roles. For example, as a stand-alone workstation, as a LAN server, or as a LAN workstation required to perform local processing. Referring to Fig. 1, system 10 comprises a CPU board 12 compatible with a host bus 14, an EISA bus 16, a DRAM controller (DRC) 18, a main DRAM memory array 20, a pair of advanced data path (ADP) units 22 and 24, an EISA "snoop" controller 26, an EISA bus controller (EBC) 28, an integrated systems peripheral (ISP) 30, an EISA bus buffer (EBB) 32, an EISA local I/O (LIOE) 34, a PTR 36, a bus transceiver 38 for an Xbus 39, a diskette drive controller 40, a keyboard mouse controller 42, a pair of serial interfaces 44, an IDE 46, a real time clock (RTC) 48, and a flash BIOS ROM 50. Snoop controller 26 monitors the EISA bus 16 in order to capture EISA memory cycles and initiates a snoop request to a write-back cache system. The snoop controller 26 manages all EISA snoop cycles and generates wait states for EISA hits to cache. It also provides address to cache controller for EISA read snoops. Preferably, LIOE 34 is an Intel 82351, EBB 32 is an Intel 82352, ADP 22 and 24 are Intel 82353, ISP 30 is an Intel 82357, EBC 28 is an Intel 82358DT, DRC 18 is an Intel 82359, diskette drive controller 40 is an Intel N82077AA-1, BIOS EPROM is a type 27C512, flash BIOS EEPROM 50 is a type 28F512, RTC 48 is a Dallas Semiconductor DS1287 or Motorola MC146818, configuration SRAM is a DS1225, keyboard/mouse controller 42 is an Epson 8742, and the serial/parallel port driver is a Western Digital WD16C552JT. Other components from other manufacturers may be used, but the above are known to work together in a system and their use will save the reader from undue experimentation. A summary of the major chips and there functional descriptions are

presented in Table I. There locations on the motherboard are shown in Fig. 2.

TABLE I

Chip Device	Description
EISA chipset 82351-EISA local I/O (LIOE) 34	Supports or integrates the I/O peripheral functions, including system configuration registers, status/control registers, interrupt logic, parallel port interface, local I/O bus address decoder and data buffer control.
82352 - EISA Bus Buffers (EBB) 32	Buffers and latches DMA addresses.
82353 Advanced Data Path (ADP) 22 and 24	Used with the DRC; provides dual-ported data path system host data bus and the DRAM data bus; includes posted write latch, internal parity generator/checker and byte assembly/disassembly logic. Two ADPs are required for 32-bit buses.
82357 - Integrated Systems Peripheral (ISP) Controller 30	Performs the DMA functions; includes seven 32-bit DMA channels, two 8-channel interrupt controllers, and five 16-bit timer/counters; provides for multiple MNI control/generation and refresh address generation; supports multiple EISA bus masters.
82358DT - EISA Bus Controller (EBC) 28	Provides interfaces between ISA and EISA bus, host bus, and the ISP; includes clock generator, address butter control data butter control and reset control.
82359 DRAM Controller (DRC) 18	Provides two independent address paths to DRAM; also provides address control, refresh generation, critical DRAM timing generation; with the ADP, provides dual-ported data path system/host data bus and the DRAM data bus.
Diskette drive controller 40	Intel N82077AA-1, controls up to two diskette drives
BIOS EPROM	27C512 EPROM (64K x 8), contains the "permanent" BIOS
BIOS EEPROM 50	28F512 flash EPROM (128K x 8), contains the CPU-dependent BIOS

Real-time clock 48	Dallas Semiconductor DS1287 (24-pin DIP): MC146818 compatible RTC (includes 50 bytes of ISA CMOS configuration RAM and battery)
Configuration SRAM	DS1225 contains system configuration information (includes battery)
Keyboard/mouse controller 42	Epson 8742
Serial/parallel port driver 44	Western Digital WD16C552JT
DRAM 20	Eight SIMM sockets. Standard configuration is 4 MB on four 256 KB x 36-bit, 72-pin, 70-ns SIMMs, expandable to 128 MB using 1,2, 4, 8, or 16 MB SIMMs

CPU board 12 is typical of a whole series of different CPUs compatible with system 10. CPU board 12 comprises a counter/timer 52, an EPROM 54, an FPA 56, an R3000 type CPU 58, an instruction cache 60, a data cache 62, a data RB 64, an address buffer 66, an R3020 WB 68, a first 512 MB map 70, a snoop address register 72, and a control circuit 74.

System 10 preferably has a diskette drive (3.5 inch or 5.25 inch), 4 MB of main memory 20 expandable to 128 MB, a pair of RS-232C serial ports 44, a parallel port, a PS/2 compatible mouse and keyboard ports, a set of five EISA option slots (that support 8-, 16- and 32-bit option cards) connected to bus 16, and means for supporting up to two diskette drives and up to two IDE hard disk drives. System 10 is such that a user can select from a variety of other processor boards, e.g., those based on the Intel (Santa Clara, CA) i486SX/25, i486DX/33, or i486DX/50. Any of several video controllers from VGA to high-resolution graphics are also useful options.

Fig. 3 shows how the connectors are positioned on the main system board (motherboard) in system 10. Connectors are symbolically labelled "CN" and the SIMM sockets are designated as "U35-U42." Table II lists the major connector available on the motherboard.

TABLE II

Number	Connector	Description
CN1, CN2	Serial ports (two)	9-pin, D-shell (rear panel)
CN3	Parallel port	25-pin, 0-shell (rear panel)
CN4	Diskette drive	Supports up to two diskette drives
CN5	Keyboard port	6-pin mini-DIN (rear panel)

CN6	Mouse port	6-pin mini-DIN (rear panel)
CN7	Speaker	Connects to the ISA speaker on the front panel
CN8	IDE HDD	Supports up to two IDE hard disk drives
CN9-CN13	Option slots (five)	32-bit EISA expansion slots that accept 32-bit EISA bus-master and slave option boards, and 8-bit and 1 &bit ISA option boards
CN14	RESET button and front panel LEDs	Connects the Main System Board to the RESET button, and POWER, HDD and Turbo LEDs on the front panel
CN1 6, CN17	Processor board (two)	Dedicated connectors for the Processor Board
CN18, CN24	Power supply (two)	Connects the power supply to the Main System Board.
CN22		Can be connected to a hard disk controller card installed in an option slot. Allows the front panel HDD LED to show when the hard disk controlled by the card is accessed
CN25	Fan	2-pin connector supplying power to the fan on the rear panel
U35-U42	SIMM sockets	Eight sockets for industry-standard, 36-bit SIMMs

Memory

System 10 has a dual-ported memory architecture, i.e., CPU 12 has its own port into memory (via bus 14 and DRC 18), which is completely separate from the access route from EISA bus 16. System 10 supports bus widths up to 128 bits in order to provide zero-wait burst read at the maximum speed of CPU 12. Memory array 20 is 144 bits wide (128 data bits, with 16 parity bits). A memory system will preferably have the following features: EISA/CPU bus concurrency (set by bit 4 of register 0C08h), zero-wait burst read, zero-wait posted writes (set by bit 1 of register 0C08h), support for shadow RAM, support for shadow RAM,

support for split memory block remapping, and it should be LIMS 4.0 EMS compatible.

System Board I/O

Serial Ports--The serial ports is programmable and suports all standard communication rates from 50 to 19,200 baud. It also provides support of the first-in-first-out (FIFO) mode.

A standard 9-pin male D-shell connector provides the RS-232C interface. Pinouts and signal assignments are shown in Table III.

TABLE III

PIN	I/O	DESCRIPTION
1	I	Data Carrier Detect
2	I	Receive Data
3	O	Transmit Data
4	O	Data Terminal Ready
5	--	Signal Ground
6	I	Data Set Ready
7	I	Signal Ground
8	I	Data Carrier Detect
9	I	Ring Indicator

Parallel Port--The parallel port is compatible with IBM Personal Computer parallel port implementations. The parallel port has an extended mode that supports bidirectional input and output. The parallel port connector is a 25-pin female D-shell connector. Pinouts and signal assignments are shown Table IV. Until Intel fixes a chip design problem of theirs, preferably all input and output pins (pins 1 to 17) are overvoltage protected to protect some of the integrated circuit I/O devices from damage.

TABLE IV

PIN	I/O	DESCRIPTION
1	I/O	-Strobe
2	I/O	Data 0
3	I/O	Data 1
4	I/O	Data 2
5	I/O	Data 3
6	I/O	Data 4
7	I/O	Data 5
8	I/O	Data 6
9	I	Data 7
10	I	-Ack
11	I	Busy
12	I	PE
13	I	SLCT
14	O	-Auto FD XT
15	I	-Error
16	O	-Init
17	O	-Slct In
18-25		Ground

Keyboard and Auxiliary Ports--The Keyboard and Auxiliary interfaces are based on an Intel 8742 micro-controller. The connectors use 6-pin miniature DIN connectors. One connector is dedicated to the Keyboard, the other is available for a pointing device such as mouse, trackball or touchpad. Pinouts and signal assignments are shown in Table V.

TABLE V

PIN	I/O	DESCRIPTION
1	I/O	Data
2		Reserved
3		Ground
4		+5 VDC
5	I/O	Clock
6		Reserved

IDE HDD Interface--The 40-pin header is provided to support up to 2 IDE hard disk drives. Pinouts and signal assignments are shown Table VI.

TABLE VI

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	-Host Reset	2	GND
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	GND	20	Key
21	Reserved	22	GND
23	-Host IOW	24	GND
25	-Host IOR	26	GND
27	Reserved	28	Host ALE
29	Reserved	30	GND
31	Host IRQ14	32	-Host IO16
33	Host ADDR 1	34	Host PDIAG
35	Host ADDR 0	36	Host Addr 2
37	-Host CSO	38	-Host CS1
39	-Host SLV/ACT	40	GND

Floppy Disk Interface--The floppy disk controller are based on Intel 82077. The 34-pin header provides interface-signal sequences and timings are compatible with the industry standard 3.5-inch and 5.25-inch floppy drive interface. The following Table VIIshows the signals for the floppy interface pinouts.

TABLE VII

PIN NO.	SIGNAL	PIN NO.	SIGNAL
ODD PINS	Ground	18	-Direction
2	-RWC	20	-Step
4	RESERVED	22	-Write Data
6	RESERVED	24	-Write Enable
8	-Index	26	-Track 0
10	-Motor Enable 0	28	-Write Protect
12	-Drive Select 1	30	-Read Data
14	-Drive Select 0	32	-Head 1 Select
16	-Motor Enable 1	34	-Diskette Change

Speaker--The speaker circuitry provides four discrete levels, one of which is inaudible (speaker off) level. The volume levels is software selectable. Pinouts are shown in Table VIII.

TABLE VIII

PIN	SIGNAL
1	Speaker
2	NC
3	NC
4	GND

Concurrency

The software may enable the memory system to run in one of two modes: Concurrent mode, and Non-concurrent mode. The mode is selected by programming Mode Register C, bit 0 appropriately.

In CONCURRENT mode, EISA masters can run system bus cycles independently of the ownership of the main memory. A CPU may run cycles to main memory without ownership of the EISA bus. In concurrent mode, any EISA bus master can use EISA bus 16 regardless of who owns main memory 20. Similarly, CPU 12 can access main memory 20 without acquiring ownership of EISA bus 16. In non-concurrent mode, EISA bus masters can only run cycles when they own both EISA bus 16 and main memory 20. CPU 12 can only execute cycles when it owns both main memory 20 and EISA bus 16. A memory map is shown in Table IX.

TABLE IX

FFFFFFFFh	Permanent BIOS ROM: 64 KB	4 GB
FFFFO000Oh 00OEO000Oh	Not Accessible	128 MB Max Sys.
00100000h	Extended Memory (on System Board or option Boards)	1 MB
000E0000h	CPU-dependent BIOS: 128 KB	
000C8000h	Available	
000C0000h	VGA BIOS (Shadow RAM)	
000B0000h	Video memory: 64 KB (MDA or CGA)	
000A0000h	Video memory: 64 KB (EGA or VGA)	640 KB
0000000h	Conventional System Memory: 640 KB	

Note: System 10 memory may be limited to 128 MB by the maximum size of SIMM currently available (16 Ms). 32-MB SIMMs are preferably supported, but such devices may not be immediately available. The maximum system memory is at least 256 MB.

The areas of memory used for video memory and BIOS depend on the type of video controller installed.

In NON-CONCURRENT mode, the EISA bus and main memory become one resource. This requires that EISA master cycles can be run only after the EISA master has gained ownership of the EISA bus AND main memory. Likewise, CPU cycles must gain ownership of the EISA bus regardless of the cycle's destination. This mode is advisable in a system which incoporates the Austek A38403 Cache Controller. Since the A38403 can only perform snoops when in a "Hold" condition.

Installing memory

The main circuit board (motherboard) has eight SIMM sockets, each of which are divided into two banks. A bank 0 comprises SIMM sockets U35, U37, U38 and U39. A bank 1 comprises SIMM sockets U36, U40, U41

and U42. Logically, each bank is made up of rows. Bank 0 has rows 0 and 1. Bank 1 has rows 2 and 3. Each row is independent, even though they may be physically made up of the same sockets. The SIMMs should preferably be 70 ns, 36-bit fast-page-mode SIMMs (36-bit SIMMs use 32 bits for data and 4 bits for parity). Table X shows this more graphically.

TABLE X

SIMM size (MB)	DESCRIPTION	size per row (MB)
1	single-sided, 256 K x 36	1
2	double-sided, 256 K x 36	1
4	single-sided,1M x 36	4
8	double-sided, 1M x 36	4
16	single-sided, 4M x 36	16
32	double-sided, 4M x 36	16

If the SIMM configuration is changed, a system configuration program (utility) should be used to display to the user the amount of memory recognized, and it should indicate if the combination is allowable. Table XI shows some exemplary SIMM configurations.

TABLE XI

Total Mem	**Bank 0**				**Bank 1**			
(MB)	U35	U37	U38	U39	U36	U40	U41	U42
4	1	1	1	1				
5	1	1	1	1	1			
6	1	1	1	1	2			
8	1	1	1	1	4			
12	1	1	1	1	8			
20	1	1	1	1	16			
24	8	8	8					
32	8	8	8	8				4
40	8	8	8	8	2	2	2	2
	8	8	8	8	4	4		
48	16	16			16	16		
	16	16			8	8	8	8
80	16	16	16	16	16			
96	16	16	16	16	16	16		
128	16	16	16	16	16	16	16	16

Configuration Registers

A set of configuration registers, beyond the standard I/O registers needed for an EISA system, are used to control various features of system 10. The registers are set during system initialization by the BIOS program. The registers can later be dynamically changed under software control, if need be. The only software that would normally modify the configuration registers is a specially invoked system configuration program.

Register: 0C08h (Read/Write)

Register 0C08h is used to set up the way memory is used, to enable/disable disk drive interfaces and to indicate the type of monitor being used.

Bit 0: Reserved

Bit 1: Posted write

0 = Enabled

1 = Disabled

Bit 2: On-board IDE interface

0 = Enabled

1 = Disabled

Bit 3: Color/Monochrome monitor

0 = Color

1 = Monochrome

Bit 4: Concurrent mode

0 = Disabled

1 = Enabled

Bit 5: External diskette drive

0 = Disabled

1 = Enabled

Bit 6: Write-back Cache

0 = Disabled

1 = Enabled

Bit 7: Long wait between I/O cycles

0 = Enabled

1 = Disabled

Register: 0C09h CPU Type and

Main System Board Revision (read-only)

Register 0C07h indicates the type of processor board installed and the revision level of the Main System board.

Bits 0-5: Processor board

000001 = i486DX/50 with 256 KB cache
000010 = reserved
000011 = reserved
000100 = i386DX with 16 KB cache
001100 = i486DX with 64 KB cache
010000 = i486SX/20 with 8 KB cache
010001 = i486SX/25 with 8 KB cache
010010 = i486DX/50 with 8 KB cache
Bits 6-7: Main System Board revision

Register: 0C0Ah Speaker Volume and Flash Memory (Write-only)

Register 0C08h is used to set speaker volume, and to enable or disable the flash memory program and write.

Bits 0-1: Speaker volume
00 = HIGH
01 = Medium
10 = LOW
11 = Off
Bit 2: Flash memory program
0 = Disable
1 = Enable
Bit 3: Flash memory write
1 = Disable
0 = Enable
Bits 4-5: Reserved
Bits 6-7: Not used

Processor Boards

System 10 is compatible with several different processor boards, such as processor board 12. For example, it is compatible with an Intel i486DX-based processor board 200 (Fig. 7) having a 50 MHz CPU clock, an i486DX-based processor board 300 (Fig. 8) with a 33 MHz CPU clock, an i486SX-based processor board 400 (Fig. 9) using 20, 25, or 50 MHz CPU clocks, an i486DX-based processor board 500 (Fig. 10) with a 50 MHz CPU clock and discrete implementation of a cache, and the MIPS RISC-based processor board 12 (Fig. 1). Besides the variety of speeds, there is a variety of machine codes that are needed to support the CPUs on these boards.

It would, on first inspection, appear to make sense to include the CPU boot (referred to elsewhere as the "permanent BIOS") and BIOS firmware needed for each processor board on the processor board itself. But the architecture of system 10, which must conform in part to an architecture

made popular by IBM Corporation in its line of personal computers, is such that the BIOS ROM must reside on Xbus 39. A connection of processor board 12, for example, to Xbus 39 would be necessary if BIOS 50 were to be located on the printed circuit card for processor board 12. Many pins would be necessary, and more room would be needed.

System 10 therefore locates the BIOS firmware on the motherboard in a flash memory 50 so that it can be field updated (downloaded) from a floppy disk. This is preferable to updating by swapping out memory 50 physically, because the user is usually left to do this, and typical users are not skilled in such technical procedures. The downloadable BIOS and hardware system ID are described below.

Processor board 200, Fig. 5, uses a 50 MHz Intel i486DX CPU-cache module 202 which has an internal 8 KB cache 206 and a 82495DX cache controller 208. The cache 206 uses nine Intel C8 cache RAM chips to form a 256 KB cache. A state machine 209, called a programmable state tracker (PST), comprises a control logic 210 and an address modifier 212. The state machine PST 209 does a two-way simultaneous translation between the CPU pin out and system bus 14. Edge card connectors plug into the main system bus 14.

PST 209, Fig. 6, is preferably implemented with several programmable logic arrays (PALs) rated at better than ten nanoseconds propagation delay. PALs are particularly attractive since they can be easily programmed from Boolean equations and since manufacturers like Intel make frequent changes to the published and actual microcomputer CPU timing characteristics. The use of combinatorial logic inputting or on the outputs of PST 209 is avoided due to the delays and signal skewing that would be introduced. Signals therefore transition PST 209 in substantially one device delay time. Another way of describing PST 209 is that it is a flat, single-level logic network. Such a flat architecture is not quite as crucial at CPU speeds below 50 MHz and host bus speeds below 66 MHz, because the timing delays constitute a lesser significant portion of each CPU or bus cycle, for common device propagation times. A clock driver 213 generates the timing on PST 209. The functional blocks of Fig. 6 are distributed amongst several discrete PALs on the basis of space availability. The following therefore discusses the function rather that a particular PAL. A synchronizer 221 pseudo-synchronizes CPU 202 to bus 14. Snoop control 217 and arbitrator 220 are thus synchronized. A strobe detector 215 is responsive to a cycle counter 219 and triggers snoop controller 217. A host address strobe (HAS) controller 222 issues bus 14

compatible signals when the arbiter 220 indicates bus 14 has been acquired. The configuration control 226 is coupled to both CPU 202 and bus 14. Deterministic and non-deterministic cycles are tracked by units 214 and 218 and signal ready generator 224.

Since the CPU module 202 can operate at 50 MHz and bus 14 can run as high as 66 MHz, a difference of a few nanoseconds in the interfacing of PST 209 between them can make a big difference. Therefore, the PALs used should be the same type, and it may be necessary for them to be from the same manufacturer's batch number, or at least matched. Clock driver 213 is a National 74B2525, or equivalent. Driver 213 is special in that it will produce several simultaneous, buffered clock outputs from a single clock input. The timing derived from these clocks are so critical, on PST 209, that the trace lengths between clock driver 213 and PALs 214-226 should be adjusted such that the clocks arrive at each PAL at practically the same time.

Processor board 300, Fig. 8, uses the Intel i486DX processor 302 which has an internal 8 KB cache. The board also includes a Intel 82485M Turbocache module 308 that contains both 128 KB of cache memory and the necessary cache controller. The performance can be enhanced by installing a Weitek WTL4167 coprocessor 304. A socket is provided for it to be added later by the user. The WTL4167 offers high speed performance. Edge card connectors plug into the main system bus 14.

Processor board 400, Fig. 9, uses the i486SX processor 402 which has an internal 8 KB cache. The performance can be enhanced by installing either a Weitek WTL4167 coprocessor 406 or an Intel i487SX coprocessor 404. Sockets are provided for both. The WTL4167 offers high speed performance, and the i487SX coprocessor offers the user economy. Edge card connectors plug into the main system bus 14.

MIPS RISC-Based Processor Board

The MIPS RISC-BASED processor board 12 can also plug in to the standard CPU bus connector of system 10, see Fig. 1. Processor board 12 can be a "server" system, which is able to run RISC OS. Preferably, it is configured to be readily convertible into an ARC-compliant system with minor changes in its configuration.

Processor board comprises an R3000 RISC CPU 58 and an R3010 FPU 56, configurable instruction and data caches 60 and 62 for up to 256KB each, an eight-word write buffer 68, and a read buffer 64. A means for full R3000 block refill and streaming support, a cache invalidation snooper to assist in maintaining cache coherency, means for fully utilizing

the burst data transfer capability of the system 10 motherboard are all contained in block 74. The architecture is an ARC-compatible structure, with bi-endian capability. ("Endian" refers to whether the more significant bytes in a longword are stored at higher or lower byte addresses inm the system memory.) The CPU Clock is preferably 40 MHz, which will deliver 43 VAX Mips performance. A local bus extension connector is used to support Graphic, SCSI, etc. Processor board 12 further comprises a one megabyte EPROM memory with 32-bit data width.

Burst Cycles--The Intel i486 CPU can accept burst cycles for any bus requests that require more than a single data cycle. The fastest burst cycle requires two clocks for the first data item, with subsequent data items returned every clock thereafter. The i486 cannot burst multiple 32-bit writes within a single burst cycle.

Burst cycles begin by asserting an ADS* signal. If BLAST* is sampled as being inactive at the next clock, then the i486 is able to do a burst cycle. The external system indicates its ability to do a burst cycle by returning a burst ready signal BRDY* active.

The addresses of the data items in a burst cycle will all fall within the same 16-byte aligned area (corresponding to an internal i486 cache line). It begins at location XXXXXXX0, and ends at location XXXXXXXF. During a burst cycle, only BE0*-3*, A2, and A3 may change. Signals A4-A31, M/IO*, D/C*, and R/W* will remain stable throughout a burst. Given the first address in a burst (lead-off cycle), the external hardware can easily calculate the address of subsequent transfers in advance. In system 10, during host read sequences, the 82359/82353s will latch each of the 32-bit words in the entire row being accessed, for a total of sixteen bytes. The SEL(1:0) bits tell the 82353s which of the latched words should be sent to the host. Should the host cycle be a burst, the remaining sequence of words is known by the 82353s based on IF(1:0) (since the i486 burst sequence is fixed, determined by the lead-off address). The burst ordering is as follows.

First Address	Second Address	Third Address	Fourth Address
0	4	8	C
4	0	C	8
8	C	0	4
C	8	4	0

R3000A--Block transfer or block refill is further divided into the two cases, stall refill and run refill. Stall refill, or simply refill, occurs while the processor is in a non-run state, e.g., instructions are not being executed.

Run refill or streaming, so called because processing is occurring on a data stream from memory, occurs while the processor is in the run state. The R3000 supports refill for both instructions and data and streaming on instructions only. During block refill, the AdrLo bus can be divided into two parts, AdrLo(17:k) and AdrLo(k-1:0). (Where k is log based 2 of the block size in bytes, e.g., k equals to 4 for a block size of 16 bytes.) AdrLo(17:k) is held constant during the entire memory read stall. The address presented on AdrLo(k-1:0) is forced to the missed address during the first stall cycle. On subsequent stall cycles, its value is dependent on the state of CpCond(0) during the previous cycle, e.g., the address presented is either the missed address or the start of block address.

The processor expects the memory system to return the block of words sequentially beginning with word zero and proceeding to word n-1 where n is the block size. This ordering is expected regardless of the original miss address. The processor will pick up the data corresponding to the actual miss address and present that data during the fix-up cycle for the purpose of restarting the instruction pipeline.

PR3400 & PR3100--The PR3400 is an integrated advanced R3000A CPU and R3010A FPU in a monolithic VLSI package, and is commercially available at 40 MHz. The PR3400 features an on-chip clock generation unit and a programmable FPA/CPU interrupt connection.

The PR3100A is a single-chip write/read buffer designed to support the PR3000A RISC microprocessor. The PR3100A features an 8-word write buffer with a byte-gathering and readback capability. It has a read buffer with a programmable depth of up to 32 words. and it supports bus snooping to assist in maintaining cache coherency.

Memory Latency Analysis--Assuming PR3100A's block transfer, using 82353s/82359's burst of 4 words (or 4-word deep read buffer), a pagehit at 40 MHz, a page miss and refresh cycles are negligible, the following is distilled:

RdMem* to HAS*	3CLK x 25 ns	75 ns
HAS* to first word valid	24.61+20+9+12.5	66 ns
Burst of 4 words	4CLK x 25 ns	100 ns
PR3100A Latency	2CLK x 25 ns	50 ns
	Total	291 ns

Bandwidth/Transfer Rate: 16 Bytes/291 ns = 55 MBytes/S

Note: If NOT implementing burst/block transfer, then the actual transfer rate would be: 4 Bytes/191 ns = 21 MBytes/s

Timing Equations for Cache Design--Assuming the use of generic SRAMs (without built-in latches), all calculations are based on specifications published for the 40 MHz R3400A. The SRAMs are 16K x 4 IDT7198. An 74FCT373CT is used with a t_{PD} = 4.2 ns. (The superscript 'd', in the following equations, denotes deratings to be taken into account, e.g., capacitive loading and trace delays.

Phase Delays for PR3440

t_{Rd} = [2.40, 2.60];
t_{Smp} = [3.00, 3.25];
t_{Sys} = [6.00, 6.50];
$t_{Sys\text{-}Smp}$ = [3.00, 3.25];
$t_{Sys\text{-}Rd}$ = [3.60, 3.90];

RAM Address Access Time

$$t_{RAMAA} \leq t_{Cyc} - t_{Smp} - t_{DS} - t_{373PD} - t_{AdrLo}{}^{d} - t_{RAMAA}{}^{d}$$
$$25 - 3.25 - 4 - 4.2 - 2 - 2$$
$$t_{RAMAA} \leq 9.55 \text{ ns}$$

Cache Enable to Sample

$$t_{OES} \leq t_{Cyc/2} - t_{RD}{}^{d} - t_{DS} - t_{Sys\text{-}Smp} + t_{Sys\text{-}Rd} - t_{OES}{}^{d}$$
$$12.5 - 2 - 4 - 3.25 + 3.6 - 2$$
$$t_{OES} \leq 4.45 \text{ ns}$$

Minimum Read Pulse Width

$$t_{OES} \leq t_{Cyc/2} - t_{Sys\text{-}Rd} - t_{OES}{}^{d}$$
$$12.5 - 3.6 - 2$$
$$t_{OES} \leq 6.9 \text{ ns}$$

Read-Write I-Cache Data Bus Contention

$$t_{RAMHZ} \leq t_{Sys} - t_{Rd}{}^{d} + t_{DEn}$$
$$6.5 - 2.4 + (-1)$$
$$t_{RAMHZ} \leq 4.1 \text{ ns}$$

Processor Data-Setup to End of Write

$$t_{RAMDs} \leq t_{Cyc/2} - t_{Sys\text{-}Smp} - t_{DVal} - t_{DVal}{}^{d} - t_{Wr}{}^{d}$$
$$12.5 - 3.25 - 2 - 2 - (-1)$$
$$t_{RAMDS} \leq 6.25 \text{ ns}$$

Processor board 12 and the system 10 motherboard use a number of signals that have been labelled symbolically. The following definitions are a partial list of the signals used in system 10, and the discussion of each is intended to give the reader some insight into to functioning of the system and the interplay between its major components. A "[O]" indicates an output, and a "[I]" indicates an input for the respective devices.

PST and 82359 Memory Controller

HAS* [O]. Host Address Strobe. Output from the PST logic. The falling edge start a bus cycle ad indicates the address ad status are valid on the

bus. Rising edge indicates the completion of a bus cycle. If MACK* is currently asserted, the falling edge of HAS* is used to guest the bus.

HBURST* [I]. Host Bunt. Output from memory controller to Indicate the current cycle is capable of a bunt type cycle. length is Bed in the hardware (2,4,8, or IQ. Should be ignored in the lead off cycle if HARDY is LOW, and should not be acknowledged until HARDY returns HIGH. HBURST* then remains valid until HAS* is negated.

BlHARDY [I]. Asynchronous Ready. Driven LOW by the memory controller to indicate a NOT ready condition to the PST. Needs sufficient address decoding time before sampling the falling edge. PST samples the rising edge asynchronously to complete a cycle. HARDY (B1HARDY # B2HARDY) is used to indicate the completion of each burst cycle.

HKEN* [I]. Host Cache Enable. Output of the 82359 to indicate the current host bus cycle is cacheable. Unused in a simple RISC CPU-based design.

HWP** [I]. Host Write Protect. Output of the 82359 to indicate the current host bus cycle is write protected. Unused in simple RISC CPU-based design.

CYCLN(2:0) [I]. Cycle length. Output of the 82359 to indicate the length of the lead-off bus cycle. If HARDY is sampled LOW in the lead-off bus cycle, then the CYCLN(2:0) is undefined and the rising edge of the HARDY should be used to terminate the cycle. If the HARDY stays HIGH in the lead-off bus cycle, the CYCLN(2:0) are valid until HAS* is negated.

PAGEHIT* [1]. DRAM Page Hit indicator to the PST. The PST will sample PAGEHlT* after it is guaranteed to be valid. If PAGEHlT* is asserted, the PST knows to run a page hit cycle and CYCLN(2:0) can be ignored. Otherwise, CYCLN(2:0) must be used to determine the wait state count.

IF(1 :0) [1]. Interleave Factor. Outputs of the 82359 to indicate the word interleave organization of the memory row being accessed. If HARDY is sampled low in the lead-off bus cycle, IF(1:0) are undefined until the rising edge of HARDY.

IF(1:0) Memory Interleave Factor

0 0	4-way
O 1	2-way
1 0	1-way
1 1	System Bus Access (Non-deterministic)

SPEED(1:0) [1]. DRAM Speed. Outputs of the 82359, this information is used by the PST conjunction with IF(1;0) to determine the number of CPU clocks for each burst cycle data transfer.

ST* [O]. Start (Continue) Host Cycle. For parallel cache design. Should be grounded.

82353 Data Path Device

HCLKI.3 [O]. Host Clock Output that is used by the 82353s. The 82358 EBC uses this clock in synchronous mode only. In a simple RISC CPU-based design, the SYSOUT3 (25 MHz) is buffered and becomes HCLKI.3.

HOE* [O]. Host Bus Enable. Driven active LOW by the PST to enable data from data path device (82353) onto the host data bus.

HWCLKEN* [O]. Host Write Clock Enable. Driven active LOW by the PST to enable write data latching from the host CPU to the data path device. Data is latched on the rising edge of the data path device input clock when HWCLKEN* is active.

B2HARDY [1]. It is used in Host-to-System burst read cycles to indicate to the PST that the valid data is available from the system with its rising edge. This 82353's B2HARDY and the 82359's HARDY are typically "OR'ed" together. The 82359's HARDY determines the state of HARDY for the Host-to-System single dword cycles and the lead-off access of a Host-to-System burst cycle. The 82353 generates the B2HARDY for the subsequent cycles of the Host-to-System burst.

HBRDY* [O]. Host Burst Ready. HBRDY* is sampled by the 82353 on the rising edge of HCLK and indicates when host is ready for the word of a burst read cycle. It is generated by the non-deterministic cycle tracker PAL of the PST logic. This signal also becomes the i486 HBRDY* input.

HINTPAR [O]. Host Internal Parity Select. If HINTPAR is LOW at reset time, Standard mode is selected. Also HINTPAR=HIGH means that the 82353s will generate and check the parity instead of the host. In a simple RISC CPU-based design, this signal should be LOW at RSTCPU falling edge and HIGH afterward.

82358 EISA Bus Controller

33/25* [0]. Host Frequency Select. In a simple RISC CPU-based design, this signal is grounded to indicate to the EISA Bus Controller 82358's CPU(0) input that the host frequency is 25MHz.

386/i486* [0]. CPU type. In a simple RISC CPU-based design, this signal is grounded to indicate to the 82358's CPU(1) input that the CPU type is i486-like.

HCLKI/2X* [O]. This pin is trapped to indicate the type of clock being used. When trapped HIGH, the HCLK input is 1x the operating frequency of the 82353, TTL clock level is expected, and the HRST input is asynchronous. It also becomes the CPU(2) input to the 82358 EISA Bus Controller). Should be NC (no connection) for a simple RISC CPU-based design since this signal is pull up to 10 kilohm on the system 10.

ASYNC/SYNC* [O]. Should be NC for a simple RISC CPU-based design since the 82358's clock source is the on-board 25MHz.

HSTRETCH* [O]. Host Bus Stretch. Use by host bus slave during EISA/ISA bus master cycles and DMA cycles to stretch the low part of the BCLK during CMD# phase. Should be pulled up.

MSBURST* [I]. I/O pin of 82358's Master Burst I/O. Indicating a Master or DMA burst cycle. In i486 design, it is used for Cache Controller with write back capability, e.g. Austek. Should be NC.

SYS_DDIS [O]. System DRAM disable. Use for write back only. Should be connected to GND.

Bus Arbitration

MREQ [I]. Memory Request. Generated by the 82359 bus arbitration logic to request the use of memory. When MREQ is asserted, the strobe bus controller must assert MACK after it has completed any pending bus cycle. After MREQ* has been acknowledged with MACK, no strobed bus cycle can be completed until MREQ has been sampled LOW.

MACK [O]. Memory Acknowledge. The rising edge is generated by the PST to the 82359 when the PST has acknowledged that it can not complete further strobe bus cycle. The PST can initiate another strobe bus cycle by activating HAS*. However, the cycle is frozen until both MREQ and MACK are de-asserted. In this case, the falling edge of MACK is used as a cycle start indicator similar to the behavior of HAS* falling edge.

SNUPRQ Snoop Request. The 82359 asserts this signal to request a cache invalidation cycle. SNUPRQ is negated from the falling edge of SNUPACK* if there are no further snoop cycles present.

SNUPACK* [O]. Snoop Acknowledge. The PST asserts this signal back to the 82359 when the CPU has tri-stated the host bus. The 82359 can use the active level of SNUPACK* as an output enable for the host address and status bus.

82351 Local I/O EISA Support

NPERROR* [0]. Numeric Coprocessor Error. Should be pulled up.

NPBUSY* [O]. Numeric Coprocessor Busy. Should be LOW during reset for i486-like and HIGH afterward.

NPPEREQ* [O]. Numeric Coprocessor Extension Request. Should be connected to GND.

NPCYCLE* [O]. Numeric Coprocessor Cycle Active. Should be pulled up.

CPUREQ [I]. CPUPEREQ. CPU Extension Request. Should be NC.

IGNNE* [I]. CPU Busy. Should be NC.

LIOFLUSH* [I]. LIOE Cache Flush. Should be NC.

i486-Processor Like Signals

HM/IO* + HD/C* + HW/R*

[O]. These are the i486-like primary bus cycle definition signals.

M/IO*	D/C*	W/R*	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Halt/Special Cycle
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Code Read
1	0	1	Reserved
1	1	0	Memory Read
1	1	1	Memory Write

HA(31:2) [O]. Host Address Bus.

BE*(3:0) [O]. Host Byte Enable indicate active byte during read/write cycles. As Little-Endian arrangement, BE* (3) applies to HD(31:24), BE*(2) applies to HD(23:16), BE*(1) applies to HD(15:8), and BE*(0) applies to HD(7:0).

HD(31:0) [I/O]. Host Data Bus.

HPD(3:0) [I/O]. Host Parity. Not used in a simple RISC CPU-based design. Parity logic must be disabled by both hardware and software.

A20M* [I]. This signal is Intel CPU specific. When asserted, it puts the CPU in real mode, masking the physical address bit A20. Should be NC.

CPUINTR [I] CPU Maskable Interrupt. Should be connected to UINTO.

NMI [I]. Non-maskable Interrupt. Parity error does cause the NMI. Should connect to IP4 as a status.

HLOCK* [O]. Host lock. From i486 to indicate that the current bus cycle is a locked cycle. It is equivalent to read-modify-write. Assertion of this signal makes the 82359 arbitrate for and obtain the system bus

ownership before the 82359 runs the host cycle, regardless of the destination of that cycle. Locked cycles are always run as non-deterministic cycles.

FLUSH* [I]. i486 Cache Flush. From 82359's (DEN* & SW/R*) to indicate a i486-initiated cache flush cycle. Actual equation at input of i486 is:

!CPUFLUSHn.d= !RSTCPU & !SLOWHn # !FLUSHn # LIOFLUSHn;

PCD [O]. Page Cache Disable. From i486 is used by the 82359 in determining the cacheability of addresses.

General Signals

WTLPRES* [O]. Weitek Coprocessor present. Should be NC.

WTLINT [O]. Weitek Interrupt.

RSTCPU [I]. Reset signal for CPU. Simple RISC CPU-based's reset signal is an OR function of this signal and the MRes* from the evaluation board.

SRST [O]. System Reset. For reset synchronization of RSTCPU from system 10 platform and the rest of the system. Use active-high of the ORed reset signal for this.

WRBACK [I]. Write Back. Should be NC.

ESNPRQ [I]. Should be NC.

SLOWH [I]. Slow Down Host CPU. From the 82357 ISP's CPU slow down timer (timer/counter 2) to slow down the CPU via its HOLD pin. After first read is done to I/O register in the 48h- 4Bh range. Should be NC. However, look closely in Processor board 12 design. Why, in the i486 design, {!SLOWHn & !CPURST} is used to flush the internal cache

MPCHK* [O]. Parity Check. Generated by i486's {HM/IO & !PCHK*}. Should be pulled up.

SID(5:0) [O]. CPU ID.

Address Map:

TABLE XII

ADDRESS RANGE	Device Accessed	Size	Total
0000 0000-0001 FFFF	Idt SRAM	128K	128K
0002 0000-07FF FFFF	system 10 DRAM	Configur-able	128M
0800 0000-1EFF FFFF	None	NA	368M
1F00 0000-1F00 FFFF	I/O Space	64K	64K

1F01 0000-1FO1 FFFF	Interrupt Acknowledge	1	64K
1F80 0000-1F80 FFFF	Timer	64K	64K
1FA0 0000-1FA0 FFFF	Reserved (UCSlA*)	64K	64K
1FA2 0000-1FA2 FFFF	Reserved (UCS1B*)	64K	64K
1FA4 0000-lFA4 FFFF	Reserved (UCS1C*)	64K	64K
1FA6 0000-1FA6 FFFF	Reserved (UCS1D*)	64K	64K
1FC0 0000-1FC1 FFFF	Idt EPROM	128K	128K
2000 0000-FFFF FFFF	Unmapped	NA	3684M

Interrupt Assignments:

INTERRUPT LEVEL	Used for
INTO	User interrupt from system 10
INT1	R3010 FPA
INT2	not used
INT3	8254 timer
INT4	8254 timer
INT5	68681 UART

Access Truth Table:

TABLE XIII

IDT 7RS382 RELATED				SYSTEM 10 RELATED				
Address Range	PMRd*	WE*	AccTyp	M/IO*	D/C*	W/R*	BE*	Note
00000000-0001FFFF	X	XXXX	XXX	Z	Z	Z	HHHH	[1]
00020000-0FFFFFFF	L	HHHH	LXX	H	H	L	LLLL	[2]
00020000-0FFFFFFF	L	HHHH	HXL	H	H	L	LLLL	[2]
00020000-0FFFFFFF	L	HHHH	HXH	H	L	L	LLLL	[3]
00020000-0FFFFFFF	H	HHHL	XXX	H	H	H	LHHH	[4]
00020000-0FFFFFFF	H	HHLH	XXX	H	H	H	HLHH	[4]
00020000-0FFFFFFF	H	HLHH	XXX	H	H	H	HHLH	[4]
00020000-0FFFFFFF	H	LHHH	XXX	H	H	H	HHHL	[4]
00020000-0FFFFFFF	H	HHLL	XXX	H	H	H	LLHH	[5]
00020000-0FFFFFFF	H	LLHH	XXX	H	H	H	HHLL	[5]
00020000-0FFFFFFF	H	HLLL	XXX	H	H	H	LLLH	[6]

00020000-0FFFFFFF	H	LLLH	XXX	H	H	H	HLLL	[6]
00020000-0FFFFFFF	H	LLLL	XXX	H	H	H	LLLL	[6]
1F000000-1F00FFFF	L	HHHH	XXX	L	H	L	LLLL	[8]
1F000000-1F00FFFF	H	?	XXX	L	H	H	WE* (3:0)	[9]
1F010000-1F01FFFF	L	HHHH	XXX	L	L	L	LLLL	[10]
1F010000-1F01FFFF	H	XXXX	XXX	Z	Z	Z	HHHH	[1]
20000000-FFFFFFFF	X	XXXX	XXX	Z	Z	Z	HHHH	[1]

Notes:

[1] No Translation. Everything is tri-stated.

[2] Memory Read.

[3] Code Read.

[4] Memory Write. Byte.

[5] Memory Write. Haft Word.

[6] Memory Write. Tri-byte.

[7] Memory Write. Word.

[8] I/O Read.

[9] I/O Write. BE* (3:0) = WE*(D:A), respectively.

[10] Interrupt Acknowledge Cycle. Read Only.

H HIGH.

L LOW.

Z HIGH impedance. Tri-stated.

? Unknown value.

X Don't care.

Endian Swap Truth Table:

TABLE XIV

LIT/ BIG*	PMR d*	WE*	BE*	BDEN*	LDEN*
L	L	HHHH	LLLL	LLLL	HHHH
L	H	HHHL	LHHH	HHHL	HHHH
L	H	HHLH	HLHH	HHLH	HHHH
L	H	HLHH	HHLH	HLHH	HHHH
L	H	LHHH	HHHL	LHHH	HHHH
L	H	HHLL	LLHH	HHLL	HHHH
L	H	LLHH	HHLL	LLHH	HHHH
L	H	HLLL	LLLH	HLLL	HHHH
L	H	LLLH	HLLL	LLLH	HHHH
L	H	LLLL	LLLL	LLLL	HHHH
H	L	HHHH	LLLL	HHHH	LLLL
H	H	HHHL	HHHL	HHHH	HHHL
H	H	HHLH	HHLH	HHHH	HHLH
H	H	HLHH	HLHH	HHHH	HLHH
H	H	LHHH	LHHH	HHHH	LHHH
H	H	HHLL	HHLL	HHHH	HHLL

H	H	LLHH	LLHH	HHHH	LLHH
H	H	HLLL	HLLL	HHHH	HLLL
H	H	LLLH	LHHH	HHHH	LLLH
H	H	LLLL	LLLL	HHHH	LLLL

Ready and Acknowledge Signals:

In the PAL equations, the XACK* is asserted one clock earlier than RDY* because the R3000 samples the read data at the next rising edge of SYSOUT3, at which the RDY* is asserted and data is valid. During a post-write cycle, XACK* is asserted immediately with PWRDYO* asserted. Otherwise, it is asserted following the deterministic ready (XDRDY*) or the non-deterministic ready (ARDY*). XACK* is clocked with SYSOUT3 to prevent glitching. PST ready signal (RD*) is asserted independently with either XDRDYO* or ARDYO*. This ready is used as the last ready to negate the pending HAS* signal, thus ends the current cycle. Burst cycle from CPU is NOT supported so there is no burst ready mechanism.

Snoop Cycle:

The widely available Integrated Device Technology (IDT) evaluation board does not have a cache invalidation path. Therefore, no snooping is supported. Even though there is a snoop state machine to do a "fake" snoop acknowledge, if there is a snoop request from the 82359 DRAM Controller, the Block Cache Enable and the Cache Control Register should be programmed so that all system 10 memory is non-cacheable or the KEN* signal will never be asserted. The following initialization will ensure the snoop cycle will never occur:

Cache Controller Register (CCR) bit 0 = "1"

Block Cache Enable Register bit <2:0> = "111b"

DRAM Timing Parameters:

TABLE XV

Register Name	Description	Delay Value	Address	Value
HP1	HAS*/SAS* to memory start delay	2.61 ns	10h	00
HP10	Host write data setup to CASi*	3132 us	10h	00
HP11	Host cycle trigger to SAS* active	52.20 ns	11h	04
P2	RAS* precharge	60.03 ns	13h	
P3	Row address hold from RAS* falling edge	39.15 ns	14h	20
P4	RAS* to CAS* delay	62.64 ns	14h	20
P5	Column address hold from CAS* falling edge	28.71 ns	15h	76
P6	CAS* falling edge to MDS* rising edge	41.76 ns	17h	04

P7	CAS* cycle time	67.86 ns	15h	76
P8	CAS* pulse width for Read	5230 us	16h	42
P9	CAS* pulse width for Write	26.10ns	I6h	42

Disk Drives

The on-board diskette controller 40 supports up to two diskette drives for any of the following combinations: 3.5-inch, 720-KB or 1.4-MB; 5.25-inch, 360-KB or 1.2-MS drives. IDE controller 46 uses an IDE hard disk drive type table in ROM that predefines certain hard disk parameters, e.g., for the 200 millisecond Conner CP3204F. A user can define other hard disk drive parameters using a system configuration program, such the utility mentioned elsewhere. The hard disk drive types supported directly by the ROM are shown below in Table XVI.

TABLE XVI

No.	Type	Cylinder	Head	Sector	Pre-comp	Landing Zone	MB	Drive Name
00	none	installed						
01	ST-506	306	4	17	128	305	10.2	
02	ST-506	615	4	17	300	615	20.4	
03	ST-506	615	6	17	300	615	30.6	
04	ST-506	940	8	17	512	940	62.4	
05	ST-506	940	6	17	512	940	46.8	
06	ST-506	615	4	17		615	20.4	
07	ST-506	462	8	17	256	511	30.7	
08	ST-506	733	5	17		733	30.4	
09	ST-506	900	15	17		901	112.1	
10	ST-506	620	3	17		820	20.4	
11	ST-506	855	5	17		855	35.5	
12	ST-506	855	7	17		655	49.7	
13	ST-506	306	8	17	128	319	20.3	
14	ST-506	733	7	17		733	42.6	
15	Reserved							
16	ST-506	612	4	17	0	663	20.3	
17	ST-506	977	5	17	300	977	40.5	Seagate 94205-51
18	ST-506	977	7	17	977	56.8		
19	ST-506	1024	7	17	512	1023	59.5	
20	ST-506	733	5	17	300	732	30.4	Toshiba MK-133FA
21	ST-506	733	7	17	300	732	42.6	Toshiba MK-134FA
22	ST-506	733	5	17	300	733	30.4	
23	ST-506	306	4	17	0	336	10.2	
24	ST-506	612	4	17	305	663	20.4	
25	ST-506	306	4	17		340	10.2	
26	ST-506	612	4	17		670	20.4	
27	ST-506	698	7	17	300	732	40.6	
28	ST-506	976	5	17	468	977	40.5	
29	ST-506	306	4	17	0	340	10.2	
30	ST-506	611	4	17	306	663	20.4	
31	ST-506	732	7	17	300	732	42.6	
32	ST-506	1023	5	17		1023	42.5	
33	None							
34	None							
35	None							

36	None							
37	None							
38	None							
39	None							
40	None							
41	ESDI	1022	5	34	--	1022	84.8	Seagate 94216-106
42	ESDI	1022	5	36	--	1022	69.8	Seagate 94216-106
43	ST-506	1024	8	17	512	1023	68.0	
44	ESDI	828	10	34	--	828	137.5	Toshiba MK-156F
45	ST-506	1024	5	17	512	1023	42.5	
46	ST-506	615	8	17	128	618	40.8	NEC D5147H
47	None							
48	ST-506	820	6	17	--	820	40.8	Seagate ST251
49	ST-506	830	10	17	--	830	68.9	Toshiba MK56FB
50	ST-506	1024	9	17	--	1023	76.5	Seagate ST4096
51	ESDI	828	7	34	--	828	96.2	Toshiba MK154F
52	ESDI	967	5	36	--	967	85.0	Seagate 94166-101
53	ESDI	967	7	36	--	967	119.0	Seagate 94166-141
54	ESDI	967	9	36	--	967	153.0	CDC 94166-182
55	ESDI	1022	7	34	1022	1022	118.8	Micropolis 1354A
56	ESDI	967	5	34	967	967	80.3	Seagate 94166-101
57	ESDI	967	7	34	967	967	112.4	Seagate 94166-141
58	ESDI	967	9	34	967	967	144.5	Seagate 94166-182
59	IDE	980	5	17	979	979	40.7	Conner CP-344
60	IDE	776	8	33	775	775	100.0	Conner CP-3104
61	IDE	745	4	28	744	744	40.7	Miniscribe 8051A

BIOS

System 10 has a BIOS program in memory 50 that is similar to that used in Epson EISA Series computers, but without the VGA BIOS. The BIOS preferably conforms to the EISA Committee specification, revision 3.1. (This specification is publicly available and is well-known.) The BIOS (for Intel type processors) supports substantially all applications that can run on an IBM PC/XT/AT system, and it supports substantially all EISA options cards.

The BIOS is divided into two parts, a "permanent" BIOS and a CPU-dependent BIOS. Table XVII compares the two.

TABLE XVII

	Permanent BIOS	CPU-dependent BIOS
Size(KB)	64	64
Address	FFFF0000h— FFFFFFFFh	000F0000h — 000FFFFFh
Stored in	EPROM	Flash ROM
Function	Checks for correct CPU-dependent BIOS at power-on and loads one if necessary	Interfaces I/O on system 10 to the disk operating system.

A downloadable BIOS architecture is used that allows an operator to update the system BIOS by loading a BIOS binary file from a floppy diskette. This function is needed when different types of CPU cards share a common EISA bus motherboard. The BIOS for a new CPU card can be loaded by floppy diskette when that CPU card is used to replace an original one. Field service can resolve compatibility problems or update system BIOS versions by loading a new BIOS from floppy diskette, instead of using BIOS EPROM replacements which may require opening up the system chassis and reaches the BIOS EPROM to replace it.

Due to the downloadable BIOS feature design, the BIOS for system 10 is split into two separate parts. One part, referred to as the permanent BIOS, resides at physical addresses FFFFOOOOh to FFFFFFFFh. The other part, referred to below as the CPU-dependent BIOS, is at FOOOOh to FFFFFh. The permanent BIOS uses an EPROM device (e.g., ROM 51 in Fig. 2) and the CPU-dependent BIOS is FLASH memory device (e.g., flash 50 in Fig. 2). A principal function of the permanent BIOS is to execute a downloading routine which can transfer a BIOS binary file on a floppy diskette to the CPU-dependent BIOS. The CPU-dependent BIOS is conventional and interfaces between the system 10 hardware system and the disk operating system. The permanent BIOS code is just that, permanent, while the CPU-dependent BIOS code may change in response to using one CPU card as opposed to another. Not all of the address space in the permanent BIOS area is enabled at any one time.

The edge connector of each type of processor board has several dedicated pins strapped to ground or Vcc according to a predefined code. The host bus 14 will therefore reflect these codes when a processor board is installed. Since these signal lines are hard-wired, they can be used directly on some of the higher order address lines of the ROM containing the

permanent BIOS to select a permanent BIOS machine code sequence that will be compatible with the particular processor board installed. The size of the individual permanent BIOS programs is relatively small, compared to the storage capacity of modern EPROMs, so one EPROM 51 can simultaneously accommodate several permanent BIOS programs in their respective machine code formats.

At system power-on, the CPU will begin executing instructions from the permanent BIOS. It will determine if loading BIOS file from floppy diskette to the CPU-dependent BIOS will be necessary. The permanent BIOS execute a loading sub-routine if one of following conditions exits:

the CPU card ID (I/O port reading) doesn't correspond to the ID (fixed location) on the CPU-dependent BIOS;

a valid RTC CMOS flag, as set by user through the system configuration utility, indicates that the user wants to update the CPU-dependent BIOS; or

a CPU-dependent BIOS checksum error occurs.

The permanent BIOS will continue executing and initialize a minimum required 256 Kbytes of memory, video, keyboard and floppy hardware devices, before the loading of a new BIOS binary file from the floppy diskette to the 1MB flash memory. If the permanent BIOS finds that the CPU-dependent BIOS loading is not necessary after power-on, it will transfer to the CPU-dependent BIOS and do a conventional EISA power-on procedure.

The real time clock (RTC) 48 CMOS address 1Eh and bit 7 of address 1Fh are dedicated to the enabling of the downloadable BIOS function by the configuration utility. When user enables the downloadable BIOS feature under the configuration Utility, the Configuration Utility will set RTC 48 address 1Eh equal to A5h and bit 7 of address 1Fh equal to one. A system re-boot right after the completion of the system configuration utility will involve the permanent BIOS in the CPU-dependent BIOS loading procedure.

The CPU card identification (ID) is another source which can trigger a loading of the BIOS. The CPU card ID can be read through hardware I/O ports C80h to C83h. The value should correspond to, but need not be the same as the value of the CPU-dependent BIOS locations FFFE7h to FFFEAh. A special ID checksum formula is used on location FFFEBh, as follows:

[FFFEBh] = Not ([FFFE7h]+[FFFESh]#[FFFE9h]+[FFFEAh]) XOR 55h.

The CPU-dependent BIOS ID at locations FFFE7h to FFFBAh is a group ID, instead of an individual ID for each of the several different kind of CPU cards possible, because one CPU-dependent BIOS can usually satisfy the machine code requirements of several different kinds of processor boards. The floppy-based BIOS binary file also uses the same ID for its file name. The permanent BIOS then searches for during the needed ID during the loading procedure. The BIOS binary file is preferably limited to being in the root directory only, since the permanent BIOS would be overburdened to search each sub-directory of floppy for a BIOS file name. For example, a CPU-dependent BIOS ID is defined as follows, Group 1 ID = 4Ch, A3h, 40h, 00h. CPU cards = 486SX/20 Mhz, 486SX/25 MHz, 486DX/33 MHz with C6, 486DX/33 Mhz with Austek. BIOS binary file name, SEC4000.BIO

A CPU-dependent BIOS checksum is tested by the CPU-dependent BIOS. When a bad checksum is found, an error flag is set, and control jumps back to the permanent BIOS to ask the user for the CPU-dependent BIOS updating. The user can decide to load a new BIOS, or can ignore the warning message and continue using the old CPU-dependent BIOS.

EISA Option Card Configuration

A system configuration program can be used to configure EISA option cards. The configuration and slot ID for each card are stored in 8 KB of CMOS RAM, which is battery backed and so, in effect, is non-volatile. At power-on, the BIOS should check the CMOS RAM information against the installed cards and, if the two match, the BIOS initializes the cards.

Switching System Speeds

The BIOS should support three "hot-key" sequences that change the basic clock speed of system 10.

Hot-key sequence	System speed
Ctrl Alt -	simulated 8 MHz
Ctrl Alt •	autospeed (simulated 8 MHz on diskette accesses)
Ctrl Alt +	native processor speed ("Turbo mode")

Note: System 10 speed can also be set by the system configuration program and by an ESPEED utility, described elsewhere.

Power-on Diagnostics (POD)

Before each test, a POD program writes a code that identifies the particular stage of testing (called the step ID) to address 80h, which is the POD step port. If the POD detects a fatal error, it halts system 10 and

sounds an error tone code. If a non-fatal error is detected, the POD sounds an error tone code and/or it displays a warning message on the monitor. If it is possible to continue, a "press Fl to resume" message is displayed and the user must press function key F1 to continue.

5 POD step ID number

TABLE XVIII

Step ID	Error Tone Code	Function
01 h	n/a	60286 register test in progress
02h	1-1-3	8KB & RTC 48 write/read test failure
03h	1-1-4	BIOS ROM checksum test failure
04h	1-2-1	Programmable interval timer test failure
05h	1-2-2	DMA initialization test failure
06h	1-2-3	DMA page register write/read test failure
none	1-3-0	VGA RAMDAC failure
08h	1-3-1	RAM refresh verification failure
09h	n/a	Start of the first 64 KB RAM test
0Ah	1-3-3	First 64 KB RAM chip or data line failure (multi-bit)
0Bh	1-3-4	First 64 KB RAM odd/even logic failure
OCh	1-4-1	First 64 KB RAM address line failure
ODh	1-4-2	First 64 KB RAM parity test failure
0Eh	1-4-3	Failsafe timer test failure
OFh	1-4-4	Software NMI port test failure
10h	2-1-1	First 64 KB RAM or data line failure — bit 0
11h	2-1-2	First 64 KB RAM or data line failure bit 1
12h	2-1-3	First 64 KB RAM or data line failure — bit 2
13h	2-1-4	First 64KB RAM or data line failure - bit 3
14h	2-2-1	First 64 KB RAM or data line failure - bit 4

15h	2-2-2	First 64 KB RAM or data line failure - bit 5
16h	2-2-3	First 64 KB RAM or data line failure — bit 6
17h	2-2-4	First 64 KB RAM or data line failure — bit 7
18h	2-3-1	First 64 KB RAM or data line failure - bit 8
19h	2-3-2	First 64 KB RAM or data line failure — bit 9
1Ah	2-3-3	First 64 KB RAM or data line failure — bit A
1Bh	2-3-4	First 64 KB RAM or data line failure — bit B
1Ch	2-4-1	First 64 KB RAM or data line failure - bit C
1Dh	2-4-2	First 64 KB RAM or data line failure — bit D
1Eh	2-4-3	First 64 KB RAM or data line failure — bit E
1Fh	2-4-4	First 64 KB RAM or data line failure — bit F
20h	3-1-1	Slave DMA register test failure
21h	3-1-2	Master DMA register test failure
22h	3-1-3	Master interrupt mask register test failure
23h	3-1-4	Slave interrupt mask register test failure
25h	n/a	Interrupt vector loading in progress
27h	3-2-4	Keyboard controller test failure
28h	n/a	CMOS power-fail and checksum checks in progress
29h	n/a	CMOS configuration information validation in progress
2Bh	3-3-4	Video memory test failure
2Ch	3-4-1	Display initialization test failure
2Dh	3-4-2	Display retrace test failure

2Eh	n/a	Search for video ROM in progress
30h	n/a	Display believed operable and running with video ROM
31h	n/a	Monochrome display believed operable
32h	n/a	40-column color display believed operable
33h	n/a	60-column color display believed operable
34h	4-2-1	Timer tick interrupt test failure
35h	4-2-2	Shutdown test failure
36h	4-2-3	Gate A20 failure
37h	4-2-4	Unexpected interrupt in protected mode
38h	4-3-1	RAM test failure above address OFFFFh
3Ah	4-3-3	Interval timer channel 2 test failure
3Bh	4-3-4	Time of day clock test failure
3Ch	4-4-1	Serial port test failure
3Dh	4-4-2	Parallel port test failure
3Eh	4-4-3	Coprocessor test failure

POD Screen Error Messages

TABLE XIX

Message	Step ID	Description
No timer tick interrupt	34h	Timer tick failure
Shutdown failure	35h	Shutdown failure
Gate A20 failure	36h	Gate A20 failure
Unexpected interrupt in protected mode	37h	Unexpected interrupt in protected mode
Decreasing available memory	38h	RAM failure above address 0FFFFh
Timer chip counter 2 failed	3Ah	Interval timer channel failure
Time-of-day clock stopped	3Bh	Time couldn't be read

System Configuration Program

A system configuration utility should be included with the system software for system 10, in order to:

view system 10 settings made automatically at power-on;

reconfigure system 10;

configure EISA option cards; and

display information on configuring ISA option cards.

Power-on settings

The system configuration program preferably displays the settings of the following options, which are made automatically by the BIOS at power-on:

the memory size: both internal (SIMMs on the motherboard) and external (memory option cards);

the BIOS version;

the processor type; and

any coprocessor type installed.

Configuring the System

The following options can be set using system configuration program:

TABLE XX

Option	Default	Description
Non-cache areas	None	Up to four blocks of memory addresses can be specified to be excluded from memory caching. For the i486DX/33 Processor Boar with an Intel C6 cache module, or the i486SX Processor Board, the blocks are 16 KB; for the i486DX/33 board with an Austek cache module, the blocks are 64 KB.
Cache type	Write-through	i486DX with Austek cache: write-through or write-back. i466DX/33 with C6 cache: write-through only i486SX (no cache): no settings

Power-on simulation speed		System speed at power-on can be set to: i486SX/33 &i486SX: 8 MHz; 33 MHz 386DX; Autospeed(*1); Native speed i486DX/50: 8 MHz; 33 MHz 386DX; 33MHz 486DX; Autospeed (*1); Native speed
Power-on password		If set, system 10 cannot be accessed until the correct password is entered.
Network server mode		Used with the power-on password. If turned on, system 10 will boot from the hard disk drive, but will not accept any keyboard input until the correct password is entered.

Power-on password

Network server mode

Off

Diagnostic Error Messages

System Board Error Code/Messages

0101 CPU ERROR
0102 ROM CHECKSUM ERROR
0103 TIMER COUNTER REGISTER ERROR
0104 TIMER COUNTER ERROR
0105 DMA REFRESH ERROR
0105 DMA CONTROLLER REGISTER ERROR
0106 DMA PAGE REGISTER ERROR
0107 KB COUNT, SELF TEST ERROR
0108 KEYBOARD KEY STUCK ERROR
0109 INT CONTROLLER ERROR
0110 CMOS SHUTDOWN BYTE ERROR
0111 CMOS BATTERY ERROR
0112 CMOS CHECKSUM ERROR
0113 CPU INSTRUCTION ERROR
0114 PROTECT MODE ERROR 1
0115 PROTECT MODE ERROR 2

Memory

0201 MEMORY ERROR

0201 PARITY ERROR

Keyboard

0301 KEYBOARD ERROR

0301 8042 ERROR

0302 KEYBOARD IS NON-STANDARD, OR KEYBOARD IS DEFECTIVE

0303 KEYBOARD LOCKING ERROR

Serial Port

1101 <control Signals> ALWAYS LOW

1102 <control Signals> ALWAYS HIGH

1102 TIMEOUT ERROR

1103 VERIFY ERROR

Parallel Port

0901 ERROR PIN p

Diskette Drives and Controller

0601 DISKETTE DRIVE CONTROLLER ERROR

0602 SEQUENTIAL SEEK ERROR

0603 RANDOM SEEK ERROR

0604 WRITE ERROR

0605 READ ERROR

0606 REMOVE ERROR

0607 INSERT ERROR

Hard Disk Drives and Controller

1701 SEEK ERROR

1702 WRITE ERROR

1703 READ ERROR

Coprocessor

0701 NOT INSTALLED

0702 COPROCESSOR INITIALIZE ERROR

0703 COPROCESSOR INVALID OPERATION MASK ERROR

0704 COPROCESSOR ST FIELD ERROR

0705 COPROCESSOR COMPARISON ERROR

0706 COPROCESSOR ZERO DIVIDE MASK ERROR

0707 COPROCESSOR ADDITION ERROR

0708 COPROCESSOR SUBTRACTION ERROR

0709 COPROCESSOR MULTIPLICATION ERROR
0711 COPROCESSOR PRECISION ERROR

ESPEED Utility

A utility that changes the clock speed of system 10 from high (native), to low (simulated 8 MHz) or to autospeed (simulated 8 MHz on diskette accesses) is desirable. Such a utility, called "ESPEED" here, will allow the use of systems and applications software that use software timing routines which depend on particular CPU speeds for their correct execution.

Fig. 10 illustrates another processor board 500 compatible with system 10. It comprises an Intel i486 CPU 502, a Weitek WTL4167 coprocessor 504, a cache controller 506, a 50 MHz clock 508, a 49FCT805 clock buffer 510, a PST 512 similar to that described in detail above, a 4K x 18 array of CY7B181 devices 514, buffers 516, 518, and 520, a 32K x 9 cache memory 522, address buffers 524 that interface to host bus 14, an R3020 controller 528, and buffers 530 and 532.

A system 1000, Fig. 11, represents a second embodiment of the present invention and comprises means for interfacing to processor boards 1002, 1004, 1006, and 1008, which are similar to processor boards 200, 300, 400, and 500. System 1000 further comprises a host bus 1014, an EISA bus 1016, an EISA bus buffer 1017, a DRAM controller 1018, a main memory 1020, a pair of ADPs 1022 and 1024, a system bus snoop controller 1026, an EBC 1028, an ISP 1030, an EBB 1032, an LIOE 1034, a PAR 1035, a disk controller 1040, an I/O controller 1042, a serial port 1044, an IDE hard disk controller 1046, a RTC 1048, and a BIOS 1050 in a 27010 device. System 1000 has a high-speed system bus 1060 for supporting peripherals that transfer data quicker than the EISA bus can handle. A SCSI or LAN master controller 1062 is shown connected.

Fig. 12 illustrates a high performance PST 1100 that supports write-back in a cache system. Such a PST will take advantage of write-back support on system 10 or 1000 when incorporated on a processor board. An ADP 1104 is equivalent to ADP 1022 and 1024. A memory controller 1102 is equivalent to DRC 1018. A snoop controller 1106 is similar to snoop controller 1026. These devices are interfaced to a cycle length tracker 1110, a snoop logic 1112, a bus cycle control 1114, a ready logic 1116, and a A38403 microcache 1120. A write-back cache system is implemented with the microcache 1120 and external cache RAM in a 2/4-way set associative configuration.

Fig. 13 is a memory map 1200 suitable for a RISC-based processor board installed in system 10 or system 1000. A virtual memory 1202 has

a non-cacheable and cacheable portions of unmapped kernal mapped to the lower 512M bytes of a physcial memory 1204. A system memory 1206 is subdivided into a free area, a boot ROM area, an I/o area, a system ROM area, an I/O ROM area, a video RAM area, 640K byte main memory, and a 255M byte memory area.

While the invention has been described in conjunction with several specific embodiments, it is evident to those skilled in the art that many further alternatives, modifications and variations is apparent in light of the forgoing description. Thus, the invention described herein is intended to embrace all such alternatives, modifications, applications and variations as may fall within the spirit and scope of the appended claims.

WHAT IS CLAIMED IS:

1. A computer system, comprising:

connector means to accept a plurality of processor cards that have CPUs which operate at different clock speeds and execute different machine code sets;

encoding means for registering which type of CPU is on a particular processor card and that is accessible to the connector means;

decoding means for reading the encoding of the CPU type as communicated with the connector means; and

program initialization memory means having a plurality of storage areas one of which contains machine code compatible with at least one of said processor cards, the memory means having means for selecting which of said storage areas is to be coupled to the connector means, said selecting means responsive to the decoding means.

2. The system of claim 1, wherein:

the connectors means comprises a connector pin and circuit board system;

the encoding means comprises strapping predetermined connector pins in binary combinations to ground;

the decoding means comprises wiring signal lines corresponding to said predetermined connector pins directly to at least one of the address lines of a ROM which comprises the memory means; and

the memory means separates storage areas on the basis of address lines which are wired to said connector pins.

3. A computer system, comprising:

a programmable read only memory (PROM) located on a motherboard that is accessible to a CPU located on a processor board plugged into said motherboard;

means for reading a basic input/output system (BIOS) file; and

means for programming the PROM with data representing said BIOS.

4. The system of claim 3, wherein:

the PROM is a flash memory located on a motherboard within the system; and

said BIOS file is recorded on a floppy disk.

5. The system of claim 3, wherein:

the BIOS file reading means comprises,

initialization means for recognizing whether or not a BIOS presently loaded in the PROM is compatible with said CPU;

man-machine interface means for informing a user of the system that a floppy disk must be inserted into the system in order for a correct BIOS to be loaded into the PROM, the interface means responsive to the initialization means;

floppy disk means to receive said floppy disk and to communicate the fact that said floppy disk has been mounted; and

file reading means to access and read a particular floppy disk file containing a BIOS program compatible with said CPU, the file reading means responsive to the floppy disk means.

6. A computer system, comprising:

a microcomputer CPU having a clock speed of at least 50 MHz;

a system bus having a data transfer rate of at least 66 MHz; and

a programmable state tracker (PST) means for two-way simultaneous interfacing of the CPU with the system bus, the PST means comprising means for snoop control for cache write-back, means for strobe detection of the CPU, means for arbitration of the host bus, means for cycle counting of the CPU, means for host address strobe (HAS) generation to the system bus, means for synchronization of the CPU to the host bus, and means for ready generation to both the CPU and host bus.

7. The system of claim 6, wherein:

the microcomputer CPU has a clock speed of at least 50 MHz; and

the system bus has a data transfer rate of at least 66 MHz.

8. The system of claim 6, wherein:

the PST means comprises more than one programmable logic array (PLA) over which are distributed the implementations of said snoop control, strobe detection, arbitration, cycle counting, HAS generation, synchronization, and ready generation means.

9. The system of claim 8, wherein:

said PALs comprise the same type of device from the same manufacturer such that the propagation times through the respective devices are substantially the same.

10. The system of claim 9, wherein:

the PST means further comprises a 74B2525-type of clock driver and where the individual lead lengths at the outputs of the clock driver are such that clocks derived from a clock at the input of the clock driver all arrive at each of the several PALs and a plurality other clocked receiver elements in support of the PALs at practically the same time.

11. The system of claim 6, wherein:

the PST means further comprises non-deterministic cycle tracking means and deterministic cycle tracking means both responsive to said HAS control means and the host bus and both able to signal said ready generator means.

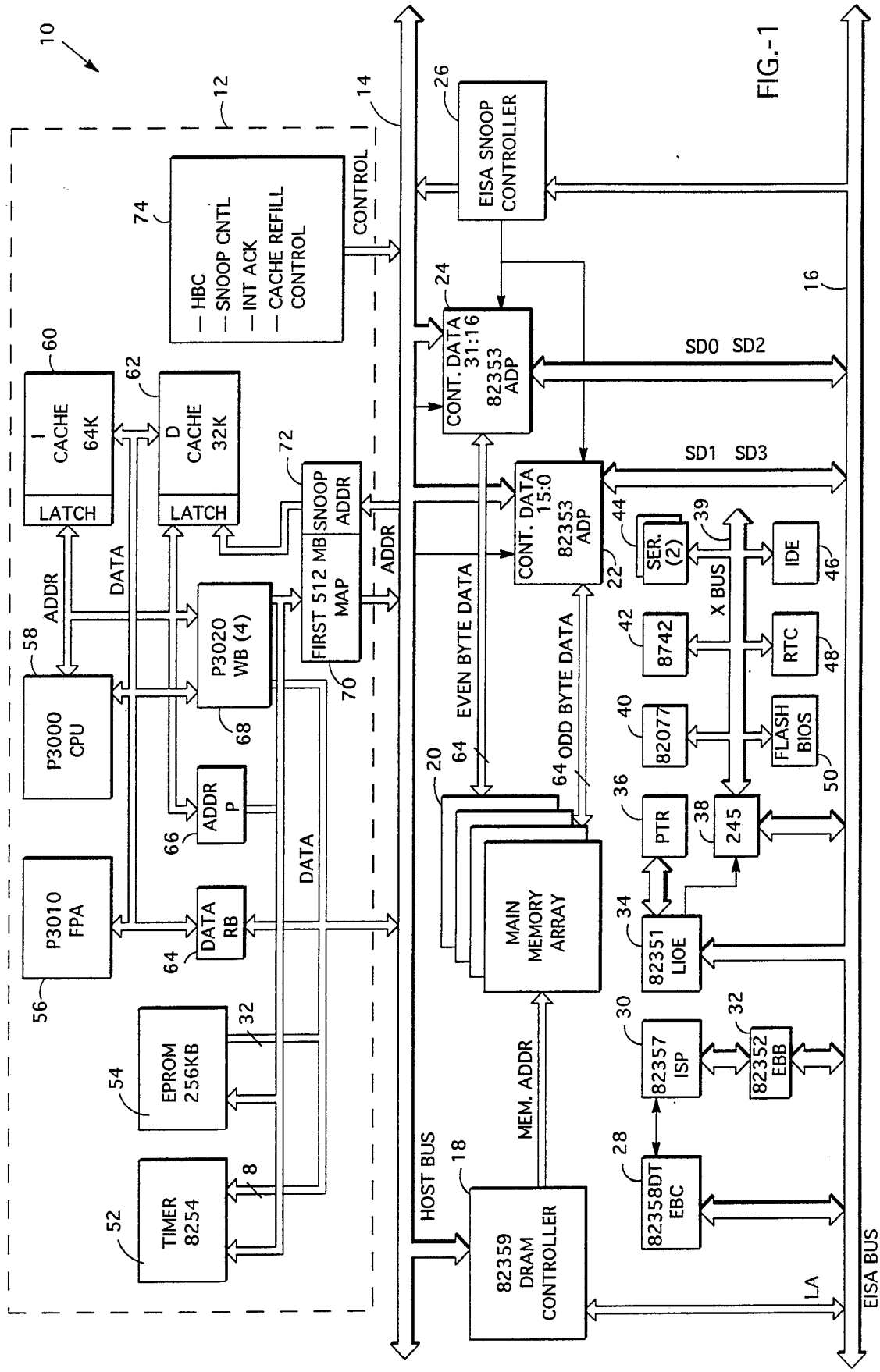

FIG.-1

SUBSTITUTE SHEET

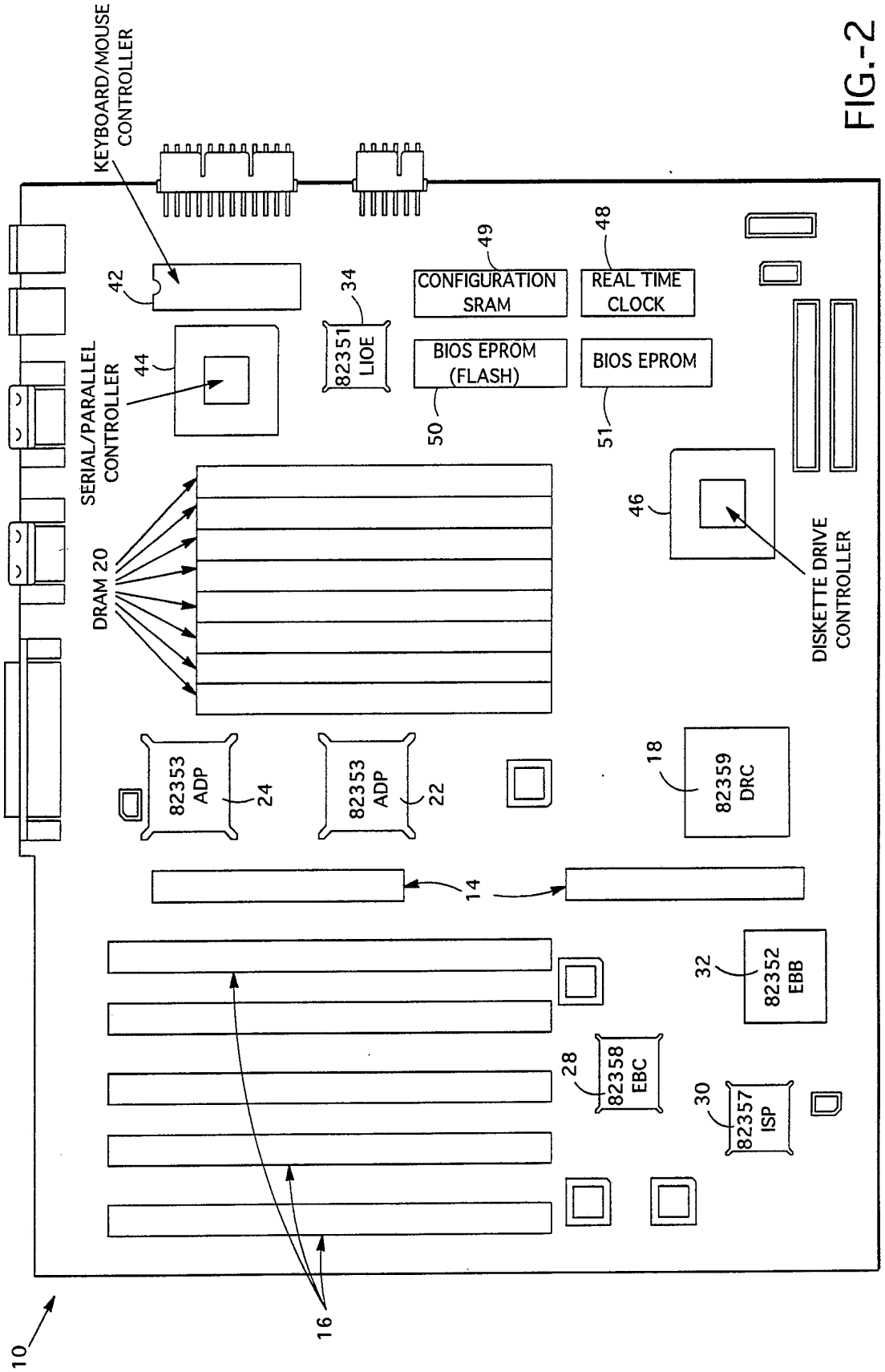

FIG.-2

SUBSTITUTE SHEET

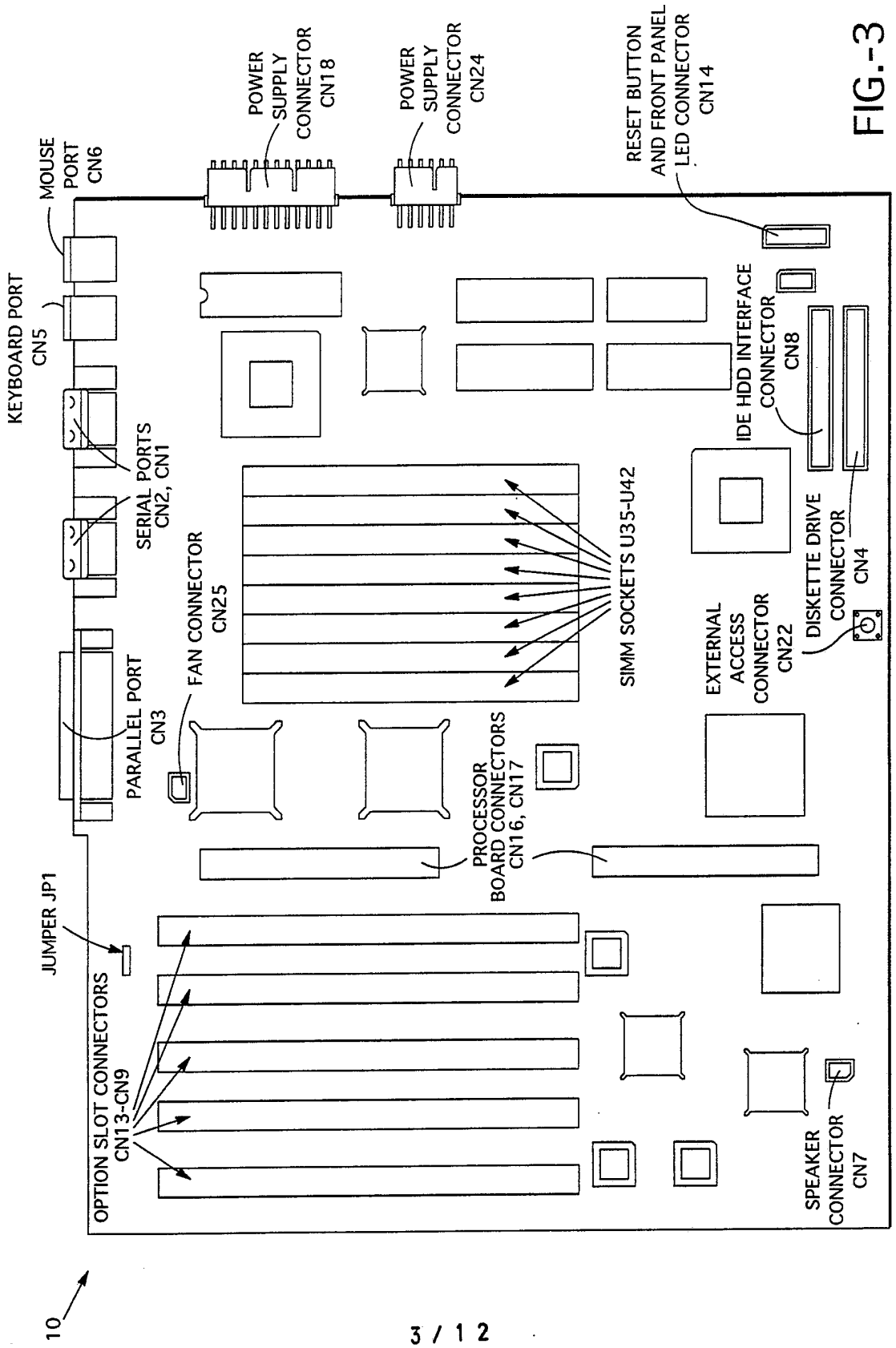

FIG.-3

SUBSTITUTE SHEET

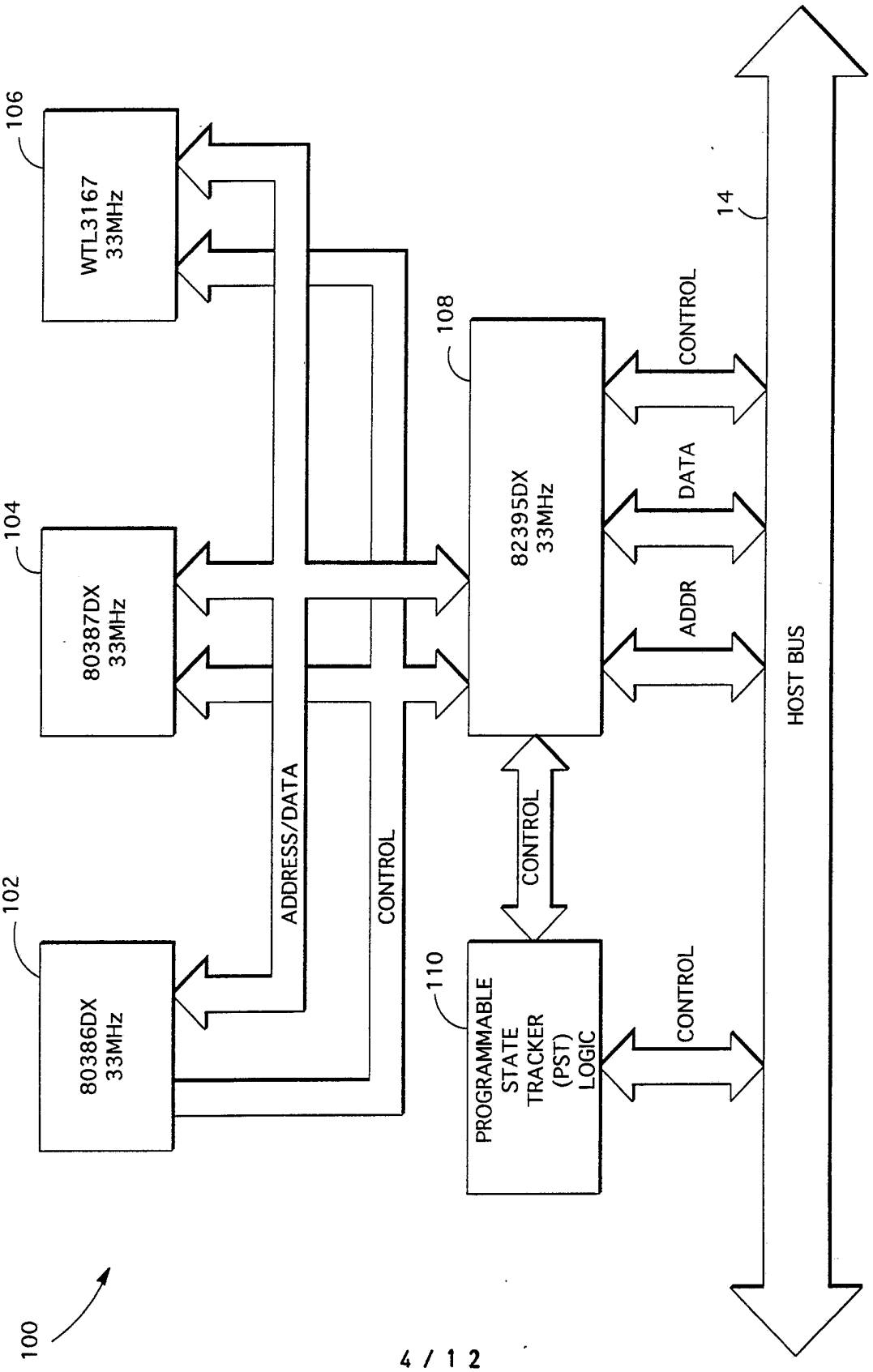
100
102
80386DX
33MHz
104
80387DX
33MHz
106
WTL3167
33MHz
108
82395DX
33MHz
110
PROGRAMMABLE
STATE
TRACKER
(PST)
LOGIC
14
HOST BUS
ADDRESS/DATA
CONTROL
CONTROL
CONTROL
DATA
ADDR
CONTROL

FIG.-4

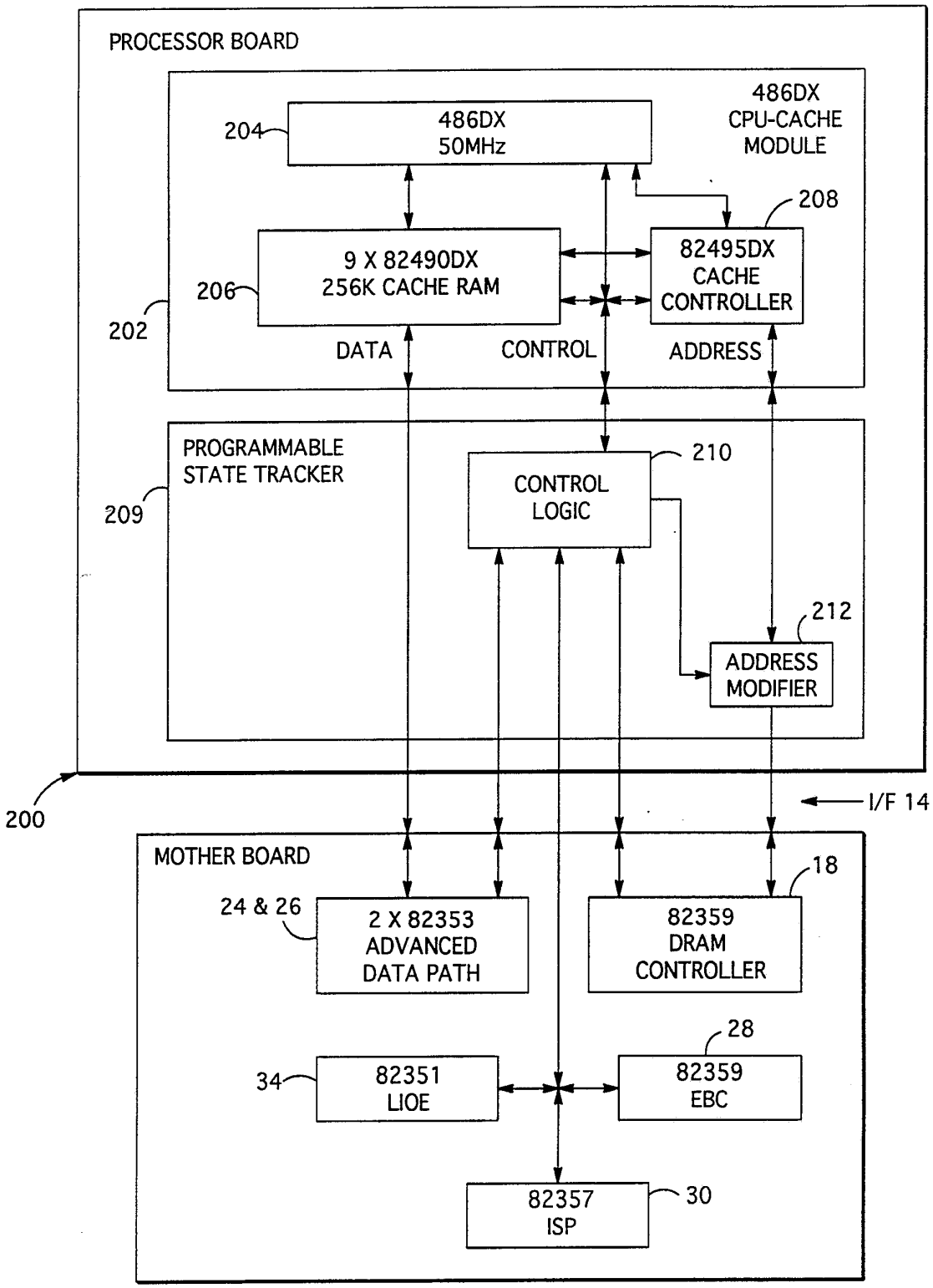

FIG.-5

SUBSTITUTE SHEET

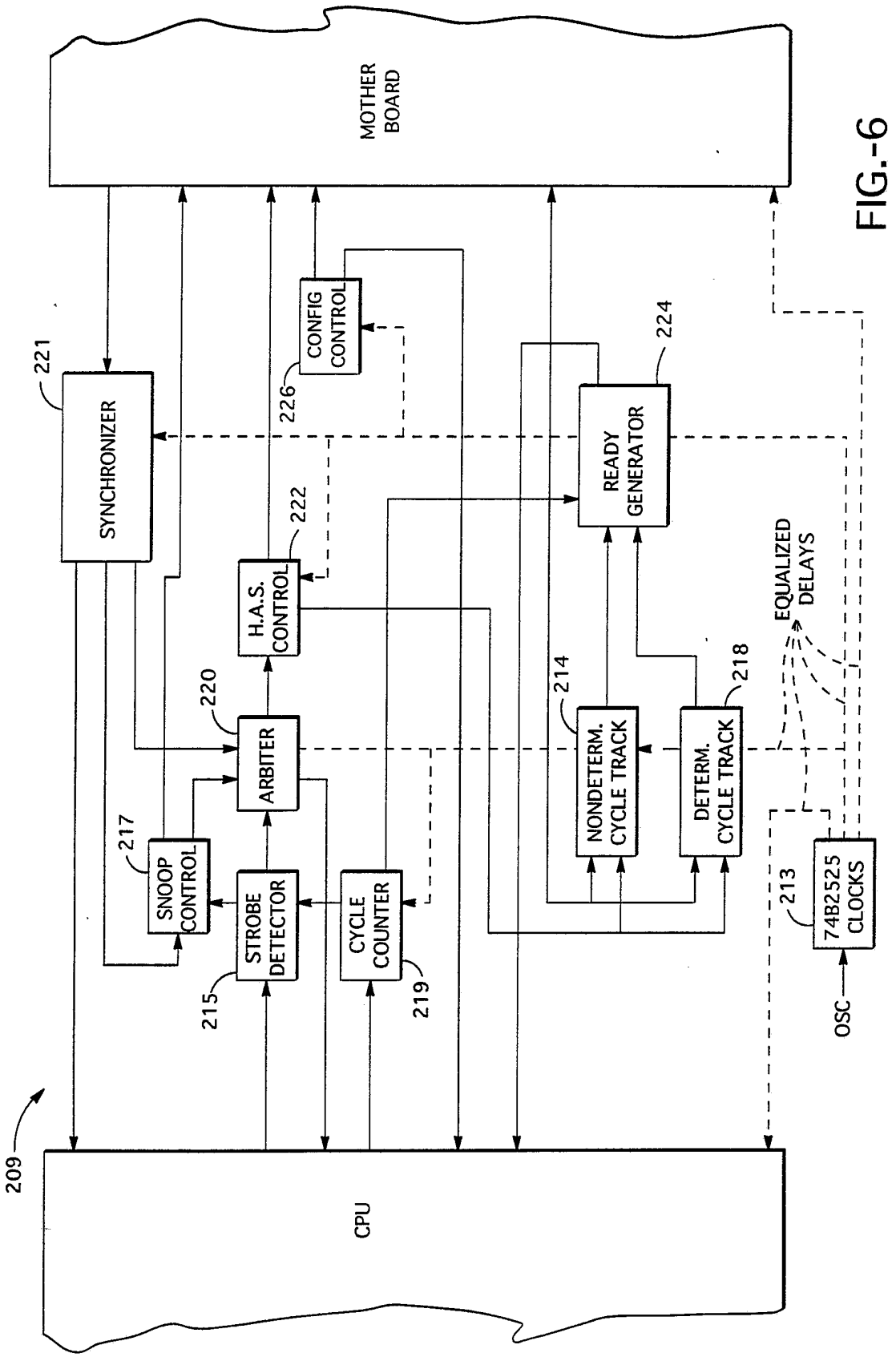

FIG.-6

SUBSTITUTE SHEET

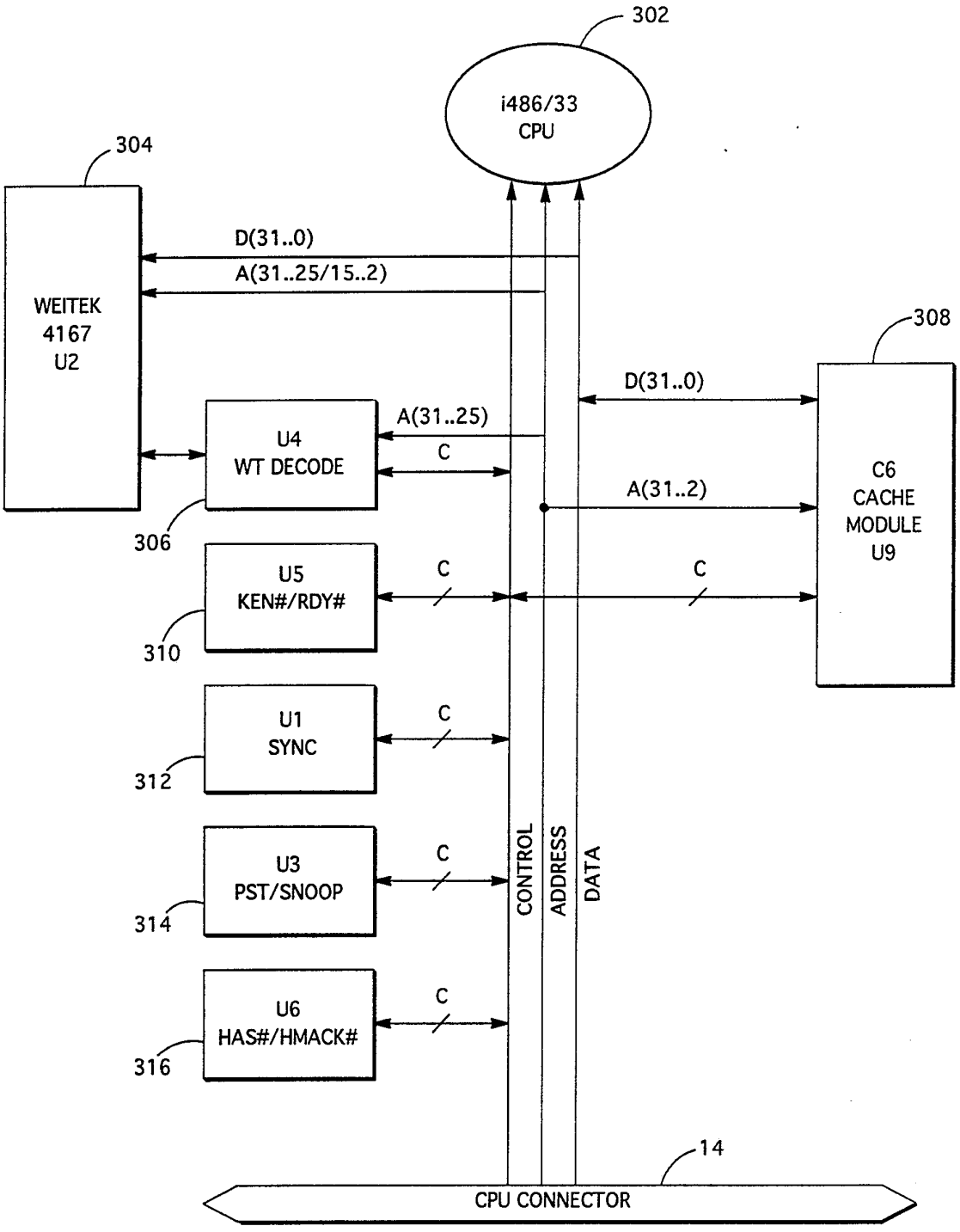
302
i486/33
CPU
304
WEITEK
4167
U2
D(31..0)
A(31..25/15..2)
308
D(31..0)
A(31..25)
C
U4
WT DECODE
306
A(31..2)
C6
CACHE
MODULE
U9
U5
KEN#/RDY#
C
C
310
U1
SYNC
C
312
U3
PST/SNOOP
C
314
U6
HAS#/HMACK#
C
316
CONTROL
ADDRESS
DATA
14
CPU CONNECTOR

FIG.-7

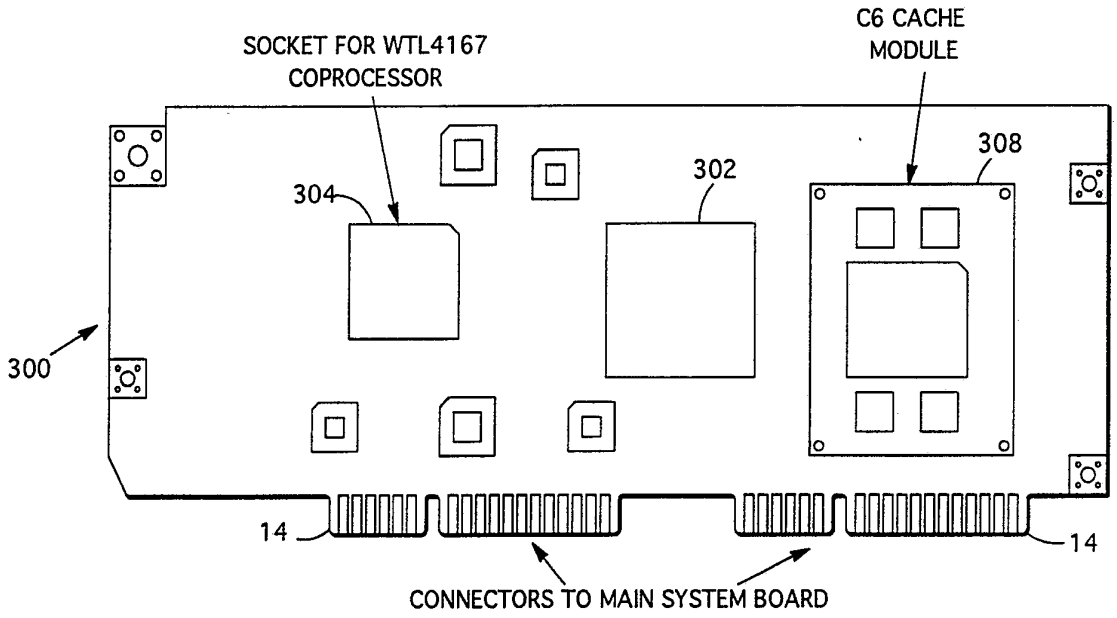
SOCKET FOR WTL4167
COPROCESSOR
C6 CACHE
MODULE
308
302
304
300
14
14
CONNECTORS TO MAIN SYSTEM BOARD

FIG.-8

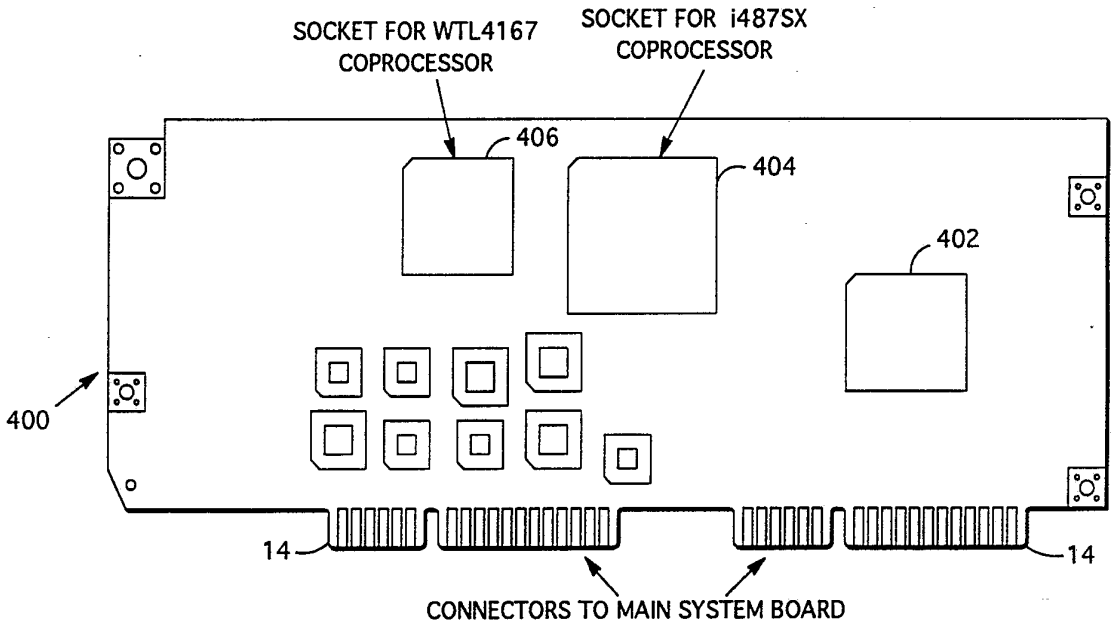
SOCKET FOR WTL4167
COPROCESSOR
SOCKET FOR i487SX
COPROCESSOR
406
404
402
400
14
14
CONNECTORS TO MAIN SYSTEM BOARD

FIG.-9

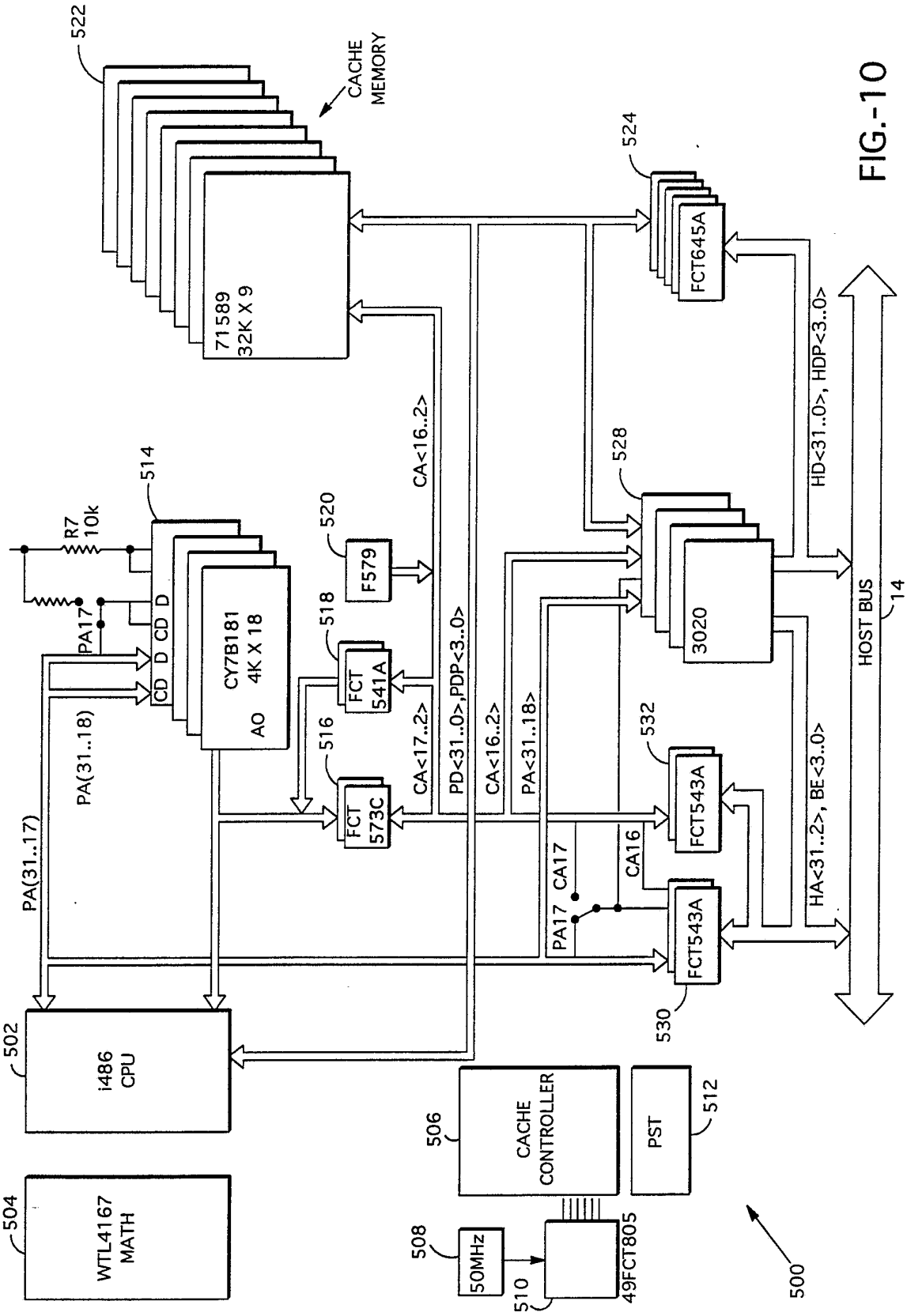

FIG.-10

SUBSTITUTE SHEET

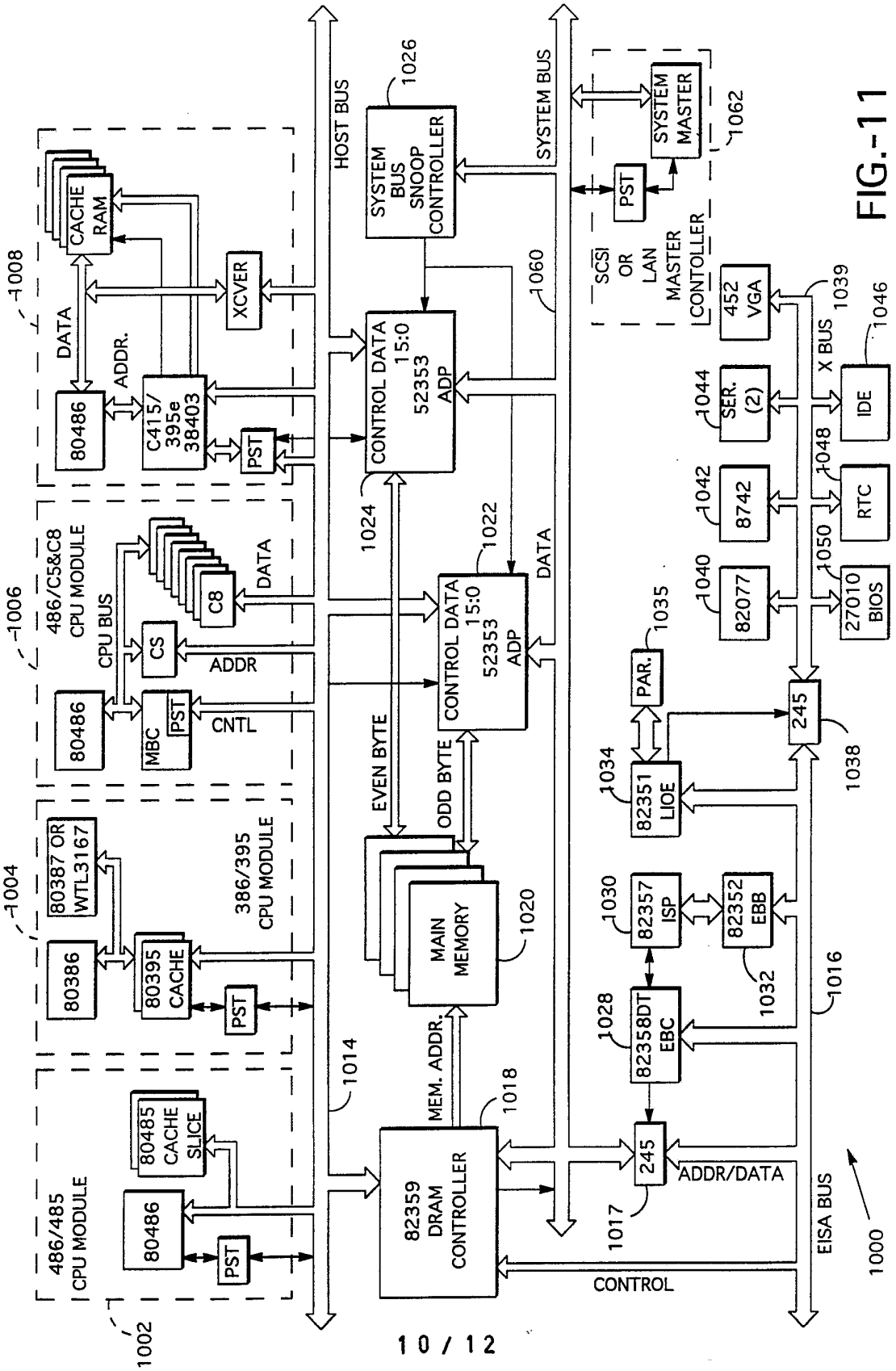

FIG.-11

SUBSTITUTE SHEET

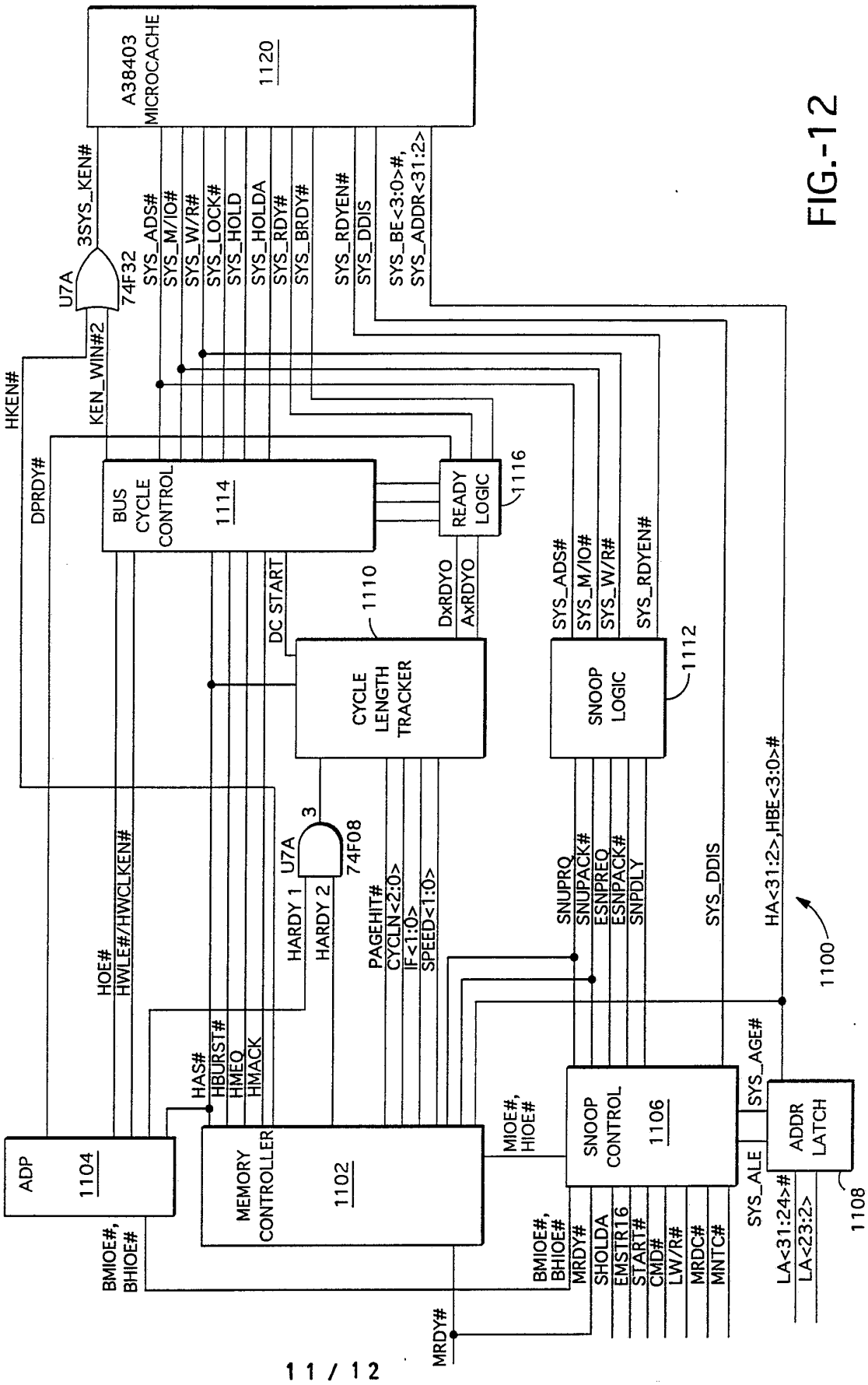

FIG.-12

SUBSTITUTE SHEET

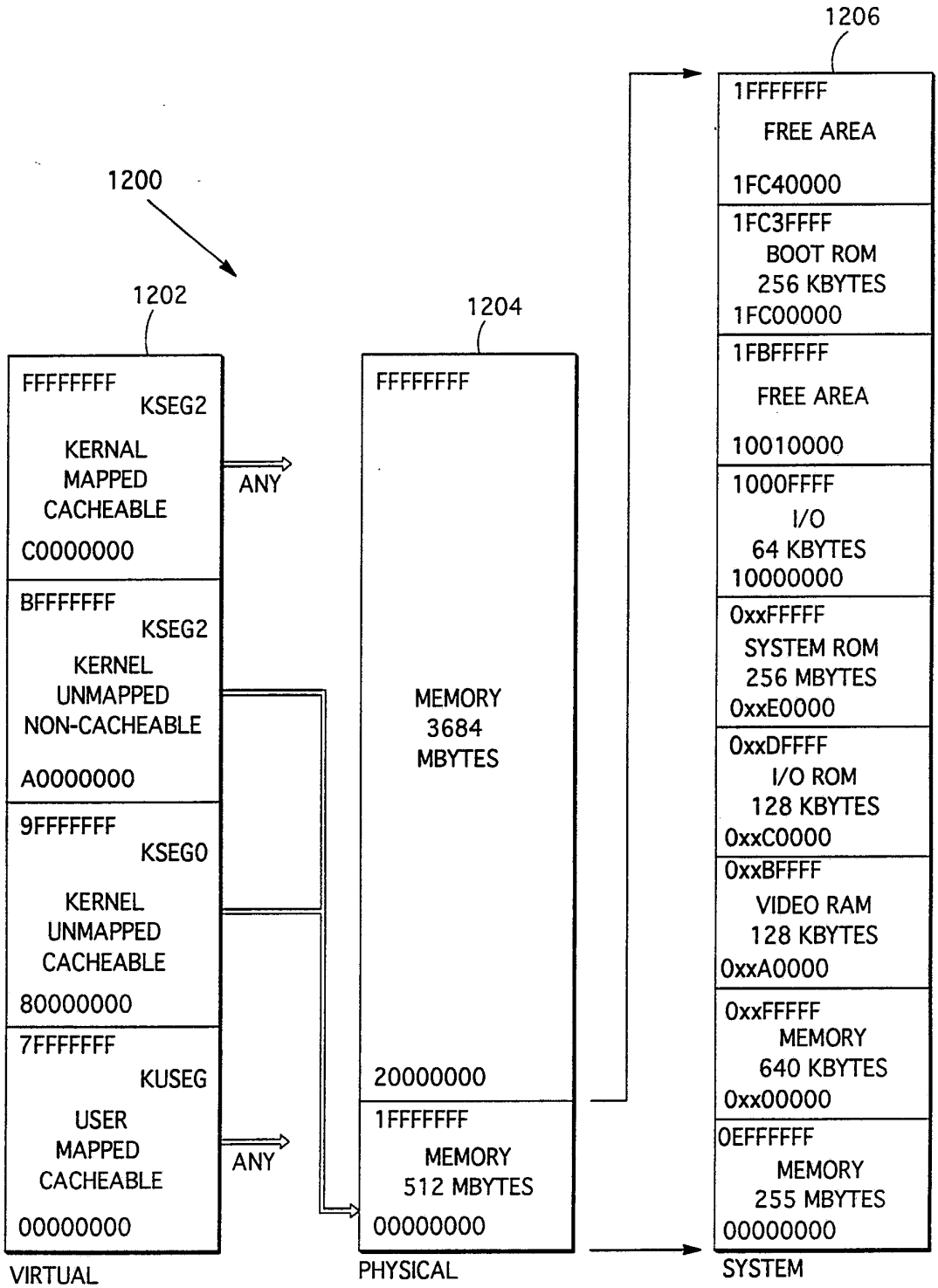
1206
1200
1202
1204
FFFFFFFF
KSEG2
KERNAL
MAPPED
CACHEABLE
C0000000
BFFFFFFF
KSEG2
KERNEL
UNMAPPED
NON-CACHEABLE
A0000000
9FFFFFFF
KSEG0
KERNEL
UNMAPPED
CACHEABLE
80000000
7FFFFFFF
KUSEG
USER
MAPPED
CACHEABLE
00000000
VIRTUAL
ANY
ANY
FFFFFFFF
MEMORY
3684
MBYTES
20000000
1FFFFFFF
MEMORY
512 MBYTES
00000000
PHYSICAL
1FFFFFFF
FREE AREA
1FC40000
1FC3FFFF
BOOT ROM
256 KBYTES
1FC00000
1FBFFFFF
FREE AREA
10010000
1000FFFF
I/O
64 KBYTES
10000000
0xxFFFFF
SYSTEM ROM
256 MBYTES
0xxE0000
0xxDFFFF
I/O ROM
128 KBYTES
0xxC0000
0xxBFFFF
VIDEO RAM
128 KBYTES
0xxA0000
0xxFFFFF
MEMORY
640 KBYTES
0xx00000
0EFFFFFF
MEMORY
255 MBYTES
00000000
SYSTEM

FIG.-13