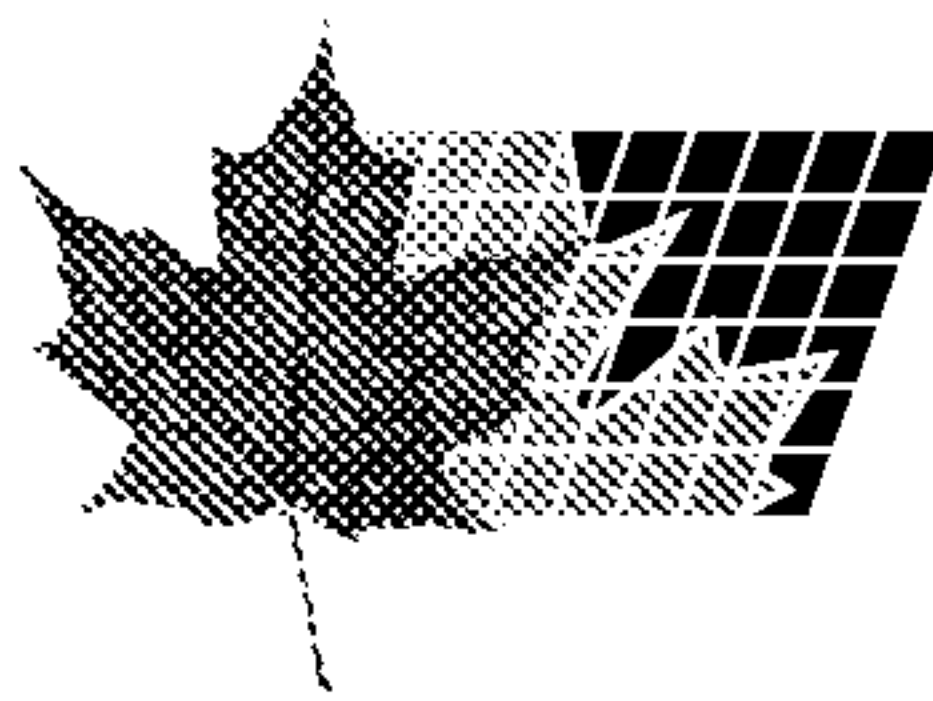




(11) (21) (C) **2,208,333**
(22) 1997/06/20
(43) 1997/12/21
(45) 2000/08/22

(72) AOYAMA, Akio, JP

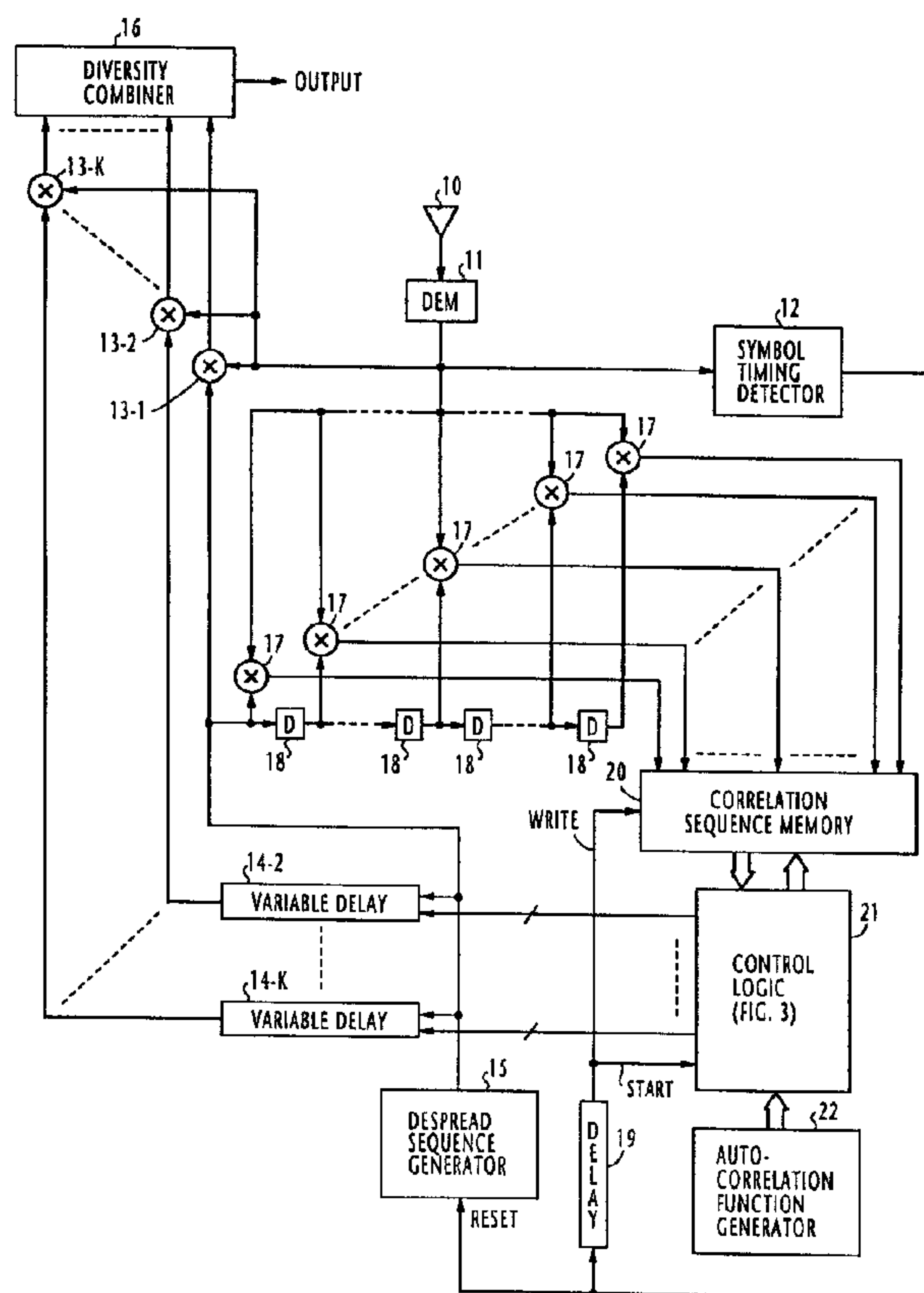
(73) NEC CORPORATION, JP

(51) Int.Cl.⁶ H04B 1/69, H04B 7/216, H04B 7/02

(30) 1996/06/21 (JP 8-162097) JP

(54) **RECEPTION DE LA DIVERSITE CDMA DE VOIE D'ACCES EN
DETECTANT L'ORDRE DE CORRELATION MAXIMAL
INFERIEUR APRES LE DEPLACEMENT PLUS ELEVES DES
ORDRES**

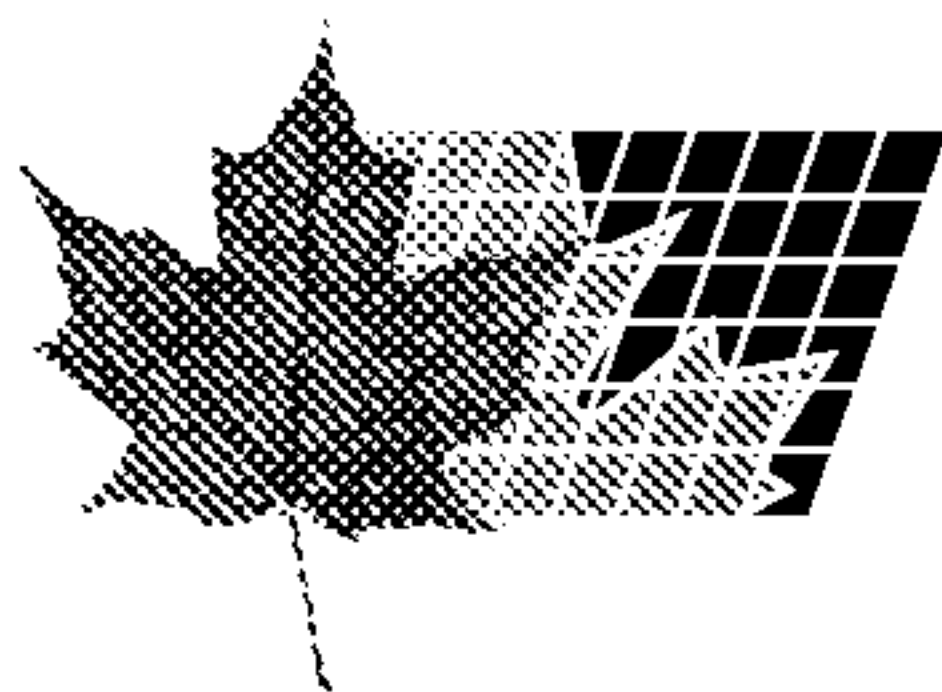
(54) **PATH-DIVERSITY CDMA RECEPTION BY DETECTING
LOWER-PEAK CORRELATION SEQUENCE FOLLOWING
REMOVAL OF HIGHER-PEAK SEQUENCES**



(57) Dans un récepteur DS-CDMA, des empreintes programmées successivement d'un ordre de désétalement servent à détecter les corrélations avec une séquence d'éléments reçue, et les ordres de corrélation résultants sont stockés en mémoire. Un ordre de corrélation à crête maximale et les ordres de corrélation

(57) In a DS-CDMA receiver, successively time shifted replicas of a despreading sequence are used to detect correlations with a received chip sequence and resulting correlation sequences are stored in a memory. A correlation sequence having a maximum peak and correlation sequences having side peaks inherently





(11) (21) (C) **2,208,333**
(22) 1997/06/20
(43) 1997/12/21
(45) 2000/08/22

à crête latérale associés, de façon intrinsèque, à la crête maximale sont détectés dans la mémoire, et tous les ordres de corrélation détectés sont supprimés de la mémoire. la suite de cette suppression, un ordre de corrélation à crête maximale est détecté à partir des ordres de corrélation qui restent, et la synchronisation de l'ordre de corrélation est déterminée. Un ordre de désétalement est produit en différé par rapport à la synchronisation déterminée, et la séquence d'éléments est désétalée à l'aide de l'ordre de désétalement en différé afin de produire un signal de voie de diversité.

associated with the maximum peak are detected in the memory and all of the detected correlation sequences are removed from the memory. Following this removal, a correlation sequence having a maximum peak is detected from the remaining correlation sequences and the timing of the correlation sequence is determined. A despreading sequence which is delayed in accordance with the determined timing is produced and the chip sequence is despread with the delayed despreading sequence to produce a diversity branch signal.

NE-793

- 16 -

ABSTRACT OF THE DISCLOSURE

1 In a DS-CDMA receiver, successively time shifted replicas of a
2 despread sequence are used to detect correlations with a received chip
3 sequence and resulting correlation sequences are stored in a memory. A
4 correlation sequence having a maximum peak and correlation sequences
5 having side peaks inherently associated with the maximum peak are
6 detected in the memory and all of the detected correlation sequences are
7 removed from the memory. Following this removal, a correlation sequence
8 having a maximum peak is detected from the remaining correlation
9 sequences and the timing of the correlation sequence is determined. A
10 despread sequence which is delayed in accordance with the determined
11 timing is produced and the chip sequence is despread with the delayed
12 despread sequence to produce a diversity branch signal.

NE-793

- 1 -

1 TITLE OF THE INVENTION

2 "Path-Diversity CDMA Reception By Detecting Lower-Peak Correlation
3 Sequence Following Removal of Higher-Peak Sequences"

4 BACKGROUND OF THE INVENTION

5 Field of the Invention

6 The present invention relates generally to direct sequence spread
7 spectrum, or DS-CDMA (code division multiple access) receivers, and
8 more specifically to path-diversity reception of a DS spread spectrum signal
9 propagated on multiple radio paths.

10 Description of the Related Art

11 Diversity reception of a direct sequence spread spectrum signal
12 involves the detection of correlations (comparisons) between a received chip
13 sequence and a despreading sequence on a chip-by-chip basis and the
14 detection of the time instant of a correlation sequence having a maximum
15 value as the sync timing of the chip sequence. The correlation sequence is a
16 convolution integral of the auto-correlation of the despreading sequence and
17 a channel impulse response and is usually represented by a complex value. If
18 the transmitted signal undergoes multiple reflections and so it propagates
19 along radio paths of different channel responses, the correlation sequences
20 have different peaks at different time instants respectively corresponding to
21 the channel responses of the radio paths. The signal of highest strength has
22 a maximum peak at zero timing point in a spectrum of correlation
23 sequences and a weaker signal has a lower peak at a point shifted a two-chip
24 interval, for example, from the zero timing point. For establishing
25 synchronization for the multipath signals, it is the usual practice to detect
26 the peak values in descending order of their strength.

27 Although satisfactory for chip sequences where the chip interval is
28 relatively long, the prior art approach is not satisfactory for the signal having
29 relatively short chip intervals due to the presence of side peaks which
30 accompany the main peak as inherent side products. If the side peaks are

NE-793

- 2 -

1 higher than the main peak of a multipath signal, an out-of-sync condition
2 will result.

3 SUMMARY OF THE INVENTION

4 It is therefore an object of the present invention to provide successful
5 path-diversity reception of multipath CDMA signals even though the chip
6 sequence of the signals have side peaks.

7 The object of the present invention is attained by removal of
8 correlation sequences of higher peaks followed by the detection of a
9 correlation sequence having a lower peak.

10 According to a first aspect of the present invention, there is provided
11 a path-diversity CDMA receiver in which comprises a spread spectrum
12 radio frequency signal is received and a chip sequence is produced. A
13 despreading sequence of the receiver is produced by a pseudo-noise (PN)
14 sequence generator and a plurality of successively time shifted replicas of the
15 despreading sequence is produced. A plurality of correlators are provided
16 for detecting correlations between the chip sequence and the time shifted
17 replicas of the despreading sequence to produce a plurality of correlation
18 sequences, one of the correlation sequences which is produced
19 corresponding to an intermediate one of the time shifted replicas having a
20 maximum peak. The correlation sequences are stored in a memory. A
21 control logic, connected to the memory, detects a correlation sequence
22 having the maximum peak and correlation sequences having side peaks
23 inherently associated with the maximum peak and removes all the detected
24 sequences from the memory. The control logic proceeds to detect a
25 correlation sequence having a maximum peak among the correlation
26 sequences remaining in the memory and produces a timing control signal
27 corresponding to the detected correlation sequence. A variable delay
28 introduces a delay to the despreading sequence from the PN sequence
29 generator in accordance with the timing control signal. The delayed
30 despreading sequence is used by a despreader to despread the chip sequence

NE-793

- 3 -

1 to produce a diversity branch signal.

2 According to a second aspect, the present invention provides a
3 method for producing a diversity branch signal from a chip sequence
4 transmitted by a spread spectrum radio frequency signal propagating on
5 multiple radio paths. The method comprises the steps of producing a
6 plurality of successively time shifted replicas of a despreading sequence,
7 detecting correlations between the chip sequence and the time shifted
8 replicas and producing therefrom a plurality of correlation sequences, one of
9 the correlation sequences which corresponds to an intermediate point of the
10 time shifted replicas having a maximum peak, and storing the correlation
11 sequences in a memory. A correlation sequence having a maximum peak
12 and correlation sequences having side peaks inherently associated with the
13 maximum peak are detected in the memory and all of the detected
14 correlation sequences are removed from the memory. A correlation
15 sequence having a maximum peak is then detected from the remaining
16 correlation sequences and the timing of the correlation sequence is
17 determined. A despreading sequence which is delayed in accordance with
18 the determined timing is produced and the chip sequence is despread with
19 the delayed despreading sequence to produce the diversity branch signal.

20 According to a third aspect, the present invention provides a
21 method for producing a diversity branch signal from a chip sequence
22 transmitted by a spread spectrum radio frequency signal propagating on
23 multiple radio paths. The method comprises the steps of:

24 a) producing a plurality of successively time shifted replicas of a
25 despreading sequence;

26 b) detecting correlations between the chip sequence and the time
27 shifted replicas and producing therefrom a plurality of correlation
28 sequences, one of the correlation sequences which corresponds to an
29 intermediate point of the time shifted replicas having a maximum peak;

30 c) storing the correlation sequences in a memory;

NE-793

- 4 -

- 1 d) setting a variable n to 1;
- 2 e) detecting, in the memory, a correlation sequence having a
- 3 maximum peak and identifying the correlation sequence having the
- 4 maximum peak as an n^{th} correlation sequence;
- 5 f) incrementing the variable n by 1;
- 6 g) removing the $(n-1)^{th}$ correlation sequence from the memory;
- 7 h) detecting, in the memory, correlation sequences having side
- 8 peaks inherently associated with the maximum peak of the $(n-1)^{th}$
- 9 correlation sequence and removing the detected correlation sequences from
- 10 the memory;
- 11 i) repeating the step (e) to detect a correlation sequence having a
- 12 maximum peak;
- 13 j) determining the timing of the detected correlation sequence
- 14 and producing a despreading sequence delayed according to the
- 15 determined timing;
- 16 k) repeating the steps (e) to (j) to produce a plurality of the
- 17 delayed despreading sequences; and
- 18 l) despreading the chip sequence with the plurality of delayed
- 19 despreading sequences to produce a plurality of the diversity branch signals.

20 BRIEF DESCRIPTION OF THE DRAWINGS

21 The present invention will be described in further detail with
22 reference to the accompanying drawings, in which:

23 Fig. 1 is a block diagram of a path-diversity DS-CDMA (direct
24 sequence code division multiple access) receiver according to the present
25 invention;

26 Fig. 2 is a graphic representation of an auto-correlation of the
27 receiver's despread PN sequence;

28 Fig. 3 is a flowchart of the operation of the control logic of Fig. 1;
29 and

30 Fig. 4 is a graphic representation of a typical example of a

NE-793

- 5 -

1 correlation sequence spectrum.

2 DETAILED DESCRIPTION

3 Referring now to Fig. 1, there is shown a path-diversity DS-CDMA
4 receiver according to the present invention. A direct-sequence spread
5 spectrum radio frequency signal, received at antenna 10, is converted by a
6 demodulator 11 to a baseband chip sequence, which is applied to a symbol
7 timing detector 12. The chip sequence is also fed to despreader, or
8 multipliers 13-1 through 13-K which respectively correspond to radio paths
9 on which the transmitted signal may be propagated due to multiple
10 reflections. Symbol timing detector 12 is implemented with a known
11 technique. One example is a matched filter which produces a logic-1
12 output when the symbol timing of the incoming chip sequence is matched
13 to the receiver's despread PN (pseudo-noise) sequence. This despread
14 sequence is produced by a despread sequence generator 15 and directly
15 supplied to multiplier 13-1. When the symbol timing detector produces a
16 logic-1 output, the despread sequence generator 15 is reset so that the start
17 timing of the despread sequence is time-coincident with the symbol
18 timing of the strongest chip sequence. Multiplier 13-1 uses the time-
19 coincident despread sequence to recover the strongest signal for coupling
20 to a diversity combiner 16.

21 The output of despread sequence generator 15 is fed to the input
22 end of a tapped-delay line formed by a series of delay elements 18, each
23 introducing a delay corresponding to a "subchip" interval "r", i.e., an
24 integral submultiple of chip interval T_c . A plurality of successively time
25 shifted replicas of the despread sequence are produced at subchip
26 intervals "r" along the taps of the delay line. The incoming chip sequence is
27 further supplied to a plurality of correlators, or multipliers 17 where it is
28 multiplied by the despread sequences from the tapped-delay line. As a
29 result, a plurality of correlation sequences are produced in this way by
30 multipliers 17.

NE-793

- 6 -

1 The logic-1 output of symbol timing detector 19 is further coupled
2 to a delay element 19 where it is delayed by an interval corresponding to
3 the length of time the despreading sequence takes to travel from the input
4 end of the tapped-delay line to its center tap. The output of delay element
5 19 is supplied to a correlation sequence memory 20, which uses it as a write
6 command to store the correlation sequences produced by multipliers 17. It
7 is seen therefore that the correlation sequence delivered from the center-tap
8 multiplier has a maximum (mainlobe) correlation value and correlation
9 sequences having side peaks inherently associated with the mainlobe appear
10 on both sides of the maximum correlation sequence.

11 The output of despread sequence generator 15 is also supplied via
12 variable delay elements 14-2 to 14-K to multipliers 13-2 to 13-K,
13 respectively. Variable delay elements 14-2 through 14-K are controlled by
14 the control logic 21 to introduce certain amounts of delay to the despread
15 PN sequence in order to allow multipliers 13-2 to 13-K to despread the
16 incoming chip sequence at time instants which are matched to lower
17 strength signals propagating on the multiple radio paths. The outputs of
18 multipliers 13-2 to 13-K are coupled to the diversity combiner 16 to
19 produce a diversity-combined signal. As will be understood, the diversity
20 combiner 16 is sequentially supplied with output signals from despreaders
21 13-1 through 13-K in descending order of their strength, with the signal
22 from multiplier 13-1 being the strongest and that from multiplier 13-K
23 being the weakest.

24 The output of delay element 19 is also used as a start command
25 signal for instructing a control logic 21 to start processing the correlation
26 sequences stored in the memory 20 by using an auto-correlation function of
27 the receiver's despread PN sequence produced by an auto-correlation
28 function generator 22. In general, auto-correlation is defined by a
29 convolution integral as a measure of similarity between a signal and a time-
30 shifted replica of itself. As illustrated in Fig. 2, the auto-correlation

NE-793

- 7 -

1 function has a mainlobe 50 at the zero sync timing of the time scale which is
2 divided into chip intervals T_c and sidelobes 51 and 52 which appear at $\pm 4T_c$
3 inherent to mainlobe 50. The timing at which the sidelobes occur is false
4 timing and must be distinguished from the timing of a diversity branch
5 signal.

6 In order to prevent the multipliers 13 from synchronizing to the
7 false sidelobe timing, the control logic 21 operates in accordance with the
8 flowchart of Fig. 3.

9 In Fig. 3, the operation of control logic 21 starts with step 30 where
10 it initializes the settings of variable delay elements 14-2 through 14-K. At
11 step 31, control logic 21 checks to see if a start command is received. If so,
12 flow proceeds from step 31 to step 32 to set a variable "n" to 1. At step 33,
13 memory 20 is searched for a correlation sequence having a maximum peak
14 and this sequence is identified as *n*th correlation sequence. Flow proceeds
15 to decision step 34 to determine whether the variable "n" is equal to or
16 greater than 2. If not, flow branches off to step 36. If the answer is
17 affirmative at step 34, flow branches off to step 35 to set the *n*th variable
18 delay element 14-n according to the timing of the *n*th correlation sequence,
19 where the "n" is greater than 1.

20 At step 36, the variable "n" is checked to see if it is equal to or
21 greater than the integer K, i. e, the number of radio paths which may be
22 taken by the arriving signal. If the decision at step 36 is affirmative, control
23 returns to step 31. Otherwise, it proceeds to step 37 to increment the
24 variable "n" by 1.

25 The (*n*-1)th correlation sequence is removed from memory 20 at
26 step 38, and "m" neighboring correlation sequences of the (*n*-1)th
27 correlation sequence are removed from the memory (step 39). If *n* = 2, the
28 first correlation sequence detected at step 33 as having the maximum peak
29 and its neighboring sequences are now nonexistent in memory 20.

30 At step 40, the subchip distances from the (*n*-1)th correlation

NE-793

- 8 -

1 sequence to sequences having sidelobe peaks which are associated with the
2 $(n-1)th$ correlation sequence are calculated using the auto-correlation
3 function. At step 41, the correlation sequences located at the distances
4 calculated at step 40 are removed from memory 20.

5 When steps 38 to 41 are first executed, correlation sequences having
6 mainlobe 60 and sidelobes 61 and 62 are removed from memory 20 as
7 illustrated in Fig. 4.

8 Following the execution of step 41, flow returns to step 33 to make
9 a search through correlation sequences that remain in the memory and
10 detects a correlation sequence having a maximum value. This sequence is
11 now identified as a new nth correlation sequence. When step 33 is executed
12 second time, the decision at subsequent step 34 is affirmative, and flow
13 proceeds to step 35 to set the nth variable delay element 14 according to the
14 subchip timing of the nth correlation sequence. If the incoming signal
15 contains a second strongest (diversity branch) signal arriving on a path with
16 a propagation delay of $2T_C$, it occurs as indicated by numeral 63 in Fig. 4.
17 Since step 33 is executed second time, the timing position of the nth
18 correlation sequence represents the interval by which this diversity branch
19 signal has been delayed with respect to the signal of the highest strength.
20 Therefore, at step 35 the setting of the variable delay element 14-2 is
21 adjusted so that the multiplier 13-2 performs despreading of this signal
22 using a despreading sequence delayed by $2T_C$ with respect to the timing of
23 the strongest signal.

24 When control logic 21 continues to execute steps 36 to 41, the
25 correlation sequence having the peak 63 is removed from memory 20 and
26 those having its inherently associated sidelobes are eliminated. The process
27 is repeated and a still weaker diversity branch signal will be detected from
28 remaining correlation sequences and correlation sequences with the
29 mainlobe and sidelobes of this signal are erased from memory 20. The
30 process is continued until the variable n becomes equal to the integer K at

NE-793

- 9 -

- 1 step 36 and control returns to step 31.
- 2 The control logic 21 starts over the above process if it receives a start
- 3 command signal again. Synchronization for path-diversity reception is thus
- 4 retained by tracking the arbitrarily varying timing of the signals arriving on
- 5 multiple paths.

NE-793

- 10 -

What is claimed is:

1 1. A path-diversity CDMA receiver comprising:
2 means for receiving a spread spectrum radio frequency signal and
3 producing therefrom a chip sequence;
4 a pseudo-noise (PN) sequence generator for producing a
5 despreading sequence;
6 means, connected to said PN sequence generator, for producing a
7 plurality of successively time shifted replicas of said despreading sequence;
8 a plurality of correlators for detecting correlations between the chip
9 sequence and the time shifted replicas of the despreading sequence and
10 producing therefrom a plurality of correlation sequences, one of the
11 correlation sequences which is produced corresponding to an intermediate
12 one of said time shifted replicas having a maximum peak;
13 a memory for storing said correlation sequences;
14 control means for detecting a correlation sequence having said
15 maximum peak and correlation sequences having side peaks inherently
16 associated with said maximum peak and removing all the detected
17 sequences from said memory, detecting a correlation sequence having a
18 maximum peak among the correlation sequences remaining in said memory
19 and producing a timing control signal corresponding to the detected
20 correlation sequence;
21 variable delay means for introducing a delay to the despreading
22 sequence from the PN sequence generator in accordance with said timing
23 control signal; and
24 a despreader for despreading the chip sequence with the
25 despreading sequence from the variable delay means to produce a diversity
26 branch signal.

1 2. A path-diversity CDMA receiver as claimed in claim 1, wherein

NE-793

- 11 -

2 said time shifted replicas of the despread sequence are shifted by an
3 integral submultiple of a chip interval of said chip sequence.

1 3. A path-diversity CDMA receiver as claimed in claim 2, wherein
2 the control means is arranged to detect a plurality of neighboring
3 correlation sequences of the correlation sequence having said maximum
4 peak and remove the detected neighboring correlation sequences from said
5 memory.

1 4. A path-diversity CDMA receiver as claimed in claim 1, further
2 comprising means for producing an auto-correlation function of said
3 despread sequence, wherein said control means is arranged to detect the
4 correlation sequences having said side peaks using said auto-correlation
5 function.

1 5. A path-diversity CDMA receiver comprising:
2 means for receiving a spread spectrum radio frequency signal and
3 producing therefrom a chip sequence;
4 a pseudo-noise (PN) sequence generator for producing a
5 despread sequence;
6 a tapped-delay line, connected to said PN sequence generator, for
7 producing a plurality of successively time shifted replicas of said
8 despread sequence;
9 a plurality of correlators for detecting correlations between the chip
10 sequence and the time shifted replicas of the despread sequence and
11 producing therefrom a plurality of correlation sequences, one of the
12 correlation sequences which is produced by the correlator of an intermediate
13 tap located at or near the center of the delay line having a maximum peak;
14 a memory for storing said correlation sequences;
15 control means for (a) detecting a correlation sequence having said
16 maximum peak and correlation sequences having side peaks inherently

NE-793

- 12 -

17 associated with said maximum peak and removing the detected sequences
18 from said memory, (b) detecting a correlation sequence having a maximum
19 peak among the correlation sequences remaining in said memory and
20 producing a first timing control signal corresponding to the detected
21 correlation sequence, (c) detecting a correlation sequence having a
22 maximum peak and correlation sequences having side peaks inherently
23 associated with the maximum peak and removing the detected sequences
24 from said memory, and (d) detecting a correlation sequence having a
25 maximum peak among the correlation sequences remaining in said memory
26 and producing a second timing control signal corresponding to the detected
27 correlation sequence;

28 first and second variable delay means for introducing delays to the
29 despreading sequence from the PN sequence generator in accordance with
30 said first and second timing control signals, respectively; and

31 first and second despreaders for despreading the chip sequence with
32 the despreading sequences from the first and second variable delay means to
33 produce first and second diversity branch signals.

1 6. A path-diversity CDMA receiver as claimed in claim 5, wherein
2 said time shifted replicas of the despreading sequence are shifted by an
3 integral submultiple of a chip interval of said chip sequence.

1 7. A path-diversity CDMA receiver as claimed in claim 6, wherein
2 the control means is arranged to detect a plurality of neighboring
3 correlation sequences of the correlation sequence having said maximum
4 peak and remove the detected neighboring correlation sequences from said
5 memory.

1 8. A path-diversity CDMA receiver as claimed in claim 5, further
2 comprising means for producing an auto-correlation function of said
3 despreading sequence, wherein said control means is arranged to detect the

NE-793

- 13 -

4 correlation sequences having said side peaks using said auto-correlation
5 function.

1 9. A method for producing a diversity branch signal from a chip
2 sequence transmitted by a spread spectrum radio frequency signal
3 propagating on multiple radio paths, comprising the steps of:
4 a) producing a plurality of successively time shifted replicas of a
5 despreading sequence;
6 b) detecting correlations between the chip sequence and said time
7 shifted replicas and producing therefrom a plurality of correlation
8 sequences, one of the correlation sequences which corresponds to an
9 intermediate point of said time shifted replicas having a maximum peak;
10 c) storing said correlation sequences in a memory;
11 d) detecting, in said memory, a correlation sequence having a
12 maximum peak and correlation sequences having side peaks inherently
13 associated with the maximum peak and removing all of the detected
14 correlation sequences from said memory;
15 e) detecting, in said memory, a correlation sequence having a
16 maximum peak and detecting the timing of the correlation sequence;
17 f) producing a despreading sequence delayed in accordance with
18 the detected timing; and
19 g) despreading the chip sequence with the delayed despreading
20 sequence to produce said diversity branch signal.

1 10. The method of claim 9, further comprising the step of
2 repeating the steps (d) to (g).

1 11. The method of claim 9, wherein said time shifted replicas of
2 the despreading sequence are shifted by an integral submultiple of a chip
3 interval of said chip sequence.

NE-793

- 14 -

1 12. The method of claim 11, wherein the step (d) comprises the
2 steps of detecting a plurality of neighboring correlation sequences of the
3 correlation sequence having said maximum peak and removing the detected
4 neighboring correlation sequences from said memory.

1 13. The method of claim 9, wherein the step (e) includes the step
2 of using an auto-correlation function of said despreading sequence for
3 detecting the correlation sequences having said side peaks.

1 14. A method for producing a diversity branch signal from a chip
2 sequence transmitted by a spread spectrum radio frequency signal
3 propagating on multiple radio paths, comprising the steps of:
4 a) producing a plurality of successively time shifted replicas of a
5 despreading sequence;
6 b) detecting correlations between the chip sequence and said time
7 shifted replicas and producing therefrom a plurality of correlation
8 sequences, one of the correlation sequences which corresponds to an
9 intermediate point of said time shifted replicas having a maximum peak;
10 c) storing said correlation sequences in a memory;
11 d) setting a variable n to 1;
12 e) detecting, in said memory, a correlation sequence having a
13 maximum peak and identifying the correlation sequence having said
14 maximum peak as an n^{th} correlation sequence;
15 f) incrementing the variable n by 1;
16 g) removing the $(n-1)^{th}$ correlation sequence from the memory;
17 h) detecting, in said memory, correlation sequences having side
18 peaks inherently associated with the maximum peak of the $(n-1)^{th}$
19 correlation sequence and removing the detected correlation sequences from
20 the memory;
21 i) repeating the step (e) to detect a correlation sequence having a

NE-793

- 15 -

22 maximum peak;

23 j) determining the timing of the detected correlation sequence
24 and producing a despreding sequence delayed according to the
25 determined timing;

26 k) repeating the steps (e) to (j) to produce a plurality of the
27 delayed despreding sequences; and

28 l) despreding the chip sequence with the plurality of delayed
29 despreding sequences to produce a plurality of said diversity branch
30 signals.

1 15. The method of claim 14, wherein said time shifted replicas of
2 the despreding sequence are shifted by an integral submultiple of a chip
3 interval of said chip sequence.

1 16. The method of claim 15, wherein the step (g) comprises the
2 steps of detecting a plurality of neighboring correlation sequences of the (n-
3 1)th correlation sequence and removing the detected neighboring
4 correlation sequences from the memory.

1 17. The method of claim 14, wherein the step (h) includes the step
2 of using an auto-correlation function of said despreding sequence for
3 detecting the correlation sequences having said side peaks.

**Smart & Biggar
Ottawa, Canada
Patent Agents**

FIG. 1

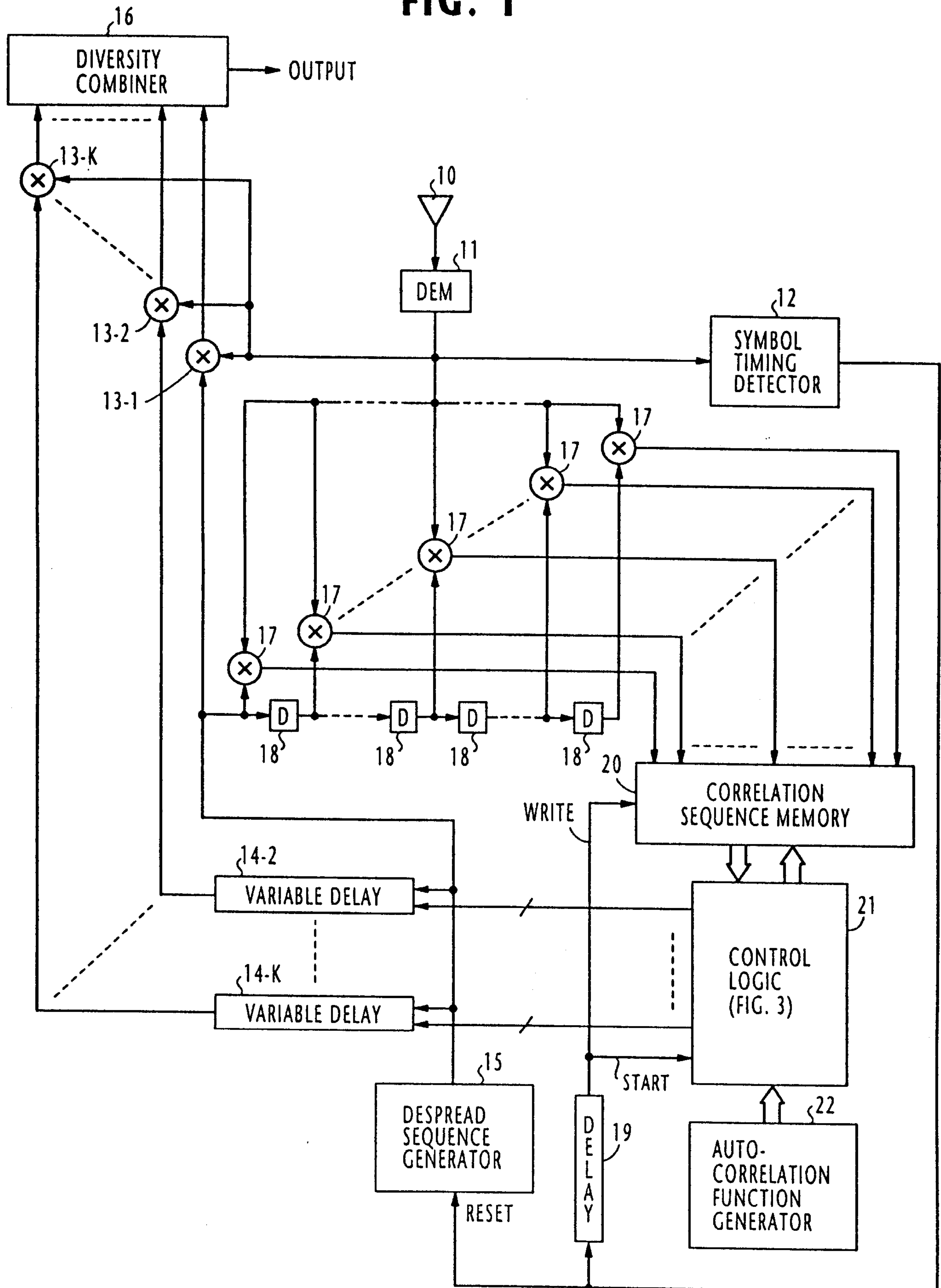
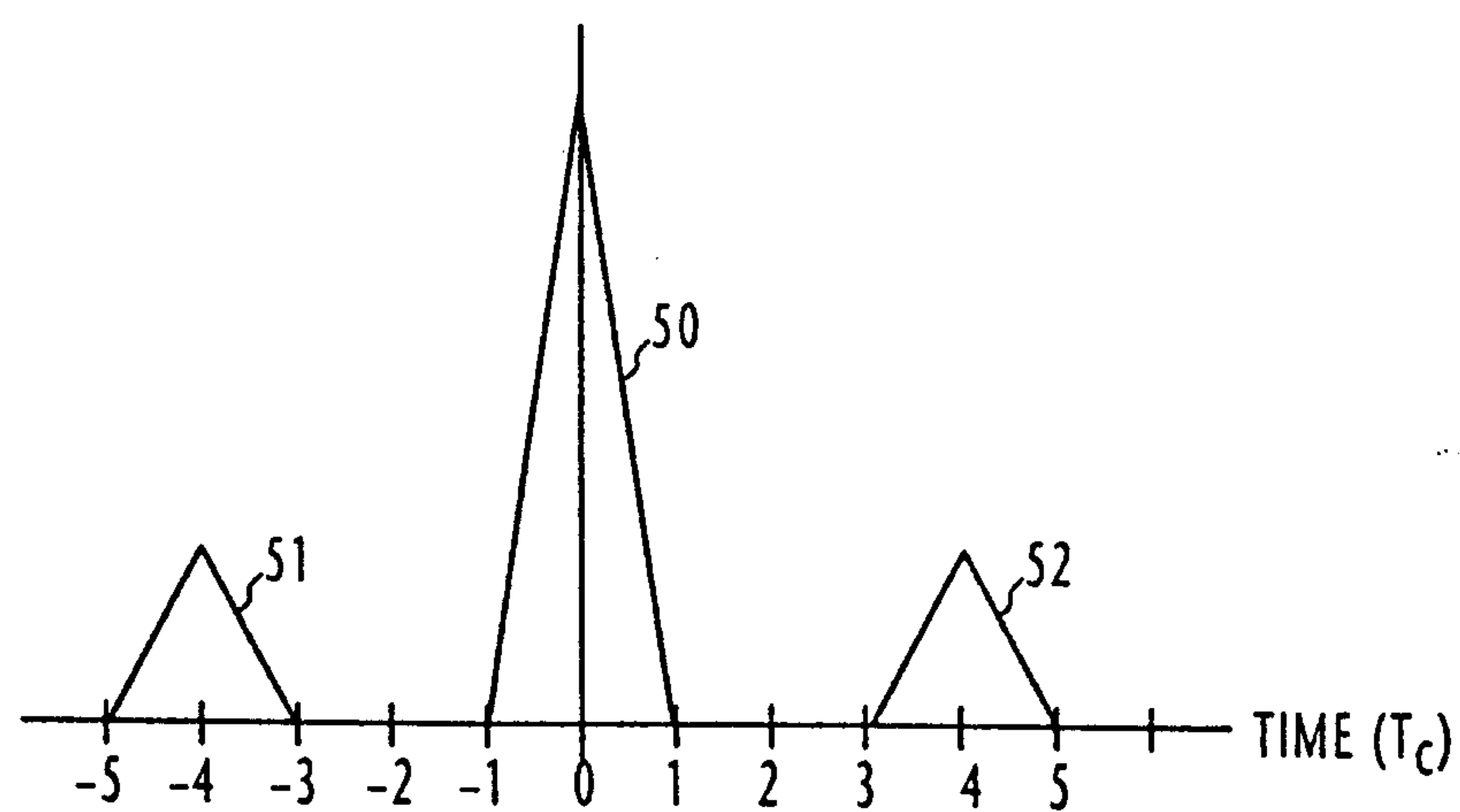


FIG. 2

AUTO-CORRELATION VALUE

**FIG. 4**

CORRELATION VALUE

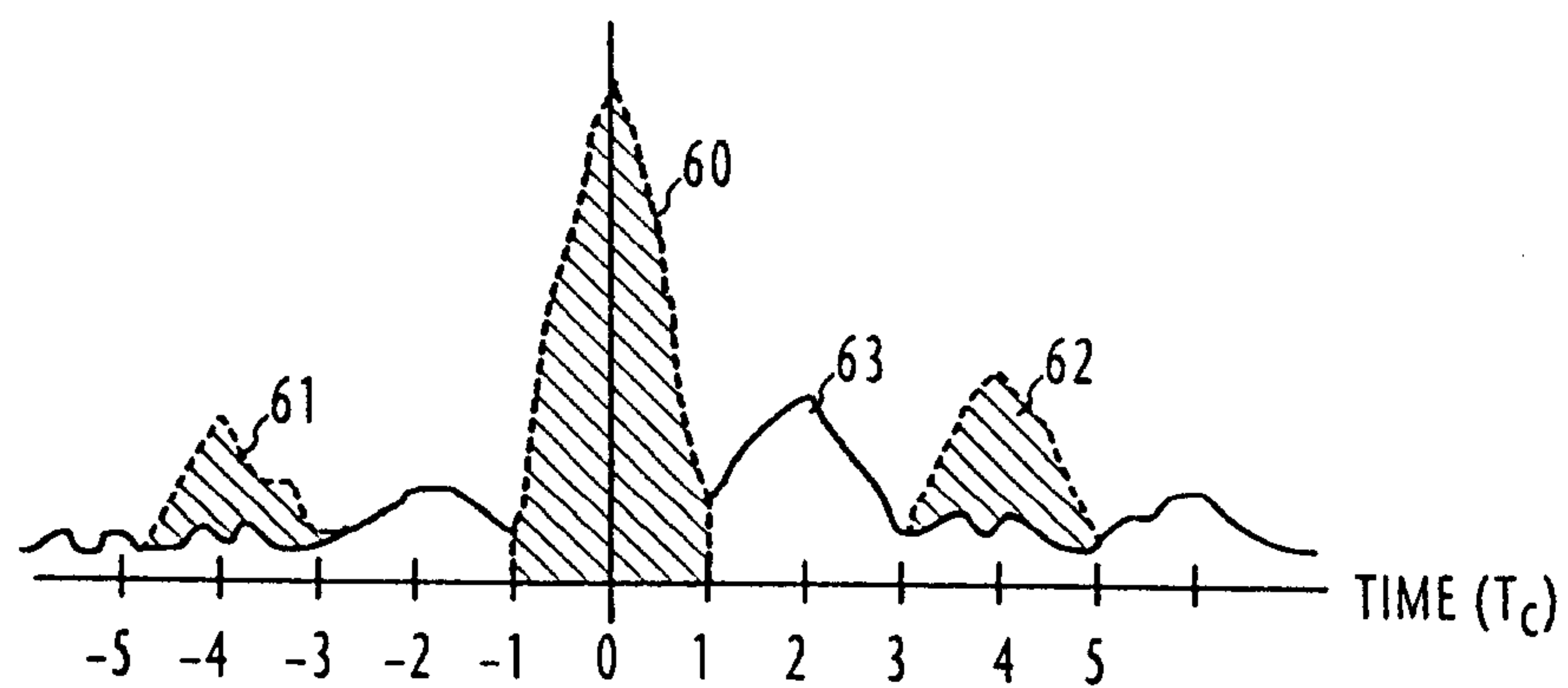


FIG. 3

