



(51) International Patent Classification:

H02J 50/10 (2016.01) H02J 50/80 (2016.01)

(21) International Application Number:

PCT/EP2019/050976

(22) International Filing Date:

15 January 2019 (15.01.2019)

(25) Filing Language:

English

(26) Publication Language:

English

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(81) Designated States (unless otherwise indicated, for every

kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,

CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every

kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: INDUCTOR-CAPACITOR RESONANT CIRCUIT

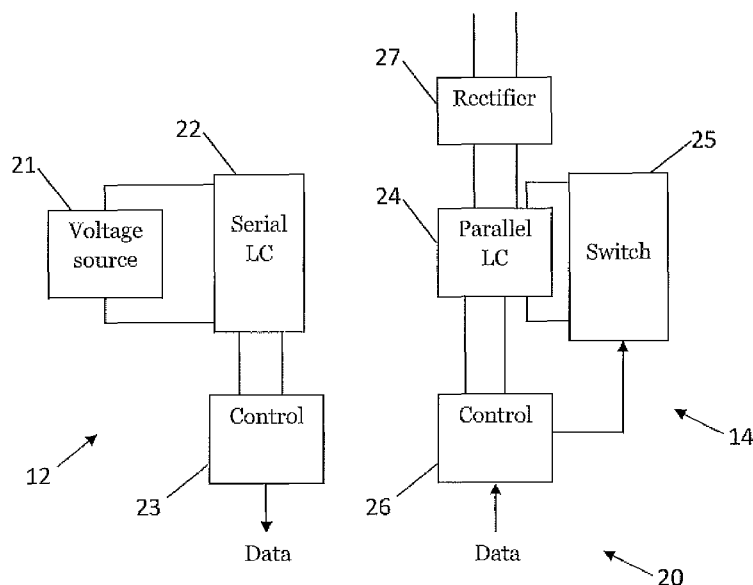


FIG. 2

(57) Abstract: An apparatus, method and computer program is described comprising means for detecting a phase of a current and/or a voltage in a parallel inductor-capacitor resonant circuit (14) and means (25) for switching terminals of a capacitor of the parallel inductor-capacitor resonant circuit (14) based on a phase signal and a data signal, wherein data is transmitted to a primary resonant circuit (12) as a result of the switching of the terminals of the capacitor.



Inductor-Capacitor Resonant Circuit

Field

The present specification relates to inductor-capacitor resonant circuits, such as
5 parallel inductor-capacitor resonant circuits for use in wireless power and data transfer systems.

Background

Simultaneous wireless power and data transfer systems are known, for example in
10 systems in which power is transferred to a device and data is transferred from the device. However, there remains a need for alternative and improved systems in this field.

Summary

15 In a first aspect, this specification describes an apparatus (such as a secondary resonant circuit of a system comprising a primary resonant circuit and the secondary resonant circuit), the apparatus comprising: a parallel inductor-capacitor resonant circuit; means for detecting a phase of a current and/or a voltage in the parallel inductor-capacitor resonant circuit; and means for switching terminals of a capacitor of the
20 parallel inductor-capacitor resonant circuit based on a phase signal (e.g. as output by the phase detecting means) and a data signal.

Some embodiments provide means for generating a modulator signal based on the phase signal and the data signal. The said means for switching terminals of the
25 capacitor may comprise a first switch and a second switch, wherein the first switch and the second switch are controlled by the modulator signal.

The phase signal may indicate a periodic cycle for switching terminals of the capacitor. Further, some embodiments further comprise means for defining the periodic cycle
30 dependent on a data rate of the data to be transmitted.

The means for switching the terminals of the capacitor may switch said terminals from a default position to a reversed position for a first time period, and may then switch the terminals back to the default position after the first time period.

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In some embodiments, the parallel inductor-capacitor resonant circuit is comprised within a wearable implant device. Indeed, the apparatus (e.g. the secondary resonant circuit) may be comprised within such a wearable implant device.

- 5 The said means may comprise: at least one processor; and at least one memory including computer program code, the at least one memory and the computer program configured, with the at least one processor, to cause the performance of the apparatus.

10 In a second aspect, this specification describes a system comprising: a primary resonant circuit comprising a serial inductor-capacitor resonant circuit; a secondary resonant circuit comprising: a parallel inductor-capacitor resonant circuit; means for detecting a phase of a current and/or a voltage in the parallel inductor-capacitor resonant circuit; and means for switching terminals of a capacitor of the parallel inductor-capacitor resonant circuit based on a phase signal (e.g. as output by the phase
15 detecting means) and a data signal, wherein data is transmitted to the primary resonant circuit as a result of the switching of the terminals of the capacitor. The primary resonant circuit may further comprise an envelope detector for decoding a signal received from the secondary resonant circuit to determine an estimate of the data transmitted.

20 The secondary resonant circuit may further comprise means for generating a modulator signal based on the phase signal and the data signal. The said means for switching terminals of the capacitor may comprise a first switch and a second switch, wherein the first switch and the second switch are controlled by the modulator signal.

25 The phase signal may indicate a periodic cycle for switching terminals of the capacitor. Further, some embodiments further comprise means for defining the periodic cycle dependent on a data rate of the data to be transmitted.

30 The means for switching the terminals of the capacitor may switch said terminals from a default position to a reversed position for a first time period, and then switches the terminals back to the default position after the first time period.

35 In some embodiments, the parallel inductor-capacitor resonant circuit is comprised within a wearable implant device. Indeed, the secondary resonant circuit may be comprised within a wearable implant device.

The said means may comprise: at least one processor; and at least one memory including computer program code, the at least one memory and the computer program configured, with the at least one processor, to cause the performance of the apparatus.

5

In a third aspect, the specification describes a method comprising: detecting a phase of a current and/or a voltage in a parallel inductor-capacitor resonant circuit of a secondary resonant circuit; and switching terminals of a capacitor of the parallel inductor-capacitor resonant circuit based on a phase signal (e.g. as detected in the
10 phase detecting step) and a data signal, wherein data is transmitted to a primary resonant circuit as a result of the switching of the terminals of the capacitor.

The method may further comprise generating a modulator signal based on the phase signal and the data signal. Further, switching terminals of the capacitor may comprise
15 switching a first switch and a second switch under the control of the modulator signal.

The phase signal may indicate a periodic cycle for switching terminals of the capacitor and the method may further comprise defining the periodic cycle dependent on a data rate of the data to be transmitted.

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Switching the terminals of the capacitor may comprise switching said terminals from a default position to a reversed position for a first time period, and then switching the terminals back to the default position after the first time period.

25 The method may further comprise decoding a signal received at the primary resonant circuit from the secondary resonant circuit to determine an estimate of the data transmitted from the secondary resonant circuit to the primary resonant circuit.

In a fourth aspect, this specification describes any apparatus configured to perform any
30 method as described with reference to the third aspect.

In a fifth aspect, this specification describes computer-readable instructions which, when executed by computing apparatus, cause the computing apparatus to perform any method as described with reference to the third aspect.

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In a sixth aspect, this specification describes a computer program comprising instructions for causing an apparatus to perform at least the following: detecting a phase of a current and/or a voltage in a parallel inductor-capacitor resonant circuit (e.g. of a secondary resonant circuit); and switching terminals of a capacitor of the parallel inductor-capacitor resonant circuit based on a phase signal (e.g. as detected in the phase detecting step) and a data signal, wherein data is transmitted to a primary resonant circuit as a result of the switching of the terminals of the capacitor.

In a seventh aspect, this specification describes a computer-readable medium (such as a non-transitory computer readable medium) comprising program instructions stored thereon for performing at least the following: detecting a phase of a current and/or a voltage in a parallel inductor-capacitor resonant circuit (e.g. of a secondary resonant circuit); and switching terminals of a capacitor of the parallel inductor-capacitor resonant circuit based on a phase signal (e.g. as detected in the phase detecting step) and a data signal, wherein data is transmitted to a primary resonant circuit as a result of the switching of the terminals of the capacitor.

In an eighth aspect, this specification describes an apparatus comprising: at least one processor; and at least one memory including computer program code which, when executed by the at least one processor, causes the apparatus to: detect a phase of a current and/or a voltage in a parallel inductor-capacitor resonant circuit (e.g. of a secondary resonant circuit); and switch terminals of a capacitor of the parallel inductor-capacitor resonant circuit based on a phase signal (e.g. as detected in the phase detecting step) and a data signal, wherein data is transmitted to a primary resonant circuit as a result of the switching of the terminals of the capacitor.

In a ninth aspect, this specification describes an apparatus (such as a control module or a server) comprising: a first control module (such as a phase detector) for detecting a phase of a current and/or a voltage in a parallel inductor-capacitor resonant circuit (e.g. of a secondary resonant circuit); and a switching arrangement for switching terminals of a capacitor of the parallel inductor-capacitor resonant circuit based on a phase signal (e.g. as detected by the first control module) and a data signal. The apparatus may be configured to transmit data to a primary resonant circuit as a result of the switching, by the switching arrangement, of the terminals of the capacitor.

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Brief description of the drawings

Example embodiments will now be described, by way of non-limiting examples, with reference to the following schematic drawings, in which:

FIG. 1 is a block diagram of a system in accordance with an example embodiment;

5 FIG. 2 is a block diagram of a system in accordance with an example embodiment;

FIG. 3 is a block diagram of an implementation of a secondary resonant circuit in accordance with an example embodiment;

FIG. 4 is a flow chart showing an algorithm in accordance with an example embodiment;

10 FIG. 5 is a block diagram of an implementation of a primary resonant circuit in accordance with an example embodiment;

FIG. 6 is a flow chart showing an algorithm in accordance with an example embodiment;

FIGS. 7 and 8 show plots of waveforms in accordance with example embodiments;

15 FIG. 9 is a block diagram of components of a system in accordance with an example embodiment; and

FIGS. 10A and 10B show tangible media, respectively a removable memory unit and a compact disc (CD) storing computer-readable code which when run by a computer perform operations according to example embodiments.

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Detailed description

FIG. 1 is a block diagram of a system, indicated generally by the reference numeral 10, in accordance with an example embodiment. The system 10 comprises a primary resonant circuit 12 and a secondary resonant circuit 14. In the use of the system, power
25 may be transferred from the primary resonant circuit 12 to the secondary resonant circuit 14 and data may be transferred from the secondary resonant circuit to the primary resonant circuit. Thus, the system 10 can be used for simultaneous wireless power and data transfer.

30 By way of example, the secondary resonant circuit may be an implant, such as an implant of a biomedical system. Such an implant may therefore be able to receive power wirelessly and to provide data wirelessly. In an alternative implementation, the secondary resonant circuit may be a radio frequency identification (RFID) device.

35 The system 10 may be implemented using near-field inductive coupling, with the primary resonant circuit including a power source and a serial inductor-capacitor

resonant circuit and the secondary resonant circuit including a parallel inductor-capacitor resonant circuit followed by a rectifier.

5 Data transfer from the secondary resonant circuit 14 to the primary resonant circuit 12 may be achieved using load shift keying modulation (LSK). In LSK, data may be transmitted by short-circuiting the parallel LC circuit at the secondary resonant circuit if a bit “1” is to be sent and not short-circuiting the parallel LC circuit at the secondary resonant circuit if a bit “0” is to be sent. (Of course, this arrangement could be reversed, with short-circuiting being used to transmit a bit “0”.)

10

The effect of the short-circuiting may be detected at the primary resonant circuit by sensing the changes of the primary coil current. During the transmission of bit “1”, a loss of power occurs at the secondary resonant circuit, since the input to the rectifier is short-circuited and therefore no power can be acquired. This arrangement can be a limiting factor on data transmission rates, since, as data rates increase, the time during which the LC circuit is likely to be short-circuited may increase.

FIG. 2 is a block diagram of a system, indicated generally by the reference numeral 20, in accordance with an example embodiment. The system includes example implementations of the primary resonant circuit 12 and the secondary resonant circuit 14 described above.

20 The primary resonant circuit 12 comprises a voltage source 21, a serial inductor-capacitor (LC) circuit 22 and a first control circuit 23. The secondary resonant circuit 14 comprises a parallel inductor-capacitor (LC) circuit 24, a switching arrangement 25, a second control circuit 26 and a rectifier 27.

As discussed above, power is transferred from the primary resonant circuit 12 to the secondary resonant circuit 14. Specifically, the output of voltage source 21 (V_s) is fed to the serial inductor-capacitor circuit 22. The frequency of the voltage source 21 may be equal to the resonant frequency (f_s) of the serial inductor-capacitor circuit 22, which is given by the equation: $f_s = \frac{1}{2\pi\sqrt{L_1C_1}}$ (where L_1 and C_1 are the inductance and capacitance of the serial inductor-capacitor circuit 22 respectively).

The inductance (L_1) of the serial inductor-capacitor circuit 22 of the primary resonant circuit 12 and the inductance (L_2) of the parallel inductor-capacitor circuit 24 of the secondary resonant circuit 14 are coupled with a coupling coefficient k . The parallel inductor-capacitor circuit 24 may have the same resonant frequency f_s as the serial inductor-capacitor circuit 22 in order to maximize the power transfer between primary and secondary resonant circuits 12 and 14. The power transferred from the serial inductor-capacitor circuit 22 to the parallel inductor-capacitor circuit 24 is harvested by the rectifier circuit 27, which rectifier circuit may, for example, convert AC power signals induced at the parallel inductor-capacitor circuit 24 into DC power signals.

10

FIG. 3 is a block diagram of an implementation of the secondary resonant circuit 14 in accordance with an example embodiment. The secondary resonant circuit 14 comprises an inductor 31 and a capacitor 32 (that collectively form the parallel inductor-capacitor circuit 24 discussed above), a first switch 33 and a second switch 34 (that collectively form the switching arrangement 25), a phase detector 35 and a modulator 36 (that collectively form the second control circuit 26), and a load resistance 37 (that models the effect of the rectifier 27).

15

The first switch 33 and the second switch 34 work together to swap the connections of the capacitor 32 of the parallel inductor-capacitor circuit, depending on the output of the modulator 36. The modulator 36 generates the signal(s) controlling the switches 33 and 34 depending on both the data signal to be transmitted and the output of the phase detector 35. Thus, the connections of the capacitor 32 are switched depending on the data to be transmitted by the secondary resonant circuit 14. The phase detector 35 provides an output depending on the phase of the voltage and/or current signals at the parallel inductor-capacitor circuit of the secondary resonant circuit 14.

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As discussed further below, the phase detector 35 may be a simple circuit, which generates one or more outputs depending on local voltage and/or current signals (i.e. signals within the secondary resonant circuit 14). Similarly, the modulator 36 may implement a simple logic. Accordingly, implementing the secondary resonant circuit 14 is relatively straightforward.

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FIG. 4 is a flow chart showing an algorithm, indicated generally by the reference numeral 40, in accordance with an example embodiment. The algorithm 40 is implemented at the secondary resonant circuit 14.

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The algorithm 40 starts at operation 42, where the phase of the voltages and/or currents of the parallel inductor-capacitor circuit 24 are determined. The operation 42 is implemented by the phase detector 35. For example, the phase detector 35 may
5 provide a signal to the modulator 35 indicating when the voltage across the capacitor 32 (V_{C2} as shown in FIG. 3) is at a maximum (or indicating when the current flowing through the inductor 31 (the current I_{L2} as shown in FIG. 3) is at a zero-crossing). In one example embodiment, the phase detector 35 provides a signal to the modulator 35 after a defined number of instances of a voltage maximum or current zero-crossing
10 (wherein the defined number may be a definable parameter).

Next, at operation 44, a switching signal is modulated, based on the data input received at the modulator 36 and the phase determined in the operation 42. The switching signal instructs the terminals of the capacitor 32 to be switched for half a cycle of the
15 voltages/current induced in the parallel inductor-capacitor circuit of the secondary resonant circuit.

Finally, at operation 46, the terminals of the capacitor 32 of the parallel inductor-capacitor circuit 24 are switched depending on the output of the operation 44.
20

In one implementation, in order to transmit a data "1", the connections of the capacitor 32 are switched for the last half-cycle of the voltages/current induced in the parallel inductor-capacitor circuit 24 of the secondary resonant circuit 14. This switch results in the phase of the current through the inductor 31 (i.e. the current I_{L2}) reversing. As a
25 result, the current flowing through the inductor of the serial inductor-capacitor circuit 22 of the primary resonant circuit is increased, which increase can be detected at the primary resonant circuit 12.

Thus, the second control circuit 26 referred to above may be implemented by using
30 zero-crossing detection and simple logic circuitry.

FIG. 5 is a block diagram of an implementation of the primary resonant circuit 12 in accordance with an example embodiment. As shown in FIG. 5, the voltage source 21 is modelled by a voltage source 51 (having a voltage V_s) and a source resistance 52 (having
35 a resistance R_s), the serial inductor-capacitor resonant circuit 22 is implemented by an

inductor 53 (having an inductance L_1) and a capacitor 54 (having a capacitance C_1), and the first control circuit 23 is implemented by an envelope detector 55 and a decoder 56.

FIG. 6 is a flow chart showing an algorithm, indicated generally by the reference numeral 60, in accordance with an example embodiment.

The algorithm 60 starts at operation 62, where an envelope of the voltage across the inductor 53 (the voltage V_{L1} shown in FIG. 5) is determined (using the envelope detector 55, which envelope detector receives input from either side of the inductor 53).
As discussed above, the voltage across the inductor 53 is affected by the switching of the capacitor 32 in response to the data signal received at the secondary resonant circuit. Thus, the envelope of the voltage V_{L1} is indicative of the data signal.

At operation 64, the data is decoded to provide the data output of the primary resonant circuit 12. Thus, the decoder 66 generates the data output that seeks to regenerate the data originally transmitted by the second resonant circuit 14.

FIG. 7 shows plots, indicated generally by the reference numeral 70, of waveforms in accordance with an example embodiment. The plot 70 includes a first plot 70a (showing currents and voltages in the secondary resonant circuit 14) and a second plot 70b (showing currents and voltages in the primary resonant circuit 12). The plots 70 were generated in simulations of a 13.56 MHz inductive link.

The first plot 70a includes a first waveform 71a showing the voltage (V_{C2}) across the capacitor 32 of the parallel inductor-capacitor circuit 24, a second waveform 72a showing the current (I_{L2}) in the inductor 31 of the parallel inductor-capacitor circuit 24, and a third waveform 73a showing a switching voltage (V_{switch}) output by the modulator 36 to the switches 33 and 34 of the switching arrangement 25 of the secondary resonant circuit.

Similarly, the second plot 70b includes a first waveform 71b showing the voltage (V_{L1}) across the inductor 53 of the serial inductor-capacitor circuit 22, a second waveform 72b showing the current (I_{L1}) in the inductor 53 of the serial inductor-capacitor circuit 22, and a third waveform 73b showing a switching voltage (V_{switch}) output by the envelope detector 55 of the primary resonant circuit.

In one example embodiment, to send a data bit “1”, the capacitance C_2 of the secondary resonant circuit is switched (effectively turned upside down) with respect to L_2 at the point where the voltage across the capacitor (V_{C2}) is at maximum (at that point current I_{L2} is zero). The capacitor is switched for the last half of cycle of the induced voltages
5 and current ($T_{\text{switch}}=1/(2f_s)$). As a result, the phase of current I_{L2} is switched by 180 degrees, which as a consequence will cause the increase of current I_{L1} . As shown in the plot 70a, this switching of the phase of the current occurs in synchronism with the switching signal (as indicated, for example, by the reference 73a).

10 As shown in the second plot 70b, the switching of the capacitance C_2 of the secondary resonant circuit causes an increase in the inductor current 72b at the primary resonant circuit. As a consequence, the inductor voltage 71b at the primary resonant circuit increases. Therefore, by using an envelope detector for measuring the inductor voltage, the received data can be estimated.

15 In the example plot 70a, only data “1”s are sent (which could be seen as a worst-case scenario). Data is sent every fourth cycle, such that the data rate is 3.39 Mb/s.

20 Whilst the capacitor is switched, the energy acquired at the secondary resonant circuit 14 may be slightly reduced (due to a conflict of the current I_{L2} caused by the switching of the capacitor C_2 and the part of the current contributed by a coupling of L_1 and L_2), but will not be lost entirely.

25 As noted above, the capacitor switching may take place at a period starting and ending at a zero-crossing of the current (I_{L2}) flowing through the inductor 31. Accordingly, the phase detector 35 may simply be required to identify selected zero crossings of the inductor current.

FIG. 8 shows plots, indicated generally by the reference numeral 80, of waveforms in
30 accordance with an example embodiment. The plot 80 includes a first plot 80a (showing currents and voltages in the secondary resonant circuit 14) and a second plot 80b (showing currents and voltages in the primary resonant circuit 12). As with the plots 70 described above, the plots 80 were generated in simulations of a 13.56 MHz inductive link. In the plots 80, the waveforms are shown for a data rate equal to 6.73
35 Mb/s (such that data changes on every second signal cycle).

The phase detector 35 is used for determining when the terminals of the capacitor should be switched, in the event that switching is required (i.e. depending on the data signal). Thus, the phase detector 35 provides a signal indicating a periodic cycle for switching terminals of the capacitor. The periodic signal is dependent on the data rate
5 of the data to be transmitted. Thus, the periodic signal occurs twice as often in the plots 80 than in the plots 70. Other data rates are possible. Moreover, an arrangement for setting data rates could be provided.

As discussed above, the second control circuit 26 of the secondary resonant circuit 14
10 that is used to transfer data to the primary resonant circuit 12 may be implemented using a simple phase detector and modulator logic arrangement. Similarly, the first control circuit 23 of the primary resonant circuit 12 may be implemented using a simple envelope detection arrangement. Implementations of, and modifications to, the principles described herein are therefore relatively straightforward.

15 For completeness, FIG. 9 is a schematic diagram of components of one or more of the example embodiments described previously, which hereafter are referred to generically as processing systems 300. A processing system 300 may have a processor 302, a memory 304 closely coupled to the processor and comprised of a RAM 314 and ROM
20 312, and, optionally, user input 310 and a display 318. The processing system 300 may comprise one or more network/apparatus interfaces 308 for connection to a network/apparatus, e.g. a modem which may be wired or wireless. Interface 308 may also operate as a connection to other apparatus such as device/apparatus which is not network side apparatus. Thus direct connection between devices/apparatus without
25 network participation is possible. User input 310 and display 318 may be connected to a remote processor like ground control station. Remote connection may be LTE or 5G type fast connection between remote processor and processor.

The processor 302 is connected to each of the other components in order to control
30 operation thereof.

The memory 304 may comprise a non-volatile memory, such as a hard disk drive (HDD) or a solid state drive (SSD). The ROM 312 of the memory 314 stores, amongst other things, an operating system 315 and may store software applications 316. The
35 RAM 314 of the memory 304 is used by the processor 302 for the temporary storage of data. The operating system 315 may contain code which, when executed by the

processor implements aspects of the algorithms 40 and 60 described above. The code may, for example, determine data rates for modulation and detection of signals for data transfer. Moreover, a user interface for adjusting such data transfer rates could readily be implemented (e.g. using the user inputs 310 and the display 318). Note that in the
5 case of small device/apparatus the memory can be most suitable for small size usage i.e. not always hard disk drive (HDD) or solid state drive (SSD) is used.

The processor 302 may take any suitable form. For instance, it may be a microcontroller, a plurality of microcontrollers, a processor, or a plurality of
10 processors.

The processing system 300 may be a standalone computer, a server, a console, or a network thereof. The processing system 300 and needed structural parts may be all inside device/apparatus such as IoT device/apparatus i.e. embedded to very small size.
15

In some example embodiments, the processing system 300 may also be associated with external software applications. These may be applications stored on a remote server device/apparatus and may run partly or exclusively on the remote server device/apparatus. These applications may be termed cloud-hosted applications. The
20 processing system 300 may be in communication with the remote server device/apparatus in order to utilize the software application stored there.

FIGS. 10A and 10B show tangible media, respectively a removable memory unit 365 and a compact disc (CD) 368, storing computer-readable code which when run by a
25 computer may perform methods according to example embodiments described above. The removable memory unit 365 may be a memory stick, e.g. a USB memory stick, having internal memory 366 storing the computer-readable code. The memory 366 may be accessed by a computer system via a connector 367. The CD 368 may be a CD-ROM or a DVD or similar. Other forms of tangible storage media may be used.
30 Tangible media can be any device/apparatus capable of storing data/information which data/information can be exchanged between devices/apparatus/network.

Embodiments of the present invention may be implemented in software, hardware, application logic or a combination of software, hardware and application logic. The
35 software, application logic and/or hardware may reside on memory, or any computer media. In an example embodiment, the application logic, software or an instruction set

is maintained on any one of various conventional computer-readable media. In the context of this document, a “memory” or “computer-readable medium” may be any non-transitory media or means that can contain, store, communicate, propagate or transport the instructions for use by or in connection with an instruction execution
5 system, apparatus, or device, such as a computer.

Reference to, where relevant, “computer-readable storage medium”, “computer program product”, “tangibly embodied computer program” etc., or a “processor” or “processing circuitry” etc. should be understood to encompass not only computers
10 having differing architectures such as single/multi-processor architectures and sequencers/parallel architectures, but also specialised circuits such as field programmable gate arrays FPGA, application specific circuits ASIC, signal processing devices/apparatus and other devices/apparatus. References to computer program, instructions, code etc. should be understood to express software for a programmable
15 processor firmware such as the programmable content of a hardware device/apparatus as instructions for a processor or configured or configuration settings for a fixed function device/apparatus, gate array, programmable logic device/apparatus, etc.

As used in this application, the term “circuitry” refers to all of the following: (a)
20 hardware-only circuit implementations (such as implementations in only analogue and/or digital circuitry) and (b) to combinations of circuits and software (and/or firmware), such as (as applicable): (i) to a combination of processor(s) or (ii) to portions of processor(s)/software (including digital signal processor(s)), software, and memory(ies) that work together to cause an apparatus, such as a server, to perform
25 various functions) and (c) to circuits, such as a microprocessor(s) or a portion of a microprocessor(s), that require software or firmware for operation, even if the software or firmware is not physically present.

If desired, the different functions discussed herein may be performed in a different
30 order and/or concurrently with each other. Furthermore, if desired, one or more of the above-described functions may be optional or may be combined. Similarly, it will also be appreciated that the flow diagrams of Figures 4 and 6 are examples only and that various operations depicted therein may be omitted, reordered and/or combined.

35 It will be appreciated that the above described example embodiments are purely illustrative and are not limiting on the scope of the invention. Other variations and

modifications will be apparent to persons skilled in the art upon reading the present specification. For example, it would be possible to extend the principles described herein to other applications, such as the control of robots or similar objects.

- 5 Moreover, the disclosure of the present application should be understood to include any novel features or any novel combination of features either explicitly or implicitly disclosed herein or any generalization thereof and during the prosecution of the present application or of any application derived therefrom, new claims may be formulated to cover any such features and/or combination of such features.

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Although various aspects of the invention are set out in the independent claims, other aspects of the invention comprise other combinations of features from the described example embodiments and/or the dependent claims with the features of the independent claims, and not solely the combinations explicitly set out in the claims.

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It is also noted herein that while the above describes various examples, these descriptions should not be viewed in a limiting sense. Rather, there are several variations and modifications which may be made without departing from the scope of the present invention as defined in the appended claims.

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Claims:

1. An apparatus comprising:
a parallel inductor-capacitor resonant circuit;
5 means for detecting a phase of a current and/or a voltage in the parallel inductor-capacitor resonant circuit; and
means for switching terminals of a capacitor of the parallel inductor-capacitor resonant circuit based on a phase signal and a data signal.
- 10 2. An apparatus as claimed in claim 1, further comprising means for generating a modulator signal based on the phase signal and the data signal.
3. An apparatus as claimed in claim 2, wherein the means for switching terminals of the capacitor comprises a first switch and a second switch, wherein the first switch
15 and the second switch are controlled by the modulator signal.
4. An apparatus as claimed in any one of the preceding claims, wherein the phase signal indicates a periodic cycle for switching terminals of the capacitor.
- 20 5. An apparatus as claimed in claim 4, further comprising means for defining the periodic cycle dependent on a data rate of the data to be transmitted.
6. An apparatus as claimed in any one of the preceding claims, wherein the means for switching the terminals of the capacitor switches said terminals from a default
25 position to a reversed position for a first time period, and then switches the terminals back to the default position after the first time period.
7. An apparatus as claimed in any one of the preceding claims, wherein the parallel inductor-capacitor resonant circuit is comprised within a wearable implant device.
30
8. A system comprising:
a primary resonant circuit comprising a serial inductor-capacitor resonant circuit;
a secondary resonant circuit comprising:
35 a parallel inductor-capacitor resonant circuit;

means for detecting a phase of a current and/or a voltage in the parallel inductor-capacitor resonant circuit; and

means for switching terminals of a capacitor of the parallel inductor-capacitor resonant circuit based on a phase signal and a data signal, wherein data is transmitted to the primary resonant circuit as a result of the switching of the terminals of the capacitor.

9. A system as claimed in claim 8, wherein the primary resonant circuit further comprises an envelope detector for decoding a signal received from the secondary resonant circuit to determine an estimate of the data transmitted.

10. A system as claimed in claim 8 or claim 9, wherein the secondary resonant circuit further comprises means for generating a modulator signal based on the phase signal and the data signal.

11. An system as claimed in any one claims 8 to 10, wherein the means for switching the terminals of the capacitor switches said terminals from a default position to a reversed position for a first time period, and then switches the terminals back to the default position after the first time period.

12. An apparatus or a system as claimed in any one of the preceding claims, wherein the means comprise:
at least one processor; and
at least one memory including computer program code, the at least one memory and the computer program configured, with the at least one processor, to cause the performance of the apparatus.

13. A method comprising:
detecting a phase of a current and/or a voltage in a parallel inductor-capacitor resonant circuit of a secondary resonant circuit; and
switching terminals of a capacitor of the parallel inductor-capacitor resonant circuit based on a phase signal and a data signal, wherein data is transmitted to a primary resonant circuit as a result of the switching of the terminals of the capacitor.

14. A method as claimed in claim 13, further comprising generating a modulator signal based on the phase signal and the data signal.

15. A method as claimed in claim 14, wherein switching terminals of the capacitor comprises switching a first switch and a second switch under the control of the modulator signal.

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16. A method as claimed in any one of claims 13 to 15, wherein the phase signal indicates a periodic cycle for switching terminals of the capacitor, the method further comprising defining the periodic cycle dependent on a data rate of the data to be transmitted.

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17. A method as claimed in any one of claims 13 to 16, wherein switching the terminals of the capacitor comprises switching said terminals from a default position to a reversed position for a first time period, and then switching the terminals back to the default position after the first time period.

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18. A method as claimed in any one of claims 13 to 17, further comprises decoding a signal received at the primary resonant circuit from the secondary resonant circuit to determine an estimate of the data transmitted from the secondary resonant circuit to the primary resonant circuit.

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19. A computer readable medium comprising program instructions stored thereon for performing at least the following:

detecting a phase of a current and/or a voltage in a parallel inductor-capacitor resonant circuit; and

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switching terminals of a capacitor of the parallel inductor-capacitor resonant circuit based on a phase signal and a data signal, wherein data is transmitted to a primary resonant circuit as a result of the switching of the terminals of the capacitor.

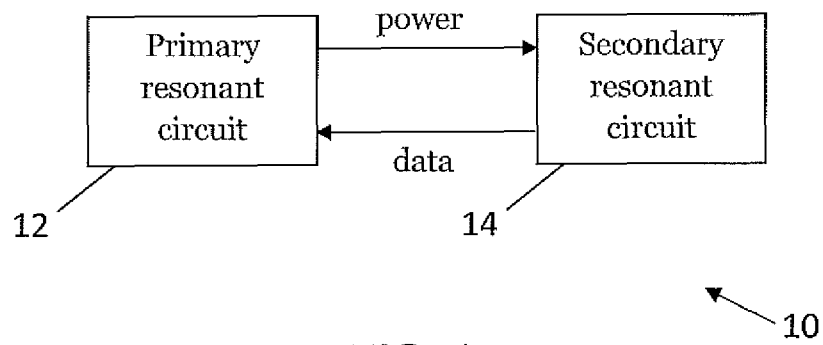


FIG. 1

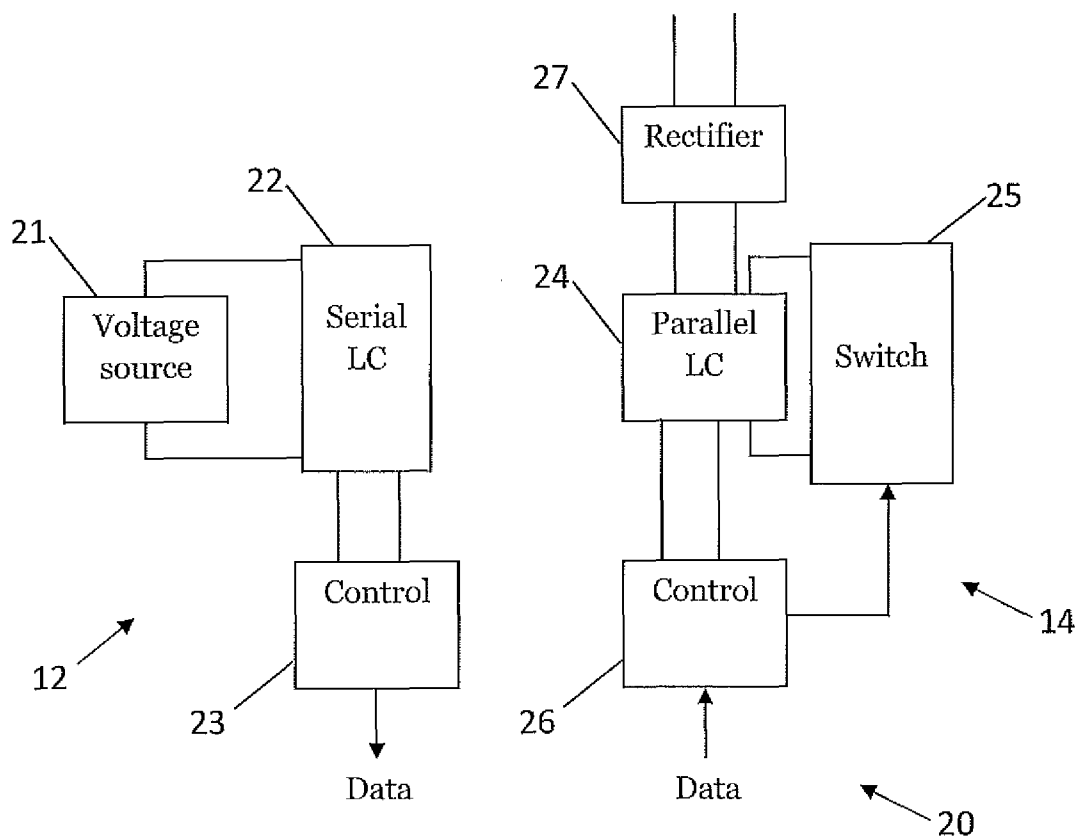


FIG. 2

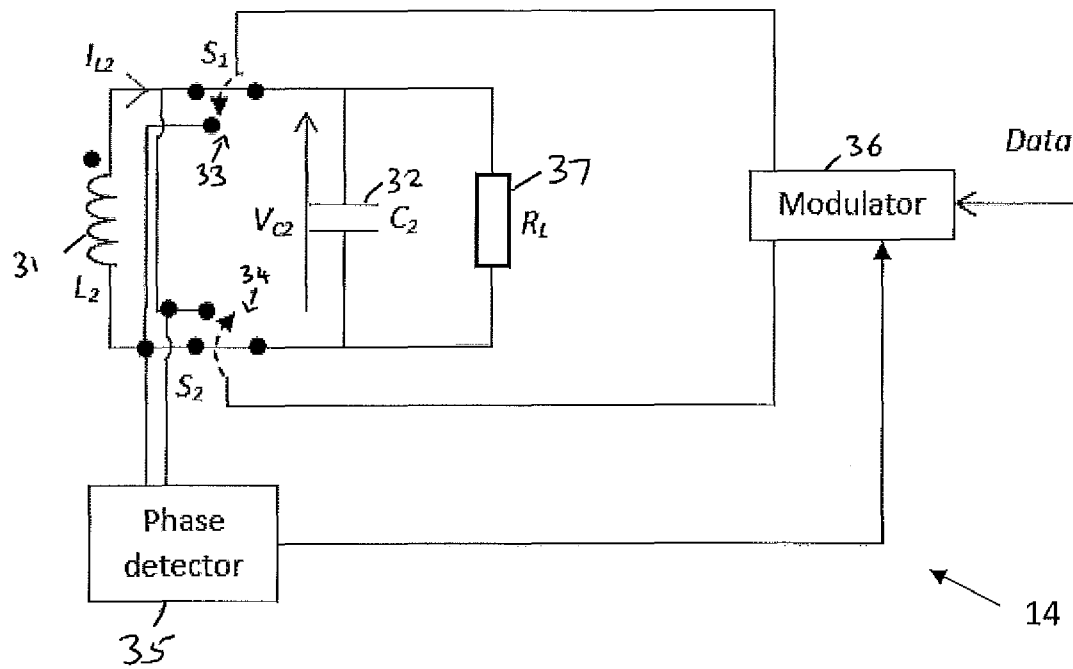


FIG. 3

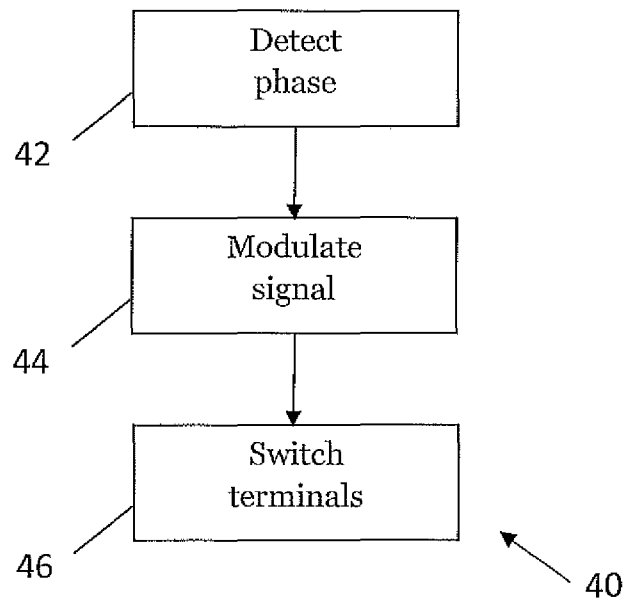


FIG. 4

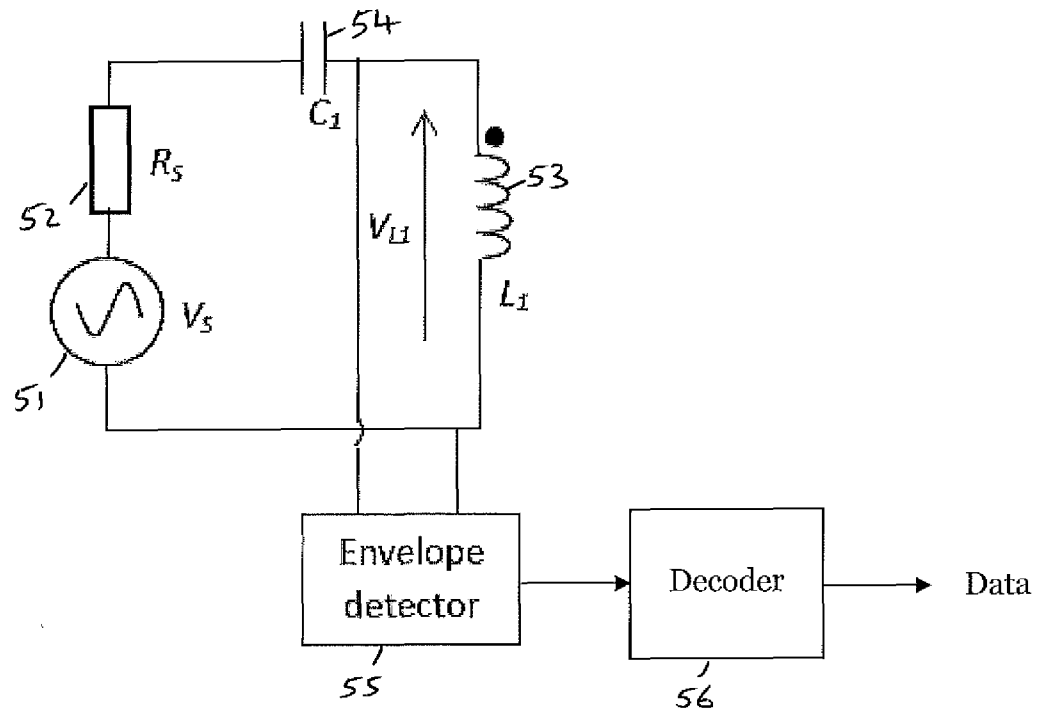


FIG. 5

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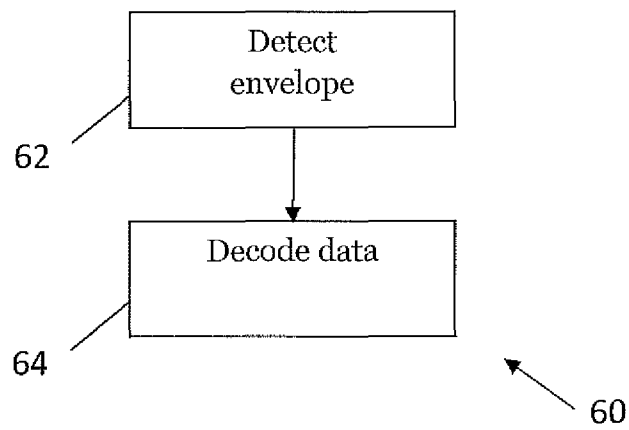


FIG. 6

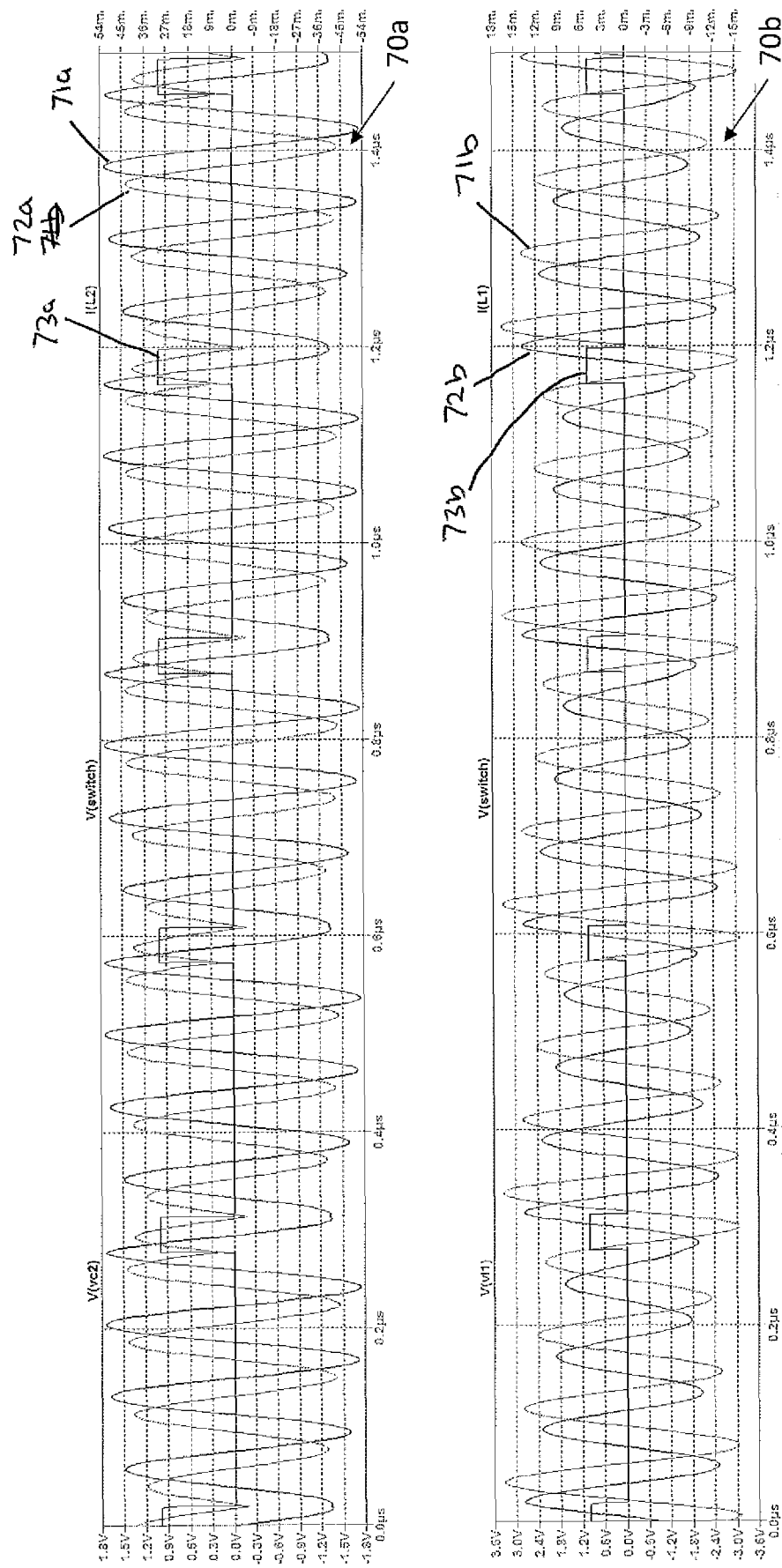


FIG. 7

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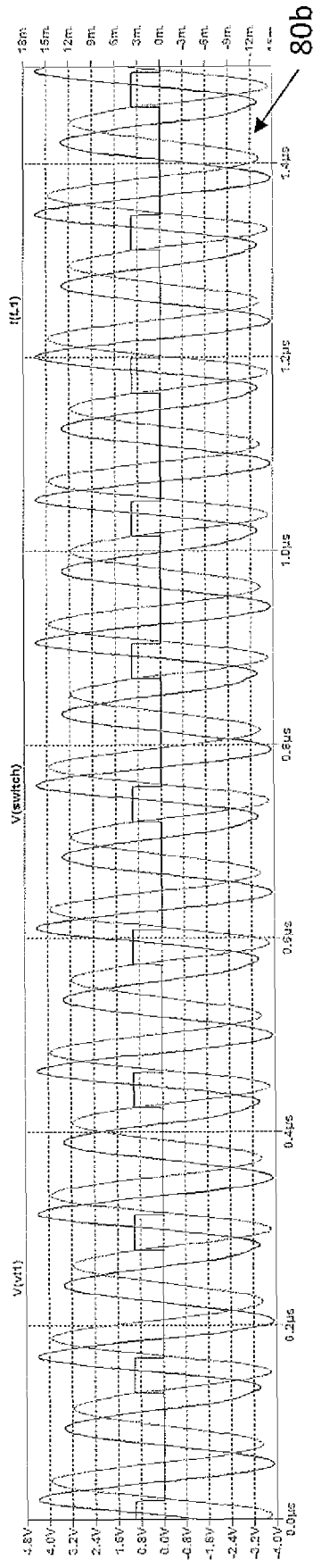
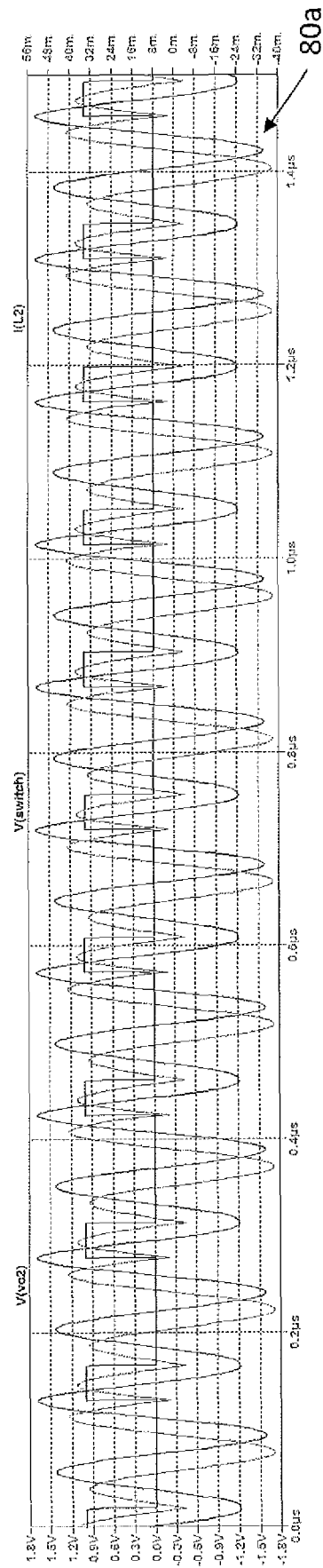


FIG. 8

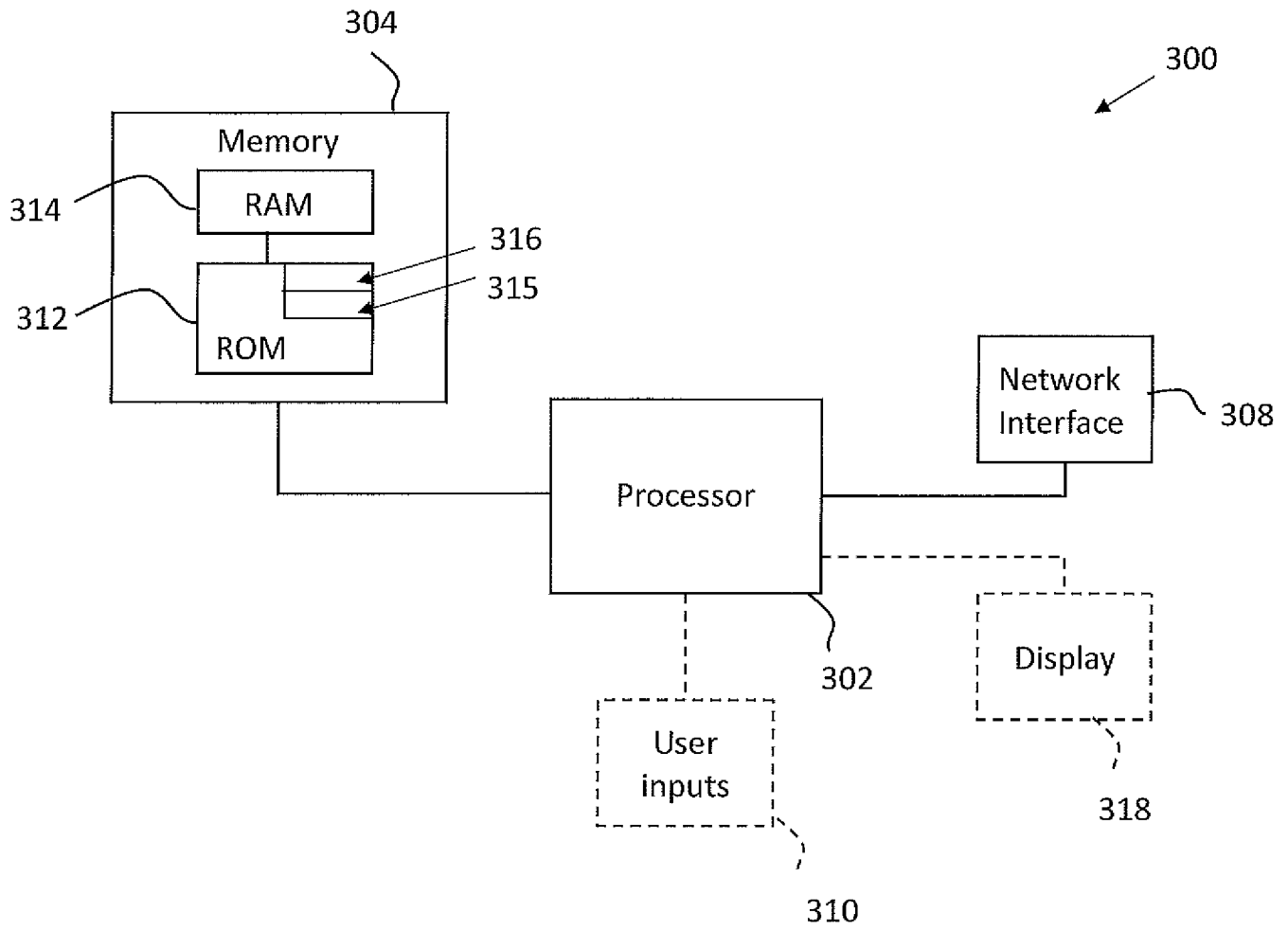


FIG. 9

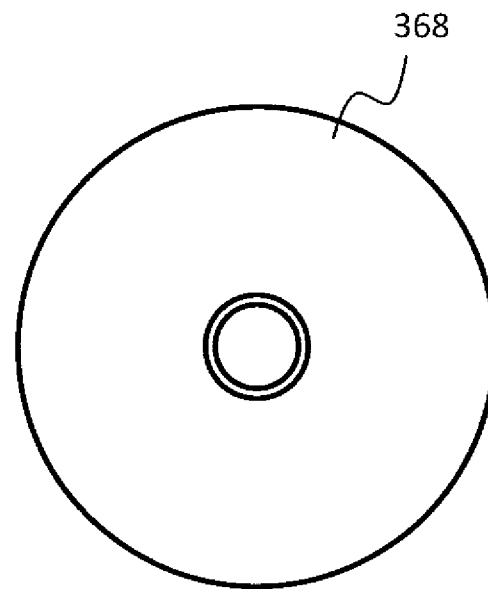
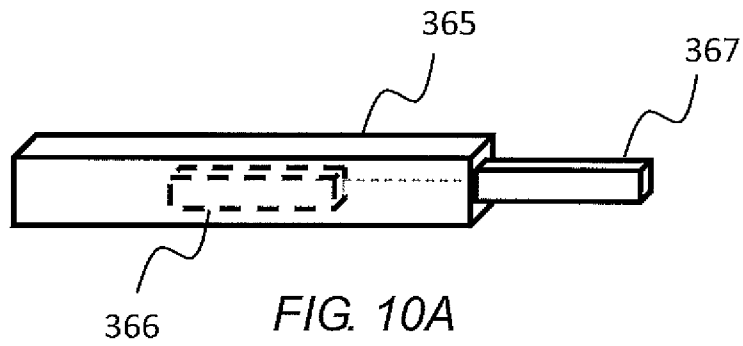


FIG. 10B

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/050976

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02J50/10 H02J50/80
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02J H04B B60L H01F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/133894 A1 (HENNIG ANDREAS [DE] ET AL) 9 June 2011 (2011-06-09)	1-5, 7-10, 12-16, 18,19
A	paragraphs [0005], [0064], [0068], [0085]; figures 10,13,16 -----	6,11,17



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"E" earlier application or patent but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

18 July 2019

Date of mailing of the international search report

28/08/2019

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Fax: (+31-70) 340-3016

Authorized officer

Varela Fraile, Pablo

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2019/050976

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011133894 A1	09-06-2011	DE 102010028991 A1	09-06-2011
		US 2011133894 A1	09-06-2011
